Scheduling Constrained-Deadline Sporadic Parallel Tasks Considering Memory Contention

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Abstract—Consider constrained-deadline sporadic tasks scheduled on a multiprocessor where (i) each task is characterized by its execution requirement, deadline, and minimum inter-arrival time, (ii) each task generates a sequence of jobs, (iii) the execution requirement of a job and its potential for parallel execution is described by one or many stages with a stage having one or many segments and different segments in the same stage can execute in parallel and a segment is only allowed to start execution if all segments of previous stages have finished execution, and (iv) there is contention for shared resources in the memory system (cache eviction, reordering in memory controller, memory bus contention). We present an algorithm that (i) performs schedulability testing for tasks scheduled with global-Earliest-Deadline-First (gEDF), (ii) configures the virtual-to-physical address translation so that a cache block fetched to the last-level cache by one task cannot be evicted by another task, (iii) configures the virtual-to-physical address translation to attempt to eliminate the extra execution time caused by the reordering effect in the memory controller and if this is not possible, then the reordering effect is considered in the schedulability analysis, and (iv) considers the effect of contention for the memory bus. Our solution is based on formulating this problem as a Mixed-Integer Linear Program (MILP). We have implemented a tool based on this theory and validated its output against measurements on a real computer.

I. INTRODUCTION

Multicore processors are the norm today. The trend is that the number of processors on a chip increases exponentially while the clock frequency stays constant. And software practitioners are under pressure to deliver improved functionality which has increased the execution requirements. This trend makes it increasingly common in real-time systems that a job has execution requirement so large that executing it sequentially causes a deadline miss and hence, the only way for a job to meet its deadline is to perform some execution in parallel. Some software is inherently sequential, however, so a software system typically consists of parts that can execute in parallel and parts that cannot. This brings the challenge:

C1. Schedule software where some parts can execute in parallel so that all deadlines are met and prove before run-time that their deadlines are met.

Timing of software executing on a COTS multicore processor depends not only on the processor scheduler but also on contention for shared resources in the memory system. This includes (i) the last-level cache shared between processors, (ii) the row buffer in each memory bank storing the most recently accessed row, and (iii) the memory bus (the bus between the memory controller and DRAM memory modules). A cache memory is typically organized as a set of cache sets where certain bits of the physical address of a memory access determine which cache set the memory access should use. Hence, if the virtual-to-physical address translation is set up so that for the physical addresses generated, it holds that no two memory accesses of different tasks use the same cache set, then it is guaranteed that a cache block fetched to the cache by one task cannot be evicted by another task. Also, DRAM memories are typically organized as a set of banks with each bank having multiple rows and each bank having one row buffer which stores the data of the most recently accessed row. When a memory access experiences a miss in the shared cache, (i) precharging is performed, that is, the data in the row buffer is written back to its row in the memory bank and then (ii) the memory access activates a row in a memory bank (the memory bank is indicated by certain bits in the physical address of the memory access and the row is indicated by other bits) so this row is loaded in the row buffer of the memory bank and then (iii) the memory access reads data from this buffer and transfers the data to the processor (if the memory access is a load) or writes data to this row buffer (if the memory access is a store). If the row needed for a memory access is already loaded in the row buffer, then precharge and activate are not performed and hence execution is faster. For this reason, memory controllers reorder memory accesses so that memory accesses to the row that is in the row buffer get ahead in certain queues in the memory controller. Consequently, a memory access can be delayed because other memory accesses, of other tasks, get ahead in the queue (reordering effect). Hence, if the virtual-to-physical address translation is set up so that for the physical addresses generated by tasks, it holds that no two of them access the same bank, then it is guaranteed that no task can suffer from this reordering effect. In addition, a memory access can also be delayed because other accesses use the memory bus. This brings the challenges:

C2. Configure the virtual-to-physical address translation so that a cache block fetched to the last-level cache by one task cannot be evicted by another task.

C3. Configure the virtual-to-physical address translation so that reordering of memory accesses from different tasks are avoided and if they do occur, then the schedulability analysis computes an upper bound on the extra execution time due to reordering.

C4. Compute an upper bound on the extra execution time caused by processors sharing the memory bus.

The research literature offers solutions for each of these challenges (see Table I). Unfortunately, the research literature offers no solution for all these challenges.

Therefore, in this paper, we present a solution for all these challenges. We assume global-EDF (gEDF) is used and
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TABLE I: Summary of the state of art.

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This paper

A job of task \( \tau_i \) finishes when all the \( \text{nseg}_{\tau_i} \) segments of the \( \text{nstages}_{i} \)th stage of this job have finished.

gEDF assigns high priority to jobs with early absolute deadlines and a segment inherits the priority of the job it belongs to. At each instant, if at most \( m \) segments are eligible for execution at this instant, then all of them execute at this instant; if \( m + 1 \) or more segments are eligible for execution, then the \( m \) highest priority segments at this instant are selected for execution at this instant. A taskset \( \tau \) is gEDF schedulable on a computer with \( m \) processors of speed \( s \) if for each jobset that \( \tau \) can generate, for each schedule that gEDF can generate for this jobset, it holds that all deadlines are met.

Each segment of a stage of a task has a virtual address space. The virtual address space is organized into pages of size PAGESIZE. (For example, for x86, PAGESIZE=4096 bytes.) The memory footprint of a segment of the \( j^{th} \) stage of \( \tau_i \) is at most \( \text{nseg}_{\tau_i} \) pages. Each page is associated with a range of virtual addresses. A virtual address is mapped to a physical address as follows. The log\(_2\) PAGESIZE least significant bits of the virtual address are copied to the least significant bits of the physical address. (These least significant bits of the physical address are called frame offset.) The other bits of the virtual address are called page index and these are translated to a frame index and the bits of the frame index are copied to the most significant bits of the physical address. sharedframes denotes a set of 8-tuples so that for each 8-tuple \( \langle i', j', g', p', l', n', r', p'' \rangle \) it is required that page \( p' \) of the \( g'^{th} \) segment of the \( j'^{th} \) stage of \( \tau_{i'} \) is mapped to the same frame as page \( p'' \) of the \( g''^{th} \) segment of the \( j''^{th} \) stage of \( \tau_{i''} \).

We assume that for such 8-tuples \( \tau_{i'} = \tau_{i''} \) (because otherwise cache coloring, as we will see, does not work).

In our previous work [13], we presented and validated a model of the memory system of typical COTS multicore processor based systems. In this paper, we use a model that improves on that model by having a more fine-grained description of memory accesses. Our model is as follows. The last-level cache (LLC) is shared between processors. This cache is organized as a set of cache sets where certain bits in the physical address determine which cache set a memory access is associated with. Some of these bits are part of the frame index and some are part of the frame offset. When a memory access experiences a miss in LLC, the memory access is passed on to the memory controller and identifies which memory bank the memory access is associated with (other bits in the frame index determine this) and which row in this memory bank it is associated with.

When a job executing contiguously for \( \Delta \) time units performs \( \Delta \times s \) units of execution. We assume \( \forall \tau_i \in \tau : D_i \leq T_i \) — such tasksets are called constrained-deadline sporadic tasksets.

When a job of task \( \tau_i \) arrives, all the \( \text{nseg}_{\tau_i} \) segments of the \( 1^{st} \) stage of task \( \tau_i \) become eligible for execution. For each \( j \geq 2 \), at the time when all the \( \text{nseg}_{\tau_i} \) segments of the \( (j-1)^{th} \) stage of task \( \tau_i \) have finished, all the \( \text{nseg}_{\tau_i} \) segments of the \( j^{th} \) stage of task \( \tau_i \) become eligible for execution. A segment becomes non-eligible when it has finished execution.

The remainder of this paper is organized as follows. Section II presents the system model we use. Section III adapts a previously known schedulability test for gEDF to a MILP formulation. Section IV presents additional constraints that express an upper bound on the execution time of a segment due to memory contention and how it depends on memory mapping, and also express other constraints. Section V puts it all together as a solution for all the four challenges. Then follow discussions and conclusions.

II. System Model

Fig. 1 illustrates the model we consider. We consider a system with (i) a computer with \( m \) processors of speed \( s \) and (ii) a software system described as a taskset \( \tau \). A task \( \tau_i \) in \( \tau \) is characterized by \( T_i \), \( D_i \), \( \text{nstages}_{i} \), \( \text{nseg}_{\tau_i} \), and \( C_{l,j} \) with the interpretation that \( \tau_i \) generates a sequence of jobs where the arrival times of two consecutive jobs of \( \tau_i \) are separated by at least \( T_i \) and a job of \( \tau_i \) needs to finish execution by the deadline of the job (the absolute deadline of a job of \( \tau_i \) is \( D_i \) time units after its arrival) and execution requirement is described with stages where \( \text{nstages}_{i} \) denotes the number of stages of a job of \( \tau_i \) and \( \text{nseg}_{\tau_i} \) denotes the number of segments of the \( j^{th} \) stage of a job of \( \tau_i \). Let \( C_{l,j} \) denote an upper bound on the execution requirement of a segment of the \( j^{th} \) stage of \( \tau_i \) (explained later in this section). A job executing contiguously for \( \Delta \) time units performs \( \Delta \times s \) units of execution. We assume \( \forall \tau_i \in \tau : D_i \leq T_i \) — such tasksets are called constrained-deadline sporadic tasksets.

When a job of task \( \tau_i \) arrives, all the \( \text{nseg}_{\tau_i} \) segments of the \( 1^{st} \) stage of task \( \tau_i \) become eligible for execution. For each \( j \geq 2 \), at the time when all the \( \text{nseg}_{\tau_i} \) segments of the \( (j-1)^{th} \) stage of task \( \tau_i \) have finished, all the \( \text{nseg}_{\tau_i} \) segments of the \( j^{th} \) stage of task \( \tau_i \) become eligible for execution. A segment becomes non-eligible when it has finished execution.

...
of other memory banks. When a memory access is granted the memory bus, the memory access precharges its associated memory bank (that is, the data in the row buffer is written back to its row in the memory bank) and then the memory access activates its associated row in its associated memory bank (that is, the data in this row is loaded to the row buffer) and finally it transfers data (from the row buffer of the memory bank to the memory controller if the memory access is a load; the other direction if it is a store). If the row associated with the memory access is already in the row buffer then precharge and activate are not performed.

\( C_{i,j}(map) \) denotes an upper bound on the execution requirement of a segment in the \( j \)th stage of \( \tau_i \) for the case that this segment does not experience contention for resources in the memory system from other segments and \( map \) is the memory mapping of all tasks in the system. \( MA_{i,j,p}(map) \) denotes an upper bound on the number of memory accesses reaching the memory controller of page \( p \) in a segment in the \( j \)th stage of \( \tau_i \) for the case that this segment does not experience contention for resources in the memory system from other segments and \( map \) is the memory mapping of all tasks in the system.

In today’s processors, typically, the bits in the physical address from which the cache set index of LLC is obtained overlaps with the bits that determine the frame index (see [28]). Also, in today’s processors, typically, the bits in the physical address from which the index bank is obtained overlaps with the bits that determine the frame index (see [28]). Therefore, one can partition memory frames of physical memory into cache colors so if two memory accesses belong to different frames and these two memory frames belong to two different cache colors, then it holds that one memory access cannot evict a row in a memory bank that another memory access has loaded. \( H \) denotes the number of cache colors and \( B \) denotes the number of bank colors. MEMCAP denotes the amount of physical memory in the computer, measured in the number of frames. Some recent multicore chips use sliced LLC; such chips prevent us from using 100% of the main memory when using cache partitioning [14]. For this reason, let HWSHARE denote the share of physical memory that we may use. Let \( \text{CAP} = \text{HWSHARE} \times \text{MEMCAP} / (H \times B) \). (In a typical x86 computer today, \( \text{MEMCAP} = 2^{31} / 4096 = 2^{19}, H = 32, B = 16, \text{HWSHARE} = 1/4 \) and this yields \( \text{CAP} = (1/4) \times 2^{19} / (32 \times 16) = 2^{8} \))

Let \( C_{i,j} \) be a value such that \( \forall \text{map} : C_{i,j}(\text{map}) \leq C_{i,j} \).

Let \( MA_{i,j,p}(\text{map}) \) be a value such that \( \forall \text{map} : MA_{i,j,p}(\text{map}) \leq MA_{i,j,p} \). In practice, if the memory mapping map is known, then it is possible to obtain \( C_{i,j}(\text{map}) \) and \( MA_{i,j,p}(\text{map}) \) (e.g. using a worst-case execution-time analysis tool) but obtaining \( C_{i,j} \) and \( MA_{i,j,p} \) is very expensive because they describe behavior of the software for all possible memory mappings of the system. Even if \( C_{i,j} \) and \( MA_{i,j,p} \) are obtained, it can happen that our algorithm selects an abstract memory mapping \( o \) and we choose a memory mapping map that is compatible with \( o \) and that \( C_{i,j} \) is much higher than \( C_{i,j}(\text{map}) \) (and analogously for \( MA_{i,j,p}(\text{map}) \)). This would result in large pessimism. We will discuss (in Section VI) how to deal with these issues. For now, assume \( C_{i,j} \) and \( MA_{i,j,p} \) are known.

We assume (as do many previous studies [31, 22, 19]) that a processor is stalled when it waits for memory. We use some notation from [13], namely, the following:

\[
L_{\text{PRE}} = t_{CK} \quad (8)
\]

\[
L_{\text{ACT}} = \max(t_{\text{RRD}}, t_{\text{FAW}} - 3 \times t_{\text{RRD}}) \times t_{CK} \quad (9)
\]

\[
L_{\text{RW}} = \max(\text{WL} + BL/2 + t_{\text{WTR}}, CL + BL/2 - 2 - \text{WL}) \times t_{CK} \quad (10)
\]

\[
L_{\text{inter}} = L_{\text{PRE}} + L_{\text{ACT}} + L_{\text{RW}} \quad (11)
\]

\[
L_{\text{conf}} = t_{\text{RP}} + t_{\text{RCD}} + \max(\text{CL} + BL/2 + 2, \text{WL} + BL/2 + \max(t_{\text{WTR}}, t_{\text{WHR}})) \times t_{CK} \quad (12)
\]

\[
L_{\text{constit}}(x) = \left( \lfloor x/2 \rfloor \times (\text{WL} + BL/2 + t_{\text{WTR}}) + \lfloor x/2 \rfloor \times \text{CL} + \max(t_{\text{WHR}} - t_{\text{WTR}}) \right) \times t_{CK} \quad (13)
\]

Fig. 1: The model we consider.
\begin{align}
C_i & \overset{\text{def}}{=} \sum_{j=1}^{\text{netages}_j} (n\text{seg}_{i,j} \times C_{i,j}) \\
\eta_i & \overset{\text{def}}{=} \sum_{j=1}^{\text{netages}_j} \left( \left\lfloor \frac{n\text{seg}_{i,j}}{m} \right\rfloor \times C_{i,j} \right)
\end{align}

\begin{align}
\text{WJS}(i, t, \tau, m, s) & \overset{\text{def}}{=} \left\{ \begin{array}{ll}
0 & \text{if } t < 0 \\
\text{WJS}(i, t - 1, \tau, m, s) & \text{if } 0 \leq t < \frac{\tau}{m} \\
\text{bsp}_{i,j} & \text{if } \frac{\tau}{m} \leq t \leq \frac{\tau}{m} + \frac{\eta_i}{m} \\
\text{sp}_{i,j} & \text{if } \frac{\tau}{m} + \frac{\eta_i}{m} < t \leq \frac{\tau}{m} + \frac{\eta_i}{m} + 1 \\
\end{array} \right.
\text{bsp}_{i,j} & \overset{\text{def}}{=} \frac{C_{i,j}}{m} \times n\text{seg}_{i,j} \\
\text{sp}_{i,j} & \overset{\text{def}}{=} \frac{C_{i,j}}{m} \times \left\lfloor \frac{n\text{seg}_{i,j}}{m} \right\rfloor
\end{align}

\begin{align}
U\text{BOMR} = \text{max}_{s \in [1, \text{netages}_i]} \text{seg}_{i,j}^{*} & \overset{\text{def}}{=} \text{UBOMR} = \text{min}(m - 1, \text{UBOMR} - 1) + \text{N}_{\text{re}}.
\end{align}

Tasks typically perform execution and access memory in an initialization phase which does not have real-time requirements. This execution and memory accesses are not considered as a job but the pages accessed need to be mapped to memory frames. Therefore, INO indicates the number of pages accessed during initialization.

### III. Schedulability Analysis for gEDF of Parallel Tasks

Previous work [1] provided a schedulability test for this problem for the special case that contention for resources in the memory system does not occur. Fig. 2 shows this schedulability test. We will now discuss how to modify this schedulability test slightly and then rewrite it as MILP.

Let us choose a value of \( K \) that is a positive integer (e.g. \( K = 20 \)). In the schedulability test expressed by Fig. 2, check only those \( \sigma \) such that there is a \( k \in \{1, 2, \ldots, K\} \) such that \( \sigma = (k/K) \times s \). This yields the following schedulability test with a slight increase in pessimism:

\begin{align}
\text{h}^{*}(\tau, m, s, k, K, t) & \overset{\text{def}}{=} \left( \sum_{\tau_j \in \tau} \text{ffdbf}(\tau_i, t, k, K, s) \right) \leq (m - (m - 1) \times K) \times t \\
\text{f}^{*}(\tau, m, s, K) & \overset{\text{def}}{=} \left( \exists k \in [1, \ldots, K] \text{ such that } (k \times s = \text{max}_{\tau_j \in \tau} \eta_i) \land (\forall t \text{ such that } t \geq 0 : \text{h}^{*}(\tau, m, s, k, K, t)) \right)
\end{align}

Clearly, \( t = \left\lfloor \frac{t}{P} \right\rfloor \times P + t \mod P \). Thus

\begin{align}
\sum_{\tau_j \in \tau} \text{ffdbf}(\tau_j, t, k, K) = \left( \sum_{\tau_j \in \tau} C_{i,j} \right) \times t \mod P
\end{align}

Consequently, when evaluating \( \forall t \text{ such that } t \geq 0 : \text{h}^{*}(\tau, m, s, k, K, t) \), it is only necessary to consider values of \( t \) that are at most \( P \). Hence, \( \text{f}^{*}(\tau, m, s, K) \) is true if and only if there is an assignment of values satisfying:

\begin{align}
\forall k \in [1, K] : w_{ik} \geq 1 \text{ and } \forall k \in [1, K] : w_{ik} \in \{0, 1\}
\end{align}

Observe that the left-hand side of the inequality defining \( \text{h}^{*}(\tau, m, s, k, K, t) \) is a piecewise linear function of \( t \) and the right-hand side of the inequality defining \( \text{h}^{*}(\tau, m, s, k, K, t) \) is a linear function of \( t \). Hence, when evaluating \( \forall t \text{ such that } t \in [0, P) : \text{h}^{*}(\tau, m, s, k, K, t) \) it is only necessary to evaluate \( \text{h}^{*}(\tau, m, s, k, K, t) \) for the following values of \( t \): (i) values of \( t \) such that the derivative of the piecewise linear function changes, (ii) \( t = P \), and (iii) \( t = 0 \). With respect to (ii), note that \( \text{h}^{*}(\tau, m, s, k, K, 0) \) is true and hence it does not need to be checked. With respect to (iii), note that \( \text{h}^{*}(\tau, m, s, k, K, t) \) can be rewritten as ((\( \text{WJS}(i, t, \tau, m, s) \leq (m - (m - 1) \times (k/K)) \times s \)). Then, with respect to (i), note that for \( t \) such that there is a positive integer \( q' \) and a task \( \tau_{q'} \in \tau \) such that \( t = (q' - 1) \times T_{\tau'} + D_{\tau'} - \frac{\eta_i}{s} \times (k/K) \), the above mentioned derivative changes but this \( t \) is dominated by other \( t's \) in the condition and hence, \( t \) does not need to
be checked. Hence, \( f^*(\tau, m, s, K) \) is true if and only if there is an assignment of values satisfying: \( \sum_{k=1}^{K} w_{ik} \geq 1 \) and 
\[ k \in [1, K] : w_{ik} \in [0, 1] \]
\( \forall (i, k) \text{ such that } (\tau_i \in \tau) \land (k \in [1, K]) : (w_{ik} = 1 \Rightarrow (\eta_i \leq \frac{k \times k \times D_i}{K}) \]
\( \forall (i', q', j', f', k) \text{ such that } (\tau_i \in \tau) \land (q' \in [1, P/T_i]) \land \]
\( j' \in [0, \text{nastages}, r - 1] \land (f' \in [0, 1]) \land (k \in [1, K]) : t_{i', q', j', f', k} = \)
\( \forall (i', q', j', f') \text{ such that } (\tau_i \in \tau) \land (q' \in [1, P/T_i]) \land \]
\( j' \in [0, \text{nastages}, r - 1] \land (f' \in [0, 1]) \land (k \in [1, K]) : (w_{ik} = 1) \Rightarrow \)
\( \left( \sum_{\tau_i \in \tau} \text{fflb}(\tau_i, i', q', j', f', k) \times \frac{k}{K} \times s \right) \leq (m - (m - 1) \times \frac{k}{K} \times t_{i', q', j', f', k} \times s) \]
\( \forall k \text{ such that } k \in [1, K] : (w_{ik} = 1) \Rightarrow \)
\( \left( \sum_{\tau_i \in \tau} C_{ij} \right) \leq (m - (m - 1) \times (k/K) \times s) \)

We will now rewrite \( \text{fflb}(\tau_i, i', q', j', f', k) \times \frac{k}{K} \times s \) to a form closer to MILP. Define \( I_{i', q', j', f', k} \times \frac{k}{K} \times s \) so that \( I_{i', q', j', f', k} \times \frac{k}{K} \times s \) is called, the first case in the definition of \( WJ \) is taken; otherwise \( \text{fflb}(\tau_i, i', q', j', f', k) = 0 \).

Then, using (4), rewrite \( \text{fflb}(\tau_i, i', q', j', f', k) \times \frac{k}{K} \times s \) as:
\[ a_{i', q', j', f', k} - WJ(\tau_i, (D_i - r_{i', q', j', f', k}) \times \frac{k}{K}, s) \]

We introduce \( w_{i,j,f,s}, w_{j,s}, w_{j,s} \), and \( w_{j,s} \) as:

1. \( w_{i,j,f,s} = 1 \) means that when \( WJ(\tau_i, (D_i - r_{i', q', j', f', k}) \times \frac{k}{K}, s) \) calls the first case in the definition of \( WJ \) is taken; otherwise \( w_{i,j,f,s} = 0 \).
2. \( w_{j,s} = 1 \) means that when \( WJ(\tau_i, (D_i - r_{i', q', j', f', k}) \times \frac{k}{K}, s) \) calls the second case in the definition of \( WJ \) is taken and recursion is performed in WJS in which stage \( j \) is the last entire stage covered and the first case in (3) is taken; otherwise \( w_{j,s} = 0 \).
3. \( w_{s,s} = 1 \) means that when \( WJ(\tau_i, (D_i - r_{i', q', j', f', k}) \times \frac{k}{K}, s) \) calls the second case in the definition of \( WJ \) is taken and recursion is performed in WJS in which stage \( j \) is the last entire stage covered and the second case in (3) is taken; otherwise \( w_{s,s} = 0 \).
4. \( w_{i,j,f,s} = 1 \) means that when \( WJ(\tau_i, (D_i - r_{i', q', j', f', k}) \times \frac{k}{K}, s) \) calls the third case in the definition of \( WJ \) is taken; otherwise \( w_{i,j,f,s} = 0 \).

Elaborating on this yields that \( f^*(\tau, m, s, K) \) is true if and only if there is an assignment of values to variables such that the constraints in Fig. 3 are satisfied. In Fig. 2, \( C_{i,j} \) denotes the upper bound on the execution requirement of a segment in the \( j \)th stage of task \( \tau_i \) but in Fig. 3 \( c_{i,j} \) denotes this. \( c_{i,j} \) means execution requirement that we will use.

IV. MEMORY CONTENTION

Previous work [13] provided a method for computing an upper bound on the response time of a task considering contention for resources in the memory system. That method assumes fixed-priority preemptive non-migrative scheduling and integrates the memory contention analysis in the schedulability analysis. In this section, we will adapt this memory contention analysis (i) to compute an upper bound on the extra execution time of a segment of a single job of a task and do it without assuming any specific processor scheduling algorithm and (ii) expressing it on a form easily translatable to MILP.

Let \( c_{i,j} \) denote an upper bound on the execution requirement of the \( g \)th segment of the \( j \)th stage of task \( \tau_i \) considering contention for resources in the memory system (the extra execution of this contention is considered to be part of the execution requirement). Also, recall that \( c_{i,j} \) was defined in the previous section. We will now redefine it. Let \( c_{i,j} \) denote an upper bound on the execution requirement of a segment of the \( j \)th stage of task \( \tau_i \) considering contention for resources in the memory system (the extra execution of this contention is considered to be part of the execution requirement). Hence:

\[ c_{i,j} = \max_{g \in \{1, \ldots, n_{o_{i,j}}\}} c_{i,j,g} \]  
(34)
∀(i′, q′, j′, f′, k) such that (τi ∈ τ) ∧ (q′ ∈ [1, P/Ti]) ∧ (j′ ∈ [0, nstagesj − 1]) ∧ (f′ ∈ {0, 1}) ∧ (k ∈ [1, K]) : 

(∀q′ ∈ [1, P/Ti]) ∧ (j′ ∈ [0, nstagesj − 1]) ∧ (f′ ∈ {0, 1}) ∧ (k ∈ [1, K]) : 

∀(i′, q′, j′, f′, k) such that (τi ∈ τ) ∧ (q′ ∈ [1, P/Ti]) ∧ (j′ ∈ [0, nstagesj − 1]) ∧ (f′ ∈ {0, 1}) ∧ (k ∈ [1, K]) : 

∀(i′, q′, j′, f′, k) such that (τi ∈ τ) ∧ (q′ ∈ [1, P/Ti]) ∧ (j′ ∈ [0, nstagesj − 1]) ∧ (f′ ∈ {0, 1}) ∧ (k ∈ [1, K]) :
upper bound on the number of memory accesses on memory bank  \( b \) from multiple jobs of all other segments than the \( g \)th segment of the \( j \)th stage of task \( \tau_i \) can suffer from because of the other \( \text{mmbo}_{i,j,g,b} \) memory accesses from other segments access memory of bank  \( b \) and hence contend on the queue for memory bank  \( b \).

Now consider memory contention. Look at the queues inside the memory controller in Fig. 1. Consider the \( g \)th segment of the \( j \)th stage of task \( \tau_i \) and its (at most \( \text{mbl}_{i,j,g,b} \)) memory accesses that it performs on memory locations of memory bank  \( b \). Let \( \text{coat}_{i,j,g,b} \) denote an upper bound on the extra execution time of this segment because other memory accesses (from other segments) access this bank (bank  \( b \)). Let \( \text{oao}_{i,j,g,b} \) denote an upper bound on the number of other memory accesses that causes extra execution time of this segment because other memory accesses (from other segments) access other banks (than bank  \( b \)). Then, we express \( \text{cm}_{i,j,g} \) as

\[
\text{cm}_{i,j,g} = C_{i,j} + s \times \sum_{h=0}^{B-1} \left( \text{coat}_{i,j,g,b} + L_{\text{inter}} \times \text{oao}_{i,j,g,b} \right)
\]

In the above equation, we multiply by  \( s \) because \( \text{coat}_{i,j,g,b} \) and \( L_{\text{inter}} \times \text{oao}_{i,j,g,b} \) measure execution time whereas \( \text{cm}_{i,j,g} \) measures execution requirement.

We will now find expressions for \( \text{coat}_{i,j,g,b} \) and \( \text{oao}_{i,j,g,b} \). For this purpose, look again at the queues inside the memory controller in Fig. 1. A single memory access accessing bank  \( b \) can be delayed by the following:

1) There are already memory accesses in the queue of bank  \( b \) when this single memory access is inserted in the queue of bank  \( b \) and because of FIFO queuing, these other memory accesses are served first.

2) After this single memory access is enqueued in the queue for bank  \( b \), there are other memory accesses enqueued in this bank and these other memory accesses’ row is currently loaded in the row buffer and hence they get ahead in the queue for this memory bank (reordering).

3) When one of the other memory accesses mentioned in 1) or 2) reaches the head of the queue of bank  \( b \), it is not served immediately; instead it has to wait for the memory bus being granted and this takes time because other memory accesses in the queues to other memory banks than bank  \( b \) use the memory bus.

About 1) and 2) Since we assume a processor stalls until its memory access has been completed, it follows that other memory accesses performing on bank  \( b \) (because of 1) and 2) above). Let \( \text{oao}_{i,j,g,b} \) be the expression in (36). (It means other accesses to this bank.) By inspecting \( L_{\text{conhit}}(x) \) and the parameters in Section II, one can see that these memory accesses have different effects; the memory accesses that are in the queue before a memory access has arrived to the queue cause more interference than the ones that arrive later that cause reordering. Fig. 4 shows an upper bound.

About 3) A memory access related to memory bank  \( b \) is inserted in the queue for the memory bus only if (i) this memory access is at the head of the queue of the memory bank  \( b \) and (ii) there is no memory access related to memory bank  \( b \) already in the queue of the memory bus. Hence, a memory access that has reached the head of the queue of its memory bank needs to wait for at most \( B-1 \) other memory accesses until it is granted the memory bus. Consequently, the \( \text{mbl}_{i,j,g,b} \) memory accesses from the \( g \)th segment of the \( j \)th stage of task \( \tau_i \) performing on bank  \( b \) has to wait for at most \( \min\{\text{mbl}_{i,j,g,b} \times \text{LIM2}, \text{mmbo}_{i,j,g,b}\} \) (36).

This reasoning yields an upper bound on the execution requirement of a segment on a form close to MILP — see Fig. 5.

V. THE MILP FORMULATION

Let \( \Pi \) denote the computer platform (the parameters \( m, s, H, B \) and the parameters describing the memory system). \( \text{fnem}(\pi, H, K) \) is a function which returns the tuple \( (\text{flag}, o) \) where \( \text{flag} \) is a boolean and \( o \) is a multi-dimensional array. If there exists an assignment of values to the variables so that the constraints in Fig. 3 and Fig. 5 are satisfied then \( \text{flag} \) is
Theorem 1. 

\[ ((\text{flag}, o) = \text{fmem}(\tau, \Pi, K)) \land (\text{flag} = \text{true}) \] 
\[ \Rightarrow \tau \text{ is gEDF schedulable on a computer with } m \text{ processors of speed } s \text{ for the case that tasks experience memory contention and the memory mapping is compatible with } o \]

Proof: If the theorem is false then there exists a \( \tau, m, s, K \) and an assignment of the number of jobs that each task generates and an assignment of arrival time to jobs and execution requirement of segments and a schedule such that the following two statements are true:

1) \( ((\text{flag}, o) = \text{fmem}(\tau, \Pi, K)) \land (\text{flag} = \text{true}) \)
2) for the jobset generated by \( \tau \) with the aforementioned assignment, it holds that gEDF can generate the aforementioned schedule and there is at least one job that misses its deadline in this schedule.

For this schedule, let \( t_0 \) denote the earliest time when a deadline miss occurs. Remove all jobs with arrival time \( \geq t_0 \). There is still a deadline miss at time \( t_0 \). Let us now reason as follow: For each job with absolute deadline \( > t_0 \) such that it performs execution after time \( t_0 \), do the following: identify the latest stage of this job such that there is a segment of this stage that performs execution after \( t_0 \). Then reduce the execution of this segment. Repeated application of this yields that no job with absolute deadline \( > t_0 \) performs execution after time \( t_0 \). Hence, it holds that: (i) 1) and 2) above are true, (ii) one or many jobs with absolute deadline at \( t_0 \) misses deadlines, (iii) each job with absolute deadline \( < t_0 \) meets its deadline, (iv) all jobs have arrival times \( < t_0 \), and (v) no job with absolute deadline \( > t_0 \) performs execution after time \( t_0 \).

For each job with absolute deadline \( < t_0 \), we can reason as follows: Let \( \tau_i \) denote the task that generates the job. Let \( A \) denote the arrival time of this job and consider the time interval \([A, A + D_i]\) and consider a task \( \tau_i' \) which is not the task that generated the job of task \( \tau_i \). Because of (iii) and (iv), there can be at most one job of task \( \tau_i' \) such that this job arrives before \( A \) and it has execution that overlaps with \([A, A + D_i]\). Also, because of (iii), there can be at most \([D_i/T_{\tau_i'}]\) jobs of task \( \tau_i' \) such that this job arrives at or after \( A \) and it has execution that that overlaps with \([A, A + D_i]\).

For each job with absolute deadline \( \geq t_0 \), we can reason as follows: Let \( \tau_i \) denote the task that generates the job. Let \( A \) denote the arrival time of this job and consider the time interval \([A, A + D_i]\) and consider a task \( \tau_i' \) which is not the task that generated the job of task \( \tau_i \). Because of (iii) and (iv), there can be at most one job of task \( \tau_i' \) such that this job arrives before \( A \) and it has execution that overlaps with \([A, A + D_i]\). Also, because of (v), there can be at most \([D_i/T_{\tau_i'}]\) jobs of task \( \tau_i' \) such that this job arrives at or after \( A \) and it has execution that that overlaps with \([A, A + D_i]\).

Consequently, for each of these cases, there are at most \((\lceil D_i/T_{\tau_i'} \rceil + 1) \times m\) memory accesses on bank \( b \) of jobs of the \( g^{th} \) segment of the \( j^{th} \) stage of task \( \tau_i' \) that overlaps with \([A, A + D_i]\). This expression is the right-hand side of the expression of (39). Hence, there are at most \( mmb_{i,i',j',g,b} \) memory accesses of jobs of the \( g^{th} \) segment of the \( j^{th} \) stage of task \( \tau_i' \) that overlaps with \([A, A + D_i]\). Since we know the values of \( mmb_{i,i',j',g,b} \), using Fig. 5 yields \( c_{ui,j,g} \). This yields \( c_{ui,j} \) which provides an upper bound on the execution requirement. Since \( c_{ui,j} \) is an upper bound on execution requirement we can treat the system as if there was no contention for resources in the memory system and execution requirements were given by \( c_{ui,j} \). Since the constraints in Fig. 3 are satisfied, all deadlines are met. This contradicts 2) above. Hence, the theorem is correct.

Note that some of the constraints mentioned are not MILP — they have binary variables and logical operators. We will discuss this now. A constraint of the form \( (x = 1) \Rightarrow (a \leq b) \) can be rewritten as: \( ((x = 1) \Rightarrow (a \leq b)) \land ((x = 1) \Rightarrow (a \geq b)) \). Note that if \( x \) is a variable with the domain \( \{0, 1\} \) and \( a \) and \( b \) are non-negative real variables and \( \text{BIG} \) is a constant selected so that \( a \leq \text{BIG} \) and \( b \leq \text{BIG} \), then a constraint \( (x = 1) \Rightarrow (a \leq b) \) can be rewritten as:

\[ a - b + \text{BIG} \times x \leq \text{BIG} \] (68)

Note that in a feasible solution to Fig. 3 and Fig. 5, for the variables in the constraints (52)-(67), the variable is at most

\[ \max_{\tau_i \in \tau} \sum_{j \leq \tau_i} ((\lceil D_{\tau_i}/T_{\tau_i'} \rceil + 1) \times (\sum_{j \in [1,t_{\tau_i'}]} \sum_{j' \in [0,t_{\tau_i']}} \sum_{p'} \sum_{m}' \sum_{\text{MA}_{j',p'}})) \] (69)

Hence, for the constraints (52)-(67), the left-hand side (lhs) is at most

\[ \max (2 \times (B - 1), L_{\text{conf}} + L_{\text{inter}}) \times (69) \] (70)

Also, for each of the other constraints, the lhs is at most

\[ (P + \text{DMAX}) \times m \times \max(1, s) + H \times B \] (71)

Applying the rewriting expressed by (68) (and minor variants of it), with \( \text{BIG} = \max(70), 71) \), yields that all of our constraints can be converted to a MILP.

VI. DISCUSSION

Recall (from Section II) that in general, it is possible to obtain (e.g. using a worst-case execution-time analysis tool) \( C_{i,j}(\text{map}) \) and \( \text{MA}_{i,j,p}(\text{map}) \) but it is very expensive to obtain \( C_{i,j} \) and \( \text{MA}_{i,j,p} \). This can be dealt with by guessing values of the latter and call the function \( \text{fmem}(\tau, \Pi, K) \) and then obtain a new memory mapping and then for this memory mapping, check whether the guess was valid. Also, note that solving the MILP produces an abstract memory mapping \( o \). It is abstract because it does not specify exactly to which memory frame a page should be mapped; it only specifies to which cache color and bank color a memory page should be mapped. We assume a method exists that converts the abstract mapping \( o \) to a mapping \( m \) that specifies for each page which frame it maps to (it is trivial to create it). An algorithm based on these ideas is shown below:

1) Choose a value of \( K \) (for example \( K = 20 \))
2) Choose a value of maxiter (for example maxiter = 3)
3) Choose one abstract memory mapping \( o' \)
4) for \( \text{iter} = 1 \) to maxiter do
5) choose a memory mapping \( m' \) that is compatible with the
6) abstract memory mapping \( o' \)
7) \forall i,j : \text{obtain } C_{i,j}(\text{map}') \text{ and assign } C_{i,j}^\text{guess} := C_{i,j}(\text{map}')
8) \forall i,j,p : \text{obtain } \text{MA}_{i,j,p}(\text{map}) \text{ then assign } \text{MA}_{i,j,p}^\text{guess} := \text{MA}_{i,j,p}(\text{map})
9) \langle \text{flag}, o \rangle = \text{fmem}(\tau, \Pi, K); \text{in this call, assume that}
10) \forall i,j : \text{obtain } \text{MA}_{i,j,p}(\text{map}) \text{ then assign } \text{MA}_{i,j,p}^\text{guess} := \text{MA}_{i,j,p}(\text{map})
11) if flag then
12) choose a memory mapping \( m' \) that is compatible with the
13) abstract memory mapping \( o' \)
ONCLUSIONS

VII. C

COTS multicore processors are the norm today but their use for hard real-time systems is challenging because (i) in order to take full advantage of such platforms for meeting tight deadlines, parallelization is necessary and (ii) the contention for shared resources in the memory system makes execution times hard to predict. In this paper, we have developed a solution that addresses these issues. Our main idea is to formulate a MILP that configures the memory mapping and performs schedulability analysis.

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