A key requirement for the effective use of multiprocessors in real-world applications is an ability to accurately predict the performance of a specific algorithm on a specific architecture. This research developed such a prediction methodology, which permits separate evaluation of algorithm and architecture performance, with only a small number of "cross" parameters required to link the models. Additional results include program behavior models that lead to effective trace compression techniques.
Models of Multiprocessor Architectures and Algorithms

Final Report

Eric E. Johnson

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U.S. Army Research Office

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New Mexico State University

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The views, opinions, and findings contained in this report are those of the author and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.
Statement of the Problem Studied

A key requirement for the effective use of multiprocessor systems in real-world applications is an ability to accurately predict the performance of a specific algorithm on a specific architecture. Such performance prediction tools assist the system designer in initially selecting suitable algorithms and architectures, and then in modifying them to improve performance.

Existing techniques for joint performance prediction of multiprocessor algorithms and architectures generally require joint evaluation of the model for each algorithm/architecture pair of interest. This results in significantly more computation than an approach that models algorithms and architectures separately, with joint performance computed from the individual performance measures. In addition, the accuracy of current techniques is often affected by assumptions about algorithm and architectural behavior for which few measurements have been available.

The objective of this research was to extend our previous work in modeling multiprocessor and distributed system performance to produce an efficient, accurate performance prediction methodology applicable to Army systems. This technique is based upon measurements of important applications, and permits separate evaluation of algorithm and architecture performance with only a small number of "cross" parameters required to link the two models.

Specific Aims: Measure the characteristics of parallel computer programs of the types used in Army systems, validate a theoretical model of parallel computer system performance, establish a data base of parallel computing performance measurements for Internet access.

Findings: Researchers supported by this contract developed the following:

1. An efficient, accurate methodology for predicting the performance of algorithms on parallel architectures. This methodology was validated both in our own work and by outside researchers.

2. A parallel algorithm for tracking multiple targets in video imagery that is portable among nearly all parallel architecture classes, and that scales well from small to large multiprocessors. Apart from its direct utility in Army programs, this algorithm is a useful vehicle for validating our performance prediction model over a very wide range of parallel machines.

3. A portable parallel architecture simulator and cache simulator.

4. A model of redundancy in instruction and data traces that can be applied to reduce trace sizes by up to two orders of magnitude. The significance of the later result is evident in the widespread use of our PDATS trace format in the computer architecture community.

5. A database of uniprocessor and multiprocessor traces that is in use by researchers worldwide.

6. Hardware to capture complete and filtered traces in real time from uniprocessors and multiprocessors.

Manuscripts Submitted


Publications and Technical Reports


Scientific personnel supported by this project and degrees awarded:

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<td>Stan Dixon</td>
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<td>Alan Taylor</td>
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<td>Sudhan Das</td>
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