In this paper, we report a promising approach for fabricating large-scale flexible and stretchable electronics using a semiconductor-enriched carbon nanotube solution. Uniform semiconducting nanotube networks with superb electrical properties (mobility of ~20 cm^2 V^{-1} s^{-1} and ION/IOFF of ~10^4) are obtained.
ABSTRACT

In this paper, we report a promising approach for fabricating large-scale flexible and stretchable electronics using a semiconductor-enriched carbon nanotube solution. Uniform semiconducting nanotube networks with superb electrical properties (mobility of \( \mu \gtrsim 20 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \) and ION/IOFF of \( \gtrsim 10^4 \)) are obtained on polyimide substrates. The substrate is made stretchable by laser cutting a honeycomb mesh structure, which combined with nanotube network transistors enables highly robust conformal electronic devices with minimal device-to-device stochastic variations. The utility of this device concept is demonstrated by fabricating an active-matrix backplane (12 × 8 pixels, physical size of 6 × 4 cm²) for pressure mapping using a pressure sensitive rubber as the sensor element.
Carbon Nanotube Active-Matrix Backplanes for Conformal Electronics and Sensors

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Supporting Information

ABSTRACT: In this paper, we report a promising approach for fabricating large-scale flexible and stretchable electronics using a semiconductor-enriched carbon nanotube solution. Uniform semiconducting nanotube networks with superb electrical properties (mobility of \( \sim 20 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1} \)) and \( I_{\text{ON}}/I_{\text{OFF}} \) of \( \sim 10^5 \) are obtained on polyimide substrates. The substrate is made stretchable by laser cutting a honeycomb mesh structure, which combined with nanotube-network transistors enables highly robust conformal electronic devices with minimal device-to-device stochastic variations. The utility of this device concept is demonstrated by fabricating an active-matrix backplane (\( 12 \times 8 \) pixels, physical size of \( 6 \times 4 \text{ cm}^2 \)) for pressure mapping using a pressure sensitive rubber as the sensor element.

KEYWORDS: Carbon nanotube electronics, macroelectronics, artificial electronic skin, stretchable sensors, semiconductor-enriched nanotubes, flexible backplane

In recent years, flexible and stretchable electronics have been intensively explored for enabling new applications otherwise unachievable with the conventional Si technology. 1–3 A wide range of active channel materials have been explored, including organics;4–6 amorphous,7,8 poly-12,13 and single-crystalline semiconductors in the shape of thin films and strips;9,14,15 printed semiconducting nanowires (NWs);16–18 and single-walled carbon nanotubes (SWNTs).19,20 Each of these material systems presents unique opportunities and challenges for large-area electronics. For instance, randomly deposited films of SWNTs are attractive candidates given their high carrier mobility, high chemical stability, ability to deposit through solution processing, and superb mechanical properties such as high bendability.21–23 A challenge, however, has been to fabricate devices with high ON/OFF current ratio, given that nanotube networks often consist of a mixture of semiconductor and metallic SWNTs.24 In this regard, highly semiconductor-enriched (99%) SWNTs have been recently reported and commercialized through the use of a density gradient ultracentrifugation technique.25,26 This development has allowed for the fabrication of high performance SWNT thin-film transistors (TFTs) that exhibit high \( I_{\text{ON}}/I_{\text{OFF}} \) (\( > 10^5 \)) and mobility (\( > 10 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1} \)) on rigid Si substrates.27–30

This presents an important advance in the field and could result in the development of highly scalable and low-cost electronics with performances drastically superior to those of conventional organics or a-Si. Here, we extend on this work and report the development of mechanically flexible and stretchable active-matrix backplanes based on semiconductor-enriched SWNT networks. We demonstrate fully passivated and highly uniform SWNT TFT arrays, covering large areas of \( \sim 7.5 \text{ cm} \times 7.5 \text{ cm} \). As an example system, we utilize this active-matrix backplane for an artificial electronic skin (e-skin) device,8,9,16,31 capable of spatial mapping of touch.

The device schematic of a mechanically deformable active-matrix backplane based on SWNT TFTs is shown in Figure 1a. A 24 \( \mu \text{m} \) thick polyimide (PI) layer (PI-2525, HD MicroSystem) is used as the substrate. First, the PI is spin-coated twice (2000 rpm for 1 min) on a Si/SiO\(_2\) handle 4 in. wafer, followed by Ni gate electrode deposition by thermal evaporation. The gate oxide consists of three layers with a 20 nm thick Al\(_2\)O\(_3\) layer deposited by atomic layer deposition (ALD) sandwiched between electron-beam deposited SiO\(_2\) layers (thicknesses, 10 and 15 nm on bottom and top, respectively). The bottom SiO\(_2\) layer is used to enable nucleation of ALD Al\(_2\)O\(_3\) on the substrate, while the top SiO\(_2\) layer is used for adhesion of SWNTs. Note that it is observed that SWNTs are highly nonstick to ALD Al\(_2\)O\(_3\) surfaces, presumably due to fixed charges in the as-deposited alumina layer. To deposit highly dense and uniform SWNT networks, the SiO\(_2\) surface is modified with poly-L-lysine by solution casting for \( \sim 5 \text{ min} \) followed by a rinse with DI water. In this study, we use as-received 99% semiconductor enriched SWNT solution (IsoNanotubes-S from NanoIntegris, Inc.)

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without any densification. SWNTs were then deposited by solution casting followed by rinse with DI water.

Figure 1b shows the atomic force microscopy (AFM) images of the SWNT coated substrates for three different nanotube deposition times. As evident, the density of SWNTs on the evaporated SiO$_x$ depends on the deposition time and is estimated to be $\sim 6$, 8, and 10 SWNTs/$\mu$m for the deposition time of 5, 30, and 90 min, respectively (Figure 1b). It should be noted that the density of SWNTs as a function of deposition time is highly dependent on the particular surface being explored. For instance, higher densities of SWNTs with higher bundling probability are observed for similar deposition times on thermally grown SiO$_2$ layers (see Supporting Information, Figure S2). Furthermore, the density depends on the surface functionalization of the substrate and the nanotube surfactants (Supporting Information, Figure S1). Next, vacuum annealing at 200 °C for 1 h is performed to remove surfactant residues. This annealing process is essential to improve both the transconductance and $I_{ON}/I_{OFF}$ of the devices (see Supporting Information, Figure S3). Pd (thickness, $\sim 35$ nm) source/drain (S/D) electrodes are then patterned using photolithography, metallization, and lift-off to enable ohmic contacts to the valence band of nanotubes for hole transport.$^{32}$ Finally, the fabrication process is completed by encapsulating the active matrix with parylene-C ($\sim 500$ nm) to improve the mechanical robustness and chemical stability by removing environmental effects, including surface-absorbed water molecules (Figure 1a). Via contacts are made by pattern etching of parylene using photolithography and O$_2$ plasma etch. After the completion of the entire process, the PI layer is readily peeled off from the handling wafer, resulting in a mechanically flexible device. Here, after cutting the edge of the substrate with a razor blade, the PI layer is readily released due to the poor adhesion between PI and SiO$_2$. During this process no breakage of the metal lines or active regions is observed due to the parylene encapsulation.

Figure 2a shows the transfer characteristics of SWNT TFTs measured at $V_{DS} = -5$ V for three different deposition times. For each condition, 30 devices with channel length of $L \sim 3 \mu$m and width of $W \sim 250 \mu$m are randomly chosen across a 4 in. substrate and measured to study the stochastic device-to-device fluctuation. Figure 2b–e shows the histograms of width-normalized transconductance, peak field-effect mobility, log-scale of $I_{ON}/I_{OFF}$, and threshold voltage for each deposition condition. In (b,d), the devices are measured at $V_{DS} = -5$ V, and in (c,e) the devices are measured at $V_{DS} = -50$ mV. (f) Peak field-effective mobility as a function of $I_{ON}/I_{OFF}$ for various measured devices. Here, the channel length is $\sim 3 \mu$m and width is $250 \mu$m.

$V_{DS} = -5$ V for three different deposition times of 5, 30, and 90 min, corresponding to different nanotube densities. (b–e) Histograms of width-normalized transconductance, peak field-effect mobility, log-scale of $I_{ON}/I_{OFF}$, and threshold voltage for each deposition condition. In (b,d), the devices are measured at $V_{DS} = -5$ V, and in (c,e) the devices are measured at $V_{DS} = -50$ mV. (f) Peak field-effective mobility as a function of $I_{ON}/I_{OFF}$ for various measured devices. Here, the channel length is $\sim 3 \mu$m and width is $250 \mu$m.
threshold voltage are measured at $V_{DS} = -50$ mV. Calculation of the gate oxide capacitance must be addressed in the case of the SWNT network device. Here, the effect of electrostatic coupling between nanotubes is considered with the following equation:

$$C_i = \left\{ \frac{1}{2\pi \varepsilon} \ln \left[ \frac{A_0}{R} \frac{\sinh \left( \frac{\pi d}{A_0} \right)}{\pi} \right] + C_Q^{-1} \right\}^{-1} A_0^{-1}$$

where $1/A_0$ is the density of nanotubes, $C_Q = 4.0 \times 10^{-10}$ F/m is the quantum capacitance of nanotubes (refs 34 and 35), $d$ is the oxide thickness, and $R = 0.7$ nm is the average radius of nanotubes. The calculated gate oxide capacitance values are $2.45 \times 10^8$ F/cm$^2$, $3.16 \times 10^8$ F/cm$^2$, and $3.78 \times 10^8$ F/cm$^2$ for SWNT deposition time of 5, 30, and 90 min, respectively. The field-effect mobility can then be extracted as $\mu = (L/V_{DS}C_i)(g_m/W)$. As the nanotube deposition time increases from 5 to 90 min, average peak $g_m$ increases from ~0.4 to 1.5 $\mu$S/um at $V_{DS} = -5$ V, resulting in an increased hole mobility from ~18 to ~27 cm$^2$ V$^{-1}$ s$^{-1}$. On the other hand, $I_{ON}/I_{OFF}$ shows the opposite trend, decreasing as the nanotube density increases. This is due to the bundling of SWNTs that makes gate control less effective, causing increased OFF-currents. In addition, by increasing the nanotube density, the probability of a direct metallic interconnection between the S/D electrodes increases given that 1% of SWNTs in the solution are still metallic.

This point might be further improved in the future by using higher purity SWNTs and/or different surface chemistry. The relationship between mobility and $I_{ON}/I_{OFF}$ is summarized in Figure 2f. Because of the 99% semiconductor-enriched SWNTs used in this work, a high mobility of ~27 cm$^2$ V$^{-1}$ s$^{-1}$ is obtained without sacrificing $I_{ON}/I_{OFF}$ (~10$^5$) even for a relatively shorter channel length ($L \sim 3 \mu$m). Our superior electrical properties compared to previous reports, where the same purity of SWNTs (99%) is used, mainly comes from the process difference. In this work, the SiO$_2$ surface is modified with poly-L-lysine, as opposed to APTES in previous reports, resulting in denser SWNT networks. And subsequent removal of surfactant residue by vacuum annealing improves the $I_{ON}/I_{OFF}$ (see Supporting Information, Figure S3). Of particular importance, uniformity of the explored SWNT TFT technology on flexible substrates is impressive. Focusing on the 90 min deposition condition, the standard deviation for $g_m$, $\mu$, $\log(I_{ON}/I_{OFF})$, and $V_t$ are ~11, 17, 11, and 3%, respectively.

The variations of the key performance metrics listed above are slightly larger than the state-of-the-art organic materials although the devices are processed in noncleanroom environment, but are sufficient for applications such as active-matrix backplanes. Of particular importance, a high mobility, such as those obtained here, is highly desired for lowering the operating voltage and the size (i.e., width) of the FETs. This presents a major advantage for the use of SWNT TFTs over their organic counterparts for use as the active matrix backplanes, although both are solution-processed. In addition, given the graphitic nature of SWNTs, they are highly robust and chemically stable, without degradation over time. These remarkable properties clearly set the advantage of semiconductor-enriched SWNT networks for large-area electronics. Here, we focus on the use of SWNT TFFTs for mechanically flexible and stretchable backplanes using PI as the support substrate. These backplanes could serve for development of displays, sensor arrays and imagers, just to name a few examples.

To obtain mechanically stretchable electronics, several approaches have been previously reported such as micro/nanostructures in “wavy” layouts and open mesh substrate geometries. Here, to reduce process complexity and make the substrate more robust against unidirectional stretching, we utilize a honeycomb mesh structure, where an array of holes in the shape of hexagons are laser cut on a thin PI substrate with a fixed pitch of 3.3 mm and a varied hole side-length of $a = 1.25$ mm. Mechanical simulation of (a) $a = 1.25$ mm and (f) $a = 1.85$ mm mesh, when the substrate is stretched by 2 mm in the horizontal direction. The location where the active devices are placed is marked with the white circle.

Figure 3. Stretchable PI substrates. (a) PI mesh substrate with four different side length of hexagonal holes ($a = 1, 1.25, 1.5$, and $1.85$ mm, from bottom to top). (b) Stretchability as a function of the side length, $a$, of the hexagonal holes. Here, the period of holes is fixed at 3.3 mm as shown in the inset. Optical images of (c) relaxed and (d) stretched state of the PI substrate with $a = 1.25$ mm. Mechanical simulation of (e) $a = 1.25$ mm and (f) $a = 1.85$ mm mesh, when the substrate is stretched by 2 mm in the horizontal direction. The location where the active devices are placed is marked with the white circle.
Figure 4. Mechanical robustness of SWNT TFTs on honeycomb patterned PI substrates. (a) Optical images of a stretchable device array, showing conformal coverage on a baseball. Expanded image of an active device area (corresponding to the TFT for a single pixel) is shown in the inset (scale bar is 200 μm). Channel length and width are 5 and 200 μm, respectively. (b) Transfer characteristics at $V_{DS} = -5$ V measured at various bending radius. The inset depicts $\Delta G/G_0$ as a function of bending radius, showing minimal performance change even when bent down to 2 mm of bending radius (c) Transfer characteristic at $V_{DS} = -5$ V as a function of stretchability. The inset shows $\Delta G/G_0$ as a function of stretchability. (d) Transfer characteristics at $V_{DS} = -5$ V as a function of temperature.

3.3) as shown in Figure 3e and Figure S5. It is clearly seen that most of the stress is introduced at the bridge regions, not on the active device regions.

Next, the mechanical stability of the fully encapsulated SWNT TFTs is explored. The devices were heated in air from room temperature to 100 °C. Only a minimal change in $V_t$ is observed (Figure 4d), which could be attributed to a slight change of the dielectric constant of the various layers used in the devices. The results here suggest that the TFT array technology presented here are not only uniform over large-areas, but exhibit superb mechanical and thermal properties, ideal for large-area conformal electronics.

To demonstrate the utility of the proposed device scheme, as an example system, SWNT TFT active matrix backplane is used for spatial pressure mapping, consisting of a $12 \times 8$ (physical size of $6 \times 4$ cm$^2$) pixel array. Here, each pixel is actively controlled by a single TFT. The device effectively functions as an artificial electrical skin (e-skin), capable of detecting and mapping touch profiles.

For this purpose, a pressure sensitive rubber (PSR - PCR Technical, Japan) is laminated on top of the parylene-passivated back-plane. The drain of each transistor is electrically connected to the PSR that is then grounded by an aluminum foil. The source and gate electrodes of the TFTs are used as the bit and word lines, respectively. PSR is near insulating (~30 Mohm) in its relaxed state. However, the resistivity decreases to <0.5 ohm/pixel by applying an external pressure of ~6 kPa due to the shortened tunneling path between the conducting carbon nanoparticles in the PSR. Figure 5a shows the output characteristics of a single pixel upon applying a normal pressure to the device. The pixel response at an operating voltage of $V_{DS} = -5$ V is shown in Figure 5b. In the linear operation regime, the sensor sensitivity, $S = dG/dP$, is ~30 μSkPa$^{-1}$, which is a threefold improvement...
compared with previous NW-based sensor4 resulting from improved on-current of SWNT devices. In this e-skin layout, transistor channels and PSR are placed in series, but after a normal pressure of >6 kPa, the resistivity of PSR becomes negligible compared to the TFTs, thereby, resulting in the saturation of the pixel response. To show the functionality of the integrated e-skin, an “L”-shaped weight is placed on top of the sensor array with the normal pressure of ~15 kPa (Figure 5c). The output conductance for each pixel is measured with the word

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ASSOCIATED CONTENT

Supporting Information. SWNT-network density as a function of surface treatment and deposition time; the effect of vacuum annealing on device properties; output characteristics of SWNT TFTs; mechanical simulations of honeycomb patterned structures. This material is available free of charge via the Internet at http://pubs.acs.org.

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