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Self-Aligned, Extremely High Frequency III–V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates

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Supporting Information

ABSTRACT: This paper reports the radio frequency (RF) performance of InAs nanomembrane transistors on both mechanically rigid and flexible substrates. We have employed a self-aligned device architecture by using a T-shaped gate structure to fabricate high performance InAs metal-oxide-semiconductor field-effect transistors (MOSFETs) with channel lengths down to 75 nm. RF measurements reveal that the InAs devices made on a silicon substrate exhibit a cutoff frequency ($f_T$) of $\sim$165 GHz, which is one of the best results achieved in III–V MOSFETs on silicon. Similarly, the devices fabricated on a bendable polyimide substrate provide a $f_T$ of $\sim$105 GHz, representing the best performance achieved for transistors fabricated directly on mechanically flexible substrates. The results demonstrate the potential of III–V-on-insulator platform for extremely high-frequency (EHF) electronics on both conventional silicon and flexible substrates.

KEYWORDS: III–V-on-insulator, XOI, two-dimensional membranes, radio frequency transistors, flexible electronics

T he growing demand on larger bandwidth for wireless communications has stimulated the quest for transistors that can be operated at fastest possible frequencies. Besides the conventional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs),1 various types of nanomaterial systems including carbon nanotubes,2–7 graphene,8–11 and III–V nanowires12–14 have been heavily explored for radio frequency (RF) applications. However, none of these material platforms have yet offered transistors that can surpass the performance achieved in III–V high electron mobility transistors (HEMTs).15–20 The record-high cutoff frequency ($f_T$) for InAs-based HEMTs has already reached 644 GHz for 30 nm long devices on InP substrates.17 Despite the tremendous success in III–V HEMT research, the platform still has a few inherent limitations. First of all, sophisticated epitaxial growth is needed to grow multiple layers with desired chemical compositions in order to form the quantum well structures. Second, due to the use of epitaxial processes, the selection of substrate is limited to expensive III–V bulk substrates such as InP or GaAs, or in some cases, silicon with thick buffer layers. Third, such HEMT devices are not compatible with flexible electronics, which has attracted significant amount of interest recently.

In light of the above-described limitations faced by III–V HEMTs, we have previously reported a III–V-on-insulator, or “XOI” approach,21 which enables the transfer of ultrathin, two-dimensional III–V membranes to virtually any type of handling substrate using a facile contact printing process.22,23 The use of the ultrathin III–V membranes allows optimal gate control and offers transistors with minimal short channel effects, which is especially important for a small bandgap semiconductor such as InAs.24 Using this XOI platform, we have already demonstrated high-performance InAs and InAsSb n-MOSFETs and InGaSb-based p-MOSFETs on silicon support substrates. In addition, the XOI platform enables easy fabrication of transistors on mechanically flexible substrates. Previously, the best reported cutoff frequencies for the flexible transistors made with various types of material platforms including carbon nanotube,27 graphene,28 silicon,29,30 and III–V nanowires31,32 typically lie in the range of a few hundred megahertz to sub-10 gigahertz. The work by Rogers et al. has demonstrated the potential of using GaAs membranes for high-performance flexible RF electronics.23 However, the reported cutoff frequency of 2 GHz is only modest due to the relatively long

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channel length used without self-aligned source/drain contact electrodes in respect to the gate.

In this paper, we study the RF characteristics of transistors fabricated using InAs XOI platform. Transistors with T-shaped gate electrodes are fabricated in order to obtain source/drain (S/D) contacts self-aligned to the gate electrode to allow minimal parasitic capacitances and resistances.\(^3\) It is well-known that the cutoff frequency \(f_t\) and maximum oscillation frequency \(f_{\text{max}}\), which are two most important figures of merit for RF transistors, can be predicted using the following relations\(^3\):

\[
f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd})}
\]

\[
f_{\text{max}} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_d (R_g + R_s) \approx \sqrt{\frac{f_t}{8\pi R_g C_{gd}}}}}
\]

where \(g_m\) is the transconductance, \(C_{gs}\) and \(C_{gd}\) are the gate/source and gate/drain capacitances, respectively, \(R_g\) and \(R_s\) are the gate and source series resistances, respectively, and \(g_d\) is the output conductance. The reduced parasitic capacitances and resistances provided by the self-aligned T-gate design would thereby lead to enhanced RF performance. Meanwhile, the use of InAs channel with a high saturation velocity of electrons (1.3 \(\times\) 10^7 cm/s for bulk)\(^3\) combined with short gate lengths (i.e., sub-100 nm) lead to high \(g_{mw}\) which is optimal for high frequency operation.

RF measurements of InAs XOI MOSFETs with self-aligned T-gate architecture reveal that the devices made on a silicon substrate exhibit a \(f_t\) of \(\sim 165.5\) GHz, which is one of the best results achieved in III–V MOSFETs on a Si substrate. The performance is truly impressive considering the simple fabrication process used on a conventional Si handling wafer, as opposed to the sophisticated multiepitaxial-layer structures of the III–V HEMTs. Similarly, the devices fabricated on flexible substrate provide a \(f_t\) of 105 GHz. The result is more than 10 times better than the fastest flexible devices reported in the literature made with graphene \((f_t = 8.7\) GHz),\(^2\) another widely studied two-dimensional (2D) material for RF applications. This work demonstrates the successful operation of flexible III–V MOSFETs at extremely high frequency (EHF) regime (30 to 300 GHz) for the first time. Although impressive performance has been previously demonstrated by bonding HEMT devices fabricated on conventional epitaxial substrate to flexible substrate,\(^3\) our work represents the best performance achieved for transistors fabricated directly on mechanically flexible substrates. Our results indicate the RF device potential of XOI platform and provide a viable approach for future flexible electronics when ultrahigh performance transistors are needed for large bandwidth wireless communication applications.

The schematic of a self-aligned InAs XOI MOSFET is shown in Figure 1a. For DC measurements, the transistors are fabricated on a heavily doped (\(\rho < 0.005\) \(\Omega\)·cm) silicon wafer to allow back-gate biasing in addition to the T-gate, while for RF measurements, a highly resistive silicon wafer (\(\rho = 10\) \(\Omega\)·cm) with 300 nm thick SiO2 was used to ensure minimum parasitic capacitances from the substrate. InAs microribbons with a width and spacing of \(\sim 5\) \(\mu\)m and a nominal thickness of \(\sim 15\) nm is transferred onto a Si wafer using a contact printing method as described in our previous publications.\(^2\) According to our previous study, a field-effect mobility of around 2300 cm^2 V^{-1} s^{-1} can be achieved in such 15 nm thick InAs
nanomembranes. Subsequently, Ti/Au probing pads are first patterned using photolithography and T-shaped Al/ZrO₂ gate stacks are defined using electron-beam (e-beam) lithography, atomic layer deposition of ZrO₂ (thickness, 10 nm) at 130 °C, evaporation of Al (thickness, 110 nm), and a lift-off process. As a final step, directional deposition of Ni (20 nm) on the T-gate forms the self-aligned S/D contacts and concludes the device fabrication. More details about the device fabrication process can be found in the Supporting Information (Figure S1).

The optical microscope images of a completed InAs RF transistor on a Si substrate is shown in Figure 1b, where the device is configured into the ground—signal—ground (GSG) coplanar waveguide structure to allow microwave measurements. As shown in the zoom-in optical microscope image, the device consists of a pair of MOSFETs with a channel width of 50 μm each. Each 50 μm wide MOSFET contains five uniformly spaced ribbons with an effective channel width of ~25 μm. The corresponding atomic force microscopy (AFM) and cross-sectional scanning electron microscopy (SEM) images showing the active region of the MOSFETs are exhibited in Figure 1c,d, respectively. From the SEM image, one can find that the S/D electrodes are self-aligned to the T-shaped gate. The T-gate has a base-length of ~75 nm and a tip-length of ~244 nm. The length of the ungated channel regions, corresponding approximately to the difference between tip- and base-lengths of the gate is ~85 nm for both source and drain contacts.

We first characterized the DC performance of the self-aligned InAs XOI MOSFETs on silicon substrates, and the results are summarized in Figure 2. The transfer (I_DS−V_DS) and output (I_DS−V_DS) characteristics of a representative device are presented in Figure 2a,b, respectively. The data is normalized to the total width of the InAs microribbons, which is 25 μm for this particular device. From the I_DS−V_DS curves, one can find that the on-state current density (I_on) of the device measured at V_DS = 0.5 V and V_GS = 1 V is ~0.26 mA/μm, average current on/off ratio (I_on/I_off) is ~500, and the subthreshold slope (SS) is 310 mV/dec. Note that the SS is higher than the values reported in our previous reports, because the forming gas (5% H₂ in N₂) anneal process at 170 °C, known to improve the SS significantly, is not compatible with the gate-first fabrication process used in this work. Specifically, diffusion of the metal atoms into the dielectric was observed at elevated temperatures. In the future, the use of high-temperature metals, such as TiN and TaN need to be explored to enable a forming gas anneal to further improve the InAs/ZrO₂ interface.

From the I_DS−V_DS characteristics presented in Figure 2b, one can roughly estimate the carrier saturation velocity (ν satu) in InAs membranes using the current equation below for classical MOSFETs with velocity saturation:

\[ I_{Sat} = W(V_{GS} - V_{th}) C_{ox} \nu_{satu} \]

where I_{Sat} is the saturation current, V_{th} is the linear extrapolated threshold voltage, and C_{ox} is the parallel plate capacitance for 10 nm ZrO₂ (ε ~ 13). The \( \nu_{satu} \) is estimated to be ~0.77 × 10⁷ cm/s for an applied electric field of 28.7 kV/cm, which is close to the value reported in the literature. Furthermore, Figure 2c compares the I_DS−V_GS characteristics measured with the back-gate (black trace) and self-aligned top gate (red trace) at V_DS = 0.5 V. From the figure, it is obvious that with the use of high-k ZrO₂ dielectric (ε = 13, effective oxide thickness EOT = 3 nm), the top-gate is significantly stronger than the back-gate (EOT = 300 nm), which requires ~40 to 40 V to achieve similar amount of gate modulation. Figure 2d shows the transconductance (g_m−V_GS) curves derived from the I_DS−V_GS characteristics. The maximum g_m is measured to be 0.39 mS/μm when V_GS and V_DS are at ~0.8 and 0.5 V, respectively. Although this value is already respectable, it is lower than the best value reported in our previous publication by a factor of ~4X. This is likely to be limited by the source/drain contact resistance and/or series resistance of the ungated regions arising from the tip to base length ratio of the T-gate. According to the SEM image in Figure 1d, the underlapped region is around 85 nm for both the source and drain sides, and the corresponding series plus contact resistance...
(R_g, R_p) is estimated to be around 900 Ω-μm (Supporting Information Figure S2).

By applying back-gate bias through the substrate, the contribution from the un gated region to the S/D series resistance is examined. Figure 2e,f shows the contour plots of I_DS/W (Figure 2e) and g_m/W (Figure 2f) as a function of the top gate (V_{TG}) and back gate (V_{BG}) voltages for the self-aligned InAs XOI MOSFET. The results indicate that as the V_{BG} changes from 0 to 30 V, I_{on} only increases slightly from 0.26 to 0.3 mA/μm, and the maximum g_m remains almost constant. This indicates that the un gated regions do not contribute significantly to the series resistance. Therefore, the S/D contact resistance should be the limiting factor for the overall device performance. Annealing of the devices in N_2 at 300 °C prior to the formation of the gate stack was previously found to drastically reduce the contact resistance values as also shown in the Supporting Information (Figure S3). However, contact thermal annealing is not compatible for the gate-first process scheme studied in this work. Annealing at 300 °C causes the Ni atoms of the gate metal to diffuse into the gate dielectric, resulting in low I_{on}/I_{off}. As shown in the Supporting Information (Figure S2), after subtracting the measured contact resistance (from transmission line method), the intrinsic transconductance (g_m) is extracted to be ∼3 mS/μm at V_{DS} = 0.5 V, which is consistent with our previously reported value. In the future, gate stacks with higher thermal budgets need to be developed to enable contacting annealing of Ni S/D electrodes, and thereby, further reducing the contact resistances. Moreover, according to Figure S3 shown in the Supporting Information, the contact resistance increases as the thickness of InAs membrane gets smaller. Therefore, for the future ultimately scaled transistors with thinner InAs channel, n-doping of InAs near the metal contacts need to be explored to further reduce the contact resistance.

The RF performance of a self-aligned InAs XOI RF transistor (dual channel with L = 75 nm and W = 50 μm) on a highly resistive silicon substrate is characterized using a vector network analyzer (Anritsu 37397C). For the measurements, the source contacts are grounded, and the DC biases are supplied to the gate and drain terminals through the bias-T. The transistor is biased at V_{GS} = −2 V and V_{DS} = 0.7 V for maximum performance. (b) As-measured (dash) and de-embedded (solid) current gain (h_{ij}) and Mason’s unilateral gain (U) derived from the S-parameters from 40 MHz to 40 GHz. The de-embedded current gain cutoff frequency is 165.5 GHz. (c,d) As-measured (dash) and de-embedded (solid) cutoff frequencies as a function of V_{DS} (c) and V_{GS} (d).

Figure 3. RF characteristics of self-aligned InAs XOI MOSFETs on Si. (a) Measured S-parameters for a self-aligned InAs XOI RF transistor (dual channel with L = 75 nm, W = 50 μm) from 40 MHz to 40 GHz. The transistor is biased at V_{GS} = −2 V and V_{DS} = 0.7 V for maximum performance. (b) As-measured (dash) and de-embedded (solid) current gain (h_{ij}) and Mason’s unilateral gain (U) derived from the S-parameters from 40 MHz to 40 GHz. The de-embedded current gain cutoff frequency is 165.5 GHz. (c,d) As-measured (dash) and de-embedded (solid) cutoff frequencies as a function of V_{DS} (c) and V_{GS} (d).

observed f_t = 165.5 GHz for a 75 nm long transistor represents the best frequency response currently achieved in III–V-based MOSFETs on silicon substrates. Furthermore, considering the fact that f_t is proportional to g_m, the ultimate performance (i.e., intrinsic f_t) of our self-aligned XOI RF transistor is projected to be ~1.27 THz when removing the effect of contact resistance. This projection is obtained by replacing g_m with the extracted g_m of 3 mS/μm from the DC measurements in the f_t equation.

We also note that f_max is lower than f_t for our devices, which can be attributed to the loss from the parasitic gate resistance. As shown in the Supporting Information (Figure S5), we have established a small-signal equivalent circuit model to extract the device parameters from the measured S-parameters and the values are summarized in Table 1. R_g is extracted to be 180 Ω, which could limit the f_max performance according to eq 2. In the future, optimized multigrid layout design can be employed to minimize the gate resistance and further increase f_max of the transistors. Additionally, the intrinsic gain of our InAs XOI RF transistor is f_m R_g = 9.24, which is high for such a small channel length.

The drain bias and gate bias dependency of the cutoff frequencies are studied and illustrated in Figure 3c,d, respectively. As the V_{DS} increases, the f_t and f_max peaks at 0.7 V, and then starts to decrease slightly (Figure 3c), which is likely resulted from the heating of the InAs membranes. Under various gate biases from −3 to −1 V, the f_t and f_max also vary and peak at V_{GS} = −2 V (Figure 3d). The variations of f_t and f_max follow the variation of g_m since they are directly proportional.

The XOI platform is also compatible with mechanically flexible substrates. As a demonstration, we report self-aligned InAs XOI MOSFETs fabricated on a bendable polyimide (PI) substrate. The fabrication process involves the spin coating and curing of polyimide (HD MicroSystems, Inc.
PI-2525) onto a silicon handling wafer, resulting in a film thickness of \( \sim 12 \mu m \). Subsequently T-gate MOSFETs are fabricated using the process scheme described above, followed by deposition of a parylene passivation layer (thickness, 500 nm). Finally, the PI substrate is detached from the handling wafer after the fabrication is completed.\(^{12,38}\) It is important to point out that parylene passivation layer is used in order to encapsulate the devices to avoid the delamination of the InAs membranes from the substrate or the shortage between the gate and source/drain during the peel-off process.

An optical photograph of a PI substrate with self-aligned InAs RF MOSFETs is shown in Figure 4a. The device schematic is also shown. The devices show excellent mechanical robustness with minimal performance change under various curvature radii down to 4.8 mm (Figure 4b). The normalized on-state conductance \( G/G_0 \) and maximum transconductance \( g_{m0} \) as a function of curvature radius are shown in Figure 4c, where \( g_{m0} \) and \( G_0 \) are the transconductance and on-state conductance in the relaxed state. The results indicate that the performance change is within 11% under all bending conditions tested. Furthermore, RF characterizations (Figure 4d,e) from 100 MHz to 20 GHz show that the flexible InAs MOSFET has an impressive de-embedded \( f_1 \) of 105 GHz.

For practical mixed-signal integrated circuits, most of the modules such as digital signal processing (DSP), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and IF-band amplifiers are typically operating at moderate frequencies (a few hundred MHz to low GHz). While power amplifiers (PA) and RF front-end such as low-noise amplifier (LNA) and mixer may require a few transistors that can be operated at faster speeds (a few GHz to tens of GHz). In the future, one can envision flexible electronic systems based on a few InAs XOI MOSFETs on a small-area that are heterogeneously integrated with low-cost-material-based transistors on large-area substrates. This represents a high-performance yet cost-effective approach. Furthermore, our XOI platform is also universal to all types of III–V material systems. Therefore, despite the relatively low breakdown electric field \( V_{BR} \) and power handling capability of InAs due to its small bandgap, it is possible to heterogeneously integrate multiple III–V materials on the same substrate for different applications. For instance, it would be attractive to have an integrated system with InAs XOI transistors in the high-speed RF front-end such as low-noise amplifiers and mixers, and GaN\(^{39}\) XOI transistors in components such as the power amplifiers.

In summary, RF performance of InAs XOI MOSFETs is explored through the use of self-aligned device geometry. Compared with graphene, which is another 2D material that has been widely studied for RF applications, the ultrathin III–V membranes used in this study exhibit comparable frequency response on Si substrate and in the meantime offer higher \( I_{on}/I_{off} \). Although for RF applications, the requirement on \( I_{on}/I_{off} \) is more relaxed as compared to digital applications, low \( I_{on}/I_{off} \) still limits the possible applications such as high efficiency power amplifiers. Our well-established XOI platform, coupled with the self-aligned device design, could provide a viable and simple approach to enable heterogeneous integration of high-speed III–V transistors with silicon CMOS. It could also serve

### Table 1. Extracted Device Parameters for the InAs XOI RF Transistor Presented in Figure 3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( g_m )</td>
<td>14 mS</td>
</tr>
<tr>
<td>( R_s )</td>
<td>17.8 Ω</td>
</tr>
<tr>
<td>( R_d )</td>
<td>500 Ω</td>
</tr>
<tr>
<td>( R_g )</td>
<td>180 Ω</td>
</tr>
<tr>
<td>( R_{ds} )</td>
<td>660 Ω</td>
</tr>
<tr>
<td>( R_{DS} )</td>
<td>14.3 Ω</td>
</tr>
<tr>
<td>( C_g )</td>
<td>8.5 fF</td>
</tr>
<tr>
<td>( C_{gd} )</td>
<td>4.8 fF</td>
</tr>
<tr>
<td>( C_{ds} )</td>
<td>22.9 fF</td>
</tr>
</tbody>
</table>

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**Figure 4.** RF characteristics of self-aligned InAs XOI MOSFETs on mechanically flexible substrates. (a) Photograph of self-aligned flexible InAs XOI MOSFETs fabricated on a polyimide substrate. Inset: schematic of the device. (b) \( I_{DS}−V_{GS} \) characteristics of a flexible device measured under various curvature radii at \( V_{DS} = 0.1 \) V. The average \( I_{on}/I_{off} \) ratio is \( \sim 100 \) and the average \( I_{on} \) is \( \sim 0.04 \) mA/μm at \( V_{DS} = 0.1 \) V. (c) Normalized on-state conductance \( G/G_0 \) and maximum transconductance \( g_{m0} \) as a function of curvature radius. (d) Measured S-parameters for a device (dual channel with \( L = 75 \) μm, \( W = 50 \) μm) from 100 MHz to 20 GHz. The transistor is biased at \( V_{DS} = 2.3 \) V and \( V_{GS} = 0.6 \) V for maximum performance. (e) As-measured (dash) and de-embedded (solid) \( h_{ij} \) and \( U \) derived from the S-parameters from 100 MHz to 20 GHz. The de-embedded current gain cutoff frequency is 105 GHz.
as a foundation for ultra high speed flexible electronics for large bandwidth wireless communication applications.

**ASSOCIATED CONTENT**

* Supporting Information
Details about the self-aligned XOI MOSFET fabrication process (S1); contact resistance and intrinsic transconductance $g_{m}$ (S2); effect of contact anneal (S3); on-chip open/short de-embedding for intrinsic RF performance (S4); and small signal RF modeling to extract the device parameters from the measured S-parameters (S5). This material is available free of charge via the Internet at http://pubs.acs.org.

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**Notes**
The authors declare no competing financial interest.

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