Programmable Architectures and Design Methods for Two-Variable Numeric Function Generators

Shinobu Nagayama,† Tsutomu Sasao,† and Jon T. Butler†

This paper proposes programmable architectures and design methods for numeric function generators (NFGs) of two-variable functions. To realize a two-variable function in hardware, we partition a given domain of the function into segments, and approximate the function by a polynomial in each segment. This paper introduces two planar segmentation algorithms that efficiently partition a domain of a two-variable function. This paper also introduces a design method for symmetric two-variable functions (i.e., $f(X,Y) = f(Y,X)$). This method can reduce the memory size needed for symmetric functions by nearly half with small speed penalty. The proposed architectures allow a systematic design of various two-variable functions. We compare our approach with one based on a one-variable NFG. FPGA implementation results show that, for a complicated function, our NFG achieves 57% of memory size and 60% of delay time of a circuit designed based on a one-variable NFG.

1. Introduction

The ability to compute numeric functions at a high speed is important in many applications, including 3D computer graphics, hardware accelerators for technical computing packages, direct digital frequency synthesizers, and digital signal processing. Various design methods for numeric function generators (NFGs) have been devised for numeric functions on one variable. Only a few methods exist for multi-variable functions (e.g., $\sqrt{X^2 + Y^2 + Z^2}$ and $\arctan(X/Y)$). However, these methods are function-specific; different functions require different methods. As far as we know, no systematic design method exists for generic multi-variable functions.

A straightforward design method for arbitrary multi-variable function is to use a single memory in which the address is a combination of values of variables and the content of that address is the corresponding value of function. This method produces a fast implementation, but requires a $2^m$-word memory to implement an $m$-variable function with $n$ bits for each variable. Thus, unlike one-variable functions, even for a computation with a small number of bits, this method is impractical because of large memory size.

To produce a practical implementation, multi-variable functions are often designed in a conventional (trivial) manner that uses a combination of one-variable function generators, multipliers, and adders. For example, the function $\sqrt{X^2 + Y^2 + Z^2}$ can be realized using three circuits, each realizing $a^2$, two adders, and a square root circuit. This design method may require small memory size. However, depending on the function implemented, it can produce a slow implementation because of long path delays. Also, such circuits make error analysis harder. That is, guaranteeing output accuracy becomes harder. Also, there are many multi-variable functions that cannot be decomposed into one-variable functions, such as probability distributions that are functions of the random variable and a parameter, like variance.

This paper proposes a systematic design method for two-variable functions. Since our design method is based on a piecewise polynomial approximation, architectures are simple even for complicated functions. To approximate a given function using piecewise polynomials, we introduce two planar segmentation algorithms that efficiently partition a given domain of a two-variable function. We also introduce programmable architectures that can realize a wide range of two-variable functions.

The rest of this paper is organized as follows: Section 2 introduces the number representation and the decision diagrams used in this paper. Section 3 presents two planar segmentation algorithms and a polynomial approximation method using bilinear interpolation. Section 4 presents programmable architectures for two-variable functions. Section 5 presents an architecture and a design method for symmetric two-variable functions. Section 6 evaluates performance of our segmentation algorithms and architectures for two-variable functions. And, Sec-
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<table>
<thead>
<tr>
<th>a. REPORT</th>
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</tr>
</thead>
<tbody>
<tr>
<td>unclassified</td>
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</table>

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<thead>
<tr>
<th>16. SECURITY CLASSIFICATION OF:</th>
<th>17. LIMITATION OF ABSTRACT</th>
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<th>19a. NAME OF RESPONSIBLE PERSON</th>
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</thead>
<tbody>
<tr>
<td>unclassified</td>
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<td>12</td>
<td></td>
</tr>
</tbody>
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2. Preliminaries

2.1 Number Representation and Errors

**Definition 1** A numeric function generator (NFG) is a logic circuit that computes approximated values for a numeric (real) function within some given acceptable error \( \varepsilon \). A **one-variable NFG** is a logic circuit for a one-variable numeric function \( f(X) \), whose input is \( X \), and output is an approximated value for \( f(X) \). A **two-variable NFG** is a logic circuit for a two-variable numeric function \( f(X,Y) \), whose inputs are \( X \) and \( Y \), and output is an approximated value for \( f(X,Y) \).

**Definition 2** A value \( X \) represented by the binary fixed-point representation is denoted by
\[
X = (x_{l-1} \ldots x_1 x_0 \ldots x_{-1} x_{-2} \ldots x_{-m}),
\]
where \( x_i \in \{0,1\} \), \( l \) is the number of bits in the integer part, and \( m \) is the number of bits in the fractional part. Each bit \( x_i \) contributes \( 2^i x_i \) to the value of \( X \), except \( x_{l-1} \), which contributes \(-2^{l-1} x_{l-1} \). That is, the fixed-point representation is in two’s complement.

**Definition 3** **Error** is the absolute difference between the exact value and the value produced by the hardware. **Acceptable error** is the maximum error that an NFG may assume; it is usually a specification to be satisfied by the hardware. **Approximation error** is the error caused by a function approximation. **Acceptable approximation error** is the maximum approximation error that a function approximation may assume. **Rounding error** is the error caused by a binary fixed-point representation.

**Definition 4** **Accuracy** is the number of bits in the fractional part of a binary fixed-point representation. **m-bit accuracy** specifies that \( m \) bits are used to represent the fractional part of the number. When the maximum error is \( 2^{-m} \), the accuracy is no greater than 1 unit in the last place (ULP)\(^{12}\). In this paper, an **m-bit accuracy NFG** is an NFG with an \( m \)-bit fractional part of the inputs, an \( m \)-bit fractional part of the output, and a 1 ULP error.

2.2 Decision Diagrams

The proposed design uses binary decision diagrams.

**Definition 5** A binary decision diagram (BDD)\(^{2,11}\) is a rooted directed acyclic graph (DAG) representing a logic function. The BDD is obtained by recursively applying the Shannon expansion \( f = \pi_i f_0 + x_i f_1 \) to the logic function, where \( f, f_0, \) and \( f_1 \) are represented by nodes. There are two types of nodes, terminal nodes that are labeled by the two function values, 0 and 1, and non-terminal nodes that are labeled by variable names. Each non-terminal node has two unweighted outgoing edges labeled 0 and 1, corresponding to the value of the node’s variable. The terminal nodes have no outgoing edges. We consider only ordered BDDs, where the order of the variables is the same for every path from the root node to a terminal node. We consider only reduced BDDs, where identical subtrees are combined into a single tree.

**Definition 6** A multi-terminal BDD (MTBDD)\(^{3}\) is an extension of a BDD, that represents an integer-valued function: \( \{0,1\}^n \rightarrow S \subseteq Z \), where \( S \) is a finite subset of the set \( Z \) of integers. In an MTBDD, the terminal nodes are labeled by values of \( S \).

**Definition 7** An edge-valued BDD (EVBDD)\(^{8,9}\) is also an extension of a BDD, that represents an integer-valued function. The EVBDD is obtained by repeatedly applying the expansion \( f = \pi_i f_0 + x_i (f'_1 + \alpha) \) to the integer-valued function, where \( f_1 = f'_1 + \alpha \), and \( \alpha \) is the constant term of \( f'_1 \). In an EVBDD, all 1-edges have an integer weight and all 0-edges have weight 0. There is only one terminal node; it is labeled 0. The incoming edge into the root node can have a non-zero weight. A non-zero weight \( \alpha \) on the incoming edge of the root node adds \( \alpha \) to all sums associated with all paths from the root to the terminal node of the EVBDD. Indeed, it occurs when the EVBDD is a sub-EVBDD to a larger EVBDD.

**Example 1** Figure 1 (b) and (c) show an MTBDD and an EVBDD for the integer-valued function \( f \) defined by Fig. 1 (a). In Fig. 1 (b) and (c), dashed lines and solid lines denote 0-edges and 1-edges, respectively. Note the non-zero weights on 1-edges of the EVBDD. In the MTBDD, terminal nodes represent function values. Thus, to evaluate the function, we traverse the MTBDD from the root node to a terminal node according to the input values, and obtain the function.
value (an integer) from the terminal node. On the other hand, in the EVBDD, we obtain the function value by summing the weights of the edges traversed from the root node to the terminal node. (End of Example)

3. Piecewise Polynomial Approximation Based on Planar Segmentation

3.1 Planar Segmentation Problem

To approximate a given two-variable function by piecewise polynomials, we partition a given domain of the function into segments, and approximate the function by a polynomial in each segment. By narrowing segments, and thus increasing the number of segments, we can decrease the approximation error to the desired value. In this case, the memory size and speed of an NFG are strongly dependent on segmentation of domain. Thus, to design fast and compact NFGs, we need to solve the following segmentation problem: Given a two-variable function, its domain, and acceptable approximation error, find an optimum segmentation.

To find an optimum segmentation, we consider the following:

1. number of words in the coefficients memory, which is the number of segments, and

2. complexity of hardware to realize segmentation, called the segment index encoder, which maps values of \( X \) and \( Y \) to a segment number.

Fewer segments are preferred because the number of segments directly affects the size of the coefficients memory of the NFG. But, the complexity of the segment index encoder is important as well. Even if the number of segments is minimum, a large NFG is produced if the segment index encoder is very large.

For one-variable functions, since the domain is formed in one-dimension (line), any segmentation can be realized compactly. Thus, we considered only the number of segments to find an optimum segmentation\(^{14,19}\). On the other hand, for two-variable functions, since the domain is formed in two-dimensions (plane), the segment index encoders tend to be much more complex than for one-variable functions. Thus, to find the optimum design of two-variable NFGs, it is necessary to carefully consider the complexity of the segment index encoder.

For one-variable functions, we have proposed linear segmentation algorithms\(^ {14,19}\) to find an optimum segmentation of a linear domain (an approximation with the fewest segments) efficiently. However, for two-variable functions, a planar segmentation algorithm is now required to find an optimum segmentation of a planar domain. In planar segmentations, we have a higher degree of freedom, and thus, finding an optimum segmentation becomes much more difficult than in linear segmentation. Because many segments may be involved in a practical design, the time needed to find an optimum segmentation can be very long. To produce an efficient planar segmentation in a short computation time, we focus on heuristic planar segmentation algorithms. The next subsection presents two heuristic planar segmentation algorithms that produce an efficient planar segmentation by regularly partitioning a given domain using squares.

3.2 Planar Segmentation Algorithms

We first present a recursive planar segmentation algorithm to reduce the hardware complexity of both the coefficients memory (the number of segments) and the segment index encoder. Figure 2 shows this algorithm. Inputs of the algorithm are a numeric function \( f(X, Y) \), a domain \( \{ [X_b, X_e], [Y_b, Y_e] \} \) for \( X \) and \( Y \), an accuracy \( m_{in} \) of \( X \) and \( Y \), and an acceptable approximation error \( \varepsilon_a \).

This algorithm begins by computing an approximate polynomial \( g(X, Y) \). This is an initial approximation. If that approximation error \( \varepsilon \) is larger than the given acceptable error \( \varepsilon_a \), then the domain is partitioned into four equal-sized square segments. For each segment, an approximate polynomial is computed again. The
same process is recursively repeated until all segments have approximation errors smaller than $\varepsilon_a$. Note that this algorithm creates a segment of size $w_i \times w_i$ where $w_i = 2^{h_i} \times 2^{m_w}$ and $h_i$ is an integer. That is, all the segmentation points $P_i$ and $Q_i$ are restricted to values such that the least significant $h_i$ bits are 0 (i.e., $P_i = (\ldots, p_{j+1} p_j 00 \ldots 0)$, where $j = m_w - h_i$). This restriction contributes to reduce the complexity of the segment index encoder.

Next, we present the planar uniform segmentation algorithm. Since the recursive planar segmentation algorithm produces non-uniform segmentation, a segment index encoder is needed to compute a segment number from values of $X$ and $Y$. However, in a uniform segmentation where the number of segments is a power of 2, a segment index encoder is not necessary because a segment number is obtained by the most significant bits of $X$ and $Y$ (see Fig. 3(b)). This eliminates the delay of the segment index encoder, and produces fast NFGs. To produce a uniform segmentation, we begin by finding the smallest square segment needed to achieve the acceptable approximation error using the recursive segmentation algorithm shown in Fig. 2. Then, we partition a given domain into square segments all with the same size as the smallest segment.

### 3.3 Approximation Using Bilinear Interpolation Polynomials

For $g(X, Y)$ in Fig. 2, we can use any approximating polynomial. In general, higher-order polynomials require fewer segments. However, for multi-variable functions, using higher-order polynomials is not always effective in reducing the memory size of NFGs. This is because, for multi-variable polynomials, higher polynomial order requires many more polynomial coefficients. Also, higher-order polynomials produce slower NFGs. Thus, for polynomial approximation methods, reducing memory size with a small speed penalty is a key issue. To accomplish this, we use the bilinear interpolation polynomials.

Bilinear interpolation is an extension of linear interpolation. It interpolates two-variable functions $f(X, Y)$ using four points. In Fig. 2, to interpolate $f(X, Y)$ in each segment $\{(B_x, E_x), (B_y, E_y)\}$, we use four corner points of the segment: $(B_x, B_y)$, $(B_x, E_y)$, $(E_x, B_y)$, and $(E_x, E_y)$. Let $f_{bb} = f(B_x, B_y)$, $f_{be} = f(B_x, E_y)$, $f_{eb} = f(E_x, B_y)$, and $f_{ee} = f(E_x, E_y)$. Then, the bilinear interpolation $g(X, Y)$ is given by:

$$g(X, Y) = \frac{f_{bb} \times (E_x - X) \times (E_y - Y) + f_{eb} \times (X - B_x) \times (E_y - Y)}{(E_x - B_x) \times (E_y - B_y)} + \frac{f_{be} \times (E_x - X) \times (Y - B_y) + f_{ee} \times (X - B_x) \times (Y - B_y)}{(E_x - B_x) \times (E_y - B_y)}.$$ 

By expanding and rearranging this, we obtain the following form:

$$g(X, Y) = C_{xy} XY + C_x X + C_y Y + C_0,$$

where

$$C_{xy} = \frac{f_{bb} - f_{eb} - f_{be} + f_{ee}}{(E_x - B_x)(E_y - B_y)},$$

$$C_x = \frac{-f_{be} E_x + f_{eb} E_y + f_{ee} B_x - f_{ee} B_y}{(E_x - B_x)(E_y - B_y)},$$

$$C_y = \frac{-f_{eb} E_x + f_{eb} B_x + f_{be} E_y - f_{be} B_y}{(E_x - B_x)(E_y - B_y)},$$

and

$$C_0 = \frac{f_{bb} E_y - f_{eb} B_x E_y - f_{be} E_x B_y + f_{ee} B_x B_y}{(E_x - B_x)(E_y - B_y)}.$$
$E_y$ hold, we can offset $X$ and $Y$ by $B_x$ and $B_y$ to compute the approximating polynomial $g(X,Y) + v$. By using the offset inputs $(X - B_x)$ and $(Y - B_y)$ instead of $X$ and $Y$, we reduce the size of multipliers needed to compute $g(X,Y) + v$. By substituting $X - B_x + B_x$ and $Y - B_y + B_y$ for $X$ and $Y$ respectively, we transform $g(X,Y) + v$ as follows:

$$g(X,Y) + v = C_{xy}(X - B_x + B_x)(Y - B_y + B_y) + C_x(X - B_x + B_x) + (C_y - B_y + B_y) + C_0 + v$$

$$= C_{xy}(X - B_x)(Y - B_y) + (C_x + C_{xy}B_y)(X - B_x) + C_xB_x + C_yB_y + C_0 + v$$

$$+ (C_y + C_{xy}B_x)(Y - B_y) + C_yB_y + C_yB_y + C_0 + v$$

where $C'_x = C_x + C_{xy}B_y$, $C'_y = C_y + C_{xy}B_x$, and $C'_0 = C_{xy}B_xB_y + C_xB_x + C_yB_y + C_0 + v$.

4. Programmable Architectures for Two-Variable NFGs

4.1 Architectures Based on Recursive and Uniform Segmentations

Figure 3 shows two architectures for two-variable NFGs realizing (1). Figure 3 (a) and (b) show architectures based on recursive segmentation and uniform segmentation, respectively. The segment index encoder converts values of $X$ and $Y$ into a segment number. This, in turn, is applied as the address input of the coefficients memory. The coefficients are applied to adders and multipliers to form the polynomial value $g(X,Y) + v$. Note that Fig. 3 (a) uses bitwise AND gates to compute $X - B_x$ and $Y - B_y$. In recursive segmentation, we can realize $X - B_x$ and $Y - B_y$ using AND gates driven on one side by $B_x$ and $B_y$, respectively.

Note that Fig. 3 (b) has neither a segment index encoder nor bitwise AND gates. In uniform segmentation, the segment index encoder and bitwise AND gates are not necessary. This is because a segment number is obtained by the most significant bits of $X$ and $Y$, and $X - B_x$ and $Y - B_y$, which are realized with bitwise AND gates in Fig. 3 (a), are obtained by the least significant bits.

4.2 Architecture and Design Method for Segment Index Encoder

The segment index encoder realizes the segment index function: \( \{0,1\}^n \times \{0,1\}^n \rightarrow \{0,1,\ldots,k-1\} \) shown in Fig. 4 (a), where $X$ and $Y$ have $n$ bits, and $k$ denotes the number of segments. We realize this function with the architecture shown in Fig. 4 (b). In this architecture, the values of interconnecting lines between adjacent LUT memories represent sub-functions in the EVBDDs labeled rails, and the outputs from each LUT memory to the adders tally the function value (labeled Arails). Consider the design of the LUT cascade and adders in Fig. 4 (b), given the segmentation produced in Fig. 2.

We begin by representing the segment index function using an MTBDD. Figure 5 illustrates the relationship between recursive segmentation and MTBDDs.
Fig. 5 Relationship between recursive segmentation and MTBDDs.

Fig. 6 Decomposition of the EVBDD.

Then, we convert the MTBDD into an EVBDD. By decomposing the EVBDD, as shown in Fig. 6, we obtain the architecture in Fig. 4 (b). In Fig. 6, the column labeled as ‘ri’ in the table of each LUT memory denotes the rails that represent sub-functions in the EVBDD. And, the column ‘ai’ in Fig. 6 denotes the rails that represent the sum of weights of edges. In the EVBDD, “(ai, ri)” assigned to edges that cut across the horizontal lines represents the sum of weights and sub-functions, respectively. For more detail on this architecture, see 15).

In this architecture, the size of LUT memories realizing the recursive segmentation depends on the number of segments. Specifically,

**Theorem 1** Let seg_func(X, Y) be a segment index function obtained by a recursive planar segmentation. The segment index function can be realized by the segment index encoder shown in Fig. 4 (b) with at most \( \lceil \log_2 k \rceil \) rails and at most \( \lceil \log_2 k \rceil \) rails, where \( k \) is the number of segments.

**Proof:** See Appendix.

The segment index encoder satisfying Theorem 1 is obtained when the variable order for the EVBDD is \( x_l-1, y_l-1, x_l-2, y_l-2, \ldots, x-m, y-m \) from the top to the bottom (see the proof in Appendix). We can also use the optimization techniques for multi-valued decision diagrams presented in 13) to optimize the variable order for EVBDD.

In our architectures, the coefficients memory and the LUT memories of the segment index encoder are implemented by RAMs. Thus, by changing the data for the coefficients memory and the LUT memories, a wide class of two-variable functions can be realized by a single architecture.

### 5. Design Method for Symmetric Functions

**Definition 8** A two-variable function \( f(X,Y) \) is symmetric if \( f(X,Y) = f(Y,X) \).

Symmetric functions are commonly found in practical applications of NFGs. For example, \( \sqrt{X^2 + Y^2} \), which is used in converting from rectangular to polar coordinates, is symmetric. This section presents an architecture and a design method taking advantage of the function’s symmetry.

**Definition 9** A segmentation is symmetric if for every segment \( \{[B_{x1}, E_{x1}], [B_{y1}, E_{y1}]\} \) such that \( B_{x1} \neq B_{y1} \) or \( E_{x1} \neq E_{y1} \), there is another segment \( \{[B_{x2}, E_{x2}], [B_{y2}, E_{y2}]\} \) such that \( B_{x1} = B_{y2}, E_{x1} = E_{y2}, B_{y1} = B_{x2}, \) and \( E_{y1} = E_{x2} \). **Symmetric segments** are a pair of such segments.

**Lemma 1** Let \( f(X,Y) \) be a symmetric function, and let \( g_1(X,Y) \) and \( g_2(X,Y) \) be bilinear interpolations of \( f(X,Y) \) for symmetric segments. Then, \( g_1(X,Y) = g_2(Y,X) \).

**Proof:** See Appendix.

**Theorem 2** The segmentation of a symmetric function produced by the recursive planar segmentation algorithm is symmetric.

**Proof:** See Appendix.

From Lemma 1 and Theorem 2, we can use only one bilinear interpolation to approximate the given symmetric function in symmetric segments. By assigning the same segment index to symmetric segments, we can reduce the size of the coefficients memory by nearly half.
Table 1 Number of segments for two segmentation methods.

<table>
<thead>
<tr>
<th>No.</th>
<th>Function</th>
<th>Domain</th>
<th>X and Y have 8-bit accuracy</th>
<th>X and Y have 12-bit accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Acceptable approx. error: $2^{-10}$)</td>
<td>(Acceptable approx. error: $2^{-14}$)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$R_{11}$</td>
<td>$R_{12}$</td>
</tr>
<tr>
<td>0</td>
<td>$f_0$</td>
<td>$\sin(\pi X)\sqrt{Y}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>1</td>
<td>$f_1$</td>
<td>$\sin(\pi XY)$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>2</td>
<td>$f_2$</td>
<td>$X^4Y^{25}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>3</td>
<td>$f_3$</td>
<td>$1/\sqrt{X^2 + Y^2}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>4</td>
<td>$f_4$</td>
<td>$X\sqrt{Y^2 + Y^2}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>5</td>
<td>$f_5$</td>
<td>WaveRings</td>
<td>[0, $\pi$]</td>
<td>[0, $\pi$]</td>
</tr>
<tr>
<td>6</td>
<td>$f_6$</td>
<td>Sombrero</td>
<td>[0, 0.8)</td>
<td>(0, 0.8)</td>
</tr>
<tr>
<td>7</td>
<td>$f_7$</td>
<td>$\sqrt{X^2 + Y^2}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
<tr>
<td>8</td>
<td>$f_8$</td>
<td>$\sqrt{X^4 + Y^5}$</td>
<td>[0, 1)</td>
<td>(0, 1)</td>
</tr>
</tbody>
</table>

Uni.: Uniform segmentation. Recur.: Recursive segmentation. Sym.: Symmetric segmentation is counted as one segment. For functions $f_0, f_1, f_2$, approximated values are computed using Lemma 1. Since the comparator and multiplexers operate in parallel with the segment index encoder, there is no speed penalty due to these additional circuits.

Fig. 7 Architecture for two-variable NFGs for symmetric functions.

6. Experimental Results

6.1 Number of Segments and Computation Time for Algorithms

Table 1 shows the number of segments produced by the two segmentation algorithms presented in Section 3, and their computation time for various functions. This table also shows the number of symmetric segments for symmetric functions. In this table, WaveRings and Sombrero are

$$WaveRings = \frac{\cos(\sqrt{X^2 + Y^2})}{\sqrt{X^2 + Y^2} + 0.25} \quad Sombrero = \frac{\sin(\sqrt{X^2 + Y^2})}{\sqrt{X^2 + Y^2}}$$

Table 1 shows that, for all functions except $\sin(\pi XY)$ and Sombrero, the recursive segmentation algorithm produces many fewer segments than the uniform segmentation algorithm. Especially, for higher accuracy, the number of segments needed in recursive segmentation is only a few percent of the number of segments needed in uniform segmentation. And, the number of symmetric segments is even smaller. Thus, the recursive segmentation algorithm and the symmetric technique significantly reduce the number of words in the coefficients memory. For $\sin(\pi XY)$ and Sombrero, the additional segments needed in uniform segmentation are not so large even for higher accuracy. This means that, for these
functions, the uniform segmentation method also produces NFGs with reasonable size.

In addition, Table 1 shows that both algorithms produce segments with small CPU time. Such quick segmentation is useful to reduce design time for NFGs.

### 6.2 Memory Sizes Needed for Numeric Function Generators

Table 2 compares total memory sizes needed for the three NFGs shown in Fig. 3 and Fig. 7. Note that the NFGs based on recursive segmentation have two kinds of memories: coefficients memory and LUT memory. The memory size shown is the sum of the coefficients memory size and the LUT memory sizes.

Table 2 shows that, for all functions, NFGs based on recursive segmentation require smaller memory size than NFGs based on uniform segmentation, even though NFGs based on recursive segmentation have a segment index encoder. For example, for \( f_4(X, Y) = \frac{XY}{\sqrt{X^2 + Y^2}} \), the 12-bit accuracy NFG using recursive segmentation requires only 0.28% of memory required by uniform segmentation. Especially for symmetric functions, using the symmetric technique shown in Section 5 reduces the memory size significantly.

To understand the relation between memory size and accuracy, we designed NFGs for \( XY/\sqrt{X^2 + Y^2} \) with various accuracies. Figure 8 plots memory sizes of the NFGs for 4 to 16-bit accuracies. There are four curves:

1. a single look-up table in which the values assigned to \( X \) and \( Y \) form an address and the contents of that address is \( f(X, Y) \),
2. NFGs using uniform segmentation,
3. NFGs using recursive non-uniform segmentation, and
4. NFGs using the symmetric technique.

Interestingly, for this function, the memory size of the NFGs using uniform segmentation increases in the same way as the memory size of a single look-up table. On the other hand, the memory sizes of the NFGs using recursive segmentation and the NFGs using symmetric technique increase much more slowly than the other two. For 16-bit accuracy, the memory sizes of the NFG using recursive segmentation and the NFG using symmetric technique are only 0.06% and 0.03% of that of the NFG using uniform segmentation, respectively.

### 6.3 FPGA Implementation Results

To show the merits and demerits of the three proposed methods, we compare the performance of the NFGs designed by the three methods. We implemented 12-bit accuracy NFGs using the Altera Stratix III FPGA. Since the FPGA has adaptive look-up tables (ALUTs) that can realize fast adders, synchronous memory blocks, and dedicated multipliers, our NFGs are efficiently implemented by those hardware resources in the FPGA. Table 3 compares the FPGA implementation results of the NFGs. In this table, the three columns labeled “Delay” show the total delay time of each NFG from the input to the output, in nanoseconds.

The NFGs based on uniform segmentation require fewer pipeline stages and have shorter delay than the recursive segmentation because they have no segment index encoder. However, for six functions, the memory needed for NFGs based
Table 3  FPGA implementation of 12-bit accuracy NFGs.

<table>
<thead>
<tr>
<th>No.</th>
<th>Uniform segmentation</th>
<th>Recursive segmentation</th>
<th>Symmetric method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#ALUTs</td>
<td>#DSPs</td>
<td>Freq. [MHz]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f₀</td>
<td>–</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>f₁</td>
<td>49</td>
<td>5</td>
<td>203</td>
</tr>
<tr>
<td>f₂</td>
<td>206</td>
<td>0</td>
<td>306</td>
</tr>
<tr>
<td>f₃</td>
<td>–</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>f₄</td>
<td>–</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>f₅</td>
<td>–</td>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td>f₆</td>
<td>153</td>
<td>4</td>
<td>230</td>
</tr>
<tr>
<td>f₇</td>
<td>–</td>
<td>1</td>
<td>–</td>
</tr>
<tr>
<td>f₈</td>
<td>–</td>
<td>1</td>
<td>–</td>
</tr>
</tbody>
</table>

–: NFGs cannot be mapped into the FPGA due to insufficient memory blocks.

#ALUTs: Number of ALUTs. #DSPs: Number of 18-bit × 18-bit DSP units. Freq.: Operating frequency. #stages: Number of pipeline stages.

Table 4  FPGA implementation of various NFGs for \( XY/\sqrt{X^2+Y^2} \).

<table>
<thead>
<tr>
<th>NFGs</th>
<th>Memory [bits]</th>
<th>#LEs</th>
<th>#DSPs</th>
<th>Freq. [MHz]</th>
<th>#stages</th>
<th>Delay [usec.]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>12-bit accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>One-variable</td>
<td>269,136</td>
<td>266</td>
<td>10</td>
<td>192</td>
<td>14</td>
<td>73</td>
</tr>
<tr>
<td>Uniform</td>
<td>34,603,008</td>
<td>–</td>
<td>0</td>
<td>–</td>
<td>4</td>
<td>–</td>
</tr>
<tr>
<td>Recursive</td>
<td>293,330</td>
<td>220</td>
<td>6</td>
<td>228</td>
<td>10</td>
<td>44</td>
</tr>
<tr>
<td>Symmetric</td>
<td>153,176</td>
<td>273</td>
<td>6</td>
<td>222</td>
<td>11</td>
<td>50</td>
</tr>
</tbody>
</table>

which is based on linear approximation and non-uniform segmentation. Table 4 compares the results with our NFGs.

Our NFG based on recursive segmentation requires fewer ALUTs and DSPs than the implementation using one-variable NFG, and has much shorter delay. Especially, the NFG designed by the symmetric method achieves both less memory and shorter delay. This shows that the speed penalties caused by the recursive segmentation and the symmetric method are small enough.

From these results, we can see that by designing two-variable functions using one-variable NFGs, the required memory size can be reduced significantly. However, depending on the functions, it can produce a slow implementation because of additional logic, such as multipliers. Also, complicated architectures using
one-variable NFGs make error analysis harder, and it is harder to guarantee output accuracy. This increases design time. On the other hand, for a large class of functions, we can automatically generate fast and compact NFGs whose output accuracy is guaranteed.

7. Concluding Remarks

We have proposed programmable architectures and design methods for numeric function generators of two-variable functions. To realize a two-variable function in hardware, we partition the given domain of the function into segments, and approximate the given function by a polynomial in each segment. In this paper, we presented two planar segmentation algorithms which partition a given domain of two-variable function efficiently. We also presented a design method for symmetric two-variable functions. To the best of our knowledge, these are the first systematic design methods based on piecewise polynomial approximation for two-variable functions. Experimental results showed that for a complicated function, our automatically generated NFG achieves higher performance than the NFG that is manually designed in a conventional manner.

In the proposed architectures, the coefficients memory and the LUT memories of the segment index encoder can be implemented by embedded RAMs in an FPGA (e.g., M4Ks in Altera FPGAs). Thus, by changing the data for the coefficients memory and the LUT memories, a wide class of two-variable functions can be realized by a single architecture. Since just changing the RAM data can switch functions, we can switch functions without reprogramming the FPGA.

The algorithms and architectures presented in this paper can be easily extended to functions with three or more variables.

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References

Therefore, from Theorem A, we have this theorem.

**Theorem 1** Let \( \text{seg\_func}(X,Y) \) be a segment index function obtained by a recursive planar segmentation. The segment index function can be realized by the segment index encoder shown in Fig. 4 (b) with at most \( \lceil \log_2 k \rceil \) rails and at most \( \lceil \log_2 k \rceil \) Arails\(^{15}\).

**Proof:** By forming a variable

\[
Z = (x_{l-1} y_{l-1} x_{l-2} y_{l-2} \ldots x_{-m} y_{-m})
\]

from \( X \) and \( Y \), \( \text{seg\_func}(X,Y) \) obtained by the recursive planar segmentation algorithm can be converted into a \( k \)-valued monotone increasing function \( g(Z) \).

Therefore, from Theorem A, we have this theorem. \( \blacksquare \)

**Lemma 1** Let \( f(X,Y) \) be a symmetric function, and let \( g_1(X,Y) \) and \( g_2(X,Y) \) be bilinear interpolations of \( f(X,Y) \) for symmetric segments. Then, \( g_1(X,Y) = g_2(Y,X) \).

**Proof:** Let \( g_1(X,Y) = C_{xy}XY + C_{xz}X + C_{yz}Y + C_{02} \). From the definition of bilinear interpolation, in symmetric segments, the following hold: \( C_{xy} = C_{xy}, C_{xz} = C_{xz}, C_{yz} = C_{yz}, \) and \( C_{01} = C_{02} \). Therefore, we have the lemma.

To prove Theorem 2, we define the following:

**Definition A** *Diagonal segment* \( \{B_x, E_x\}, \{B_y, E_y\} \) is a segment such that \( B_x = B_y \) and \( E_x = E_y \).

**Theorem 2** The segmentation of a symmetric function produced by the recursive planar segmentation algorithm is symmetric.

**Proof:** Let \( \{B_{x1}, E_{x1}\}, \{B_{y1}, E_{y1}\} \) and \( \{B_{x2}, E_{x2}\}, \{B_{y2}, E_{y2}\} \) be symmetric segments. Since \( (B_{x1} + E_{x1})/2 = (B_{y2} + E_{y2})/2 \) and \( (B_{y1} + E_{y1})/2 = (B_{x2} + E_{x2})/2 \), the segmentation of the symmetric segments into four equal-sized square segments is symmetric. The segmentation of diagonal segment into four equal-sized square segments is also symmetric.

From Lemma 1, the maximum approximation errors caused in symmetric segments are equal. Thus, if a segment is partitioned, then another segment symmetric to the segment is also partitioned.

Therefore, the recursive planar segmentation algorithm produces a symmetric segmentation for a symmetric function. \( \blacksquare \)

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