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14. ABSTRACT

A promising method for advanced circuitry is the development of hybrid CMOS/nanodevice integrated circuits. This approach combines a semiconductor transistor system with a nanowire crossbar, with simple two-terminal nanodevices self-assembled at each crosspoint.

Such a circuit would combine a level of advanced CMOS fabricated by the usual lithographic patterning, and a nanowire crossbar fabricated by an advanced patterning technique, such as Step and Flash Imprint Lithography, a type of ultra violet-based nanoimprinting technology.

In this work two distinct arrears were addressed. 32nm dense feature printing, and fabrication and testing of an example crosspoint device. 32nm lines were defined using state of the art variable shape beam pattern generators. Feature fidelity was demonstrated for a variety of different patterns. Reproducibility of two-terminal crosspoint devices was tested using inexpensive metal-oxide-metal (M-Ox-M) junctions.

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Design and Fabrication

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Introduction

Bulk silicon MOSFETs [1-4] are extremely versatile electron devices combining a (relatively) easy fabrication with very high performance in a broad variety of logic and memory circuits. Moreover, the devices are scalable to deep-submicron range. This powerful combination has allowed the bulk MOSFET devices to serve as the work horse of the leading electronic technology, CMOS, for more than 30 years. However, as the bulk MOSFETs enter the sub-100-nm range, their further scaling runs into several problems, including short-channel effects and gate oxide leakage. Despite the recent experimental demonstrations of several bulk transistors with gate length below 20 nm [5-6], performance of these prototypes is far from perfect.

There is a growing consensus that continued high performance (good saturation at high ON current and high ON/OFF ratio) below 20 nm will require the use of advanced FETs, primarily double-gate MOSFETs with thin, undoped silicon-on-insulator (SOI) channel connecting highly doped source and drain. The main reasons in favor of this choice are as follows:

- Such devices are a close approximation to what may be called the ultimate MOSFET, because two gates allow a very effective control of the electrostatic potential of the channel, and hence the carrier transport.

- Although the fabrication of double-gate transistors is certainly more complex than that of the usual bulk MOSFETs, they have already been implemented in various geometrical versions, including planar [7], n-type [8] and vertical [9] geometries.

The theoretical predictions seem to indicate that physics allows FET channel length to be scaled down below 10nm, still enabling the performance necessary for operation of logic and memory circuits. However, these results also indicate that extremely tight control of the device dimensions be required, leading to a rapid increase of fabrication cost facilities that may reach the point of diminishing economic returns. As a result, ***the Si-MOSFET-based exponential Moore's Law progress may stop at L ~ 10 nm, i.e., long before fundamental physical limits have been reached.***

New Approach

A more promising way to proceed is the development of hybrid CMOS/nanodevice integrated circuits [10-12]. Such circuit combines a semiconductor transistors system with a nanowire crossbar, with simple two-terminal nanodevices self-assembled at each crosspoint. The basic architecture and functionality is depicted below.

Such a circuit would combine a level of advanced CMOS fabricated by the usual lithographic patterning, and a nanowire crossbar (Fig. la) fabricated by an advanced patterning technique, such as Step and Flash Imprint Lithography [13], a type of ultra violet-based nanoimprinting technology. Step and Flash Imprint Lithography, or S-FIL™ has already demonstrated an ability to print features as small as 20 nm [14]. UV imprint lithography has resolved features as small as 2.4 nm.

The crossbar wires are connected, at each crosspoint, by simple, similar, two-terminal devices with the functionality of programmable diodes (Fig. 1b). The dc *I-V* curve of such device has two branches corresponding to its two possible internal states. In the low-resistive state 1, the nanodevice is essentially a diode, while in the opposite state 0 the crosspoint current is very small. In order to switch the device from state 0 to state 1, the two nanowires leading to the device are fed by voltages $\pm V_{WRITE}$, with $V_{WRITE} < V_+ < 2V_{WRITE}$. (The right inequality ensures that this operation does not disturb the state of "semi-selected" devices contacting just one of the biased nanowires.) The opposite switching is performed similarly using the reciprocal switching with threshold V_- (Fig. 1b).

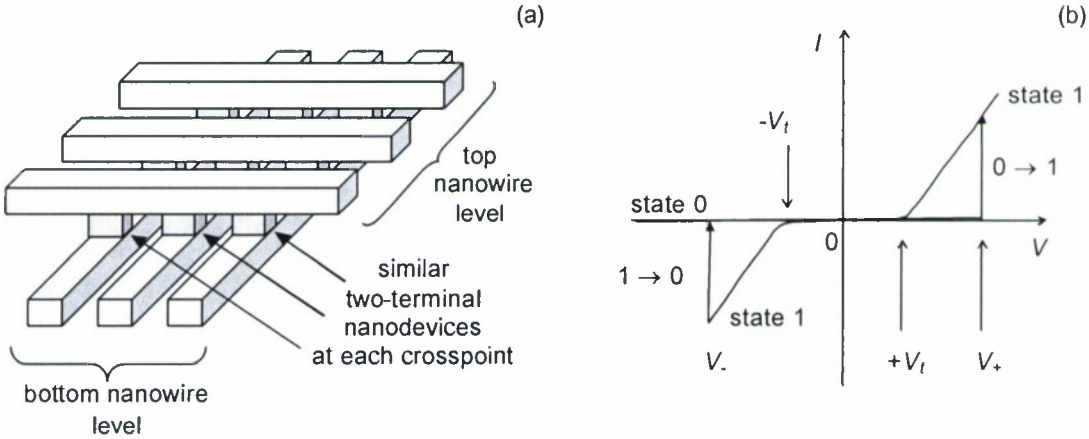

Fig. 1. (a) Crossbar array structure, and (b) *I-V* curve of a crosspoint nanodevice (schematically).

Proposed Work Plan

The proposed research is an inter-disciplinary effort that brings together the expertise in nanofabrication at Molecular Imprints, Inc., and hybrid circuit design expertise at SUNY, Stony Brook. Device architectures that are specifically suited for ease of integration of the nanowire cross-bars with their CMOS counterparts are studied. Also, these devices are designed to be tolerant to defects and alignment errors during the integration of nano-wires with CMOS. A novel nanofabrication process that includes imprint lithography in conjunction with a reverse tone etch process is proposed. This process allows for fabrication of nanowires over pre-existing topography. This is critical in fabricating fault-tolerant interconnections between the nanowire cross-bars and the underlying CMOS circuitry.

There are two aspects of S-FIL technology, that when combined, provide a novel fabrication scheme that is particularly suited for CMOL nano-wire fabrication and integration with CMOS: (i) Ability to print over topography using a reverse tone etch process known as S-FIL/R; and (ii) The ability to use the drop dispense technique to compensate for pattern density variations inherent in CMOS type designs. In particular, the via architecture that is suggested for CMOL integration in Figure 5 will require non-uniform material distribution to allow effective planarization over the topography and for high-throughput lithography [15].

The key to the formation of the hybrid device is the marriage of the traditional CMOS circuit to the nanowire crossbar array depicted in Figure 1a. The most practical interface proposed thus far, CMOL

[12] provides a network of conically shaped pins across the surface of the chip, at pitches commensurate with the CMOS subsystem. The conical shape provides a nanoscale dimension at the tip surface, thereby enabling contact to the crossbar array. A dielectric sidewall prevents shorting to the adjacent wires. A cross sectional view and a top-down view are provided in Figure 2.

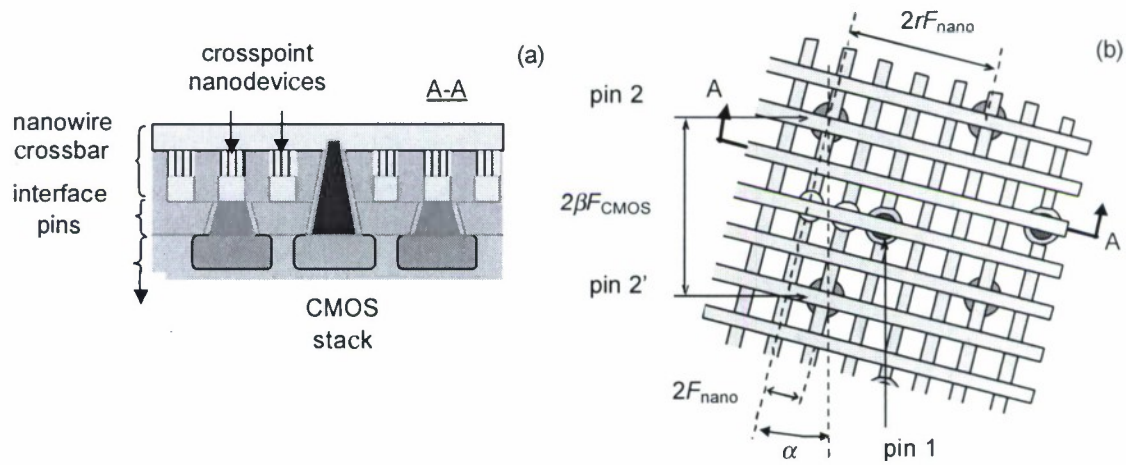

Fig. 2. The low-level structure of the generic CMOL circuit: (a) a schematic side view (cross-section along the A-A line shown in panel b) and (b) a top view. For clarity, the last panel shows only two adjacent crosspoint devices which may be addressed via pin pairs {1, 2} and {1, 2'}. The figure shows that the CMOS system has a unique access to each nanowire (and hence to each nanodevice) if the nanowire crossbar is rotated relative the interface pin array by a specific angle $\alpha = \arctan(1/r) = \arcsin(F_{nano}/\beta F_{CMOS}) << 1$. Here r is an integer, and β is the distance between the adjacent pins (leading to the same crossbar level), expressed in terms of the CMOS pitch $2F_{CMOS}$.

Phase I Technical Objectives

In order to address problems presented above, the following plan was put in place for Phase 1:

Demonstrate the formation of high density metal nanowires over a CMOL-like topography, using Step and Flash Imprint Lithography.

Several objectives need to be met in order to achieve the Phase I target:

1. *Prepare test wafers with features of comparable density to the CMOL interface level with a feature height*

Steps in this phase of the program would include:

a. Design of the CMOL-like level
b. Choice of pillar material
c. Choice of where to fabricate the test wafers
d. Fabrication of the test wafers

2. Develop a test template with a 32nm half pitch array of lines

Templates with 32nm features typically require the use of high resolution Gaussian beam electron beam writers. These tools are available through National Laboratories as well as select Commercial Mask Shops, such as Dai Nippon Printing and Hoya. A possible design would be the formation of an array of 63 nanowires at a half pitch of 32nm.

3. Develop the transfer layer and imprint layer stack necessary for defining the hardmask to be used for defining the metal nanowires.

The transfer layer properties must be compatible with both the underlying substrate and the imprint monomer. The material choice is dictated by material adhesion and cohesion, as well as whether a subtractive or lift-off process is required for metallization.

4. Develop the planarization and dry develop process and settle on either a subtractive or lift-off process.

Once the material stack is set, the etch process must be established. Steps include the Silspin coat, Silspin etch-back, and dry develop. The dry develop step will be sensitive to whether a subtractive or lift-off process is required. In the case of a subtractive etch, the dry develop must be very anisotropic, so as to minimize any CD bias. In the case of a lift-off process, the dry develop must allow for enough undercut to allow for a successful metal deposition, while avoiding contact with the adjacent feature.

5. Apply the newly fabricated template to the test wafers prepared in step 1, and form the metal nanowires across the CMOL-like surface.

In this step, the template is used to imprint the nanowire stack on the CMOL test wafers. The objective is to pattern transfer metal nanowires over the existing topography on the CMOL test wafers.

6. Verify that the metal lines are intact

To insure that the objectives are met, it will be necessary to inspect the finished wafers. Optical inspection will not be sufficient, since the 32nm half pitch lines will be too small to verify under a conventional microscope. High magnification scanning electron microscopy will be employed to verify that the array of lines are intact. Both top down and cross sectioned images will be taken of the final patterns.

A milestone chart that summarizes the work described above is shown below:

Task	Q1	Q2	Q3	Q4
1. Prepare CMOL test Wafers				
a. Design of the CMOL-like level	x			
b. Choice of pillar material	x			
c. Choice of where to fabricate the test wafers	x			
d. Fabrication of the test wafers		x		
2. 32nm Half Pitch Template				
e. Template design	x			
f. Choice of fabrication facility	x			
g. Resist optimization	x	x		
h. Fine Feature definition		x		
i. Dice and polish to form final template		x		
3. Transfer layer stack development				
j. Identification of material stack to be used on the wafer	x			
k. Choice of imprint material and transfer layer		x		
l. Imprint and transfer layer thickness optimization		x		
m. Imprint and transfer layer imprint demonstration			x	
4. S-FIL/R process development				
n. Choice of Silspin material		x		
o. Dry develop optimization			x	
p. Development of either a metal etch or a lift-off process			x	
5. CMOL integration demonstration				
q. CMOL wafer preparation			x	
r. Metal and transfer layer deposition			x	
s. Imprinting with the 32nm half pitch template				x
t. S-FIL/R patter transfer process				x
u. Metal etch				x
v. Resist Strip				x
6. Measurement Verification				
w. SEM				x
x. CD				x

Demonstration of patterned 32nm half pitch lines over topography – Molecular Imprints

The original intent of the work to be done by Molecular Imprints consisted of the following steps:

1. *Prepare test wafers with features of comparable density to the CMOL interface level with a feature height*

2. *Develop a test template with a 32nm half pitch array of lines*

3. *Develop the transfer layer and imprint layer stack necessary for defining the hardmask to be used for defining the metal nanowires.*

4. *Develop the planarization and dry develop process and settle on either a subtractive or lift-off process.*

5. *Apply the newly fabricated template to the test wafers prepared in step 1, and form the metal nanowires across the CMOL-like surface.*

6. *Verify that the metal lines are intact*

Although this work was not completed, an alternative method for fabricating the test template was explored. Originally, it was anticipated that low throughput Gaussian beam (GB) pattern generators would be required to pattern the templates. Although these systems have sufficient resolution at 32nm, they are not considered production worthy for several reasons:

a. The GB systems are slow and exposure times are not suited for full field patterns
b. Image placement of the patterns is marginal
c. The systems are not designed for production, and are therefore more likely to add defects during the writing process.

For device manufacturing, one of the major technical challenges remains the fabrication of full-field 1X templates with commercially viable write times. Recent progress in the writing of sub-40 nm patterns using commercial variable shape e-beam VSB tools and non-chemically amplified resists has demonstrated a very promising route to realizing these objectives, and in doing so, has considerably strengthened imprint lithography as a competitive manufacturing technology for the sub 32 nm node. In this report the first imprinting results from sub-40 nm full-field patterns, using a flash memory production device design. The fabrication of the template is described and the resulting critical dimension (CD) control and uniformity are reported, along with image placement results. The imprinting results are also described in terms of CD uniformity, and linewidth roughness (LWR). Finally a follow-up experiment was run to understand whether the process could be extended down to half pitches as small as 32 nm.

1. Experimental Details

To generate the template, patterns were exposed using 50 keV variable shaped beam pattern generators. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm template. [16]

The pattern chosen for full field evaluation was a 38 nm half pitch NAND Flash gate layer. The patterned area consisted of repeating core, a repeating periphery and non-repeating test chips. The approximate device size was 18 mm x 30 mm. Key elements of the repeating core are the dense 38 nm lines and the transition regions to larger pitches at right angles to the primary pattern. This is best illustrated in the lower right hand corner of Figure 3. Write time of the imprint mask was approximately 10 hours.

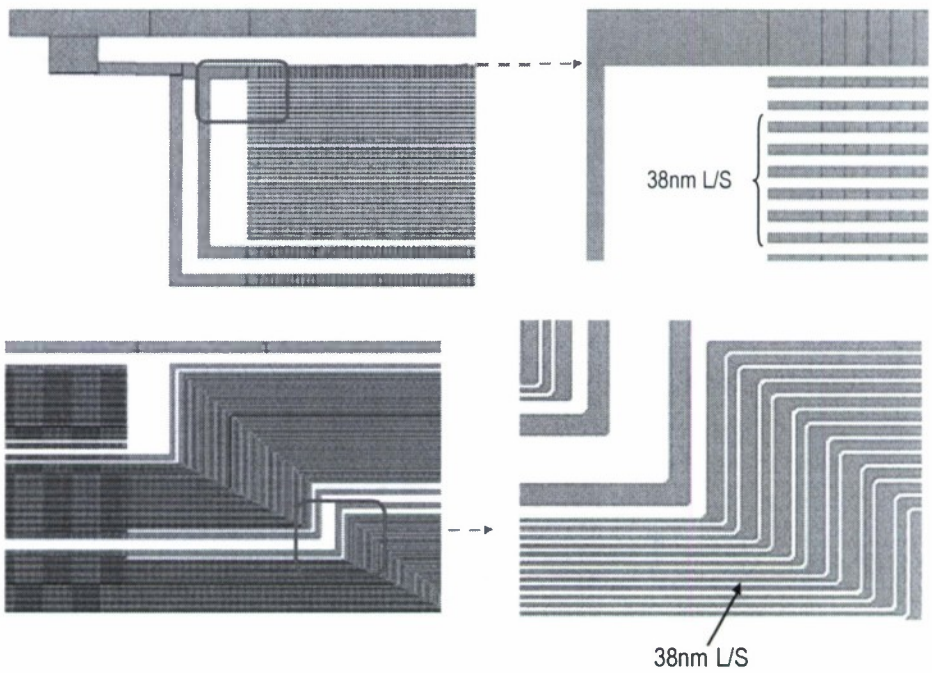

Figure 3. Key elements of gate layer, including the dense 38 nm lines and the transition regions to larger pitches at right angles to the primary pattern.

Imprinting of the template pattern was performed by using a Molecular Imprints Imprio 250 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported [17].

CD and LWR measurements were performed two different ways. In the first case, high resolution SEM images were taken with a JEOL JSM-6340F field emission cold cathode SEM equipped with a tungsten emitter. The accelerating voltage can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5 nm at 1 kV. Critical dimension (CD), linewidth roughness, and line edge roughness (LER) data were then extracted offline using the SIMAGIS® automated image metrology software suite from Smart Imaging Technologies [18]. For the analysis of within wafer uniformity and wafer-to-wafer uniformity, an AMAT NanoSEM was used to collect information on CD, LWR and LER. The beam accelerating voltage was 500V. The length of a line scan was 1 μm, and 512 scans were performed.

2. Results

a. Full Field Template Fabrication and Characterization

The template was written using a high resolution ZEP520A resist process. A multipass writing strategy was employed to compensate for the low resist sensitivity. It is important to note that the write times were still reasonable (~ 10 hours) when compared with a 4X photomask counterpart. This an expected result, due primarily to the reduced writing area and no requirement for optical proximity correction (OPC). Previously published results on two different 32 nm patterns have demonstrated a reduction in write time (relative to a 4X photomask) of 1.2x to 3x [19].

A brief analysis of the template was done after the fused silica etch, but before the chromium was stripped. Pattern fidelity is illustrated in Figure 4. The 38 nm half pitch lines are well resolved. The spaces measure 33.1 nm and the 3σ variation for five locations was 2.2 nm. The linewidth roughness measurements on the template ranged from 3.9 nm to 5.1 nm, 3σ. It should also be noted that, although no pattern optimization was done in the non-repeating test areas, several of the test patterns were resolved below 38 nm.

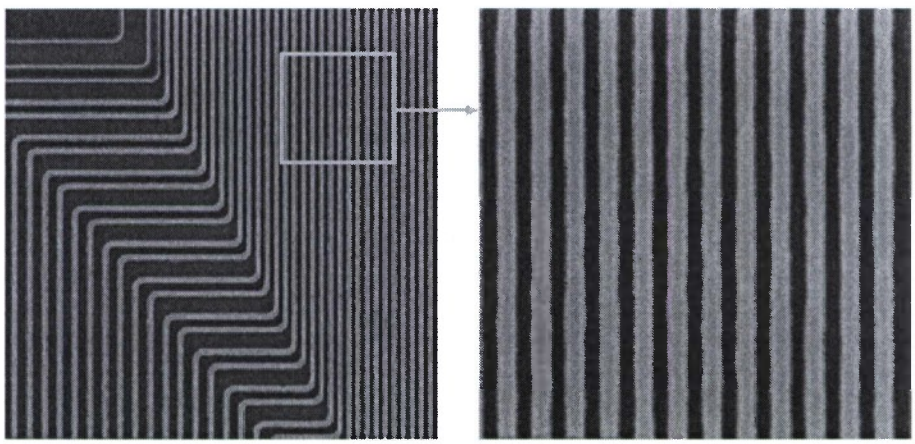

Figure 4. A template images of the primary pattern of the 38 nm NAND Flash Gate layer. The 38 nm half pitch lines are well resolved and the right angle transition regions are characterized by good fidelity in the corner areas.

A set of nine metrology marks were also included in the pattern, in order to determine image placement. An LMS IPRO II metrology system was used to read the nine marks. The 3 sigma variation in x and y, was extremely low: 1.6 nm and 2.6 nm, respectively. For future templates, a larger set of marks will be measured in an attempt to verify these results.

b. Imprint Results

The template was used to imprint the device on 300 mm wafers. The resulting imprints are shown in Figure 5. Figure 5a depicts a low magnification image of the gate layer. All patterns were clearly resolved, including both the 38 nm half pitch lines and the right angle transition regions. Figure 5b shows a larger magnification of the same region. 30 degree tilted views show the resolution of both regions described above. The 38 nm lines have a profile close to 90 degrees, and there is very little line width roughness observed. A SIMAGIS calculation of the features in Figure 5c yields a CD of 39.6 nm and LWR of only 3.7 nm, 3σ. Figure 5d depicts a magnified view of the well defined corner regions. SIMAGIS software was also used to measure in field CD uniformity. Eighteen locations were measured in the core area. Each location used eleven lines to determine CD. As a result a total of 198 lines were measured. The mean CD was 41.9 nm with a three sigma variation of 2.13 nm. LWR was 3.56 nm, 3σ.

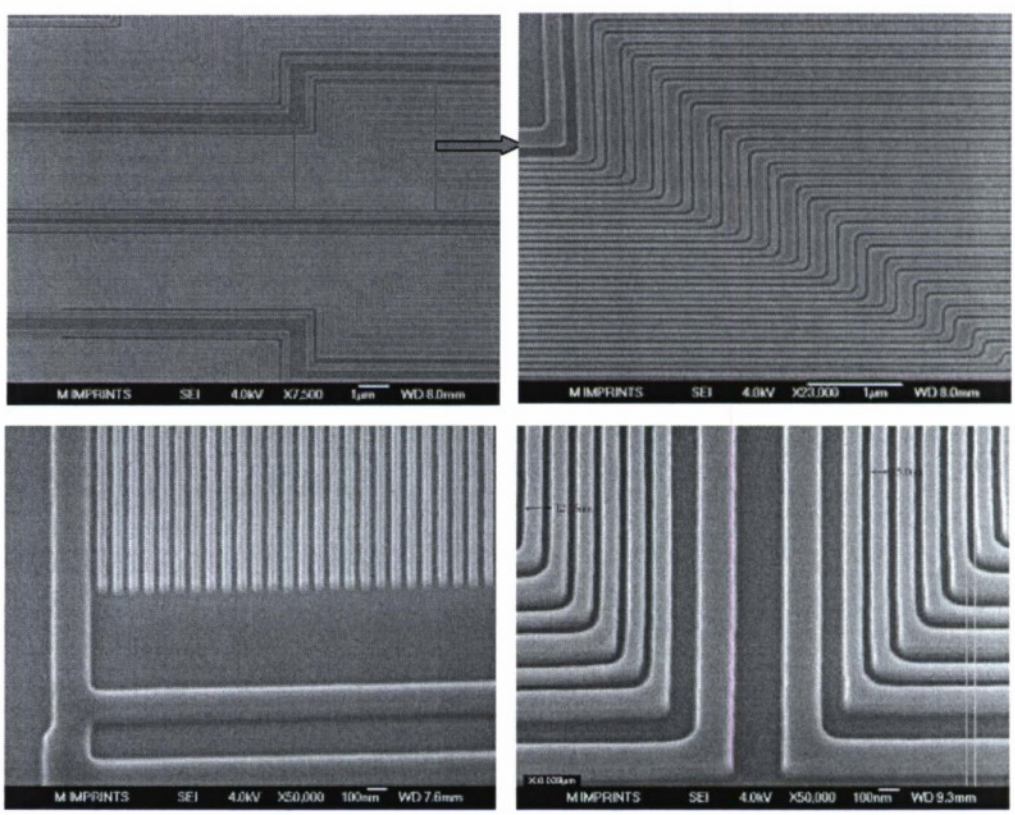

Figure 5. Imprinted 38 nm half pitch lines are resolved and feature fidelity is excellent in the transition regions.

Field-to-field and wafer-to-wafer uniformity was measured using an AMAT CD SEM. Nine measurements were made per repeating device core, for a total count of 18 measurements per field. Three fields were measured per wafer across a four wafer set (See Figure 6). The field-to-field 3σ variation was only 3.17 nm and corresponding wafer-to-wafer variation was only 0.51 nm (less than measurement repeatability of the CD SEM (~ 1 nm)). The average LWR and LER values were 3.76 nm and 2.39 nm, respectively.

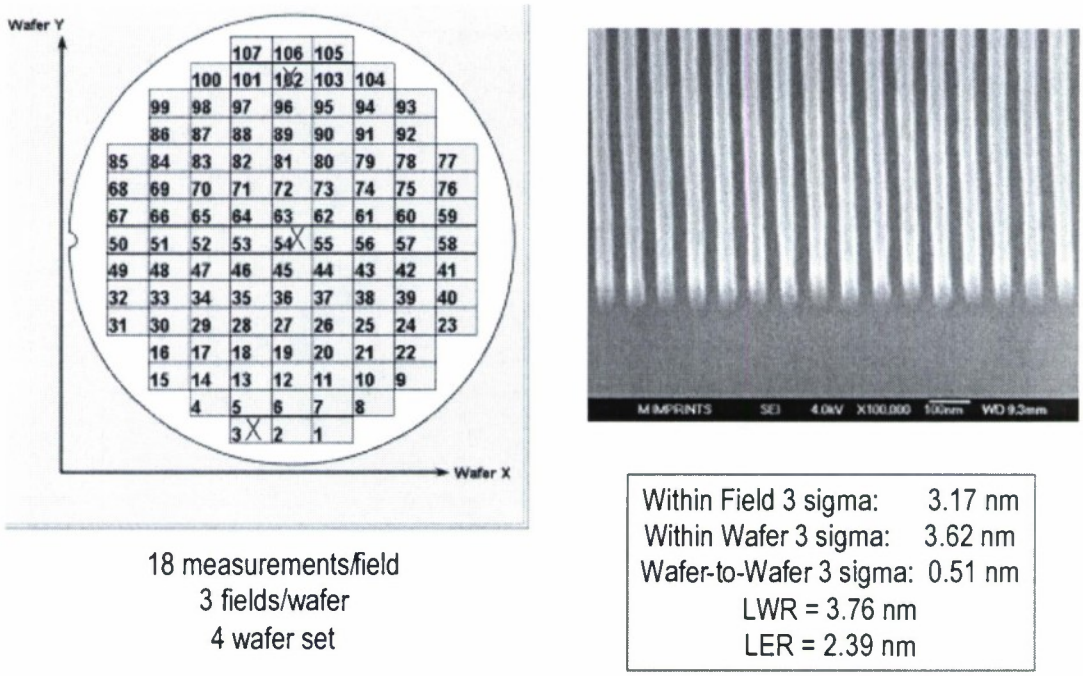

Figure 6. In order to determine field-to-field and wafer-to-wafer variations, 18 measurements were made within a field, at three field locations (marked with an "X" in the figure), across a four wafer set.

c. 32 nm Test Patterns: Template Fabrication

To determine best resolution, a second plate was written with patterns as shown in Figure 7. In addition to more conventional line/space and hole arrays, Metal1-like and CMOS test array patterns were included and are depicted in the bottom of the figure. Minimum half pitch for most patterns was 32 nm, and for the case of lines and holes, 28 nm half pitch features were also included.

The results for both lines and holes are shown in Figure 8. The SEM images depict clear resolution of the 32 nm patterns. Uniformity, shown on the bottom half of the figure was also mapped across a 20 mm x 20 mm area. Three sigma values of 3.22 nm and 4.29 nm were obtained for lines and holes, respectively.

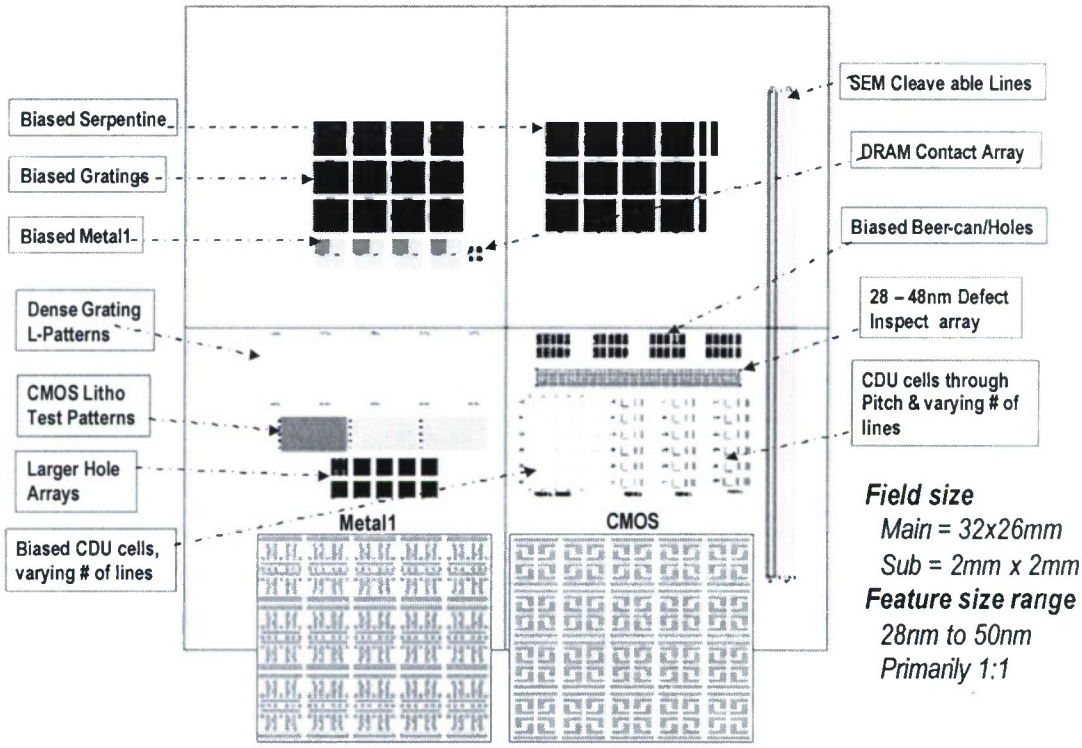

Figure 7. A schematic illustration of a test pattern used to determine resolution of VSB pattern generators. Typical minimum feature size was 32 nm for several pattern types.

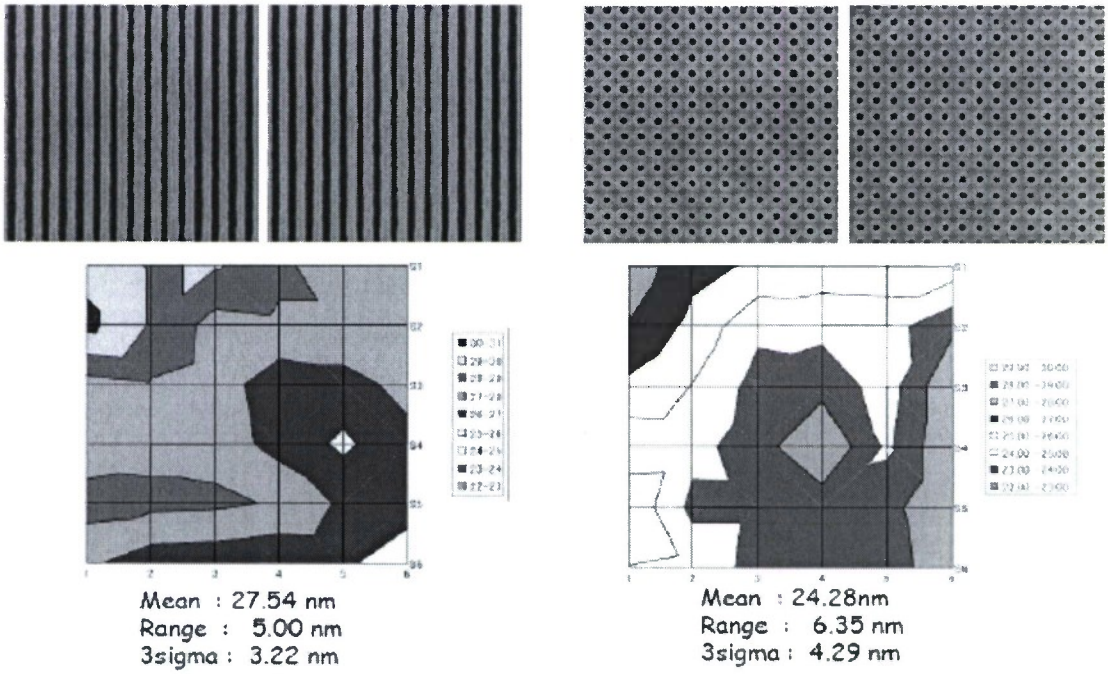

Figure 8. Results from an imprint mask, after the fused silica etch. Lines and holes were clearly resolved at half pitches of 32 nm. CD uniformity for the lines and holes was 3.22 nm and 4.29 nm (3σ), respectively.

d. 32 nm Test Patterns: Imprint Results

The template was used to imprint on 200mm wafers, and the initial results are quite promising. Pictured in Figure 9 are several different 32 nm patterns. It should also be noted that in some cases the 28 nm half pitch lines were resolved. The process window appears small however for 28 nm, and e-beam resist exposure conditions will need to be optimized. Further studies are also required to better understand the process window and CD uniformity for all feature types and sizes.

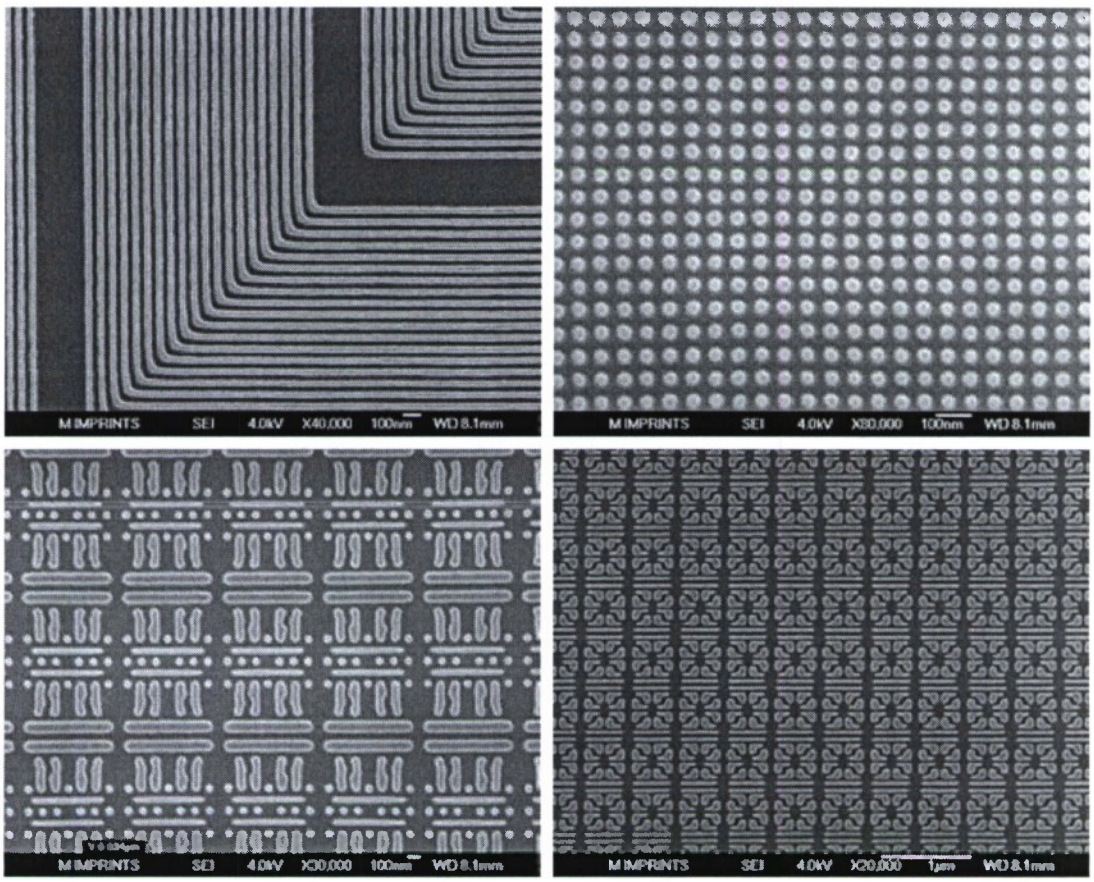

Figure 9. Imprint results for several 32 nm patterns: a) lines, b) holes, c) Metal1, and d) CMOS test pattern. In some cases, the 28 nm half pitch lines (not pictured) were also resolved.

4. Conclusion

Previous results in fabricating imprint masks using variable shape beam generators were limited in resolution, primarily through the use of fast chemically amplified resists. By applying a high resolution ZEP520A resist process, a 38 nm half pitch NAND Flash gate level template was successfully fabricated. Resolution, CD uniformity, and image placement were excellent across the full field. Mix and Match tests (not shown in this paper) demonstrated overlay better than 30 nm, 3 sigma. Further exposures have now demonstrated the ability to extend the process to dimensions of 32 nm. Next steps include further improvements in both resolution and overlay in order to address 22 nm half pitch circuitry.

SBU Device Design, Fabrication and Test

The work plan called for the following device, design and test activities:

1b. Design of the CMOL-like level
5q. CMOL wafer preparation

A key issue of hybrid circuit development is the improvement and scaling of the crosspoint devices with the functionality of programmable diodes (Fig. 1b). Devices of this type have been demonstrated using several structures, notably including amorphous metal-oxide films, relatively thick organic films (both with and without embedded metallic clusters), self-assembled molecular monolayers, and thin chalcogenide and crystalline perovskite layers [20-25]. However, the device bistability mechanisms are not yet clear, though for the (currently, most reproducible) metal-oxide devices (Fig. 10a) the mechanism is probably the single-electron trapping in localized states.

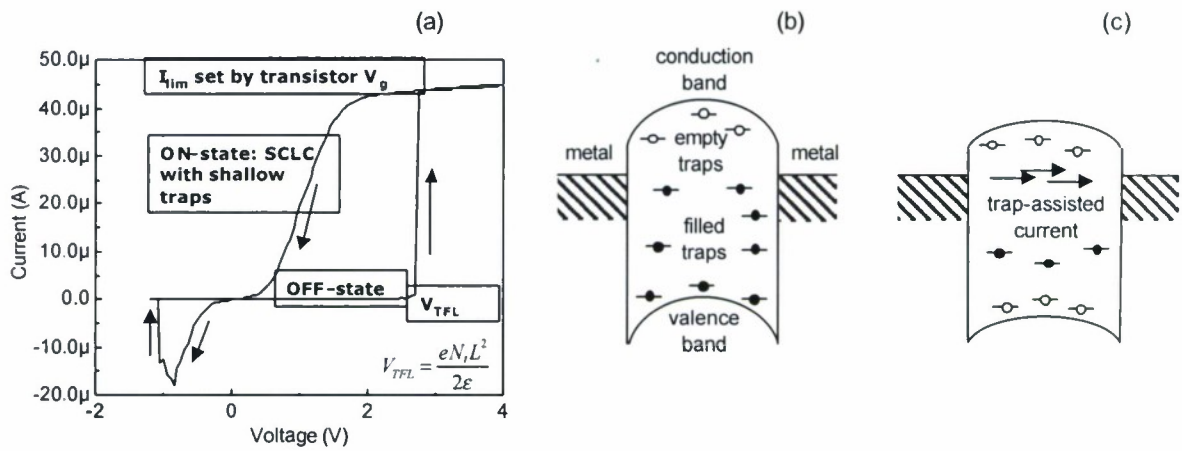

Fig. 10. (a) A typical dc *I-V* curve of a metal-oxide junction and (b, c) the band-edge diagrams of the structure in (b) OFF and (c) ON states, explaining the possible origin of its bistability.

(i) Bistable device fabrication and testing.

The goal of this work had been to explore various routes to reproducible fabrication of two-terminal crosspoint devices, with the desired latching switch functionality (resistive bistability), and recycling endurance, using inexpensive metal-oxide-metal (M-Ox-M) junctions.

We have fabricated and characterized numerous (~500) devices from 10 wafers with M-Ox-M junctions based on the three metal oxides which seemed most promising from literature data: CuO_x, NbO_x and TiO_x. Metallic base films have been deposited by either dc sputtering or e-beam evaporation. In the latter case, the wafer were then transferred in the sputtering system for cleaning/oxidation and counter-electrode and contact metal deposition. The subsequent patterning has been done with UV lithography

and reactive ion etching. After the fabrication, samples electrically characterized both "as is" and after additional rapid thermal post-annealing (RTA). Table 1 lists major parameters of these wafers.

Table 1

Interlayer material	Wafer	Oxidation	Power (W)	O_2 Pressure (mTorr)	Time (min)	Rapid thermal annealing parameters
Copper oxide	VJCuOx3	Thermal		100,000	40	n/a
	VJCuOx4	Thermal		100,000	40	400°C, 180s
	VJCuOx5	Plasma	10	15	10	200 to 300°C, 20 to 30s
	VJCuOx6	Plasma	50	15	10	400°C, 30s
	VJCuOx7	Plasma	100	15	10	400 to 800°C, 30 to 180s
Niobium oxide	VJNbOx1	Thermal		100,000	40	400°C, 30s
	VJNbOx2	Plasma	10	15	10	400°C, 30s
	VJNbOx3	Plasma	10	15	10	400 to 600°C, 30 to 180s
Titanium oxide	VJTiOx1	Thermal		100,000	40	400°C, 30s
	VJTiOx2	Plasma	50	15	10	400 to 800°C, 30s

The results of device property measurement may be summarized as follows:

1. In order to observe the desired bistability effect (illustrated on Fig. 11), junction "formation" process with current "compliance" (restriction), at a level between 10^{-4} and 10^{-2} A, is necessary.

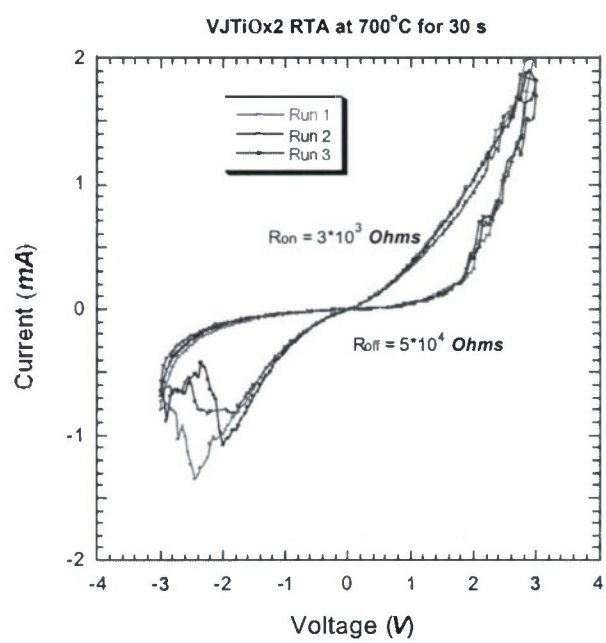

Fig. 11. A typical *I-V* curve of a M-Ox-M junction, showing the resistive bistability ("memory") effect.

2. Using that formation procedure, the bistability effect may be obtained in junctions from most fabricated wafers, though thermal oxidation provides much lower yield of bistable devices.

3. After moderate RTA, some plasma-oxide wafers have up to 50% of junctions which showing repeatable switching between two stable states, with endurance ranging from 5 to 1000 cycles (see, e.g., Fig. 12).

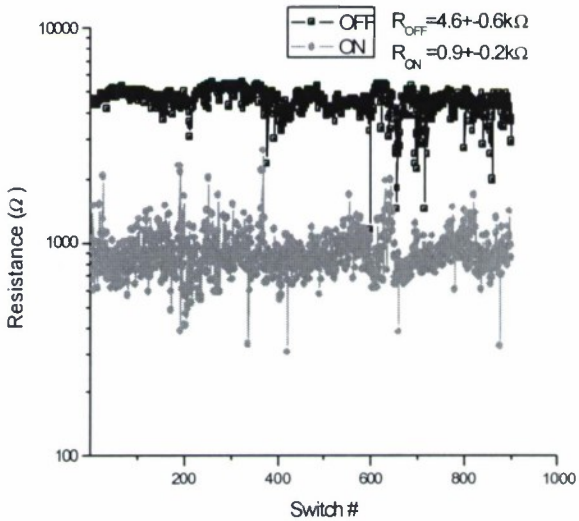

Fig. 12. Endurance testing of a bistable junction using a series of volt each positive and negative voltage pulses.

Our hopes are to improve these results significantly during the anticipated Phase 2 of the STTR project.

(ii) Interface development.

We have carried out a preliminary design of the CMOS chips which will be used for the CMOS/nanodevice interface fabrication, and are in the process of its discussion with the planned chip manufacturer (MOSIS, Inc.). We are presently in the process of negotiations with MOSIS concerning the removal of polyimide passivation which presents significant problems for CMP planarization.

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Publications

(i) K. K. Likharev, "Resistive and Hybrid CMOS/Nanodevice Memories". In: J. E. Brewer and M. Gill (eds.), *Nonvolatile Memory Technologies with Emphasis on Flash*, Wiley, Hoboken, NJ, pp. 696-703 (2008).

(ii) K. K. Likharev, "CMOL and Cousins: Hybrid CMOS/nano Circuit FAQs". Accepted for publication in *Proc. CODES-ISSS* (2008).

(iii) K. K. Likharev, "Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges". Submitted for publication in: R. Waser (ed.), *Nanoelectronics and Information Technology*, 3rd ed., Wiley-VCH, (2008).

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