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Analysis of substrate noise coupling has been performed for a 0.18μm lightly doped silicon germanium BiCMOS process. Techniques to minimize noise coupling in the chip and board design are presented, as well as methods for accurate modeling for substrate noise coupling simulations. Measurements from a test chip were taken to verify that the modeling approach used in simulation and the substrate noise model obtained using Silencer! is accurate to within 10%. The effects of a deep trench moat structure, bulk separation, and die perimeter ring were also tested as possible noise reduction methods. Strategies for simulation and measurement of substrate noise coupling in a 0.18μm SOI process are also presented.

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Substrate Noise Coupling Analysis in 0.18μm Silicon Germanium (SiGe) and Silicon on Insulator (SOI) Processes

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Substrate Noise Coupling Analysis in 0.18μm Silicon Germanium (SiGe) and Silicon on Insulator (SOI) Processes

1. INTRODUCTION

As analog, digital and RF circuits are integrated onto the same chip in CMOS technology to create system on chips (SoCs), problems like noise coupling from digital to analog and RF circuits through the common silicon substrate, the power supply and package parasitics arise. SoCs have many advantages such as reduced size and cost, and lower power consumption. However, the advantages have to be weighed against the effect of noise coupling and how much it degrades the circuit performance.

Power supply noise coupling occurs because of the presence of parasitic resistances and inductances in the supply line. When digital circuits turn on and off, current spikes create an $L\frac{di}{dt}$ voltage variation. This creates supply bounce or ground bounce. This noise can be coupled to more sensitive analog and RF circuitry through interconnects, and also injects noise into the substrate through substrate taps and junction capacitances.

It can be costly to fabricate a chip, only to find that there is noise coupling such that the sensitive analog and RF blocks do not perform as expected. Thus a method of estimating and simulating the amount of noise coupling expected before a chip is fabricated is essential. There has been work done in this area [1–6], and the work presented here further contributes by illustrating the proper inclusion of package parasitics, interconnects and parasitics from the PCB test board in design fabricated in a silicon germanium process and silicon-on-insulator process.

This thesis examines simple analog and digital blocks such as a sense amplifier and a stepped buffer, respectively, in two different 0.18μm processes. The first process is a lightly doped silicon germanium (SiGe) BiCMOS process, and the other is a fully depleted (FD) silicon-on-insulator (SOI) process. Chapter 2 provides some background on the model used in calculating the resistive substrate network between noise injector and sensor contacts, which is then used in simulations to determine the effect of substrate noise coupling on circuit performance. Other sources of noise such as power supply lines and package parasitics, and how this is modeled in simulations to obtain better agreement with measurement results is also discussed in Chapter 2. Chapter 3 describes the digital circuit that injects noise and the sensitive analog circuits that pick up this noise. Chapter 4 presents modeling techniques used in simulations. Chapter 5 explains the measurement approach and results for the 0.18μm BiCMOS test chip, packaged in a 132 pin grid array (PGA) package. These measurements verify that the simulation approach with package parasitics and the substrate noise model included is accurate to within 10%. From simulations and measurements, possible noise suppression techniques have been evaluated. Chapter 6 presents measurement results and simulation techniques for the SOI test chip. Chapter 7 generalizes the results obtained for the BiCMOS process. Chapter 8 concludes this thesis and discusses future work related to this topic.

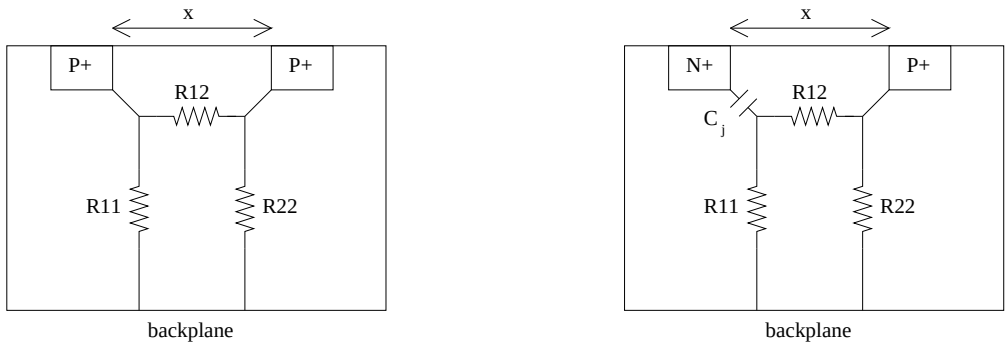
2. BACKGROUND ON SUBSTRATE COUPLING MODEL AND POWER SUPPLY AND PACKAGE PARASITICS

2.1. Substrate Coupling Model

At low frequencies (< 2GHz), the substrate network for noise coupling can be modeled as a purely resistive network. A scalable macromodel has been developed by Ozis et al. [8, 9] for the efficient calculation of a resistive substrate network. Another method for the calculation of the resistive substrate network is a Green's function based solver. In this thesis, the Green's function solver EPIC [7], is used to obtain the resistive substrate network for simulating substrate noise coupling. This method of obtaining the substrate network is computationally more intensive, but yields more accurate results than using a scalable macromodel. Another reason that EPIC was chosen over using the macromodel was because curve fitting of parameters for the macromodel has to be done for each different type of substrate, whereas the input format for using EPIC only requires a multi-layer substrate profile.

The substrate model is treated as a lumped resistive network as the frequency range of operation is below a few gigahertz. Figures 2.1(a) and 2.1(b) show the lumped substrate model for a two contact case for p+ to p+ contacts and n+ to p+ contacts, respectively. The resistance R_{12} models the coupling between the two contacts, while R_{11} and R_{22} model the coupling from each contact to the backplane, or substrate. Cj models the junction capacitance from the n+ contact to the p-type substrate.

Figures 2.2 and 2.3 show the cross-sections of a lightly doped substrate without and with a buried layer, respectively. A typical lightly doped substrate without a buried layer is represented by two layers, a heavily doped p+ channel-



(a) (b)

FIGURE 2.1. Lumped substrate model. (a) p+ to p+ model. (b) n+ to p+ model.

stop region and a lightly doped p-type bulk. A lightly doped substrate with a buried layer has an additional low resistivity buried layer added. The BiCMOS process uses a lightly doped substrate with a buried layer, and a generic four layer substrate profile is shown in Figure 2.3, and used for extraction of the resistive network with EPIC.

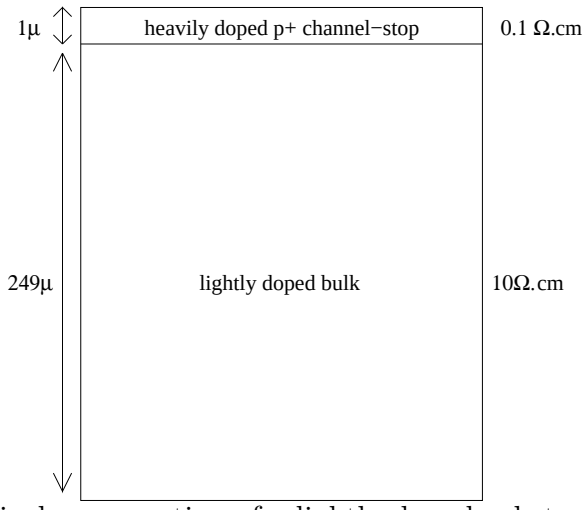


FIGURE 2.2. Typical cross-section of a lightly doped substrate without a buried layer.

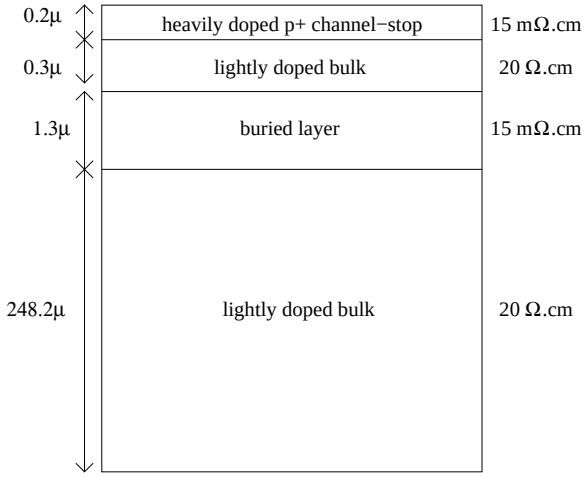


FIGURE 2.3. Typical cross-section of a lightly doped substrate with a buried layer.

Figure 2.4 shows the cross section of a FD SOI process. It differs from a regular CMOS process in that an extra buried oxide (BOX) layer is present between the substrate (bulk) and the region where the transistors are fabricated. This BOX layer isolates the body of transistors from the substrate, thus less noise is expected to be injected into the common substrate. Compared to a regular CMOS process, the performance of analog circuits should not be degraded as much due to substrate noise.

2.2. Power Supply and Package Parasitics

For accurate modeling of noise coupling from digital to analog circuitry, the power supply parasitics from the package and interconnects have to be taken into account. The choice of a package is important as the parasitic package inductance is different for each type of package. For example, flip-chip packages generally have low values of parasitic inductances ranging from 0.01nH to 0.1nH, while quad flat

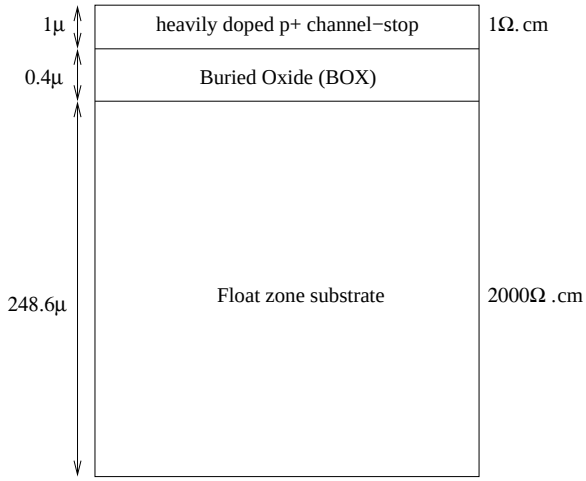


FIGURE 2.4. Cross-section of the SOI substrate (RF process).

packs (2-15nH), ball grid and pin grid arrays (2-14nH) and dual inline packages (4-23nH) have higher parasitic inductances.

The package used for both test chips in this thesis is the Kyocera 132-pin ceramic pin grid array (CPGA) package. Since the die cavity (350 square mil) in this package is much larger than the actual die size, bondwire lengths are long (4-6mm), and have to be taken into account as supply parasitics. The package characterization data was obtained from the package model from MOSIS [19]. On-chip interconnect resistances were also modeled and included in the simulations. Off-chip decoupling capacitors were used to reduce the supply bounce in measurements. Figure 2.5 [10] shows the set up for including the power supply parasitics and the substrate network for one stage of the stepped buffer in simulations.

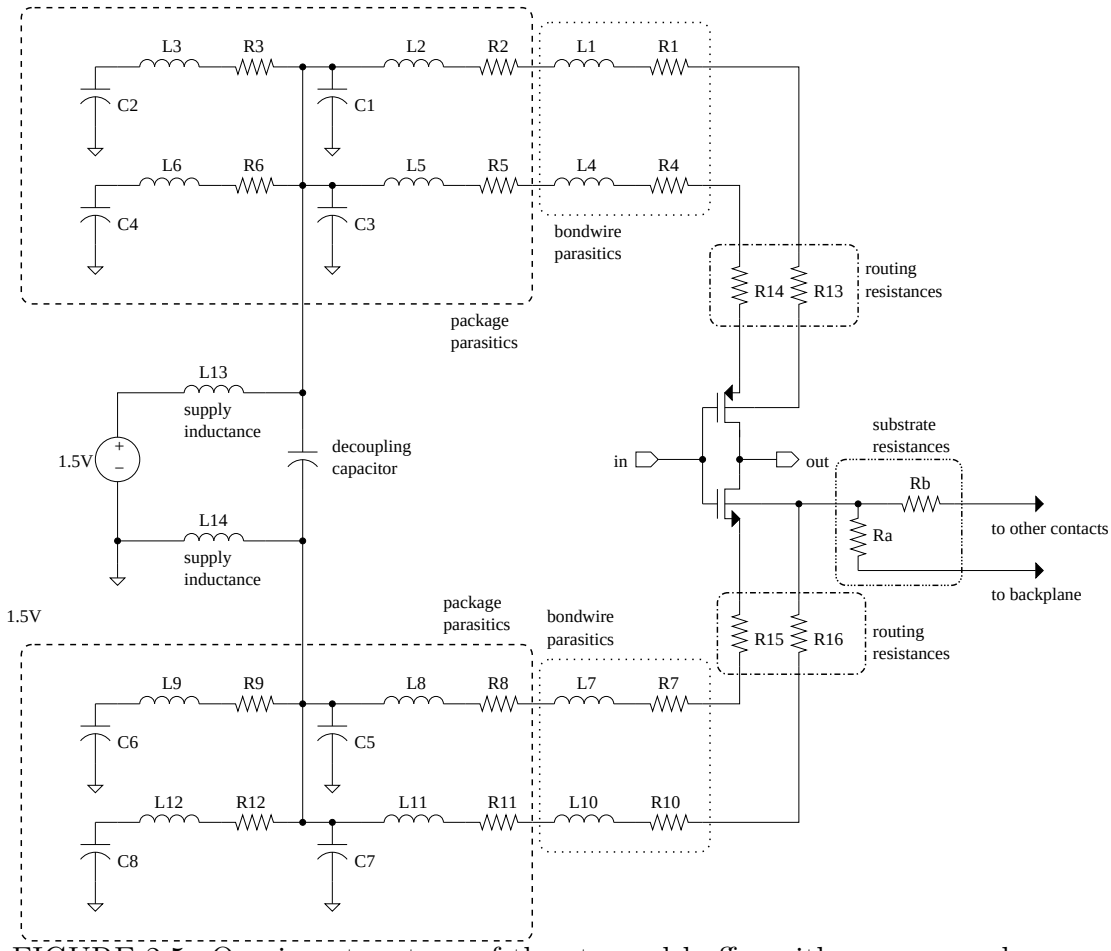


FIGURE 2.5. One inverter stage of the stepped buffer with power supply parasitics and the substrate network.

3. DIGITAL AND ANALOG TEST CIRCUITS

3.1. Stepped Buffer Circuit

Stepped buffers are commonly used in digital circuits as an output buffer to drive large off-chip capacitance or as buffer amplifiers for clock signals. A seven stage stepped buffer is used as a digital noise generator in simulations and measurements. This is a simple circuit consisting of seven inverter stages, with each stage a factor of e larger than the previous stage, as shown in Figure 3.1. The output of each inverter stage is also loaded by an inverter of the same size to inject more noise into the substrate. Figure 3.2 shows the actual transistor level implementation of the stepped buffer. APPENDIX A shows the transistor sizing for the stepped buffer.

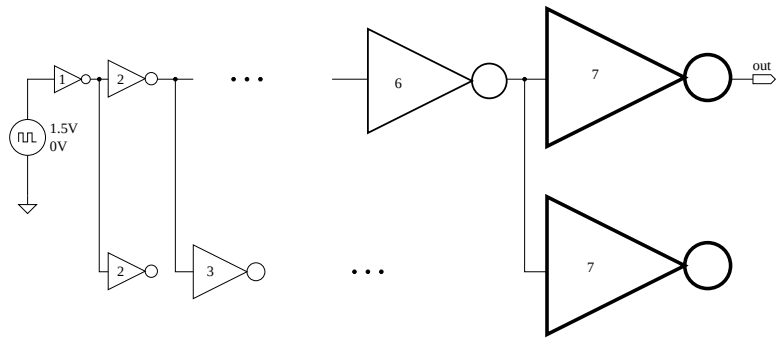


FIGURE 3.1. Seven stage stepped buffer circuit.

There were two versions of the stepped buffer on the BiCMOS chip, one with the bulk of the transistors tied to the supply rail (referred to as *step1* from this point on), and the other with the bulk of the transistors connected to a separate pin (referred to as *step2* from this point on). The layouts for *step1* and *step2* are shown in APPENDIX B. In the SOI version, *step3* is the stepped buffer with floating body transistors, and *step4* is the one with with body ties.

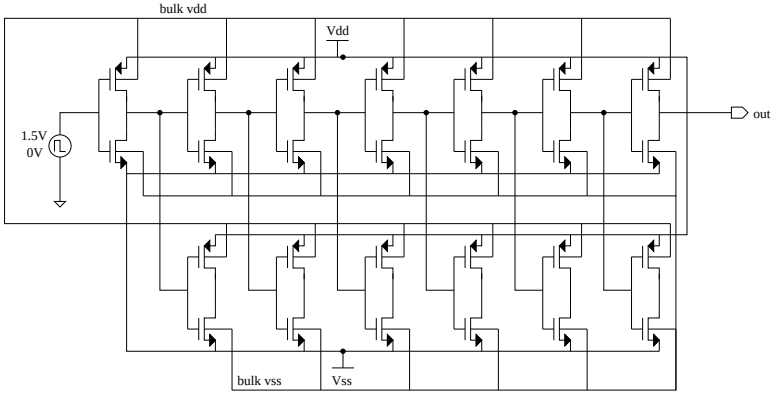


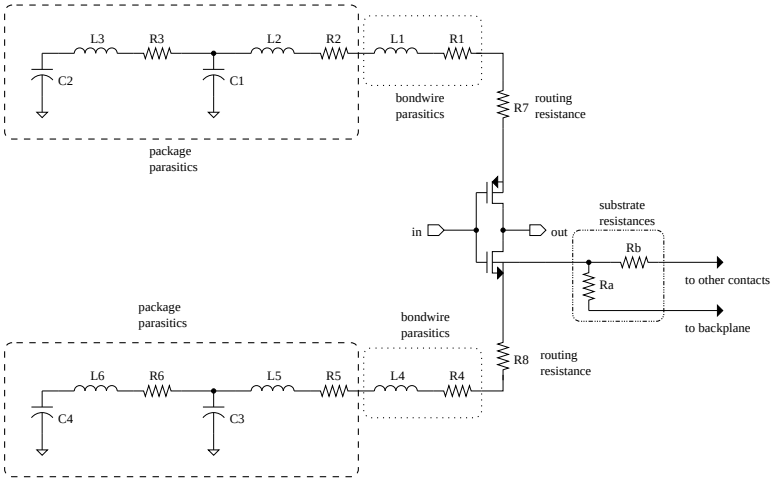
FIGURE 3.2. Seven stage stepped buffer schematic.

The layout for *step3* is shown in APPENDIX C. The layout for *step4* is similar to that of *step3*, with body ties added.

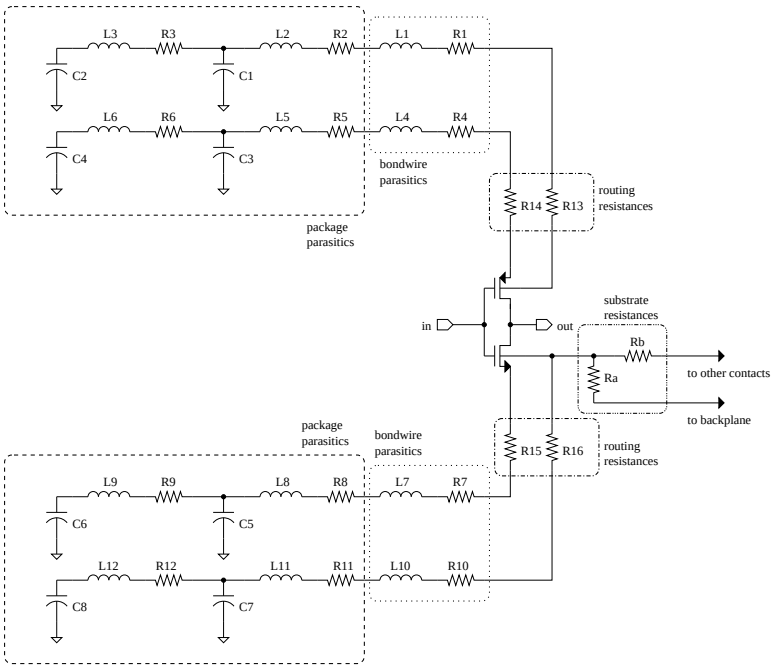
Figure 3.3 [10] show the power supply parasitics when the bulk nodes of the transistors are tied to the source nodes (using one pin per supply rail) and when the bulks are separated from the sources of the transistors (using two pins per supply rail). Less substrate noise coupling is expected in the case where the bulks are separated, because power supply bounce does not have a direct path to the bulks of the transistors. This has been shown in [6] and also it is demonstrated by measurement results in Chapter 5.

3.2. Noise-sensing Amplifier

A noise sensing amplifier [5] was designed to measure substrate noise injected by digital circuits. The amplifier (referred to as *amp1*) has supply dependent biasing, and it is reliable and easy to bias since only an off-chip 500μA DC current source is required. This makes the setup for noise measurements easier. The amplifier is also designed to work with a low supply voltage of 1.8V. Figure



(a)



(b)

FIGURE 3.3. Power supply parasitics with bulk nodes of the transistors tied to the sources shown in (a) and separated as shown in (b).

3.4 shows the schematic of the noise sensing amplifier. Transistor sizes and resistor values are given in APPENDIX A.

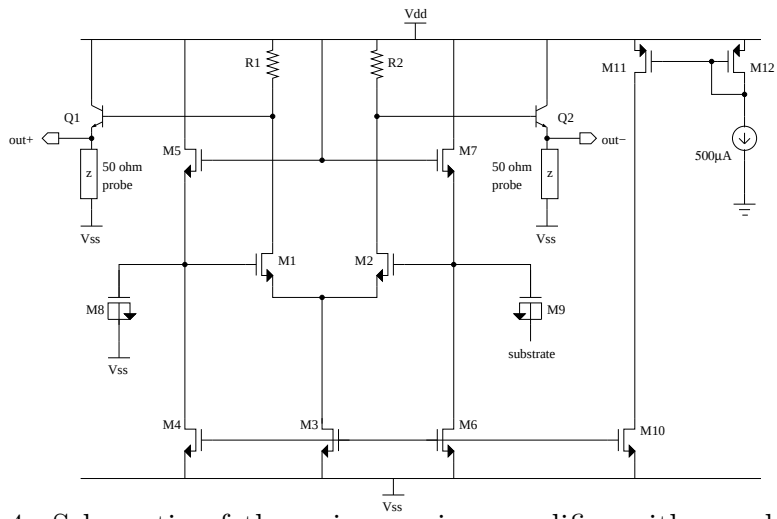


FIGURE 3.4. Schematic of the noise sensing amplifier with supply dependent biasing.

The sense amplifier is a wide-band amplifier with low gain. One input of the differential input pair (M1 and M2 in Figure 3.4) is connected to the substrate via a MOS capacitor, while the other input is connected to a quiet ground through another MOS capacitor. The MOS capacitors are large so that they act as short circuits in the frequency range of interest. The bipolar transistors (BJTs) Q1 and Q2 are the output buffers in the BiCMOS noise sensing amplifier. In the SOI process, CMOS source followers were used in place of the BJT emitter followers. The noise sensing amplifier was designed for a load of 50Ω because RF ground-signal-ground (GSG) probes were used to measure the output.

The substrate noise voltage v_{sub} at the bulks of $M_{1,2}$ and M_3 appear as common mode signals and assuming $r_{o1,2} >> R_{1,2}$, small signal analysis shows that the differential gain is approximately given by:

$$A_{DM} = g_{m_{1,2}} R_{1,2} \frac{g_{m_{Q1,2}}}{g_{m_{Q1,2}} + \frac{1}{50}}, \tag{3.1}$$

where $g_{m_{1,2}}$ is the transconductance of the input differential pair $M_{1,2}$, $g_{m_{Q1,2}}$ is the transconductance of the output buffer transistors which drive the 50Ω probes.

Before deriving the common mode gain, let us look at the output buffer stage. The small-signal gain of a source-follower [14] is given by:

$$gain_{sf} \approx \frac{g_m}{g_m + \frac{1}{R_{source}}}. \tag{3.2}$$

Similarly, the small-signal gain of an emitter-follower is given by:

$$gain_{ef} \approx \frac{g_m}{g_m + \frac{1}{R_{emitter}}}. \tag{3.3}$$

Both R_{source} and $R_{emitter}$ are equal to the 50Ω probe impedance. The transconductance gm of a BJT is much higher than that of a CMOS transistor for the same transistor size, thus a BJT emitter-follower stage has a higher gain than the equivalent CMOS source-follower stage. This means that less current is needed to achieve the same gain using a BJT compared to a CMOS transistor, hence reducing the overall power consumption. BJTs also use less chip area compared to CMOS transistors to drive the same amount of current. Since the output buffers draw about 15 mA each when driving the probes, BJTs were used at the output stage instead of CMOS transistors in the BiCMOS process. The BJT emitter-follower stage required to source 15mA has an area of $445\mu m^2$ while the equivalent CMOS source-follower stage required to source the same amount of current has an area of $600\mu m^2$. Thus, the use of BJTs provide a 35% savings in area.

The common mode gain can be derived by considering each of the v_{sub} signals present at the bulks of $M_{1,2}$ and M_3. The simplified approximate expression is given by:

$$A_{CM} = -(\frac{g_{mb_{1,2}} R_{1,2}}{2 g_{m1} r_{o3}} + \frac{g_{mb_3} R_{1,2}}{2}) \frac{g_{m_{Q1,2}}}{g_{m_{Q1,2}} + \frac{1}{50}}, \tag{3.4}$$

Figure 3.5 shows the differential gain and phase responses of *amp1*.

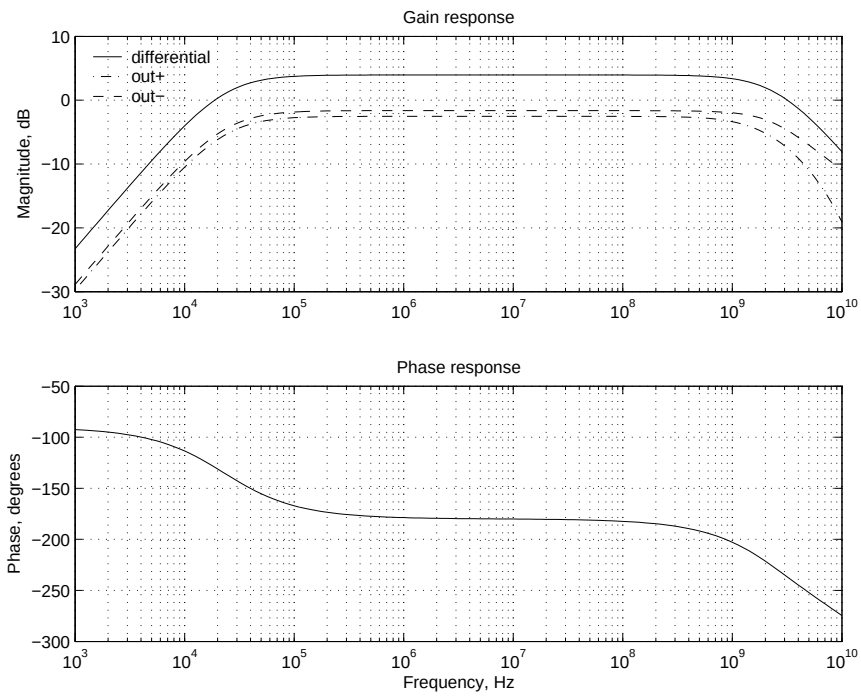


FIGURE 3.5. Differential gain and phase responses for *amp1*.

On the BiCMOS chip, there are versions of *amp1* with and without a deep trench moat around the amplifier. In this thesis, the moat refers to the deep trench moat, although the regular n- epi moat is also available in the BiCMOS process. A moat is used in a similar way to guard rings, by placing it around the analog circuit. The disadvantage of a guard ring is that it requires a low impedance path to ground to be effective in noise suppression [13]. If not, bounce on the guard ring can couple more noise to the analog circuit. A moat, on the other

hand, does not have this problem. It works by not allowing the noise to enter the analog circuit, and not by attempting to short the noise to ground. In the BiCMOS process, the deep trench moat consists of two deep trenches enclosing a blocked bipolar mask [18]. This is done by implanting the n-type subcollector into the p-type substrate, then growing approximately 2μm of undoped epitaxial silicon. During the initial epi growth, the n-type subcollector implant is exposed, making the epi layer very slightly n-type. The blocked bipolar mask blocks the p-well implant, creating a structure of high resistivity substrate, the grown epitaxial layer, and shallow trench isolation. This structure is then used to surround any analog circuitry to be shielded from noise. A top view and the cross-section of the moat are shown in Figures 3.6 and 3.7.

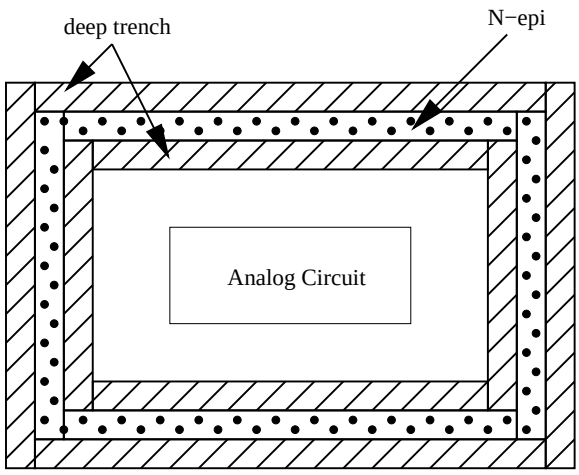


FIGURE 3.6. Top view of the deep trench moat surrounding an analog circuit.

Another noise suppression technique is the use of a die-perimeter ring (DPR), which is effective for heavily doped substrates [6, 10]. Here, the effectiveness of a die-perimeter ring in lightly doped substrates is evaluated.

In the layout for the noise sensing amplifier, matching between the input transistors and load resistors was maximized, thereby minimizing the input-

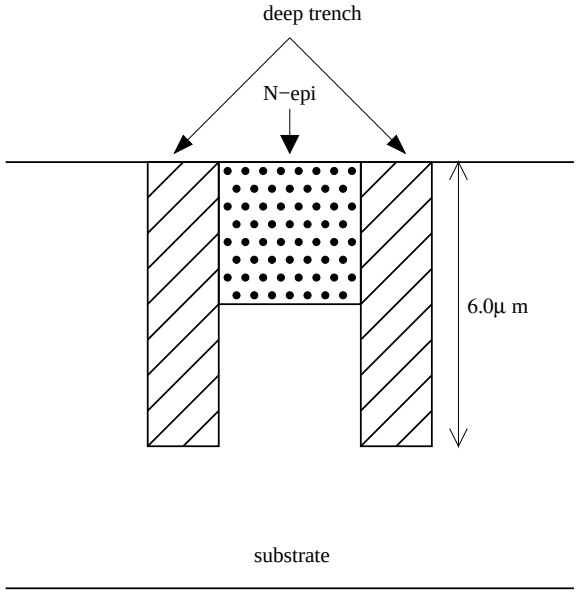


FIGURE 3.7. Cross-section of the deep trench moat.

referred offset voltage. This is accomplished by interdigitating the input transistor pair and using dummy resistors and transistors. The layouts for *amp1* with and without a moat in the BiCMOS process are shown in APPENDIX B and the layout for *amp1* in the SOI process is shown in APPENDIX C. For the BiCMOS process, each BJT output buffer was laid out as two BJTs in parallel. The BJT layout used is known as two-stripe, because they have two base, two emitter and two collector stripes, respectively, per transistor. This allows a larger amount of current to be carried by the output buffer when the 50Ω probes are connected.

4. CIRCUIT MODELING IN THE BICMOS PROCESS

Figure 4.1 shows the various parasitics taken into account in the modeling of noise coupling between the stepped buffer and the sense amplifier. This includes the substrate network, package and bondwire parasitics, routing resistances, PCB traces, decoupling capacitors, output probe and oscilloscope impedances and transmission lines.

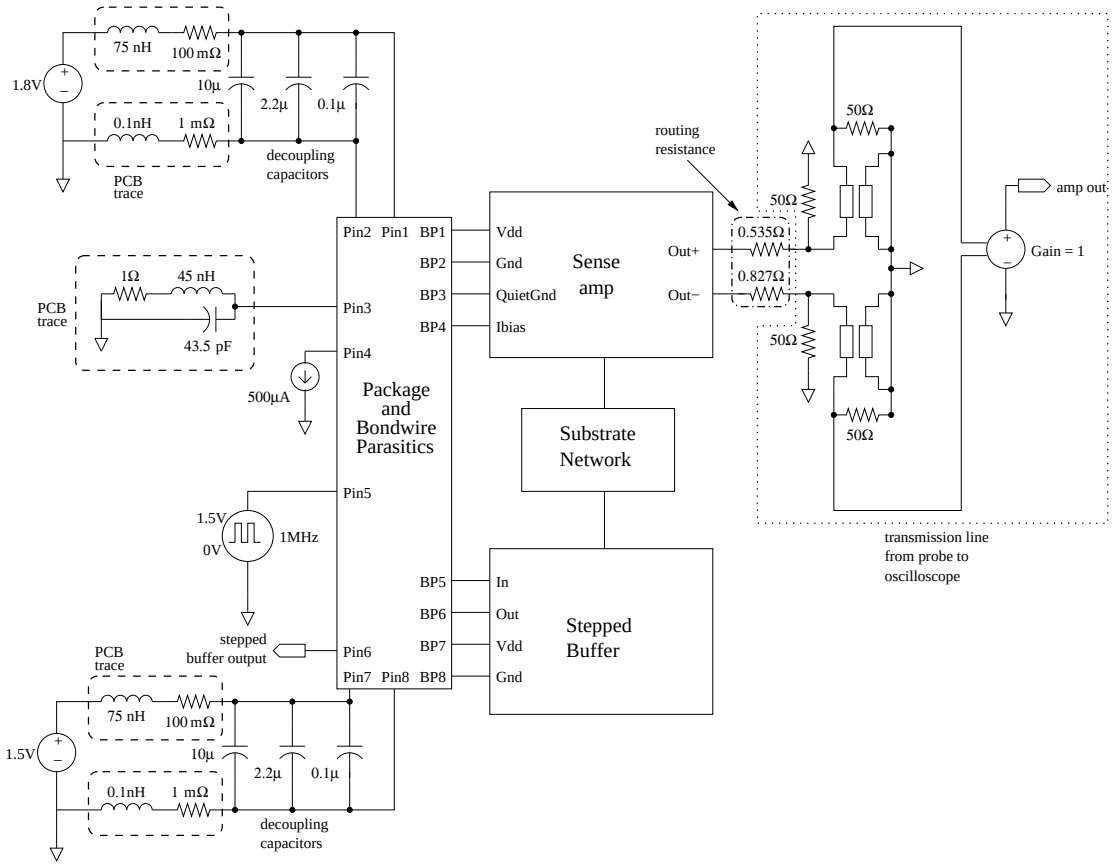


FIGURE 4.1. Overview of circuit modeling in the BiCMOS process.

4.1. Substrate Network

EPIC was used to extract the resistive substrate network. Each n-channel transistor was taken as one contact, and each substrate contact was taken as one contact. P-channel transistors were not taken into account since they are in n-wells. Since noise couples capacitively from the n-well to the bulk, and at low frequencies of operation, the capacitor is close to an open circuit, the noise coupling from p-channel transistors was ignored. Noise from the BJTs was also not included because there is a deep trench isolation around each BJT. The interconnects and bondpads were also entered as virtual contacts [12] in EPIC. Figure 4.2 shows a simplified substrate network example for two transistors, two interconnects and two bondpads. Cox is the capacitance from either an interconnect or bondpad to the substrate and Ce is the capacitance of the epoxy between the chip backplane and the die paddle. Since this is a high resistivity substrate, the substrate cannot be taken as a single node. Each self resistance R_{ii} is connected to the die paddle through a capacitance that is proportional to the size of the contact.

For the sense amplifier with a moat, the cross coupling resistances R_{ij} between the amplifier and stepped buffer were not used since the moat around the amplifier reduces the noise coupled through the p+ channel-stop region by creating a structure of high resistivity between the two circuits. The resistive network was obtained using EPIC in the same manner as that for the sense amplifier without a moat, then the cross coupling resistances R_{12} were assumed to be large enough to be ignored and were taken out. The resistive network for a simple two contact case (30μm x 30μm and 50μm x 50μm spaced 100μm away) was obtained in EPIC using the four layer lightly doped substrate profile with a buried layer (for the case

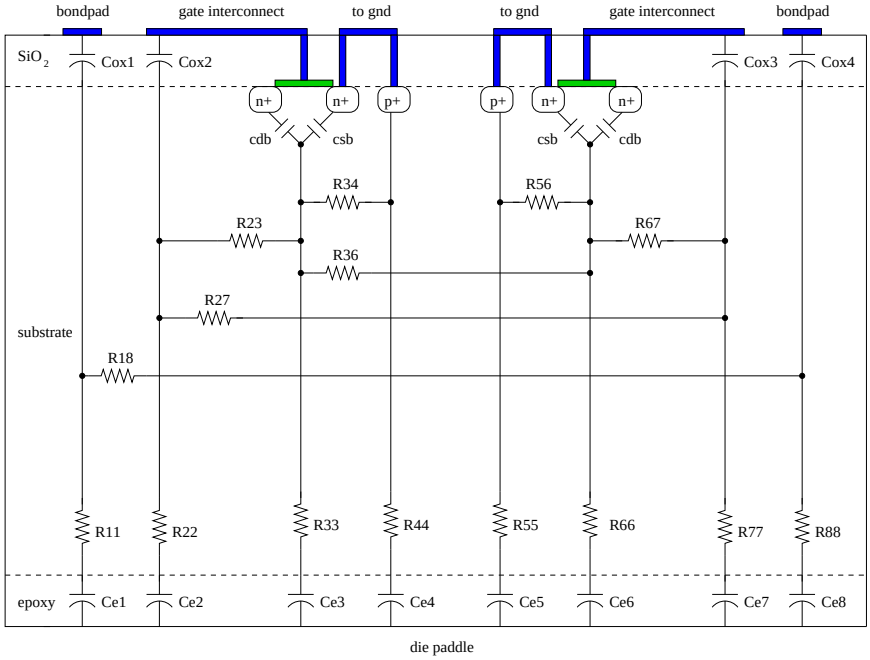


FIGURE 4.2. Substrate network example.

without a moat) and replacing the buried layer with a high resistivity substrate (for the case with a moat) to ensure that the R_{11} resistances obtained did not vary significantly. Figures 4.3(a) and 4.3(b) show the resistive networks obtained for the simple two contact case with and without the buried layer.

(a) (b)

FIGURE 4.3. Resistive substrate network for 30μm x 30μm sensor and 50μm x 50μm injector contacts separated by 100μm. (a) With buried layer. (b) Without buried layer.

4.2. Package and Bondwire Parasitics

Figure 4.4 shows the model for one pin, including the bondwire parasitics and routing resistances. The values of R1, L1, C1, R2, C2, L2 for each of the 132 pins in the PGA package used can be found in [19] and APPENDIX A.

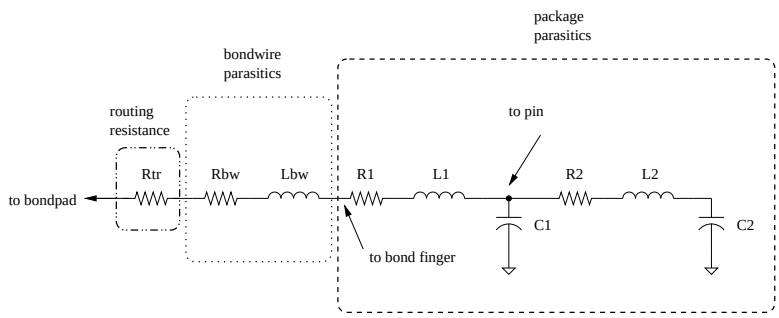


FIGURE 4.4. Package pin, bondwire, and routing resistance model.

The bondwire inductance was approximated using an inductance value of 1nH/mm. For the BiCMOS chip in the PGA132 package, the bondwire inductances ranged from 4.7nH - 5.4nH. Since the bondwires are 1 mil gold bondwires, the resistance can be calculated using the equation:

$$R_{bw} = \frac{\rho l}{A}, \tag{4.1}$$

where ρ is the resistivity of gold, l is the length of the bondwire and A is the cross-sectional area of the bondwire. For 1 mil gold bondwires, ρ is $22.1 m\Omega.\mu m$ and A is $506.7\mu m^2$, and with an average bondwire length of 5mm, the bondwire resistances averaged about 220 $m\Omega$.

For bondwires that are about the same length, the mutual inductance between them can be calculated using the equation [15]:

$$M_{ind} \approx \frac{\mu_0 l}{2\pi}[ln(\frac{2l}{D}) - 1 + \frac{D}{l}], \tag{4.2}$$

where μ_0 is the permeability of free space, l is the length of the bondwires, and D is the distance between bondwires. The coupling coefficient, K, could then be calculated using:

$$K = \frac{M_{ind}}{\sqrt{L_1 L_2}}, \tag{4.3}$$

The calculated coupling coefficients for bondwires ranged between 0.33 and 0.55. For example, for the power supply of *step1*, l is 5mm and D is 0.43mm, and M_{ind} is 2.11nH. With L_1 and L_2 equal to 4.8nH and 5.2nH, respectively, K is 0.42 for the power supply for *step1*.

4.3. PCB Traces

The inductances of the copper trace on the PCB board were calculated using the equation [16]:

$$L \approx \frac{\mu_0 l h}{w}, \tag{4.4}$$

where μ_0 is the permeability of free space, l is the length of trace, h is the distance between the trace and the ground plane, and w is the width of the trace. With a height h of 15 mils, average trace width of 15 mils and a length of 80mm, the inductance for the power trace for *step1* is about 75nH.

5. EXPERIMENTAL SETUP AND RESULTS FOR THE BICMOS PROCESS

5.1. Experimental Setup

A test chip was fabricated in the silicon germanium 0.18μm BiCMOS process. A die photo of the test chip is shown in Figure 5.1. The chip was packaged using the Kyocera 132-pin CPGA package with a 350 mil square cavity. A PCB test board was designed to provide power and biasing to the digital and analog circuitry. The schematic and layout of the test board is shown in APPENDIX D.

The stepped buffer was powered with a 1.5V supply. The sense amplifier was powered with a 1.8V supply and biased with an external 500μA DC current source. A function generator was used to generate a 1MHz input square wave with rise and fall times of 12ns and 16ns, respectively, switching between 0V and 1.5V to drive the stepped buffer, and the outputs of the sense amplifier were probed using 150μm pitch GSG RF probes. The probe station setup is shown in APPENDIX A.

The following measurements were performed:

1. *Step1* with *amp1* without a moat and with the DPR floating.
2. *Step1* with *amp1* with a moat and with the DPR floating.
3. *Step2* with *amp1* without a moat and with the DPR floating.
4. *Step2* with *amp1* with a moat and with the DPR floating.
5. *Step1* with *amp1* without a moat and with the DPR grounded.
6. *Step1* with *amp1* with a moat and with the DPR grounded.

7. *Step2* with *amp1* without a moat and with the DPR grounded.

8. *Step2* with *amp1* with a moat and with the DPR grounded.

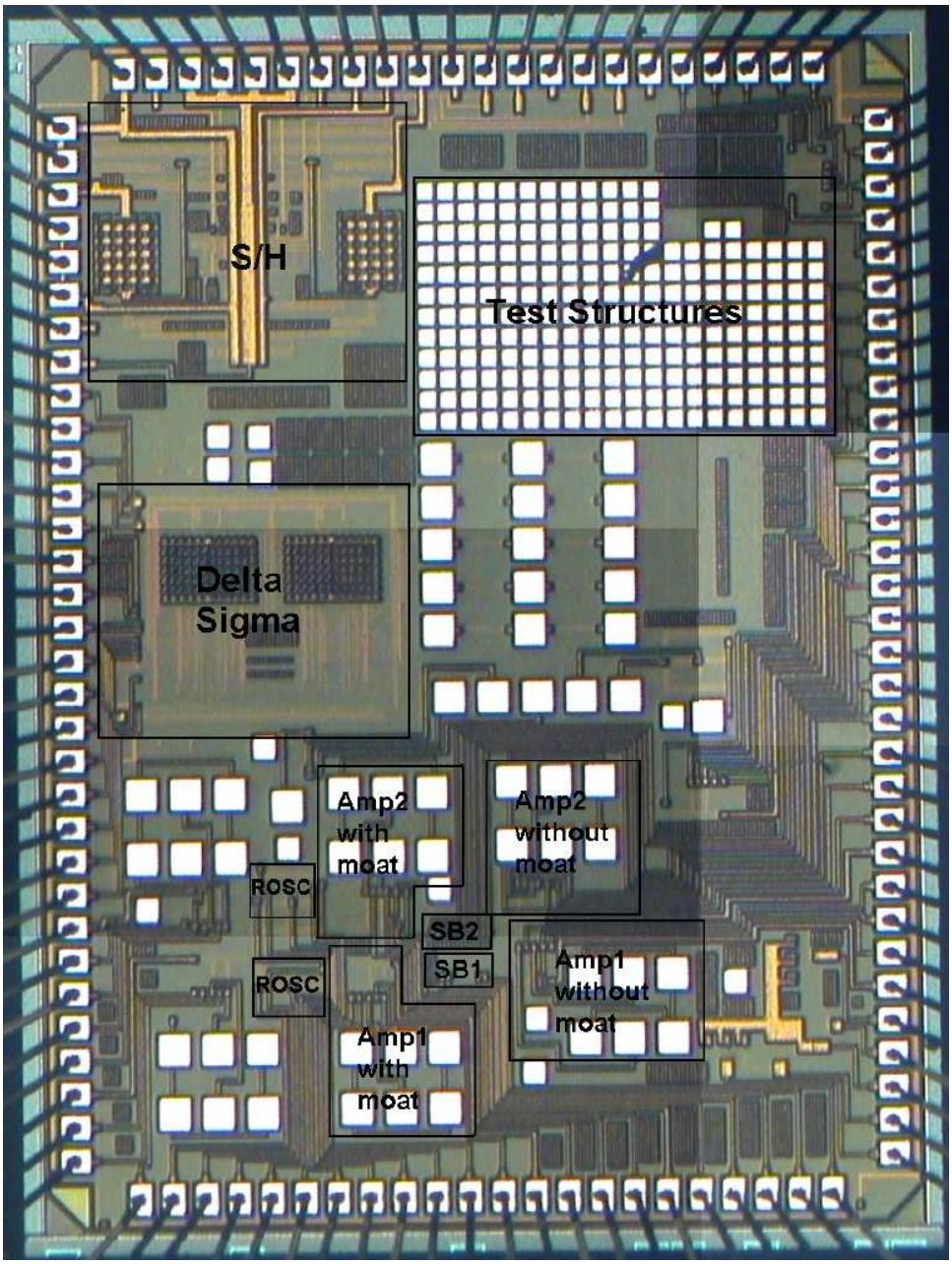


FIGURE 5.1. BiCMOS test chip die photo.

5.2. Experimental Results

Figures 5.2 and 5.3 show the measured and simulated transient differential output of *amp1* without and with a moat, respectively, when *step1* is driven with a 1MHz square wave and with the DPR floating. The peak to peak voltage of the initial spike is 113mV and 60mV without and with the moat, respectively. Thus, there is a 46.9% reduction in noise coupling with a moat. The amplifier with a moat is expected to have less noise coupled to it from the switching of the stepped buffer since the moat reduces the surface current conduction between the amplifier and the stepped buffer. However, the noise that is coupled through the backplane and package and bondwire parasitics is still present even with the moat. The initial spike and high frequency ringing is the noise coupled through the substrate. The low frequency ringing that can be seen on all the measurements is due to the long PCB trace for the quiet ground pin for the sense amplifier, as shown in Figure 5.4. The non-ideal quiet ground case includes the PCB trace while the ideal quiet ground case does not.

Measurement from a substrate tap further shows that the 83MHz low frequency ringing seen in the sense amplifier measurements is due to the sense amplifier, and not what is injected into the substrate from the stepped buffer. Figure 5.5 shows the measurement of substrate noise seen at an $80\mu m$ x $80\mu m$ substrate tap $60\mu m$ away when *step2* is driven with a 1MHz square wave and with the DPR floating.

Figures 5.6 and 5.7 show the measured and simulated transient differential output of *amp1* without and with a moat, respectively, when *step2* is driven with a 1MHz square wave and with the DPR floating. The peak to peak voltage (Vpp) of the initial spike is 50mV and 25mV without and with the moat, respectively.

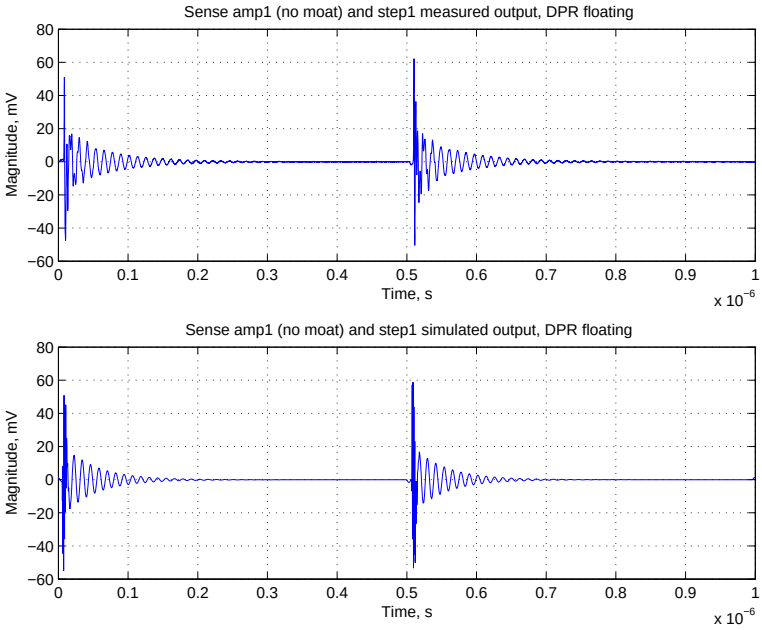


FIGURE 5.2. Measured (top) and simulated (bottom) transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR floating.

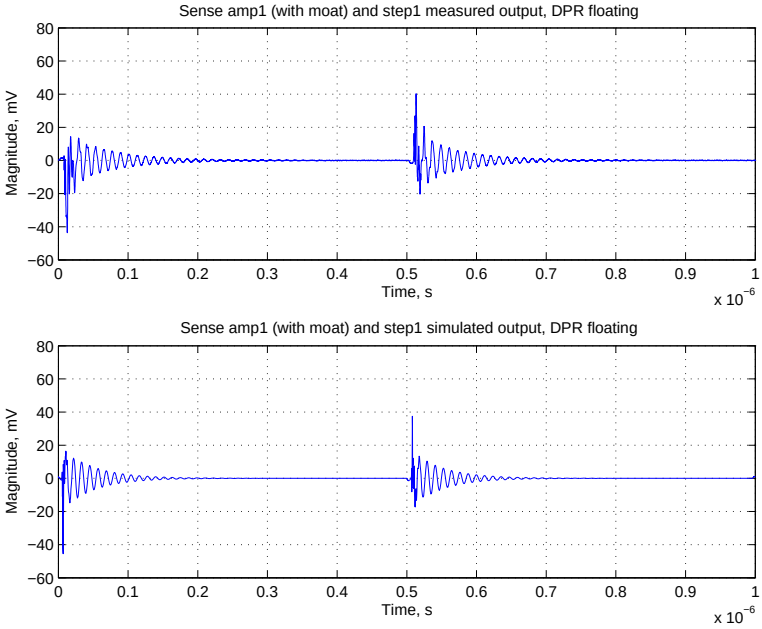


FIGURE 5.3. Measured (top) and simulated (bottom) transient output of *amp1* with a moat, with *step1* driven at 1MHz and with the DPR floating.

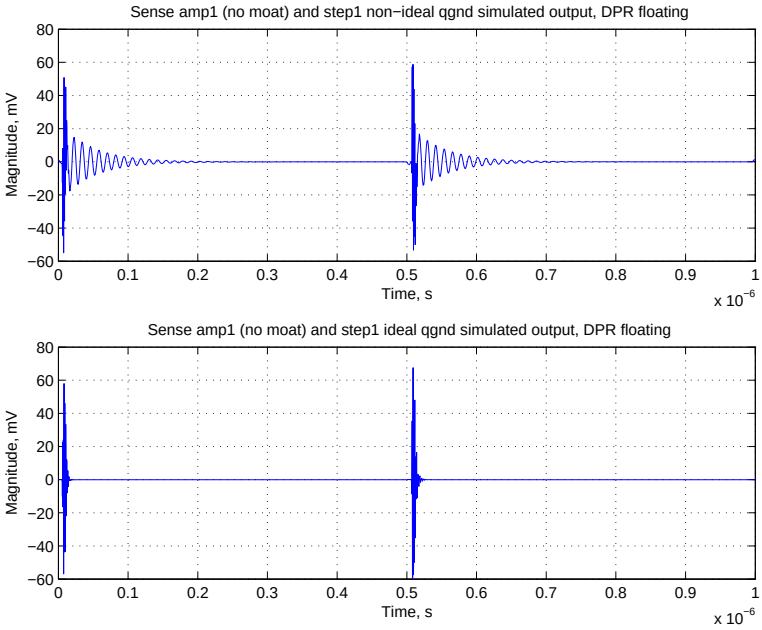


FIGURE 5.4. Simulated transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR floating, with a non-ideal (top) and ideal (bottom) quiet ground.

There is a 55.8% and 58.3% reduction in noise by separating the bulks of the transistors for the case without and with a moat, respectively. There is less noise coupling with *step2* (bulks separated) compared to *step1* (bulks tied together) because the power supply bounce does not have a direct path to the bulks of transistors when they are separated.

Figure 5.8 shows the measured transient differential output of *amp1* without a moat and with *step1* driven by a 1MHz square wave, with the DPR floating and grounded. The peak to peak voltage of the initial spike is 113mV and 107mV with the DPR floating and grounded, respectively. Grounding the DPR reduced the noise only a negligible amount. This is because the DPR did not have a low inductance path to ground. The DPR was routed to a single bondpad on the chip, and with the PGA132 package used, including bondwire parasitics, the DPR had

approximately 13nH inductance to ground. Figure 5.9 shows that if the DPR had a low inductance of 1.5nH to ground, grounding the DPR does reduce noise by 50%.

The measurement and simulation results for cases 5 - 8, where the DPR is grounded are shown in APPENDIX E. All the measurement and simulation results were within 10% agreement. Table 5.1 summarizes the results for the stepped buffer and sense amplifier measurements and simulations in the BiCMOS process. For each case, the top and bottom numbers are the peak-to-peak voltage (Vpp) of the initial spike on the rising and falling edges of the output of the stepped buffer, respectively.

The control case without a moat, with the bulks and sources tied together, and the DPR floating was also simulated with different rise and fall times for

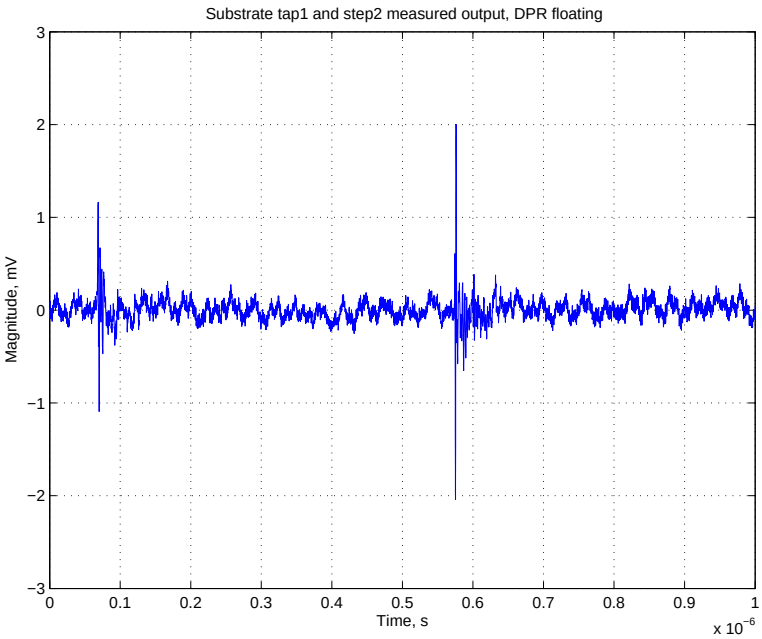


FIGURE 5.5. Measured transient output of an 80μm x 80μm substrate tap 60μm away, with *step2* driven at 1MHz and with the DPR floating.

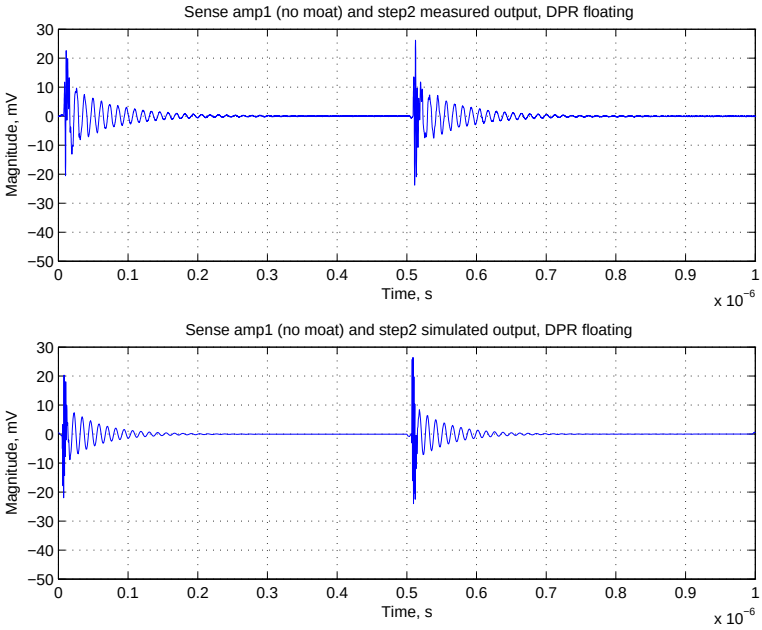


FIGURE 5.6. Measured (top) and simulated (bottom) transient output of *amp1* without a moat, with *step2* driven at 1MHz and with the DPR floating.

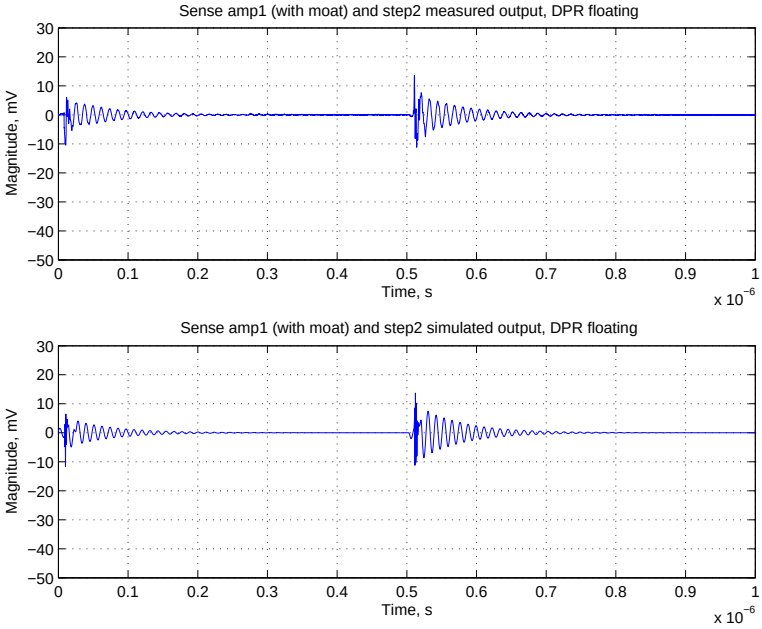


FIGURE 5.7. Measured (top) and simulated (bottom) transient output of *amp1* with a moat, with *step2* driven at 1MHz and with the DPR floating.

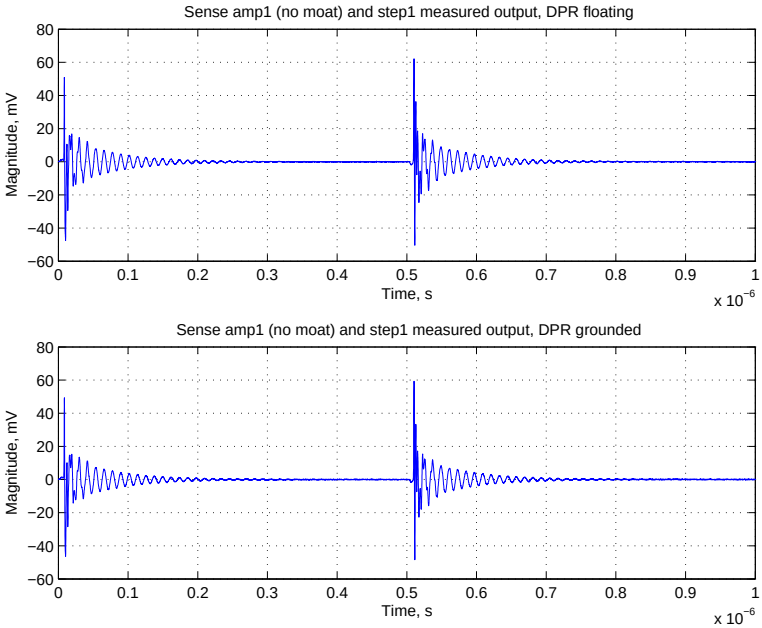


FIGURE 5.8. Measured transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR floating (top) and grounded (bottom).

the clock input to the stepped buffer. The clock frequency was kept constant at 1MHz, but simulations were done with rise and fall times of 12ns, 5ns, 1ns and 0.1ns, and the results are shown in Figures 5.10 and 5.11. The amount of noise seen in the initial spike increases as the rise and fall times are decreased, but the low frequency ringing amplitude decreases as the rise and fall times are decreased. The peak to peak voltages of the initial spikes are 106mV, 110mV, 117mV and 132mV for rise and fall times of 12ns, 5ns, 1ns and 0.1ns, respectively.

Figure 5.12 compares the effectiveness of the noise suppression techniques by means of a moat (M), separating the bulks and sources of transistors (S), and grounding a DPR (G) in the 0.18μm lightly doped BiCMOS process. All percentage improvements are relative to the control case with no moat around the sense amplifier, the bulks and sources of the stepped buffer tied together, and the DPR floating. Simulations were also done with a low inductance of 1.5nH

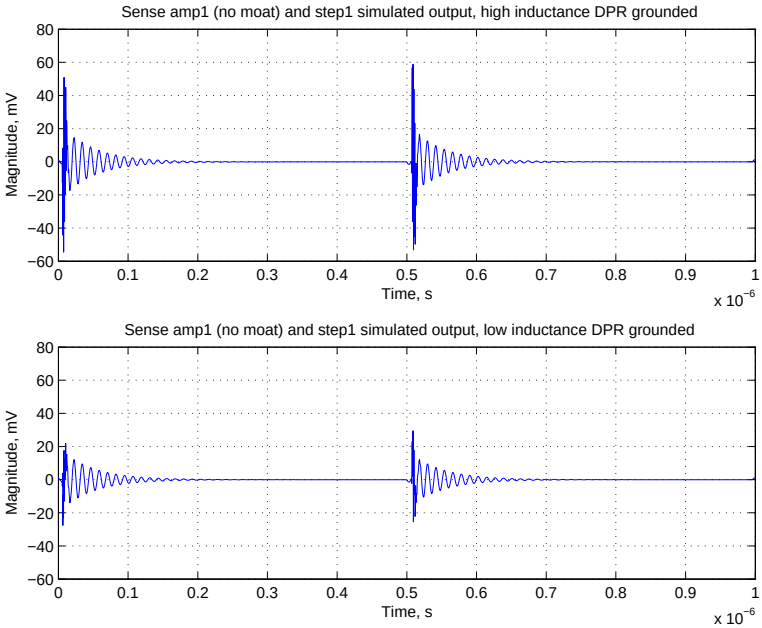


FIGURE 5.9. Simulated transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR grounded via a high inductance of 13nH (top) and low inductance of 1.5nH (bottom).

from the DPR to ground to show what the best noise performance could have been. This figure shows that using a moat and separating the bulks are effective methods for reducing noise. In Figure 5.12, grounding the DPR is not an effective noise suppression technique because of the high inductance (13nH) to ground in reality. If this inductance were much smaller (1.5nH), grounding the DPR could give a 50% reduction in noise.

			Measured Vpp (mV)	Simulated Vpp (mV)	Percent error %
DPR floating	*Step1* bulks together	no moat	99	106	7.1
		Case 1	113	113	0
		moat	59	61	3.4
		Case 2	60	55	-8.3
	Step2 bulks separate	no moat	43	42	-2.3
		Case 3	50	51	2
		moat	17	18	5.9
		Case 4	25	26	4
DPR grounded	*Step1* bulks together	no moat	96	105	9.4
		Case 5	107	112	4.7
		moat	59	60	1.7
		Case 6	59	54	-8.5
	Step2 bulks separate	no moat	41	43	4.9
		Case 7	50	51	2
		moat	17	18	5.9
		Case 8	25	25	0

TABLE 5.1. Summary of measurement and simulation results for the BiCMOS process.

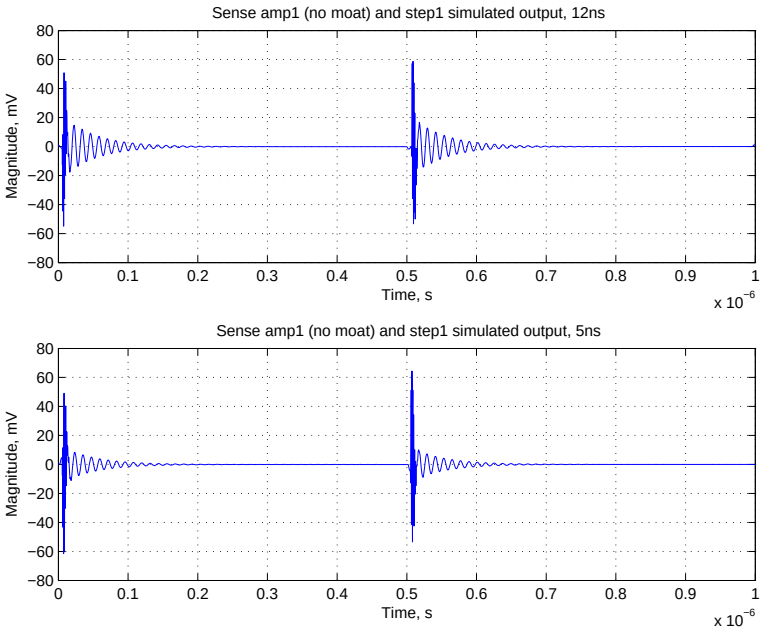


FIGURE 5.10. Simulated transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR floating, with rise and fall times of 12ns (top) and 5ns (bottom).

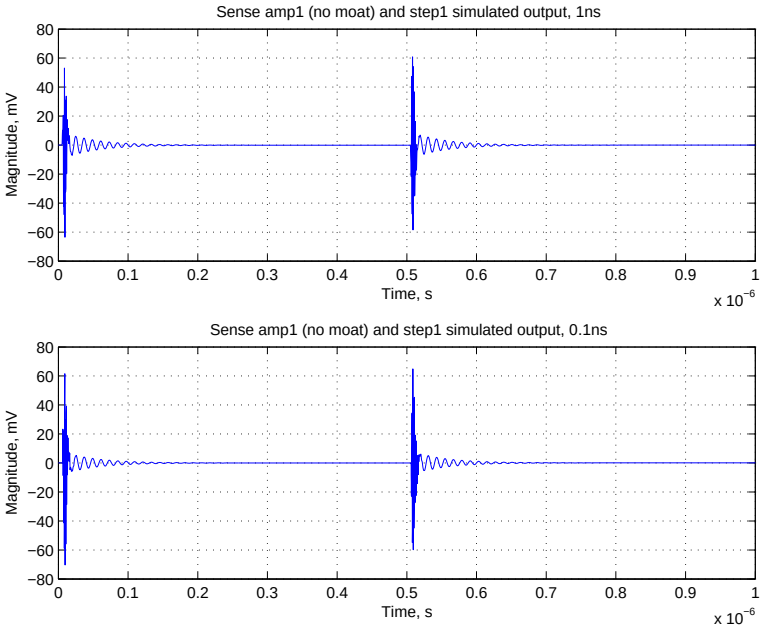


FIGURE 5.11. Simulated transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR floating, with rise and fall times of 1ns (top) and 0.1ns (bottom).

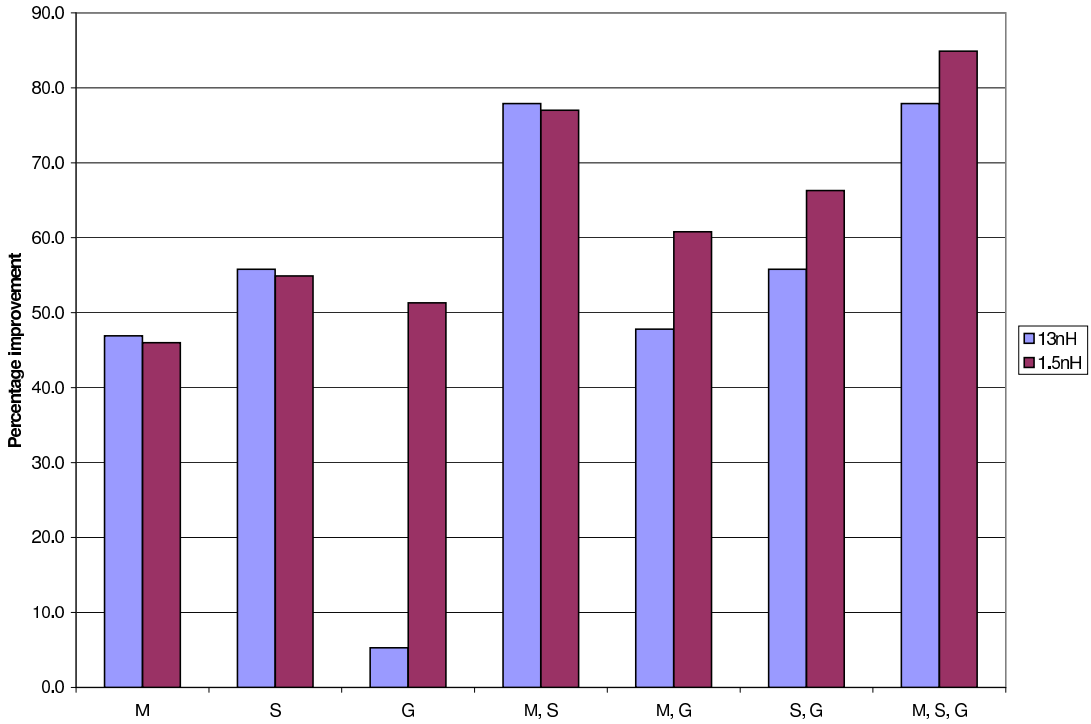


FIGURE 5.12. Comparison of noise suppression techniques in the 0.18μm lightly doped BiCMOS process for 7 cases with a ground trace inductance of 13nH (light shading) and 1.5nH (dark shading), where M is the case with a moat, S is the case with the bulks and sources separated, and G is the case with the DPR grounded.

6. MEASUREMENT AND SIMULATION OF NOISE COUPLING FOR SOI PROCESS

6.1. Experimental Setup

A die photo of the SOI test chip is shown in Figure 6.1. To compare noise coupling between similar circuits on the SOI and BiCMOS test chips, the die was packaged using the same 132-pin CPGA package that was used for the BiCMOS process. A similar PCB test board was also designed for testing and measuring noise coupling in the SOI test chip. The schematic and layout for the test board is shown in APPENDIX D.

Noise coupling measurements were not taken for the SOI test chip that was fabricated because the fabricated chips had poor yield. The measured I-V characteristic curves for several test transistors on four bare die and four packaged die show that not all the transistors were operating correctly (see APPENDIX E). A DC voltage sweep was also applied to the input of the stepped buffer, but nothing was observed, other than the fact that several milliamps (4-10mA) of current was drawn as soon as the stepped buffer was powered up. This indicates that several or all of the inverter stages are always on. The reason for this is that the tungsten shunt on the transistors did not make contact with the poly gate, leaving the gate floating [20]. Thus, the gate is capacitively coupled to the drain and source, so its voltage follows between the two, such that the inverter stages could be drawing current all the time. Tests done by MIT Lincoln Lab show that there was a tendency for such failures [20].

If these same circuits are fabricated again in the next run for this process, and the yield is better, the following can be done. Both the stepped buffer and sense amplifier need to be powered with 1.5V supplies. An external 500μA DC

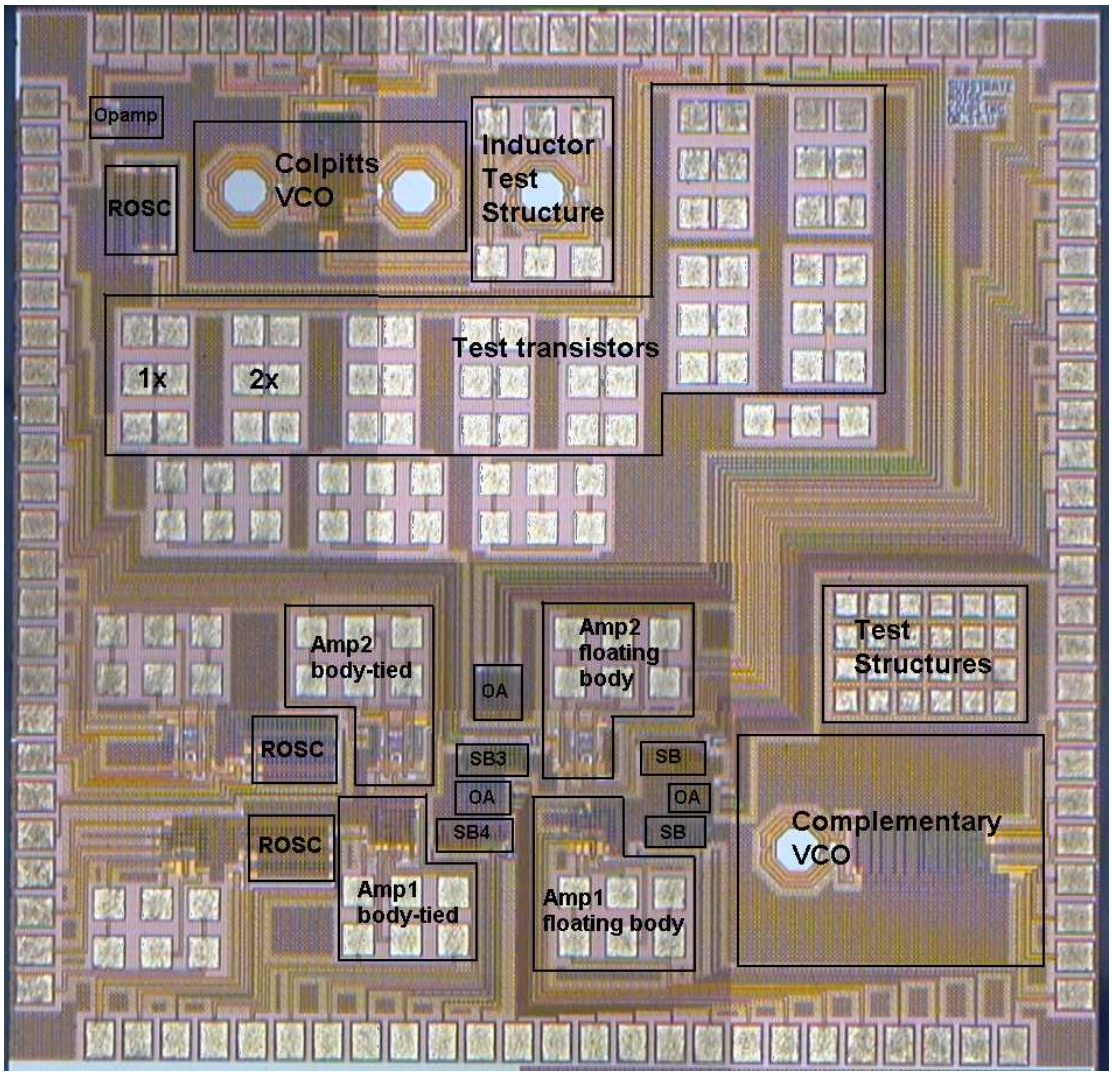


FIGURE 6.1. SOI test chip die photo.

current bias is provided on the PCB test board to bias the sense amplifier. For the input to the stepped buffer, a function generator is used to generate the 1MHz square wave input switching between 0V and 1.5V. Also different clock frequencies up to 5GHz must be applied, since noise is capacitively coupled in SOI, so more noise is expected at higher clock frequencies. The output of the sense amplifier can be probed using the 150μm pitch GSG RF probes.

The following measurement cases should be done:

1. *Step3* with *amp1* with body ties.

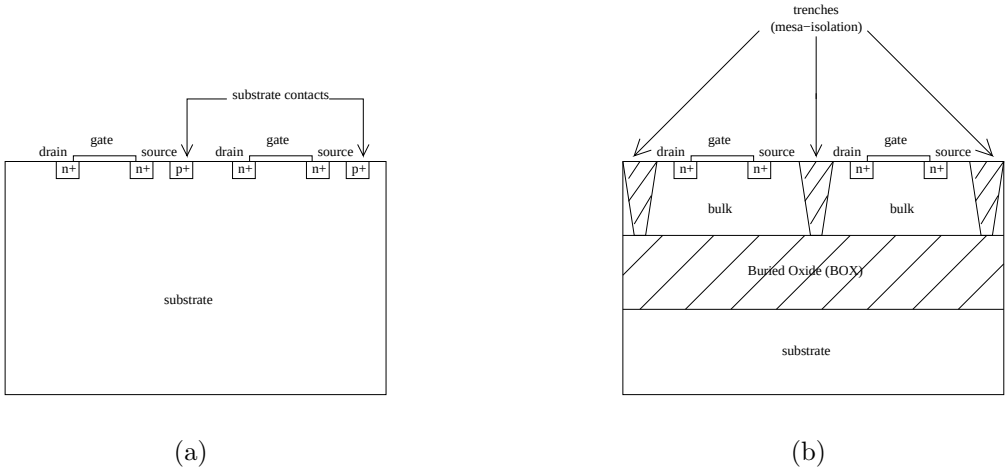
2. *Step4* with *amp1* with body ties.

Cases 1 and 2 can be compared to determine if using body ties or floating body transitors for the stepped buffer has an effect on noise coupling. The results from this process can also be compared to the control case in the BiCMOS process (no moat, bulks together, and DPR floating) to determine if there is more or less noise coupling in the SOI process as compared to a bulk CMOS process.

6.2. Simulation Setup

Since there is a BOX layer between the substrate and active transistors, and this is a mesa-isolated process (so each transistor is isolated from other transistors), substrate noise coupling is expected to be very small. Coupling from the supply and package parasitics, bondpads, interconnects, and PCB traces are likely to be the main sources of coupling. The modeling of external parasitics is similar to that for the BiCMOS process, as presented in Chapter 4. However, a substrate network model has to be developed for this SOI process.

As seen from Figure 2.4, the presence of the BOX layer introduces capacitances into the substrate network. In this process, the transistors are also mesa-isolated. In regular CMOS processes, the bulks of the transistors are connected through the common substrate, but this does not happen with the floating body transistors in the SOI process because of the BOX layer as shown in Figures 6.2(a) and 6.2(b). If body-tied transistors are used, then the bulk and source of each transistor are connected, and connecting the sources of different transistors using metal traces would connect the bulks of the transistors.



(a) (b)

FIGURE 6.2. Cross-section of transistors in CMOS and SOI processes. (a) CMOS process. (b) SOI process.

The substrate model for the SOI process has to be modified to use capacitances (Ctr12) in place of the cross-coupling resistances used in the lightly doped substrate in the case of floating body transistors. Capacitances for the BOX layer (Cbox) also have to be included. Figure 6.3 shows the substrate network for the SOI process with floating-body transistors. For body-tied transistors, the body-tie resistance has to be connected between the source and the body.

6.3. Circuit Example

A circuit example is used to look at what the substrate noise coupling will be in the SOI process. The seventh inverter stage of the stepped buffer is used as the injector, and a 30μm x 30μm sensor contact is placed 70μm away from the injector. A 1GΩ resistor to ground from the sensor contact models the use of an ideal high impedance probe for measurement of noise. The cross-coupling capacitances, BOX layer capacitances, and self-resistances were calculated and

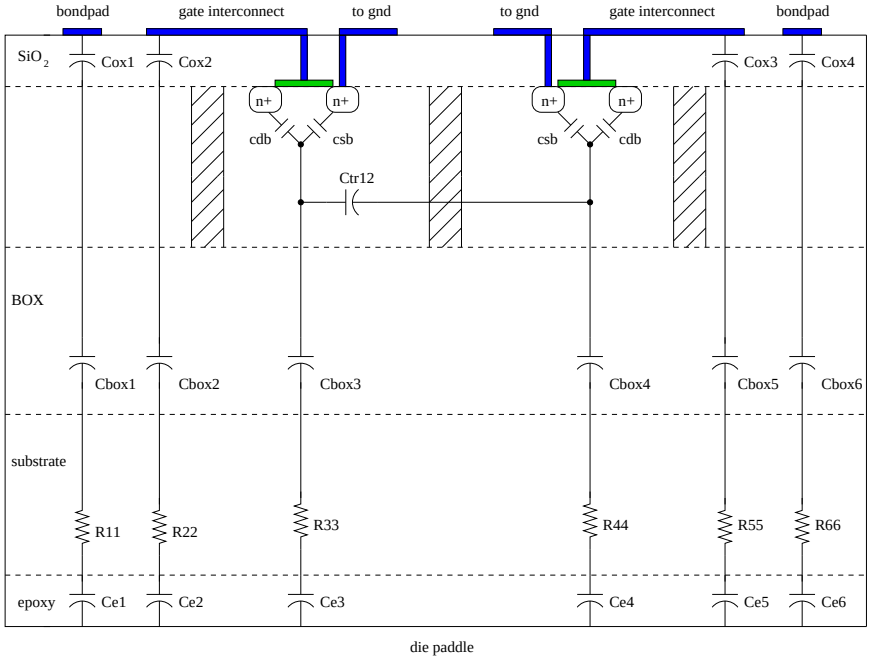


FIGURE 6.3. Generic SOI floating-body transistor substrate network example.

are shown in Figure 6.4 for the floating body transistor case. For the body-tied transistor case, the same substrate network is used, but the bulk connections were connected to the respective sources with the body-tie resistance as shown in Figure 6.5.

For comparison, this example was also simulated in the BiCMOS process, and the substrate network is shown in Figure 6.6. The noise picked up at the sensor (bulk terminal) with a clock frequency of 1MHz, with rise and fall times of 12ns and 16ns, respectively, in the BiCMOS, SOI floating body and body-tied cases is shown in Figure 6.7. These noise simulations with ideal power and ground connections were also performed for clock frequencies of 100MHz (with rise and fall times of 120ps and 160ps, respectively), 1GHz (with rise and fall times of 12ps and 16ps, respectively) and 5GHz (with rise and fall times of 3ps and 2.5ps, respectively), and the results are shown in Figure 6.8. Simulations were also

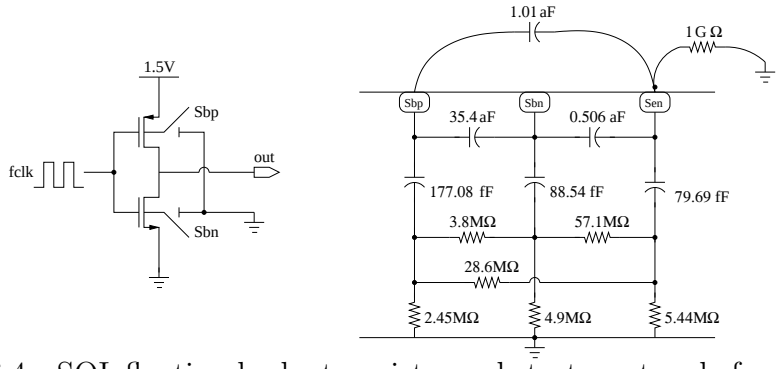


FIGURE 6.4. SOI floating-body transistor substrate network for the seventh stage of the stepped buffer and a 30μm x 30μm sensor contact placed 70μm away, where Sbp and Sbn are the bulk terminals of the p-channel and n-channel transistors, respectively, and Sen is the sensor contact.

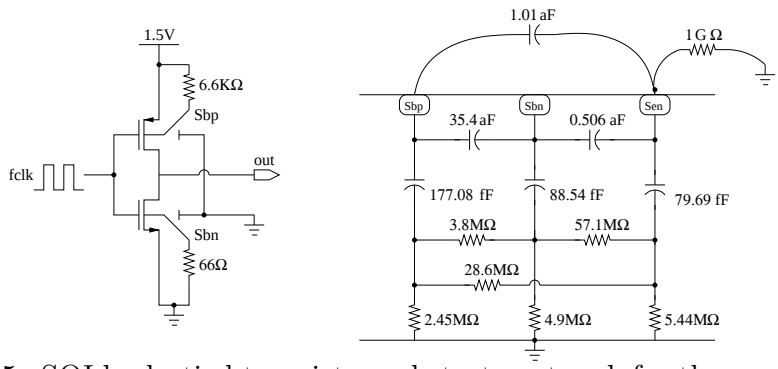


FIGURE 6.5. SOI body-tied transistor substrate network for the seventh stage of the stepped buffer and a 30μm x 30μm sensor contact placed 70μm away, where Sbp and Sbn are the bulk terminals of the p-channel and n-channel transistors, respectively, and Sen is the sensor contact.

performed using non-ideal power and ground connections. A 100$m\Omega$ resistance with an inductor in series were added to the power and ground connections for these simulations of the non-ideal behavior. A low inductance value of 1.5nH and a high inductance value of 15nH were used in simulations, and the results are shown in Figures 6.9 and 6.10.

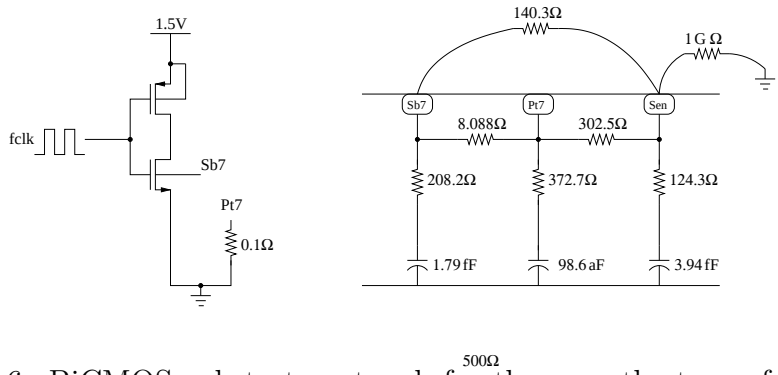


FIGURE 6.6. BiCMOS substrate network for the seventh stage of the stepped buffer and a 30μm x 30μm sensor contact placed 70μm away.

Figures 6.8 - 6.10 compare the amount of noise coupling in the BiCMOS, SOI floating body and body-tied cases at different clock frequencies. The SOI cases have much better noise performance than the BiCMOS case for clock frequencies up to 5GHz. This is expected since the SOI coupling network is capacitive, and the capacitor values are small enough such that the impedance is high for frequencies less than 5GHz. Thus, the noise performance for frequencies less than 5GHz is expected to be better than the BiCMOS case, which has a lower impedance resistive substrate network. As the clock frequency increases, more noise is seen in the BiCMOS and SOI cases. This is expected since the capacitors in the substrate networks have a lower impedance at higher frequencies, allowing more coupling of higher frequency noise. It should also be noted that there is no low frequency ringing as seen in the measurements in Chapter 5 because interconnects, package, bondwire and PCB parasitics have not been taken into account. With a high inductance of 15nH for the power and ground connections, the amount of noise coupling at higher frequencies of 1GHz and 5GHz are about the same in the BiCMOS, SOI floating body and body-tied cases. This is because supply coupling is the dominant factor here.

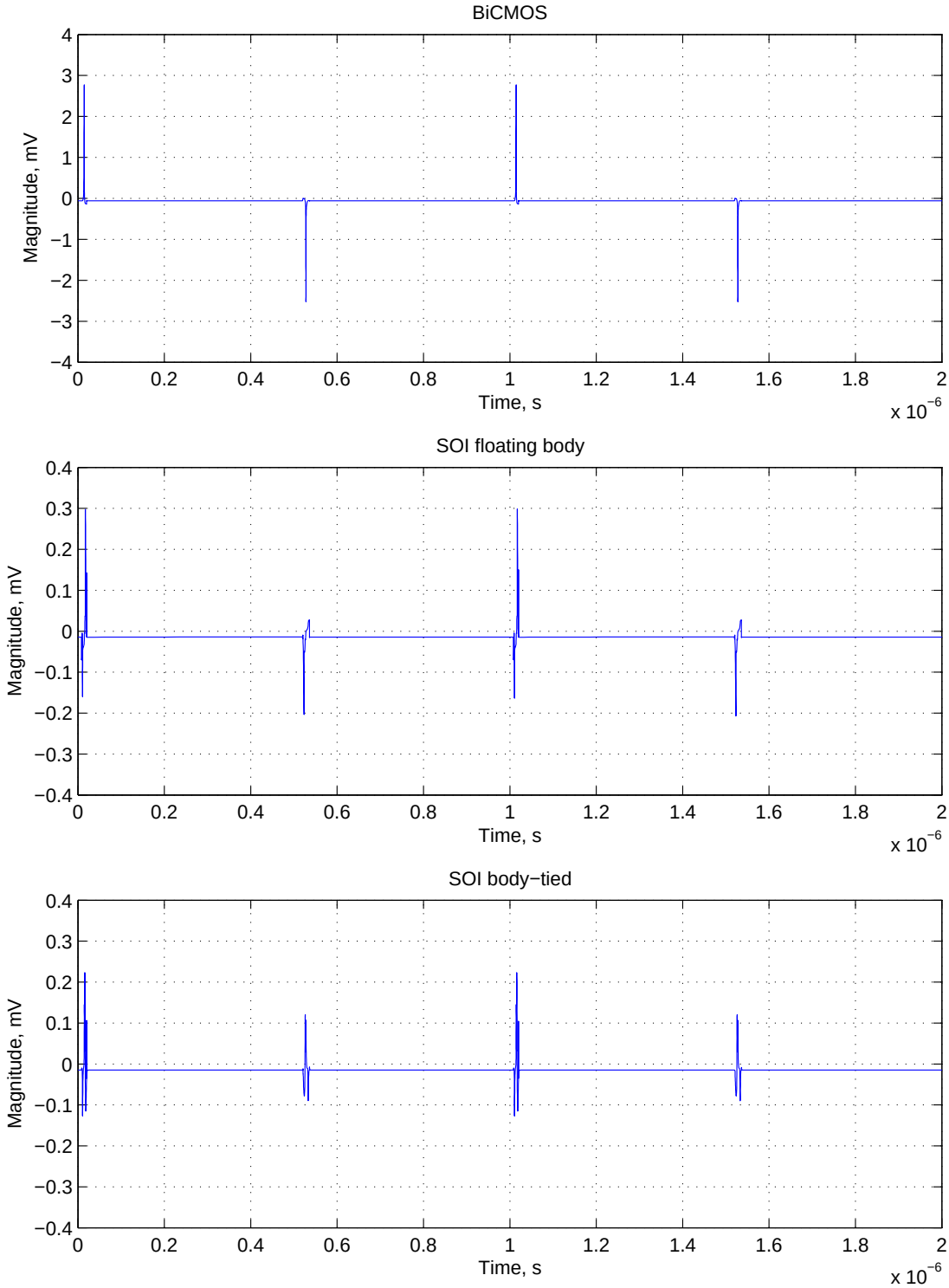


FIGURE 6.7. Noise picked up by a 30μm x 30μm sensor contact placed 70μm away from the seventh stage of the stepped buffer in the BiCMOS process (top), the SOI process with floating body transistors (middle) and with body-tied transistors (bottom) and a clock frequency of 1MHz.

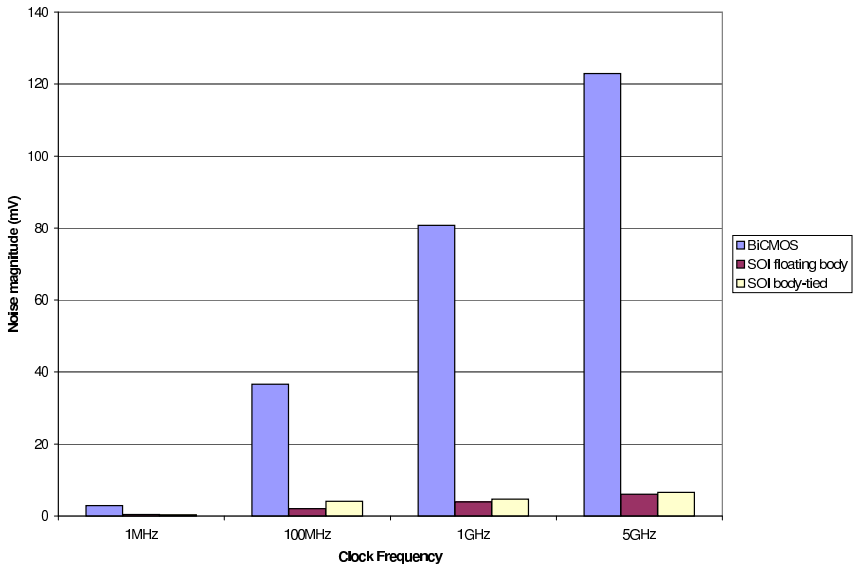


FIGURE 6.8. Comparison of noise coupling with ideal power and ground connections.

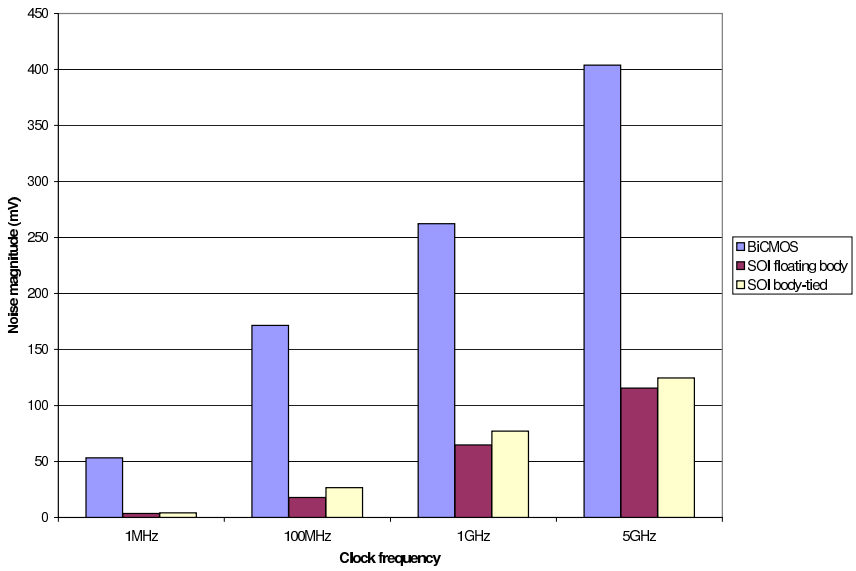


FIGURE 6.9. Comparison of noise coupling with a low inductance of 1.5nH for power and ground connections.

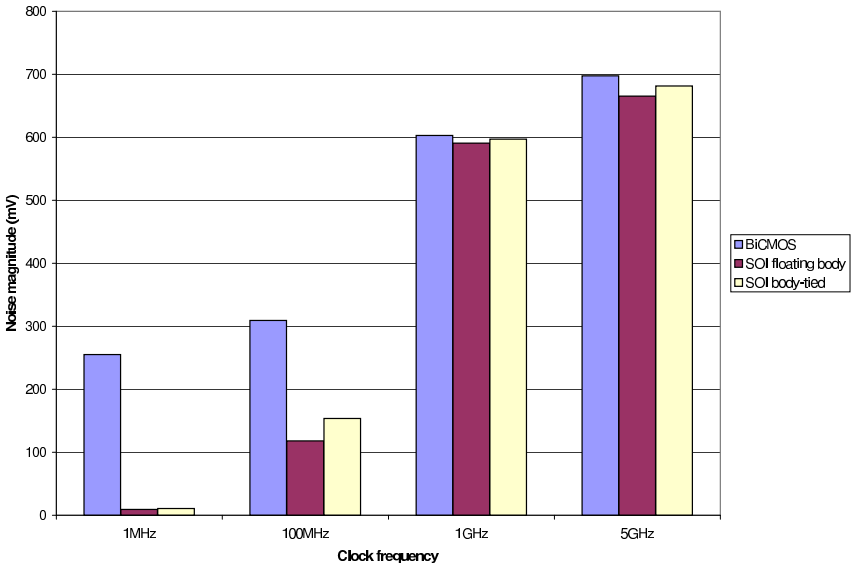


FIGURE 6.10. Comparison of noise coupling with a high inductance of 15nH for power and ground connections.

7. GENERALIZATION OF RESULTS

The circuits analyzed in Chapter 5 are hard to generalize because of the large number of transistors and all the parasitics present. The substrate network consists of over 200 contacts of different shapes and sizes when all the transistors, substrate taps, bondpads and interconnects are taken into account. Thus, this chapter considers a simplified case with a few contacts to generalize the results and compare it to the TSMC 0.25μm heavily and lightly doped processes. Large contact sizes are used to symbolize the large digital and analog blocks that can be found in mixed-signal SoCs. For comparison to the work done in [13], the injector and sensor contacts used are $1mm^2$ and $0.09mm^2$ respectively, and are spaced 200μm apart.

Figure 7.1 shows the substrate coupling model for the injector and sensor contacts in the BiCMOS process. Here, the resistance in the coupling path through the R_{12} resistor is slightly less than the resistance in the path through the two R_{11} resistors and epoxy capacitances. Since the epoxy capacitances are small in value, the impedance in the R_{11} path is much larger than the R_{12} path, unless the noise is high in frequency ($>$ 5GHz). Thus, the R_{12} resistor is the significant path for noise coupling. Comparing the resistance values for this same case in [13], it can be seen that this is a more lightly doped process than the TSMC 0.25μm lightly doped process because the R_{11} resistances are larger and the R_{12} resistance is smaller in the BiCMOS process. The overall results for both lightly doped processes are similar in that the coupling path through the R_{12} resistor is significant. This differs from the TSMC 0.25μm heavily doped process, where the dominant coupling path is through the R_{11} resistors.

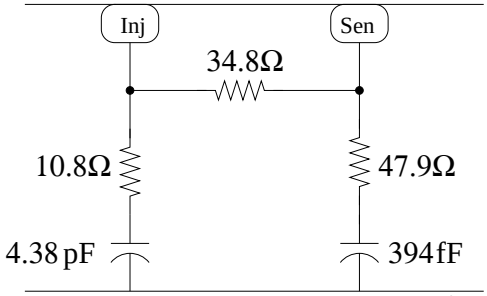


FIGURE 7.1. BiCMOS substrate network for a $1mm^2$ contact and a $0.09mm^2$ contact spaced at 200μm.

The same two contact substrate network with a 20μm wide DPR grounded is shown in Figure 7.2. The DPR is placed along the edge of a chip size of 3mm x 4mm, as it is in the case of the actual BiCMOS test chip. The injector and sensor contacts are spaced 200μm apart in the lower right corner of the chip area and are each 360μm away from the DPR. Grounding the DPR provides a lower impedance to ground through the R_{12} resistor from the injector. However, the R_{12} resistor from the injector to sensor has a value almost equal to the R_{12} resistor from the injector to the DPR, so only about half the noise is shunted to ground via the DPR, but the other half of the noise still couples from the injector to the sensor through the R_{12} path. The R_{12} resistance from the DPR to the sensor is the largest of the three, but is only about twice as large. Hence, if there is a high inductance to ground from the DPR, the DPR would be ineffective in reducing noise. This agrees with the results presented in Chapter 5.

Another possible noise suppression technique that can be used is a guard ring. This noise suppression technique is discussed for comparison to the TSMC 0.25μm heavily and lightly doped processes. Figure 7.3 shows the case with the same injector and sensor contacts spaced 200μm apart, with a 10μm wide guard ring (10μm from the sensor) around the sensor contact. It can be seen that the

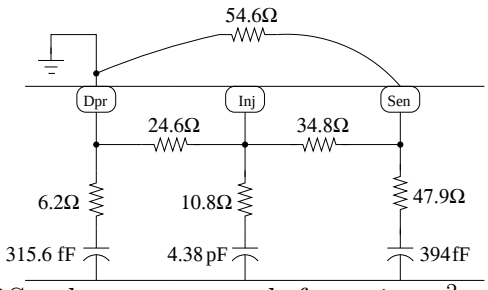


FIGURE 7.2. BiCMOS substrate network for a $1mm^2$ contact and a $0.09mm^2$ contact spaced at 200μm with a 20μm DPR grounded.

R_{12} resistor between the guard ring and the sensor is very small, and this provides a low impedance path for noise coupling. The guard ring is grounded, and most of the noise is shunted away if the guard ring has a low inductance to ground. If the inductance is too large, more noise would be injected into the sensor than in the case of no guard ring at all.

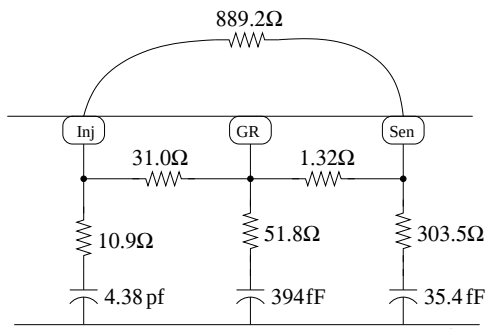


FIGURE 7.3. BiCMOS substrate network for a $1mm^2$ contact and a $0.09mm^2$ contact with a 10μm wide guard ring around the $0.09mm^2$ contact.

When guard rings are added around both contacts, the R_{12} resistances between each contact and the guard ring around it is very small, providing a low impedance path to ground to shunt noise. As seen in Figure 7.4, the R_{12} resistances between the injector and its guard ring, and the sensor and its guard ring are very small compared to the other resistances, so most of the noise is shunted through the guard rings if a low impedance path to ground is provided.

As in the single guard ring case, if there is a high impedance path to ground, more noise can be injected from the guard rings to the sensor contact. Figure 7.5 shows the substrate network for the case when the guard rings around both contacts are moved closer together so that the guard rings are spaced at 50μm. As the contacts and guard rings are moved closer together, the R_{12} resistance between the guard rings is decreased and noise coupling performance is less effective than when the guard rings are spaced further apart because coupling can take place between the guard rings, especially if a low impedance path to ground is not provided for the guard rings.

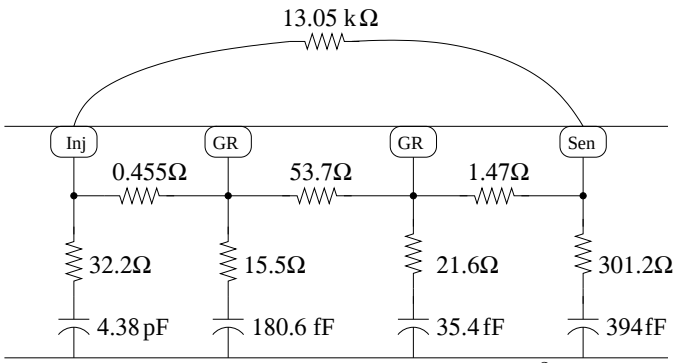


FIGURE 7.4. BiCMOS substrate network for a $1mm^2$ contact and a $0.09mm^2$ contact with 10μm wide guard rings spaced at 200μm around both contacts (spaced at 240μm).

The generalized results presented in this chapter are consistent with that of Chapter 5 and [13]. The amount of substrate noise coupling depends on the size and spacing of contacts in lightly doped processes. This differs from heavily doped processes where the R_{11} path is the dominant path for substrate noise coupling [10, 13]. Guard rings can provide improvement in noise coupling in lightly doped processes, keeping in mind that care must be taken to minimize the inductance in the guard ring connection to ground. Spacing the guard rings further apart also makes this method more effective in reducing noise coupling. Grounding

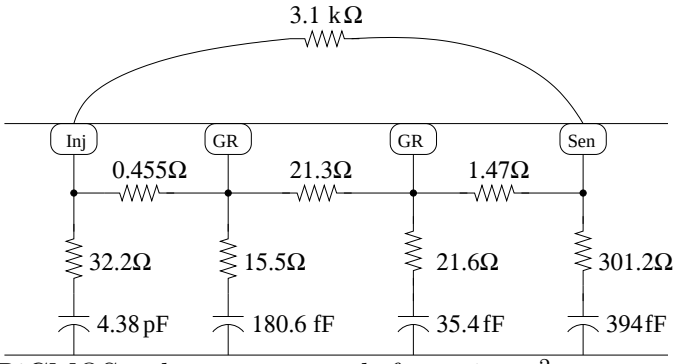


FIGURE 7.5. BiCMOS substrate network for a $1mm^2$ contact and a $0.09mm^2$ contact with 10μm wide guard rings spaced at 50μm around both contacts (spaced at 90μm.

the DPR was found to be an effective method in reducing noise coupling in the TSMC lightly and heavily doped substrates [10, 13], and also for the BiCMOS lightly doped process in this thesis, if the DPR has a low inductance to ground.

Table 7.1 summarizes the generalized results discussed in this chapter for the 0.18μm BiCMOS lightly doped process.

As seen in [12, 13], less noise coupling was seen in the TSMC 0.25μm lightly doped process compared to the TSMC 0.25μm heavily doped process. Less noise coupling is expected in the 0.18μm SiGe (BiCMOS) process over the TSMC 0.25μm heavily doped process since the BiCMOS process is also a lightly doped process. However, more noise coupling is expected in the BiCMOS process over the TSMC 0.25μm lightly doped process. This is because the R_{12} resistor path becomes more dominant in the BiCMOS process, which is a more lightly doped process. The substrate networks for all three processes are shown in Figure 7.6 for the case shown at the beginning of this chapter, with injector and sensor contacts that are $1mm^2$ and $0.09mm^2$, respectively, and spaced 200μm apart. From these networks, it can be seen that the impedance between the injector and sensor

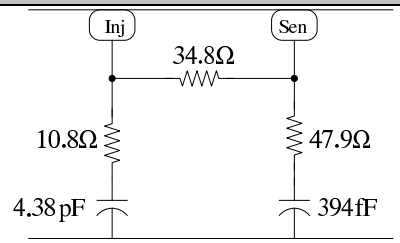
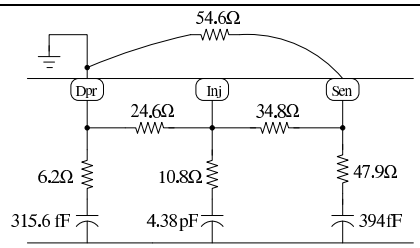
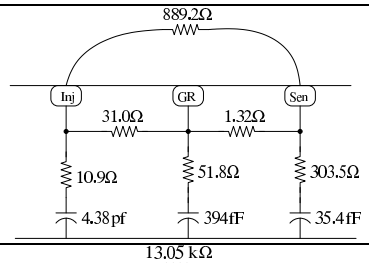
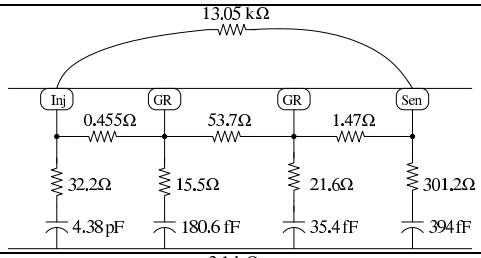
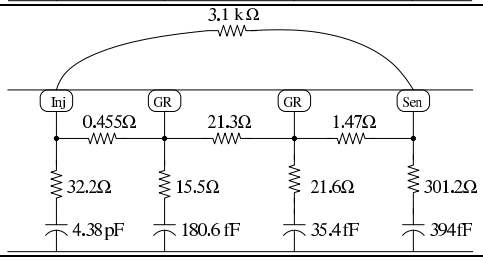
Design Technique **Performance**	Equivalent Circuit	Dominant Coupling Path Design Recommendation
No DPR or guard ring **Worst Performance**		Noise coupling occurs mainly through the R_{12} resistor. Increase distance between contacts to increase R_{12}.
DPR grounded **Good performance**		Some noise is shunted to ground through the DPR. Reduce DPR impedance to ground to minimize ground bounce.
Single guard ring around sensor contact **Good performance**		Coupling occurs mainly through the guard ring. Reduce guard ring impedance to ground to minimize ground bounce.
Dual guard rings with large spacing **Good performance**		Coupling occurs mainly through the guard rings. Reduce guard ring impedances to ground to minimize ground bounce.
Dual guard rings with small spacing **Medium performance**		Coupling occurs through and between the guard rings. Increase spacing between guard rings.

TABLE 7.1. Summary of generalized results for the BiCMOS lightly doped process.

contacts is the lowest in the TSMC heavily doped process, average in the BiCMOS process, and highest in the TSMC lightly doped process, for frequencies less than 5GHz. Thus, the noise performance in the BiCMOS process is average, compared to the TSMC heavily and lightly doped processes. However, if a deep trench moat is used in the BiCMOS process, the impedance between the injector and sensor node greatly increases. The cross-coupling resistance R_{12} is effectively an open circuit and the main path for noise coupling is through the R_{11} resistors and epoxy capacitances. This is a larger impedance than the 267Ω resistance in parallel with the higher impedance through the R_{11} resistors and epoxy capacitances in the 0.25μm lightly doped TSMC case. Thus, if a deep trench moat is used for in the BiCMOS process, the noise performance would be better than both the TSMC 0.25μm heavily and lightly doped processes.

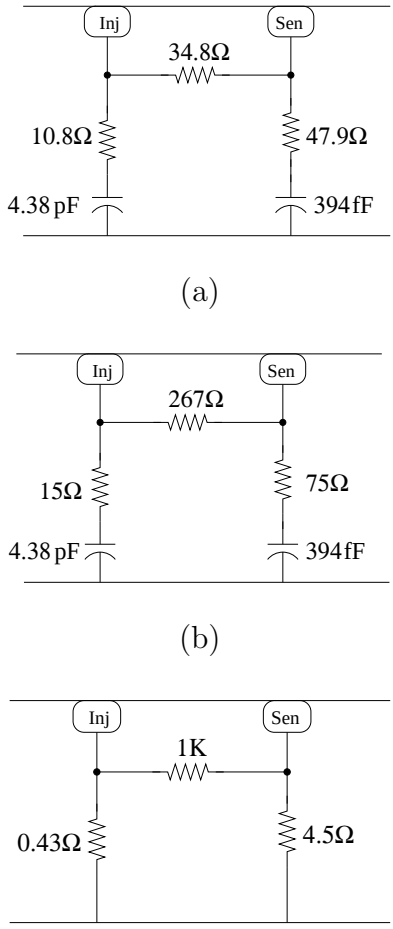


FIGURE 7.6. Substrate network for a $1mm^2$ injector contact and a $0.09mm^2$ sensor contact spaced 200μm apart in the (a) 0.18μm SiGe (BiCMOS) (b) TSMC 0.25μm lightly doped and (c) TSMC 0.25μm heavily doped processes.

8. CONCLUSION AND FUTURE WORK

8.1. Conclusions

Methods for simulating noise in the context of noise coupling between digital and analog blocks have been discussed in this thesis. Proper inclusion of interconnects, packaging, bondwires and PCB traces is essential for accurate results.

Measurements from a test chip fabricated in the IBM 0.18μm silicon germanium BiCMOS process validate the simulations performed in Cadence/Spectre using Silencer!, and verified that the simulation approach is accurate to within 10%. Measurements and simulations show that the use of a moat and the separation of the bulk from the source of a transistor reduces noise by 6dB each. Using both noise suppression techniques together results in a 12dB improvement in noise. The careful design of PCB test boards also helps to minimize the effects of external parasitics on noise coupling, as seen in the case of the DPR. Grounding the DPR has no effect if there is a large inductance to ground, but with a low inductance, a 6dB improvement is seen. Additional simulations also show that guard rings could be used as another noise suppression technique if carefully designed. Comparisons were also done across processes, and the noise performance in the BiCMOS process is expected to be better than the TSMC 0.25μm heavily doped process, but worse than the TSMC 0.25μm lightly doped process. However, the use of a deep trench moat in the BiCMOS process would give better noise performance over the TSMC 0.25μm lightly doped process as well. Simulations also show that the SOI process is expected to have the least amount of noise coupling since the noise coupling in the SOI process is at least an order of magnitude smaller compared to the BiCMOS process.

The experimental setup and simulation techniques for the MIT Lincoln Lab 0.18μm FDSOI process are also presented in this thesis. The case with floating body transistors is expected to have better noise performance than the case with body-tied transistors. Care has to be taken to minimize the impedance to ground in the case with body-tied transistors.

8.2. Future work

Future work in this area include taking measurements from a new test chip fabricated in the MIT Lincoln Lab 0.18μm FDSOI process to validate simulations. The model for extracting the substrate network for the SOI process can also be improved. Noise coupling comparisons can be done between the BiCMOS and SOI processes.

More work can also be done on the Silencer! tool that was used for extracting the resistive network to include external parasitics such as packaging and bondwires. The modeling of interconnects and bondpads could also be improved to include the oxide capacitances. For lightly doped substrates, where the substrate is not considered as a single node, automation to account for that and the capacitance of the epoxy can be done. A model for a SOI process can also be implemented in Silencer!.

The effects of packaging on noise coupling can also be explored. A chip on board (COB) type of packaging and other types of low pin inductance packaging such as flip-chip packaging can be compared.

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APPENDICES

APPENDIX A. BiCMOS Test Setup

Table A-1 shows the transistor sizing for the stepped buffer and Table A-2 shows the resistor and transistor sizing for the sense amplifier.

	BiCMOS		SOI floating body		SOI body-tied	
	p-channel	n-channel	p-channel	n-channel	p-channel	n-channel
Stage 1 (input)	$\frac{3\mu}{0.18\mu}$	$\frac{1.5\mu}{0.18\mu}$	$\frac{3\mu}{0.2\mu}$	$\frac{1.5\mu}{0.2\mu}$	$\frac{2.5\mu}{0.2\mu}$	$\frac{1\mu}{0.2\mu}$
Stage 2 (3x)	$\frac{8.16\mu}{0.18\mu}$	$\frac{4.08\mu}{0.18\mu}$	$\frac{8.175\mu}{0.2\mu}$	$\frac{4.05\mu}{0.2\mu}$	$\frac{6.675\mu}{0.2\mu}$	$\frac{2.55\mu}{0.2\mu}$
Stage 2 load (3x)	$\frac{8.16\mu}{0.18\mu}$	$\frac{4.08\mu}{0.18\mu}$	$\frac{8.175\mu}{0.2\mu}$	$\frac{4.05\mu}{0.2\mu}$	$\frac{6.675\mu}{0.2\mu}$	$\frac{2.55\mu}{0.2\mu}$
Stage 3 (8x)	$\frac{21.76\mu}{0.18\mu}$	$\frac{10.88\mu}{0.18\mu}$	$\frac{21.8\mu}{0.2\mu}$	$\frac{10.8\mu}{0.2\mu}$	$\frac{21.8\mu}{0.2\mu}$	$\frac{6.8\mu}{0.2\mu}$
Stage 3 load (8x)	$\frac{21.76\mu}{0.18\mu}$	$\frac{10.88\mu}{0.18\mu}$	$\frac{21.8\mu}{0.2\mu}$	$\frac{10.8\mu}{0.2\mu}$	$\frac{21.8\mu}{0.2\mu}$	$\frac{6.8\mu}{0.2\mu}$
Stage 4 (22x)	$\frac{58.96\mu}{0.18\mu}$	$\frac{29.48\mu}{0.18\mu}$	$\frac{58.85\mu}{0.2\mu}$	$\frac{29.7\mu}{0.2\mu}$	$\frac{47.85\mu}{0.2\mu}$	$\frac{18.7\mu}{0.2\mu}$
Stage 4 load (22x)	$\frac{58.96\mu}{0.18\mu}$	$\frac{29.48\mu}{0.18\mu}$	$\frac{58.85\mu}{0.2\mu}$	$\frac{29.7\mu}{0.2\mu}$	$\frac{47.85\mu}{0.2\mu}$	$\frac{18.7\mu}{0.2\mu}$
Stage 5 (59x)	$\frac{159.3\mu}{0.18\mu}$	$\frac{80.24\mu}{0.18\mu}$	$\frac{159.3\mu}{0.2\mu}$	$\frac{79.65\mu}{0.2\mu}$	$\frac{129.8\mu}{0.2\mu}$	$\frac{50.15\mu}{0.2\mu}$
Stage 5 load (20x)	$\frac{159.6.3\mu}{0.18\mu}$	$\frac{79.6\mu}{0.18\mu}$	$\frac{159.5\mu}{0.2\mu}$	$\frac{79.5\mu}{0.2\mu}$	$\frac{149.5\mu}{0.2\mu}$	$\frac{69.5\mu}{0.2\mu}$
Stage 6 (54x)	$\frac{430.92\mu}{0.18\mu}$	$\frac{214.92\mu}{0.18\mu}$	$\frac{430.65\mu}{0.2\mu}$	$\frac{214.65\mu}{0.2\mu}$	$\frac{403.65\mu}{0.2\mu}$	$\frac{187.65\mu}{0.2\mu}$
Stage 6 load (54x)	$\frac{430.92\mu}{0.18\mu}$	$\frac{214.92\mu}{0.18\mu}$	$\frac{430.65\mu}{0.2\mu}$	$\frac{214.65\mu}{0.2\mu}$	$\frac{403.65\mu}{0.2\mu}$	$\frac{187.65\mu}{0.2\mu}$
Stage 7 (output)	$\frac{1162.2\mu}{0.18\mu}$	$\frac{581.1\mu}{0.18\mu}$	$\frac{1161.875\mu}{0.2\mu}$	$\frac{581.75\mu}{0.2\mu}$	$\frac{1096.875\mu}{0.2\mu}$	$\frac{516.75\mu}{0.2\mu}$
Stage 7 load (65x)	$\frac{1162.2\mu}{0.18\mu}$	$\frac{581.1\mu}{0.18\mu}$	$\frac{1161.875\mu}{0.2\mu}$	$\frac{581.75\mu}{0.2\mu}$	$\frac{1096.875\mu}{0.2\mu}$	$\frac{516.75\mu}{0.2\mu}$

TABLE A-1. Transistor sizing for stepped buffer.

	BiCMOS	SOI body-tied
M1 and M2	$\frac{40\mu}{0.18\mu}$ (4x)	$\frac{72\mu}{0.2\mu}$ (8x)
M8 and M9	$\frac{1260\mu}{1\mu}$ (84x)	$\frac{1176\mu}{1\mu}$ (84x)
Q1 and Q2	$\frac{15\mu}{0.18\mu}$	$\frac{180\mu}{0.5\mu}$ (20x)
M4, M5, M6 and M7	$\frac{1\mu}{60\mu}$	$\frac{0.5\mu}{60\mu}$
M3	$\frac{80\mu}{0.18\mu}$ (8x)	$\frac{90\mu}{0.2\mu}$ (9x)
M10	$\frac{150\mu}{0.18\mu}$ (15x)	$\frac{90\mu}{0.2\mu}$ (9x)
M11	$\frac{300\mu}{0.18\mu}$ (30x)	$\frac{270\mu}{0.2\mu}$ (30x)
M12	$\frac{50\mu}{0.18\mu}$ (5x)	$\frac{45\mu}{0.2\mu}$ (5x)
R1 and R2	200Ω	200Ω

TABLE A-2. Transistor and resistor sizing for sense amplifier.

Experimental Test Setup

For the BiCMOS experimental test setup, power was supplied to just the stepped buffer and sense amplifier that were being used, and a function generator supplied the 1MHz square wave from 0V to 1.5V to the input of the stepped buffer. The output of the stepped buffer could also be viewed on the oscilloscope. The positive and negative outputs of the sense amplifiers were probed using 150μm pitch RF GSG probes (ACP40-A) from Cascade Microtech [17], which was then connected via an SMA connector to a Tektronix digital oscilloscope. Taking the difference of the two outputs using the math function on the oscilloscope produced the measured output plots shown in Chapter 5. Figure A-1 shows the experimental test setup.

The test setup for the stepped buffer and sense amplifier in the SOI process can be done in a similar fashion as that of the BiCMOS chip.

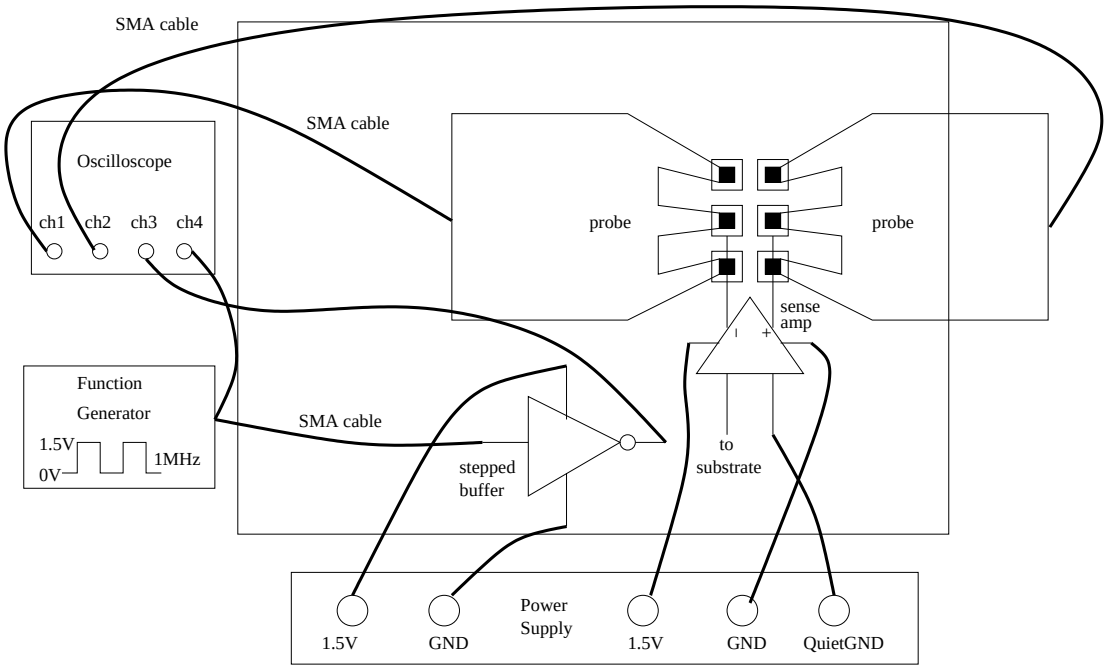


FIGURE A-1. BiCMOS experimental test setup.

Simulation Test Setup

Silencer! was setup for the BiCMOS process according to the steps in [11]. The injector (stepped buffer) and sensor (sense amplifier) regions were selected and Silencer! located the active regions or ports for the substrate network, which is used to create an EPIC input file. The layout was modified so that interconnects, bondpads and probe pads were included as ports in Silencer!. Silencer! then calls EPIC, and the resistive substrate network is calculated and automatically included in the Cadence schematic. Interconnects were also added and included in the schematic using Silencer! as well. Routing resistances, bondwire parasitics, package parasitics, PCB traces and decoupling capacitors were added by hand into the schematic. Simulations were run with the complete schematic and the substrate network and parasitics included. Figure A-2 shows the setup. A sample of part of the resistive substrate network netlist is also shown below.

Partial resistive substrate network for *step1* and *amp1* without a moat in the BiCMOS process:

```
R-86b     sb7 bckPln87 7457.97
R-86-169 sb7 ab11c     28805.9
R-86-170 sb7 ab11e     50417.7
R-86-171 sb7 ab11a     13145.6
R-86-173 sb7 ab11d     117846
R-86-174 sb7 ab11f     331752
R-86-177 sb7 ab18-19   517929
R-86-184 sb7 ab16e     212238
R-86-175 sb7 ab16a     225782
R-86-177 sb7 ab16d     182566
```

R-169b	ab11c	bckPln170	53440.5
R-169-177	ab11c	ab18-19	134915
R-169-185	ab11c	ab16a	5.78852e6
R-169-186	ab11c	ab16b	90323.7
R-169-187	ab11c	ab16d	4.59463e6
R-169-188	ab11c	ab16f	201952
R-170b	ab11e	bckPln171	57828.3
R-170-177	ab11e	ab18-19	897281
R-170-184	ab11e	ab16e	377192
R-170-186	ab11e	ab16b	104609
R-171b	ab11a	bckPln172	10738.6
R-171-177	ab11a	ab18-19	1.19893e6
R-171-183	ab11a	ab16c	156903
R-171-184	ab11a	ab16e	115690
R-171-185	ab11a	ab16a	238232
R-171-186	ab11a	ab16b	141355
R-171-187	ab11a	ab16d	464757
R-172b	ab11b	bckPln173	10967.1
R-172-177	ab11b	ab18-19	3135.56
R-172-183	ab11b	ab16c	63867.8
R-172-185	ab11b	ab16a	5581.76
R-172-186	ab11b	ab16b	31302.7
R-172-187	ab11b	ab16d	99198.4
R-173b	ab11d	bckPln174	58449.9
R-173-177	ab11d	ab18-19	123568

R-173-183	ab11d	ab16c	95484.8
R-173-184	ab11d	ab16e	229217
R-173-185	ab11d	ab16a	55254.8
R-173-186	ab11d	ab16b	154425
R-173-188	ab11d	ab16f	374110
R-174b	ab11f	bckPln175	71926.3
R-174-177	ab11f	ab18-19	56495.9
R-174-183	ab11f	ab16c	426178
R-174-185	ab11f	ab16a	1.30027e6
R-174-188	ab11f	ab16f	98211.7
R-177b	ab18-19	bckPln178	54205.6
R-177-183	ab18-19	ab16c	19725.6
R-177-185	ab18-19	ab16a	5239.21
R-177-186	ab18-19	ab16b	26710.4
R-177-188	ab18-19	ab16f	122621
R-183b	ab16c	bckPln184	71343.7
R-184b	ab16e	bckPln185	83173.7
R-185b	ab16a	bckPln186	17419.5
R-186b	ab16b	bckPln187	26275.2
R-187b	ab16d	bckPln188	86887.1
R-188b	ab16f	bckPln189	79503

PGA132 Package Model

Figure A-3 and Table A-3 show how the PGA132 package parasitics were modeled [19] in simulations.

Bond Finger	R_1 (Ω)	L_1 (nH)	C_1 (pF)	R_2 (Ω)	L_2 (nH)	C_2 (pF)
11,22,44,55,77,88,110,121	0.125	4.10	1.82	0.291	4.65	3.10
8,28,41,61,74,94,107,127	0.128	4.28	2.07	0.291	4.65	3.10
16,17,49,50,82,83,115,116	0.145	4.73	2.15	0.291	4.65	3.10
4,31,37,64,70,97,103,130	0.140	4.65	2.20	0.291	4.65	3.10
1,34,67,100	0.147	4.80	2.10	0.291	4.65	3.10
15,18,48,51,81,84,114,117	0.186	5.89	2.46	0.0433	0.69.	0.194
13,20,46,53,79,86,112,119	0.211	6.21	2.55	0.189	3.02	0.846
12,21,45,54,78,87,111,120	0.288	6.64	2.38	0.189	3.02	0.846
14,19,47,52,80,85,113,118	0.296	6.81	2.54	0.189	3.02	0.846
9,25,42,58,75,91,108,124	0.219	6.48	2.63	0.0433	0.69.	0.194
3,30,36,63,69,96,102,129	0.209	6.74	2.95	0.189	3.02	0.846
6,27,39,60,72,93,105,126	0.269	7.11	2.82	0.189	3.02	0.846
10,23,43,56,76,89,109,122	0.397	7.29	2.75	0.0433	0.69.	0.194
33,66,99,132	0.318	7.42	2.67	0.189	3.02	0.846
7,24,40,57,73,90,106,123	0.187	7.12	3.61	0.0433	0.69.	0.194
5,26,38,59,71,92,104,125	0.403	9.33	3.54	0.0433	0.69.	0.194
2,29,35,62,68,95,101,128	0.311	9.61	3.73	0.0433	0.69.	0.194
32,65,98,131	0.310	9.41	4.08	0.0433	0.69.	0.194

TABLE A-3. PGA132 package pin parasitic values.

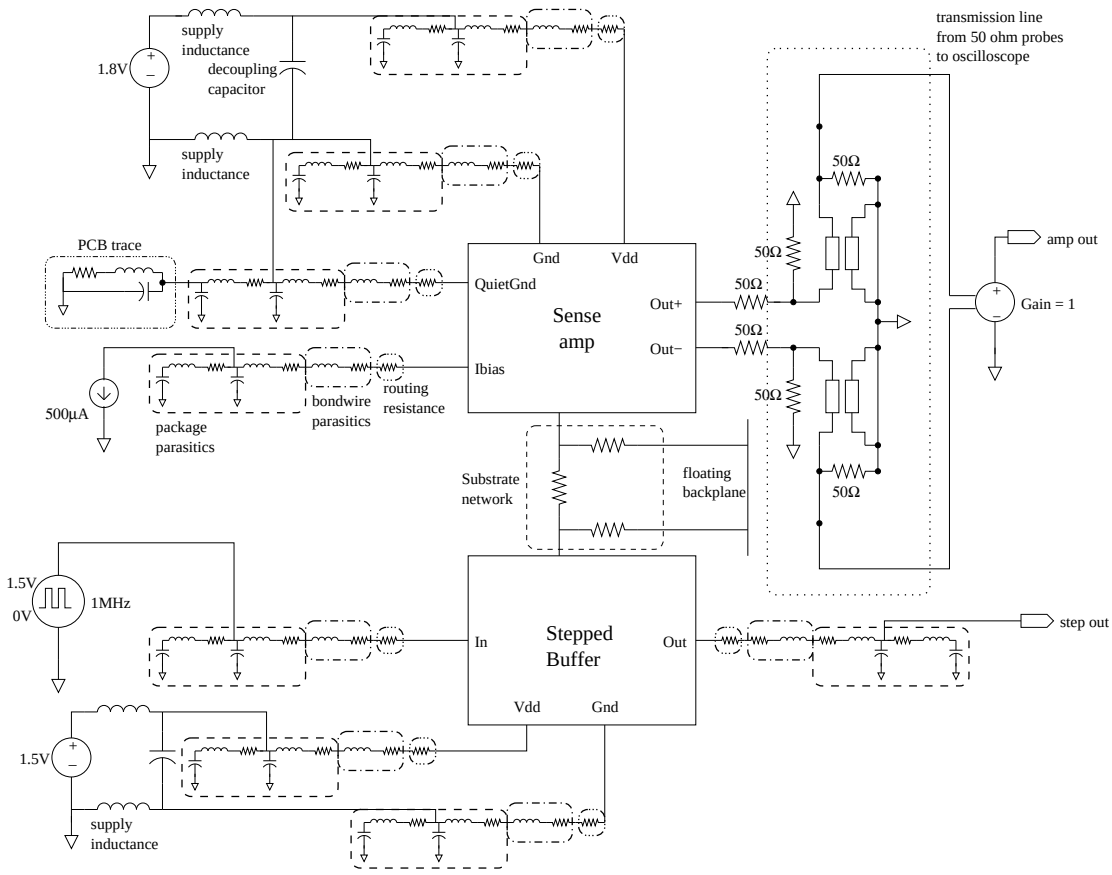


FIGURE A-2. BiCMOS simulation test setup.

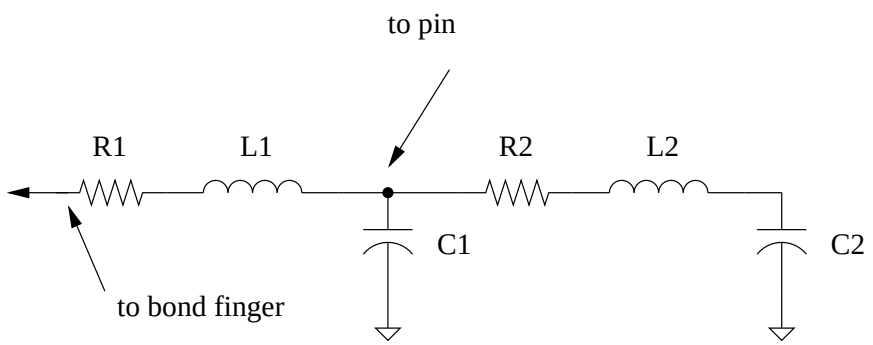


FIGURE A-3. PGA132 package pin parasitic model.

APPENDIX B. BICMOS Layouts

Figure B-4 shows the layout of the test chip for the SiGe BiCMOS process. The die size was 3mm x 4mm. The circuits tested on this die are labeled as Amp1 and Amp1 with moat, and SB is the stepped buffer. The stepped buffers with the bulks and sources separated (top) and tied together (bottom) are labeled as SB. Other circuits included on this die are a sample-and-hold circuit, a delta-sigma modulator, ring oscillators (ROSC) and some characterizatoin test structures.

The individual layouts of circuits used for measurements and simulations in this thesis are shown in Figures B-5 - B-8. The two stepped buffer layouts are similar, only the traces to the substrate contacts differ, being connected either to the transistor sources, or to separate pins.

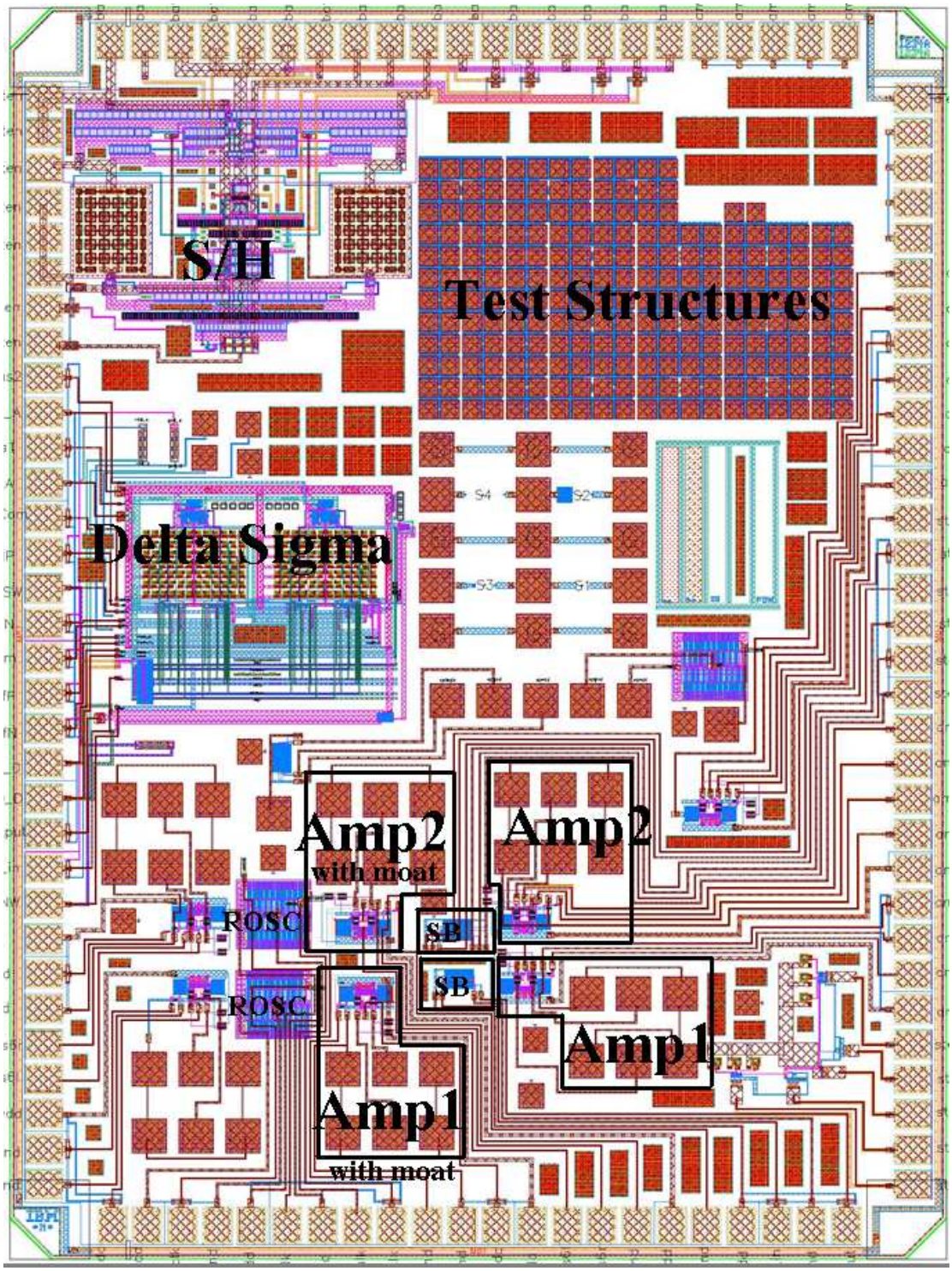


FIGURE B-4. Layout of BiCMOS test chip.

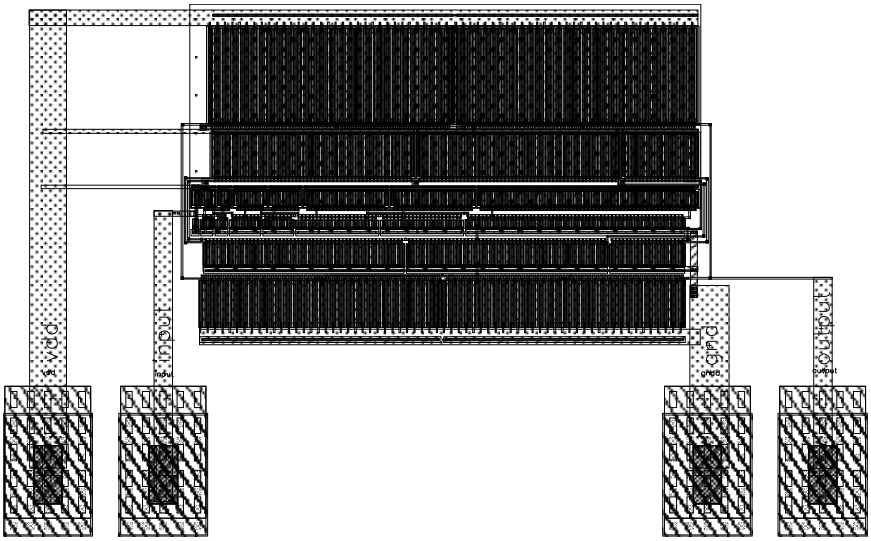


FIGURE B-5. Layout of stepped buffer (bulk together).

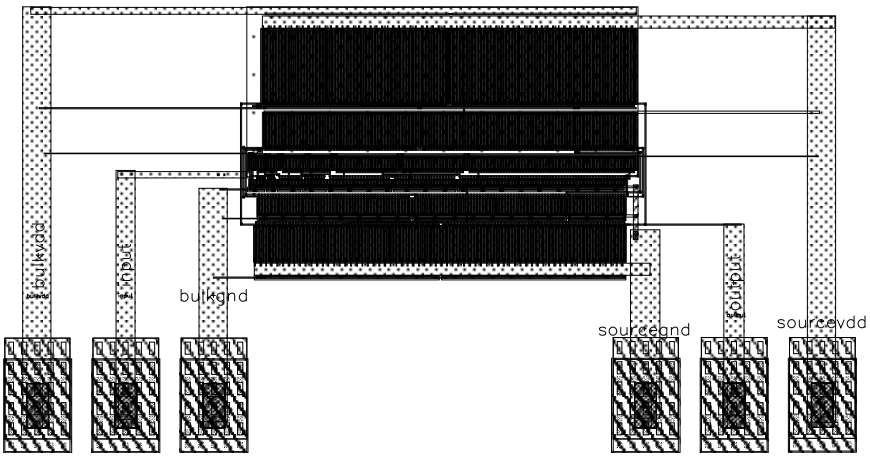


FIGURE B-6. Layout of stepped buffer (bulk separate).

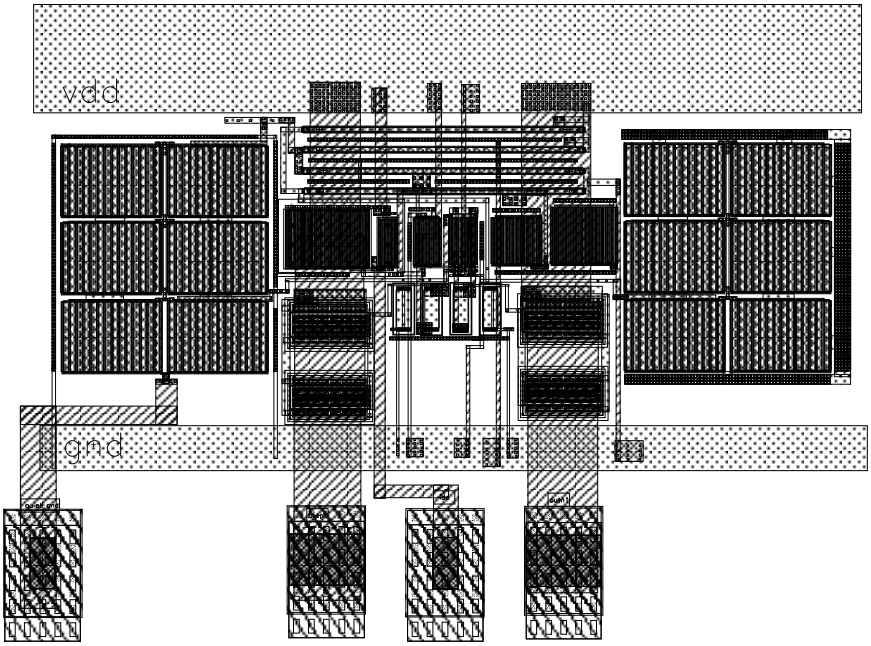


FIGURE B-7. Layout of *Amp1* without moat.

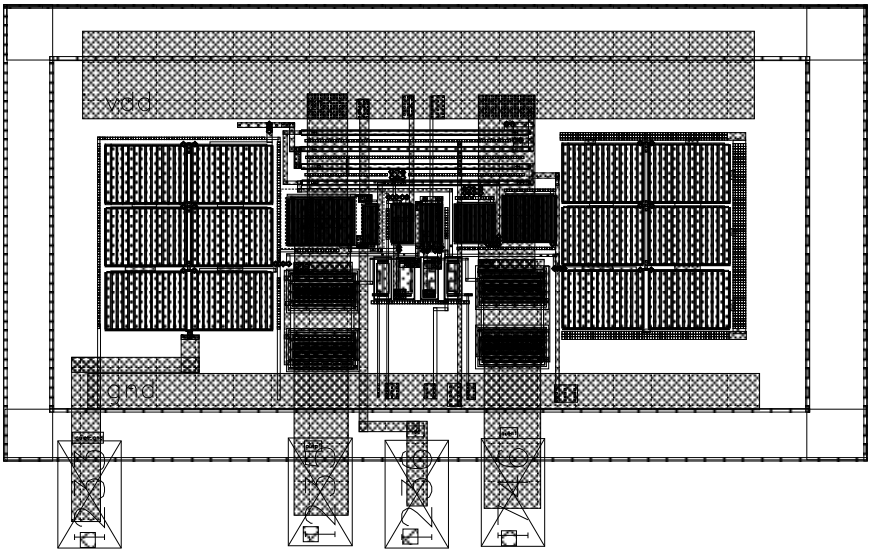


FIGURE B-8. Layout of *Amp1* with moat.

APPENDIX C. SOI Layouts

The layout of the SOI test chip is shown in Figure C-9. *Step3* and *step4* are labeled as 3 and 4, respectively in Figure C-9. The bottom circuit labeled as Body-tied Amp is *amp1* with body ties. Other circuits on the die include ring oscillators, a differential Colpitts voltage controlled oscillator (VCO) and complementary VCO, an inductor structure, test transistors and some test structures.

The floating body version of the stepped buffer layout is shown in Figure C-10, while the body-tied supply dependent sense amplifier layout is shown in Figure C-11. The body-tied version of layout only differs from the floating body version with the presence of body ties to the source along the width of the transistors.

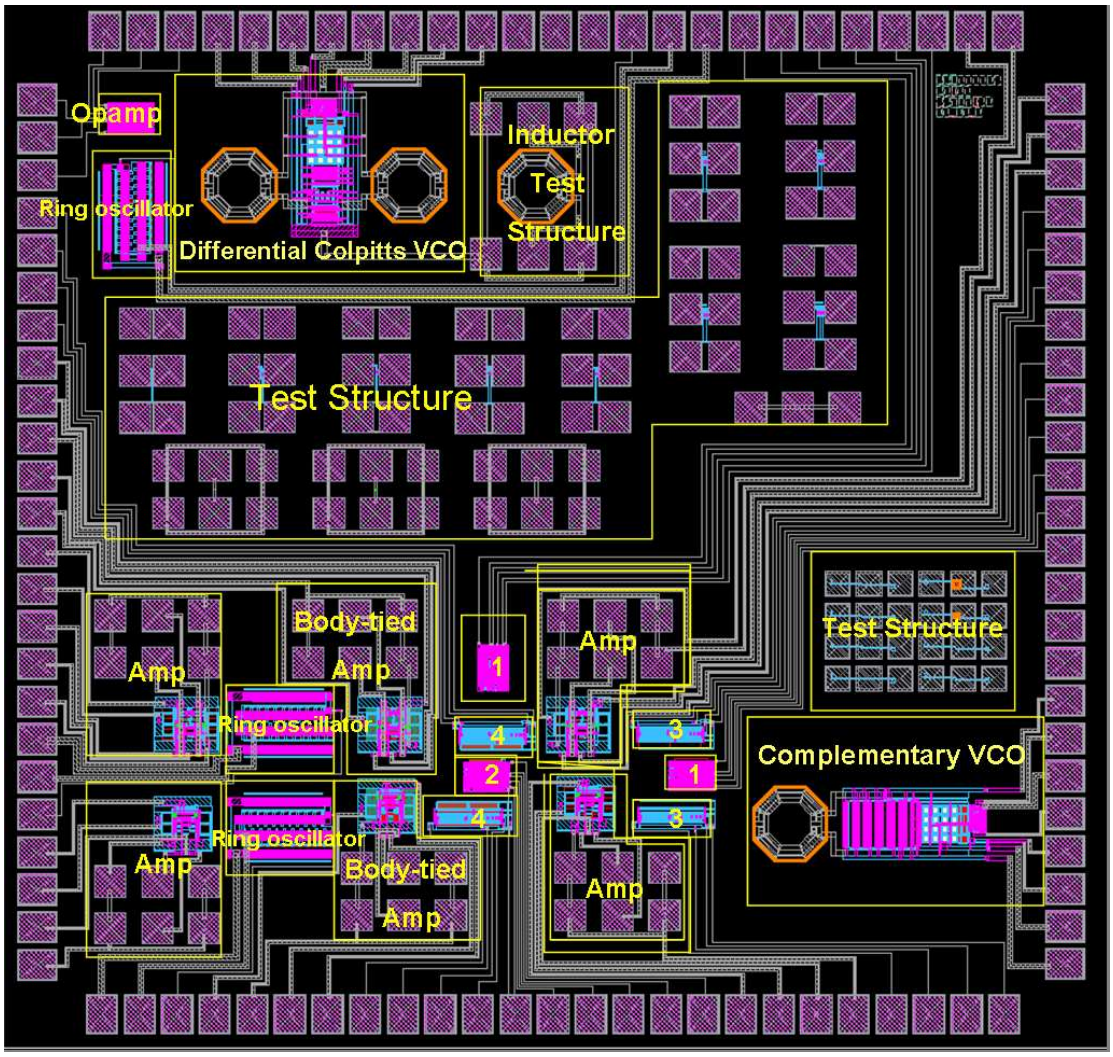


FIGURE C-9. Layout of SOI test chip.

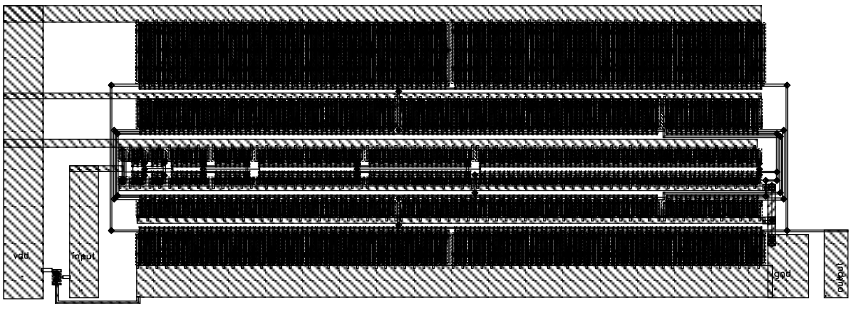


FIGURE C-10. Layout of SOI stepped buffer.

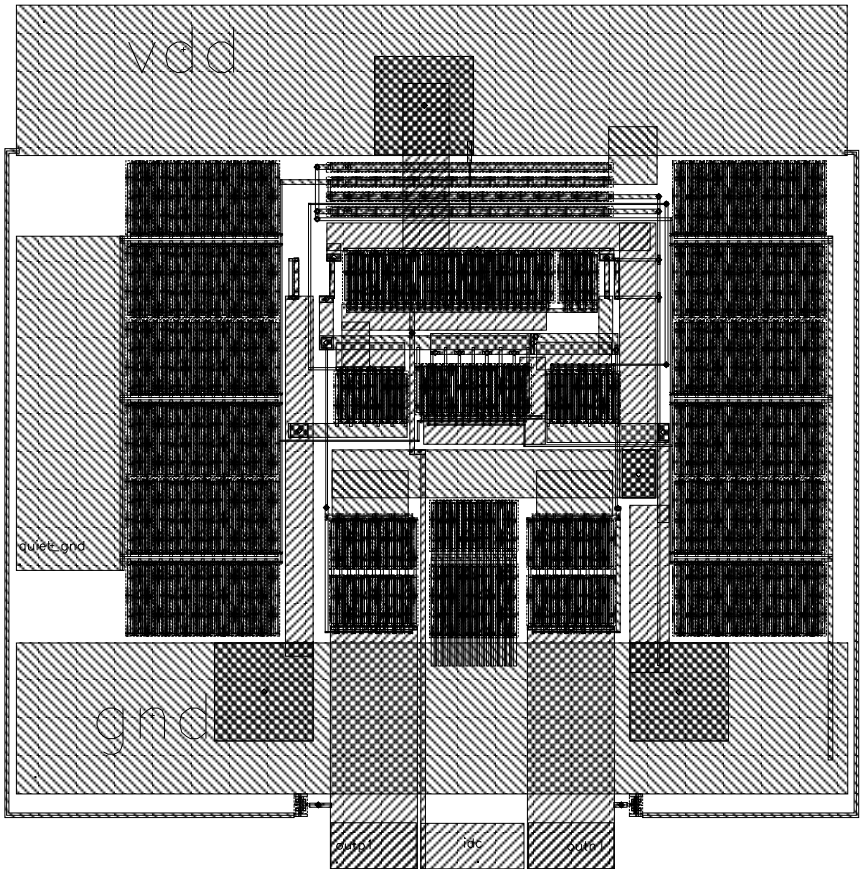


FIGURE C-11. Layout of SOI *Amp1*.

APPENDIX D. PCB Schematics and Layouts and Bondwire Diagrams

Figures D-12 and D-13 show the schematic and layout of the BiCMOS test board, respectively. The analog and digital power supplies are kept separate, and the power supply to each circuit can be turned on and off by means of a jumper. Current biases of 500μA are provided for each of the supply dependent versions of the sense amplifiers. The digital inputs to the stepped buffers and ring oscillators come from the same SMA connector, and are turned on or off with a DIP switch. The output of the stepped buffers also share the same SMA connector with a DIP switch to select the output. There are also versions of the sense amplifiers with outputs going to pins, so the outputs share SMA connectors in the same way as the stepped buffer outputs. This saved on the number of SMA connectors used. Decoupling capacitors are placed as close as possible to the pins. A zif socket was used for easy insertion and removal of the PGA packaged die. The die-perimeter ring (DPR) could be grounded or left floating by soldering or not soldering the bridge for the DPR.

A four layer board was used, with signal layers on the top and bottom, power on the second layer and ground on the third layer. For the layout of the test board, the components for the analog circuits were kept on the left side, while the components for the digital circuits were kept on the right side of the board. All the taller components also had to be placed such that they were not in the way of placing the probes. All the SMA connectors were placed on one side of the board also because probing had to be done. Figure D-14 also shows how the probes affected the layout of components on the test board. A photo of the BiCMOS PCB test board is also shown in Figure D-15.

The schematic for the SOI test board is shown in Figure D-16. It is similar to the BiCMOS test board. The inputs and outputs are connected to SMA connectors in a similar fashion as the BiCMOS test board, with the use of DIP switches. Since the SOI chip used the same PGA package as the BiCMOS chip, a zif socket was also used for easy insertion and removal of the packaged die. The layout of the SOI board is also similar to that of the BiCMOS version, taking into account the need for probing. A four layer board was also used here, with signal layers on the top and bottom layers, power on the second layer and ground on the third layer. Figures D-17 and D-18 show the layout and a photo of the SOI PCB test board, respectively.

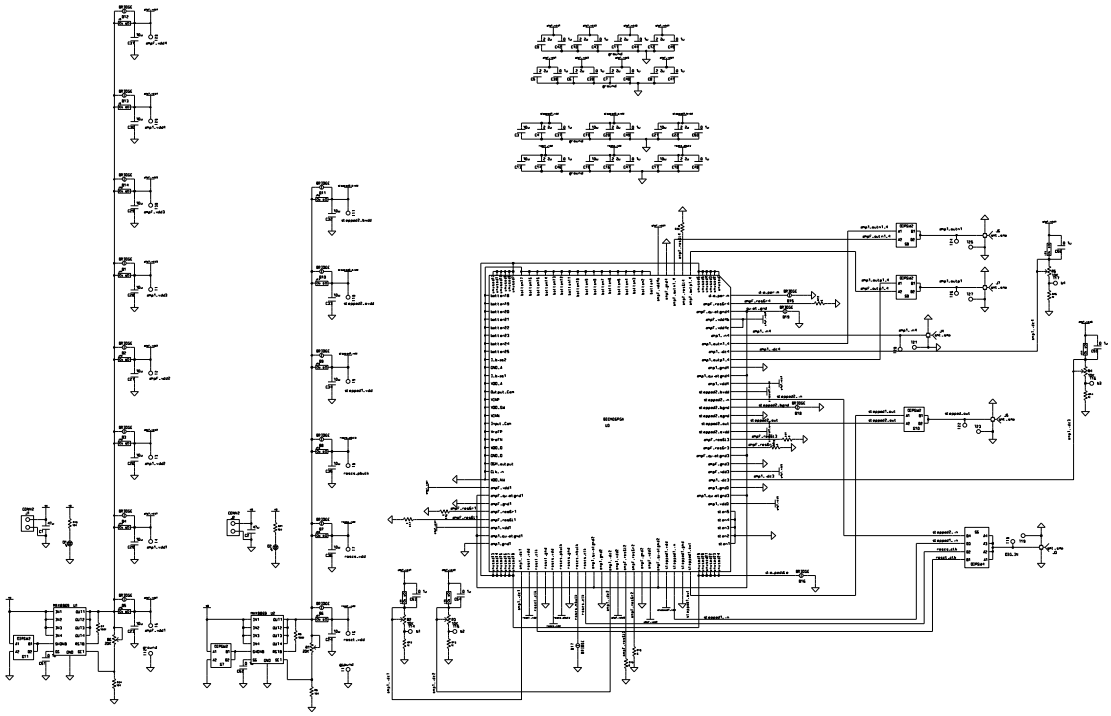


FIGURE D-12. Schematic of BiCMOS PCB test board.

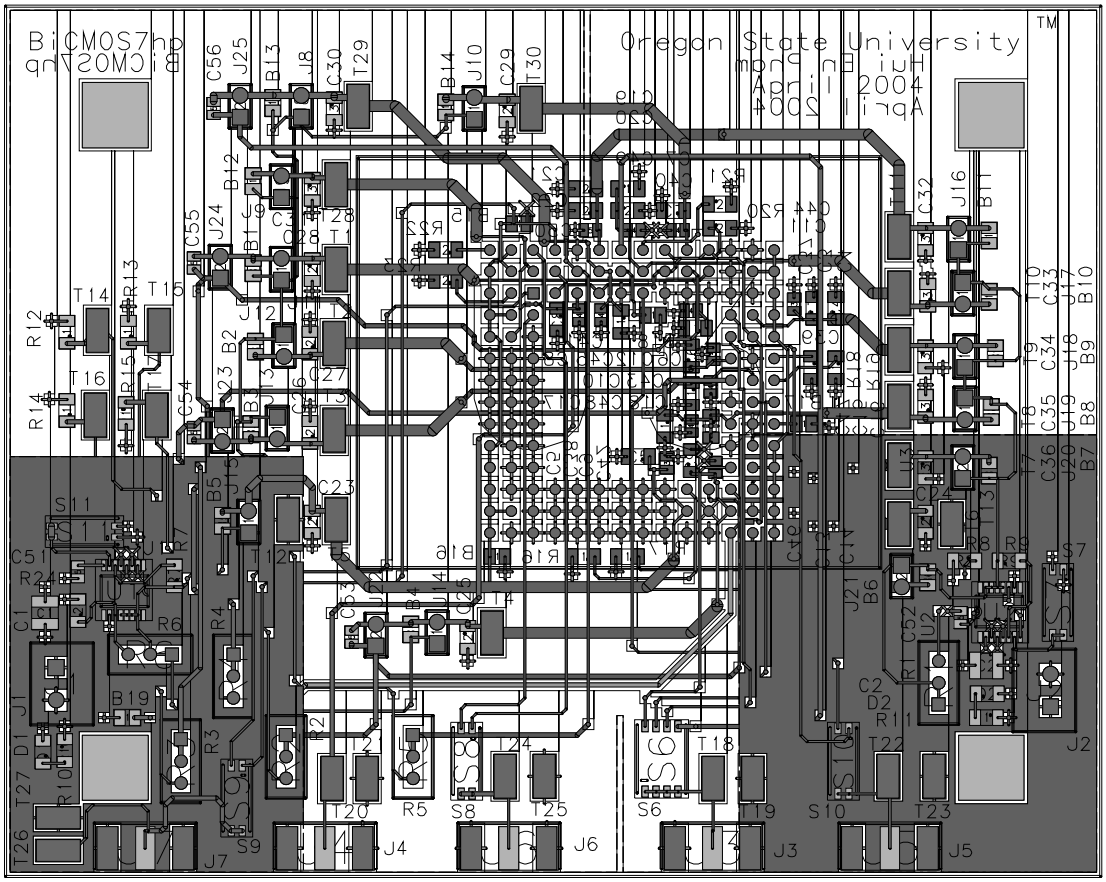
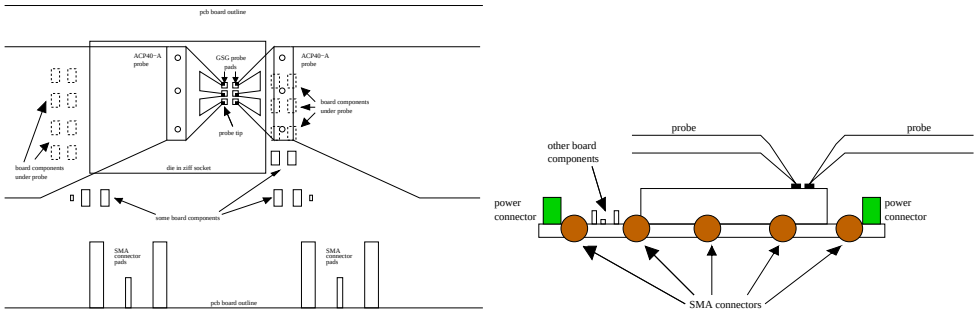


FIGURE D-13. Layout of BiCMOS PCB test board.



Top view Side view

FIGURE D-14. Position of probes in relation to test board.

FIGURE D-15. Photo of BiCMOS PCB test board.

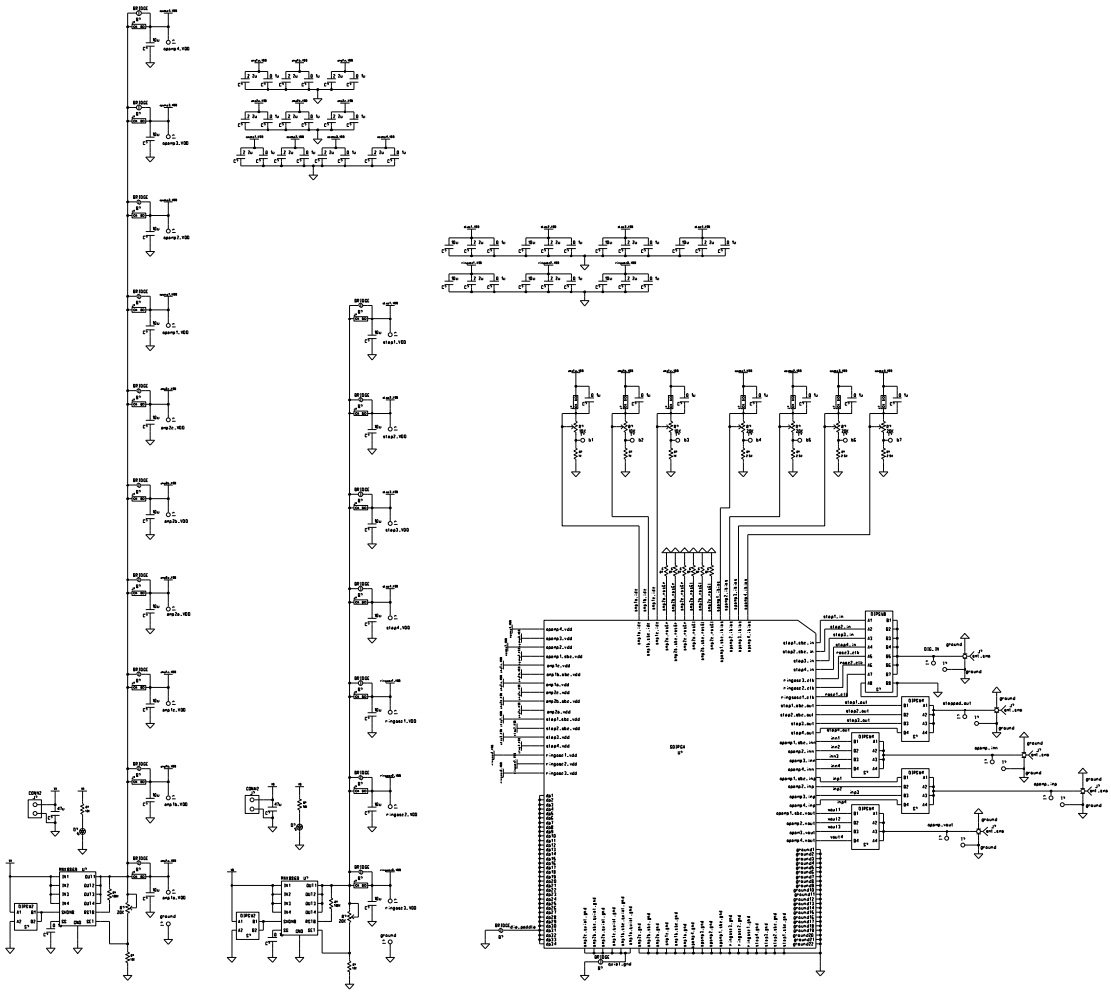


FIGURE D-16. Schematic of SOI PCB test board.

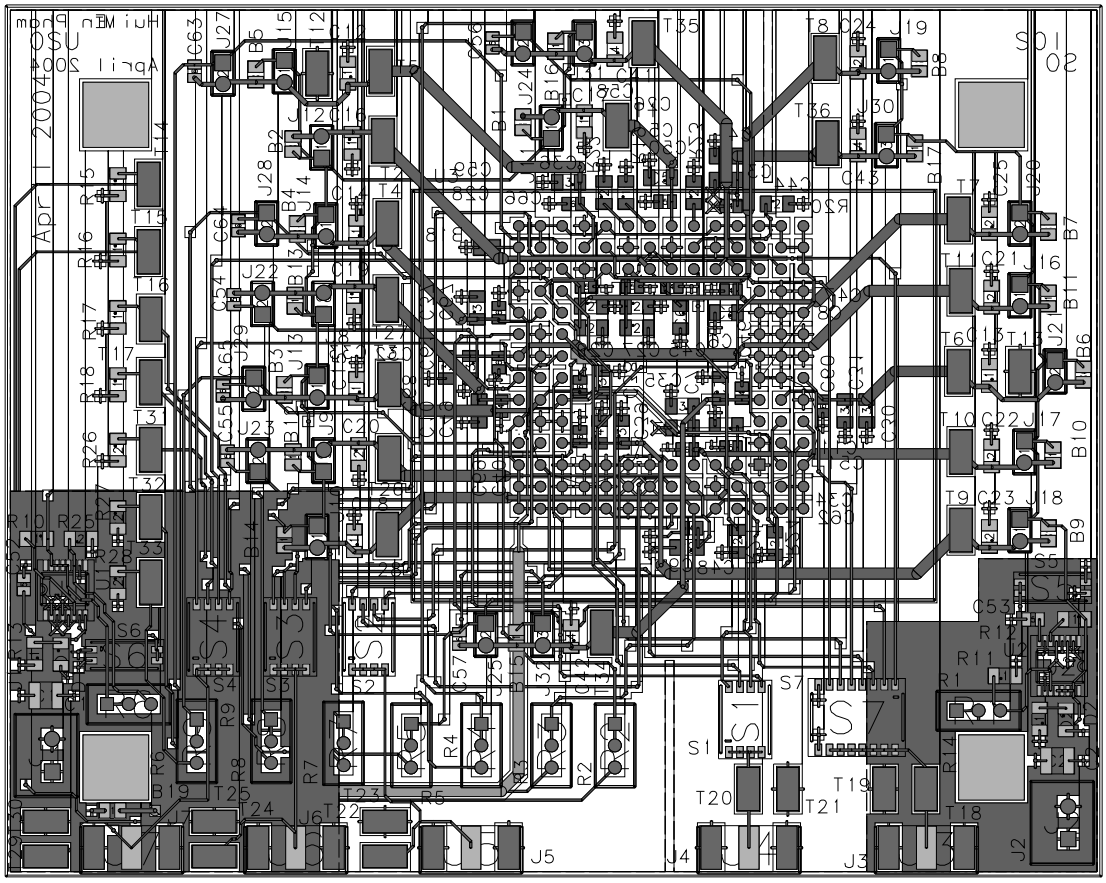


FIGURE D-17. Layout of SOI PCB test board.

FIGURE D-18. Photo of SOI PCB test board.

Bondwire Diagrams

Figures D-19 and D-20 show the bondwire diagrams for the silicon germanium (BiCMOS) and SOI die, respectively. The Kyocera 132-pin CPGA package was used for both die, and there were more pins on the package than needed. The unused pins were downbonded to the die paddle. Non-conductive epoxy was used as the die attach for the BiCMOS die, whereas conductive epoxy was used for the SOI die attach since the substrate in the SOI process has to be properly grounded for good measurements.

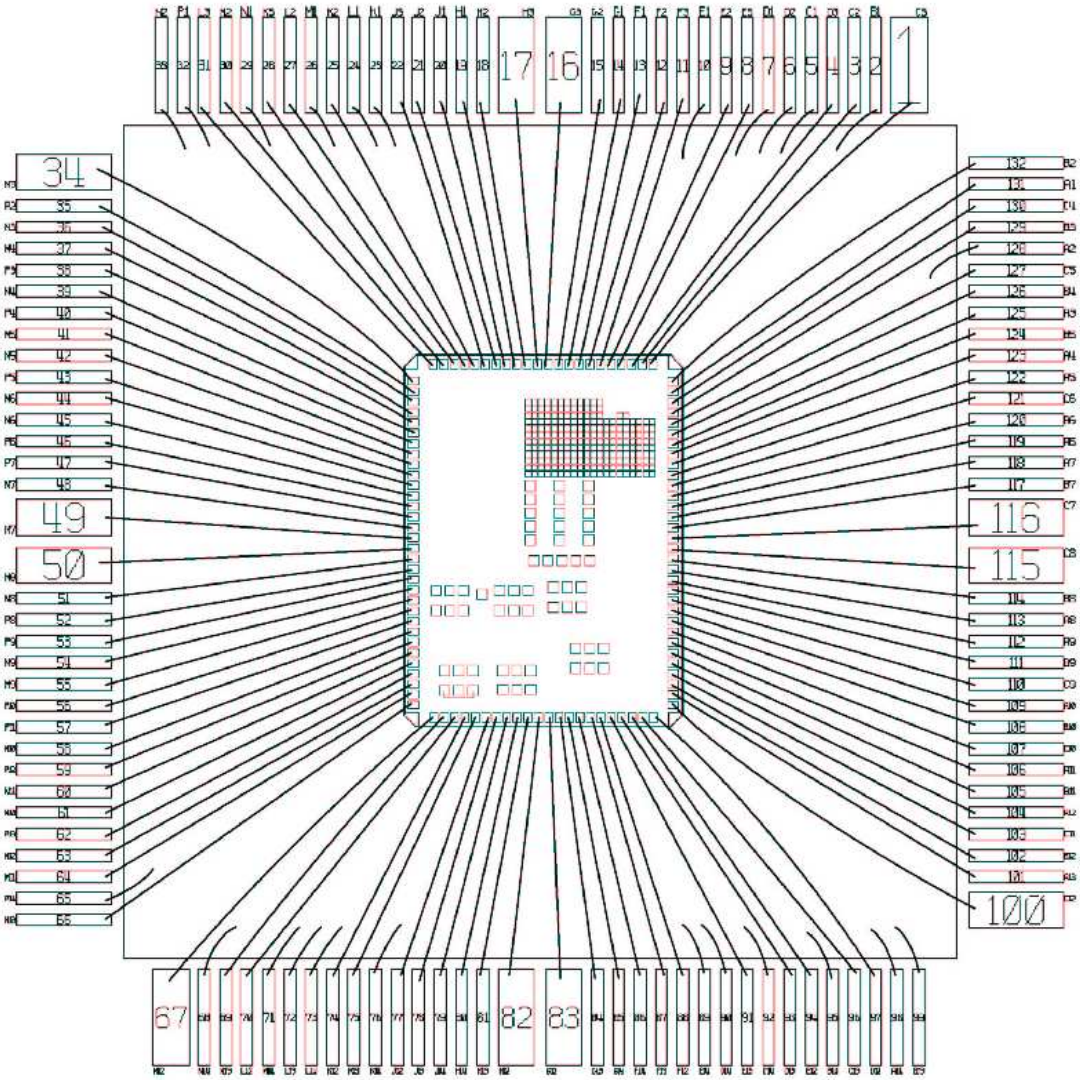


FIGURE D-19. BiCMOS bondwire diagram.

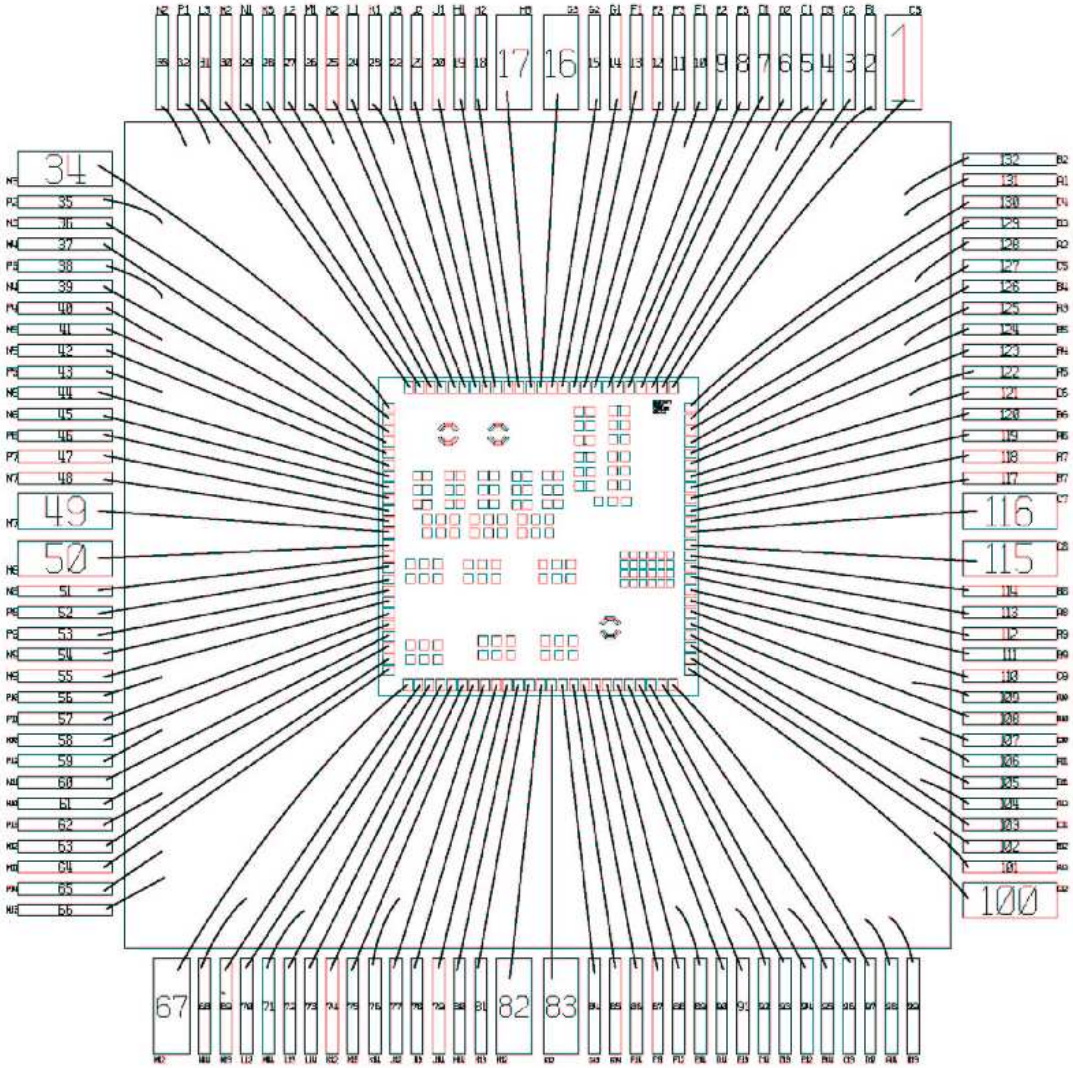


FIGURE D-20. SOI bondwire diagram.

APPENDIX E. Additional Measurements

BiCMOS Measurements

Figures E-21 and E-22 show the measured and simulated transient differential outputs of *amp1* without and with a moat, when *step1* is driven with a square wave at 1MHz and with the DPR grounded.

Figures E-23 and E-24 show the measured and simulated transient differential outputs of *amp1* without and with a moat, when *step2* is driven with a square wave at 1MHz and with the DPR grounded.

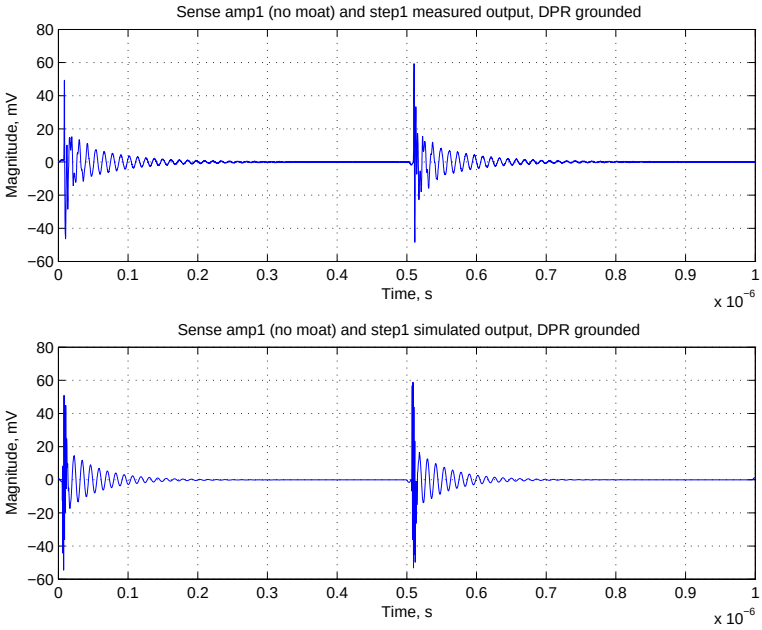


FIGURE E-21. Measured (top) and simulated (bottom) transient output of *amp1* without a moat, with *step1* driven at 1MHz and with the DPR grounded.

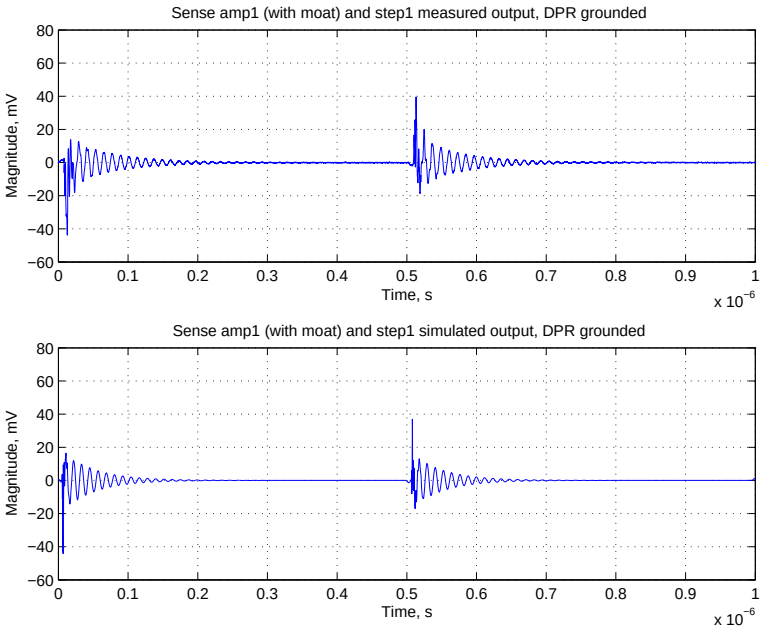


FIGURE E-22. Measured (top) and simulated (bottom) transient output of *amp1* with a moat, with *step1* driven at 1MHz and with the DPR grounded.

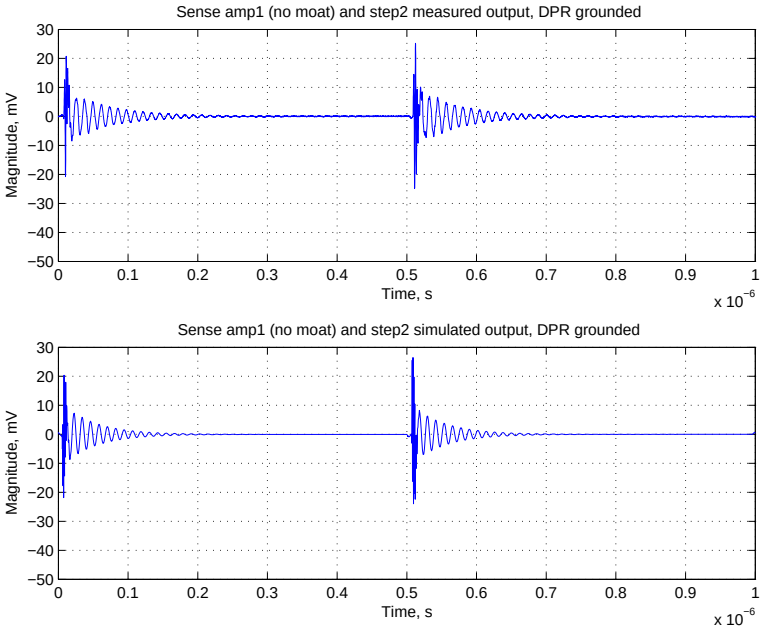


FIGURE E-23. Measured (top) and simulated (bottom) transient output of *amp1* without a moat, with *step2* driven at 1MHz and with the DPR grounded.

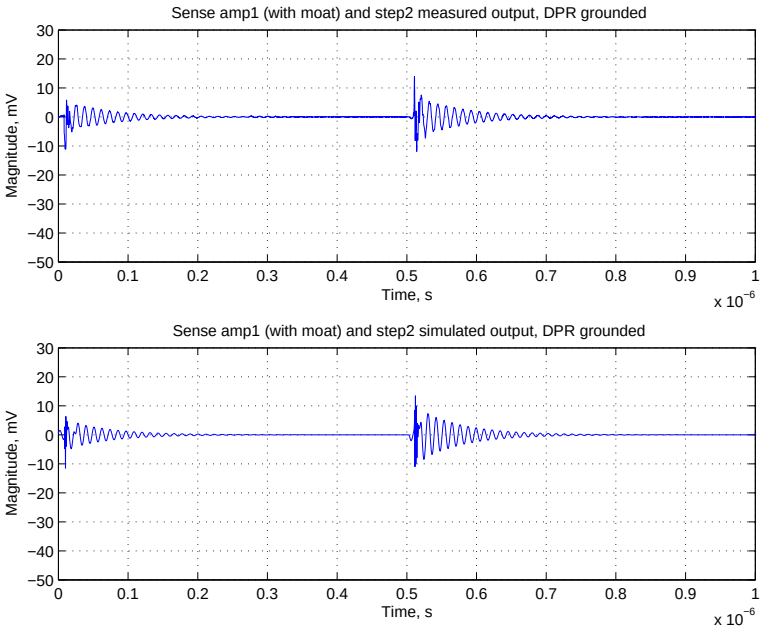


FIGURE E-24. Measured (top) and simulated (bottom) transient output of *amp1* with a moat, with *step2* driven at 1MHz and with the DPR grounded.

SOI Measurements

The I-V characteristic curves for 1-finger (1x) and 2-finger (2x) test transistors (with a unit size of $\frac{10\mu m}{0.2\mu m}$) are shown in Figures E-25 - E-32.

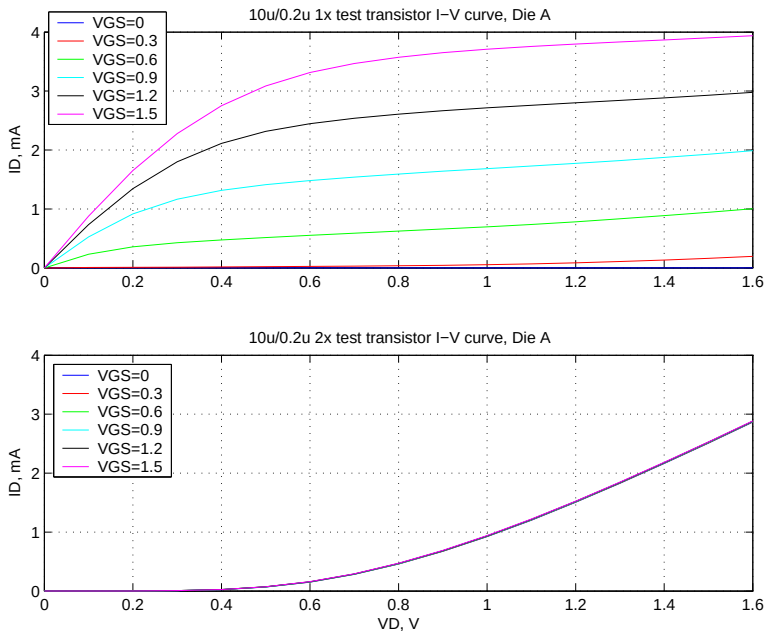


FIGURE E-25. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for bare die A.

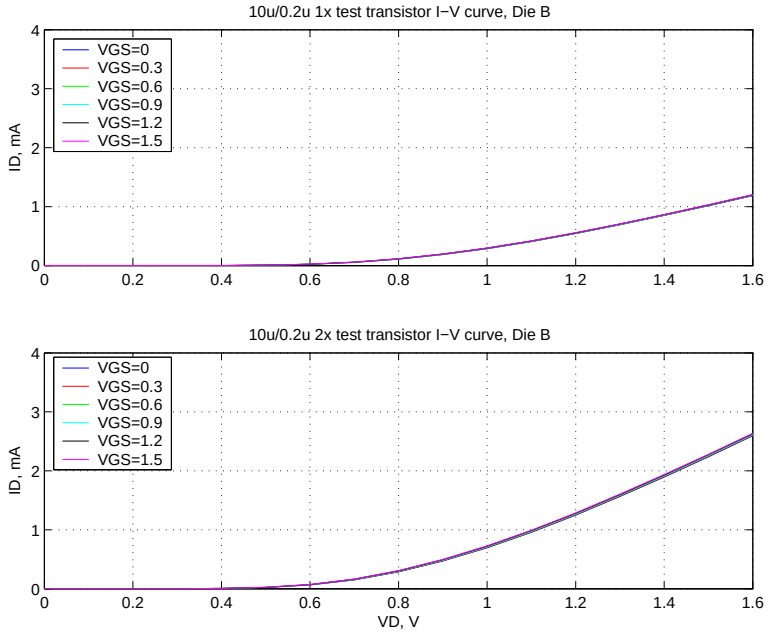


FIGURE E-26. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for bare die B.

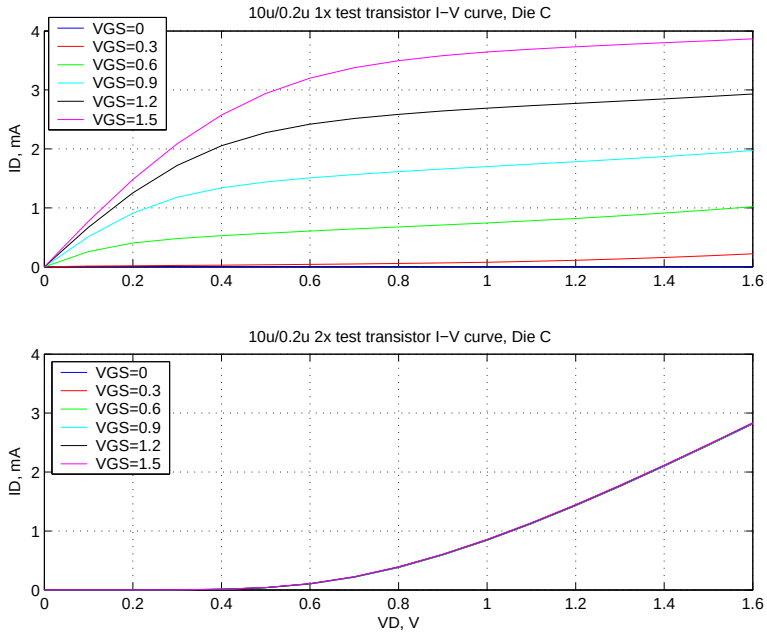


FIGURE E-27. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for bare die C.

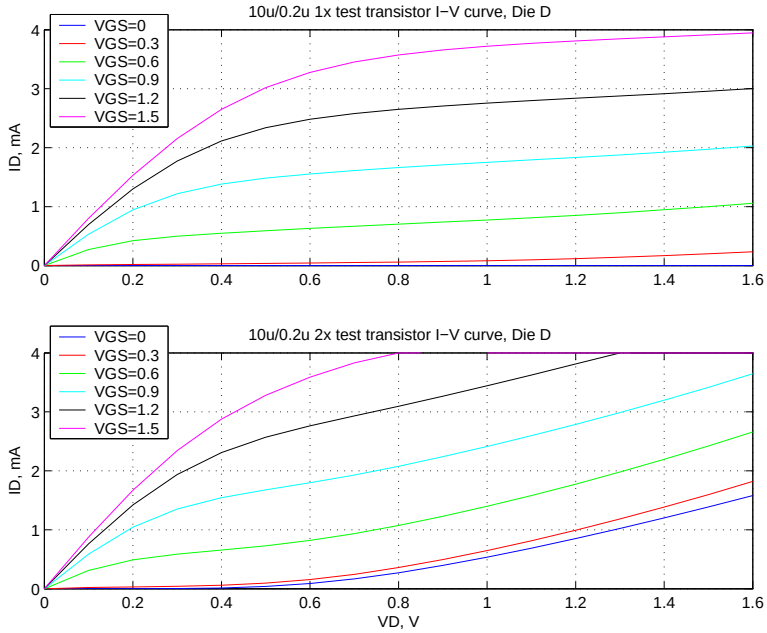


FIGURE E-28. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for bare die D.

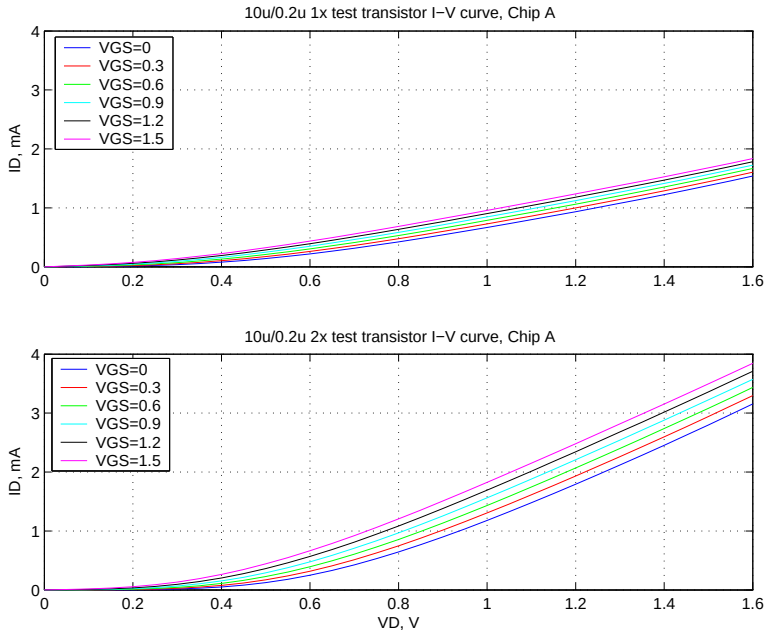


FIGURE E-29. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for packaged die A.

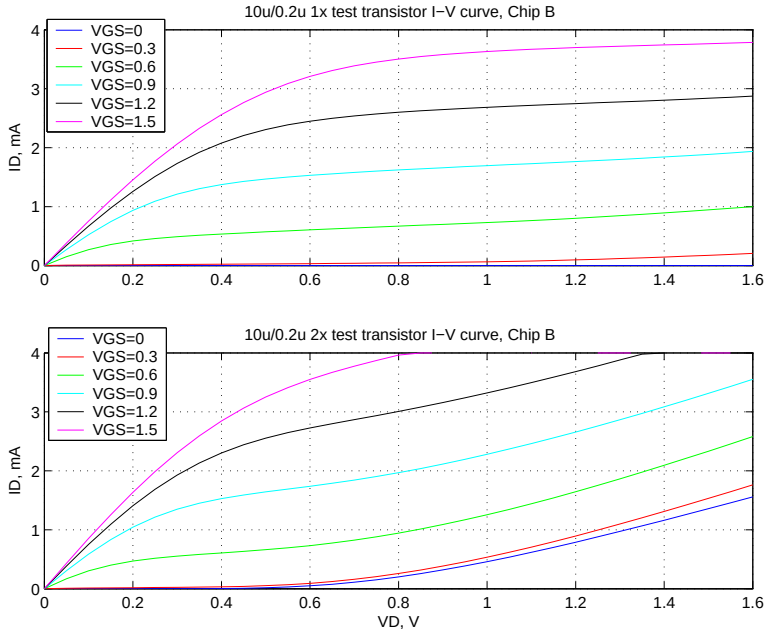


FIGURE E-30. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for packaged die B.

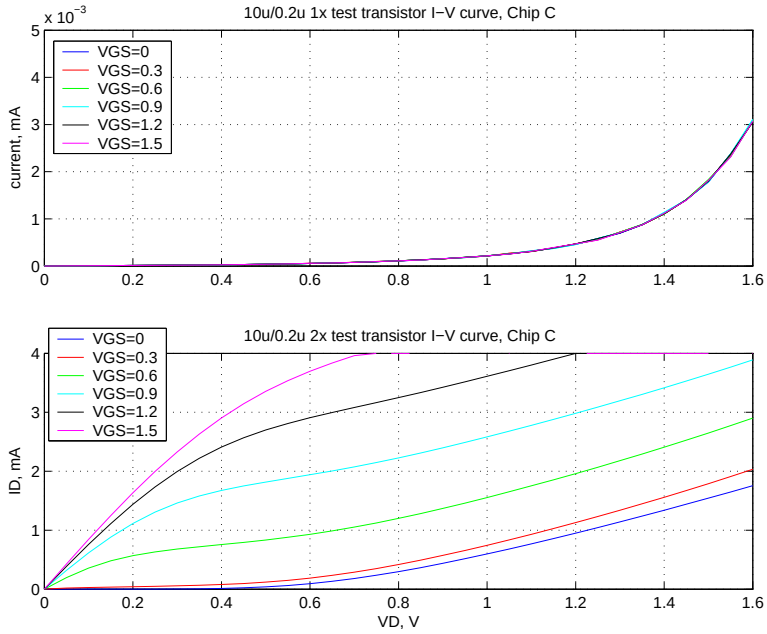


FIGURE E-31. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for packaged die C.

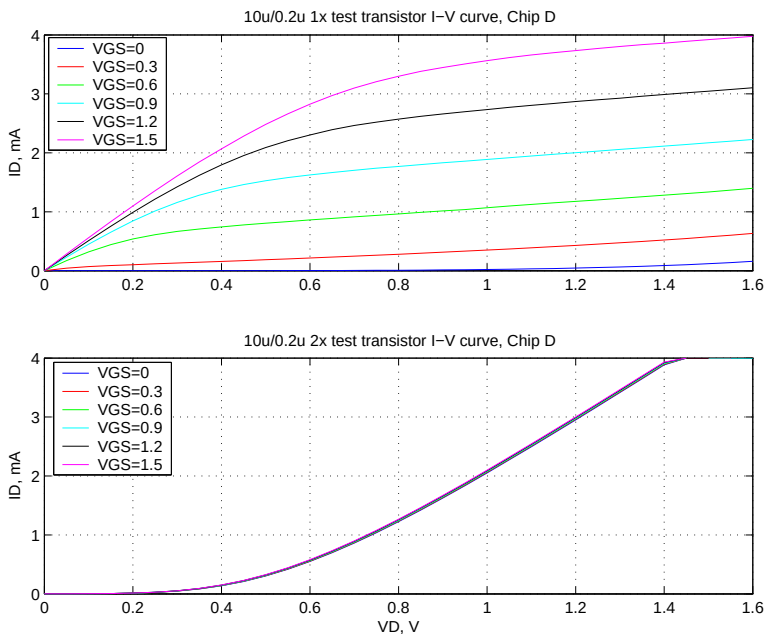


FIGURE E-32. I-V characteristic curve for 1x (top) and 2x (bottom) n-channel test transistor for packaged die D.