PERFORMANCE AND RF RELIABILITY OF GaN-ON-SiC HEMTs USING DUAL-GATE ARCHITECTURES (PREPRINT)

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AlGaN/GaN HEMTs on SiC have been fabricated with dual and single gate device geometries. Sub-threshold characteristics and drain bias dependence of large signal parameters were compared to identify differences in electric field. Degradation under RF stress reveals the relative impact of temperature and electric field. The results illustrate the beneficial effects of the dual gate geometry for performance and reliability.
Abstract — AlGaN/GaN HEMTs on SiC have been fabricated with dual and single gate device geometries. Subthreshold characteristics and drain bias dependence of large signal parameters were compared to identify differences in electric field. Degradation under RF stress reveals the relative impact of temperature and electric field. The results illustrate the beneficial effects of the dual gate geometry for performance and reliability.

Index Terms — GaN, SiC, HEMT, Dual Gate, Cascode

I. INTRODUCTION

Recently, AlGaN/GaN-based HEMT technology has emerged as a promising candidate for high efficiency, high power applications such as wireless base stations [1-3]. The competitive advantages of GaN HEMTs result from the material properties of the GaN/AlGaN material system and advantages afforded by various heterostructures possible in this material system [4-6].

Circuit parameters such as high bandwidth, low output capacitance and lower thermal resistance (due to SiC substrate) have contributed to the attractiveness of GaN-on-SiC HEMT technology for infrastructure power amplifiers [7]. Despite these advantages over incumbent Si-LDMOS or GaAs technology, control of the electric field profile by design of appropriate device structures still plays a critical role in determining the influence of traps as well as the reliability performance of GaN HEMTs [8].

Previously, dual-gate GaN HEMTs on sapphire have been reported for use as broadband amplifiers [9,10]. Further, cascode-connected GaN HEMTs have been shown to exhibit higher linear gain compared to a common source device [11].

In this paper, we present a comparison of the dc and RF characteristics of single gate and dual gate devices. We explore the sub-threshold characteristics of the device as a means to identify differences in electric field profile between the structures. The impact of the differences in electric field profile on CW output power at 2.14GHz is investigated by comparing CW loadpull measurements taken at drain voltages up to 60V. The degradation under RF stress under varying conditions of temperature and drain bias was investigated.

II. DUAL GATE HEMT DESIGN AND DC CHARACTERISTICS

Figure 1 shows a schematic cross section of the device structures studied in this work. Three different gate structures were designed, namely, standard single gate control devices, dual gate devices with the second gate (G2) being either a Schottky gate structure on GaN surface (DG-DR) or a MIS gate structure on top of SiN dielectric (DG-SR). The second gate (G2) is dc and RF connected to source. All device structures were fabricated in the same process flow on the same epitaxial material structure.

Figure 2 presents a comparison of the transfer characteristics of the three device structures obtained at 10V $V_{ds}$. As can be seen, the threshold voltage is similar for all three device structures, while for positive gate biases, they exhibit different saturated drain current values. As expected, the DG-DR structure exhibits different saturation behaviors at $V_g=0V$, due to the presence of the second Schottky gate, which is tied to the ground potential, while the DG-SR structure has a slightly lower value of saturated drain current compared to the control SG structure, due to existence of SiN dielectric under G2 for DG-SR structure.
This result indicates that the extension of the electric field to the source in reduced by the DG-SR structure and is further reduced by the DG-DR structure. This is consistent with a model that proposes that the second gate shapes the electric field, and that the magnitude of this effect is related to the proximity of the second gate to the channel.

For each device structure, the subthreshold characteristic was measured at different V_{ds} (5V to 50V). The increase of I_d with V_{ds} in the subthreshold regime (defined here as: I_d within 0.1mA/mm to 1mA/mm) is directly related to the increase of electric field at the source due to current continuity. Therefore, the spread in V_{gs} for a fixed I_d as a function of increasing V_{ds} indicates the extent of penetration of the drain induced electric field into the source region. This behavior is quantified by measuring the shift in V_{gs} (ΔV_{gs}) to maintain I_d at 0.1mA/mm as V_{ds} is increased from 5V to 50V (as explained in Fig 4(a)). This metric, ΔV_{gs}, is shown for different device structures as measured on several samples in Figure 4(b).

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III. LARGE SIGNAL CHARACTERISTICS AND COMPARISON

CW load-pull measurements at 2.14GHz were conducted for drain bias voltages of 28V, 48V, and 60V. Representative large signal characteristics are shown in Fig 5. The data shown in Fig 5 is obtained at drain bias of 48V and quiescent drain current of 0.1A/mm. Table 1 summarizes the key performance parameters for the three structures. The DG-DR and DG-SR structures have ~3dB higher small signal gain, as expected due to the decreased input capacitance and enhanced output conductance of these structures versus a single gate structure. The DG-DR structure has the highest PAE at V_{ds}=28V, however, the P_{sat} (defined as the Pout at maximum PAE) is approximately half the P_{sat} of the DG-SR and SG devices structures. This reduction in P_{sat} for the DG-DR structure is consistent with
the decreased value of \( I_{ds\text{max}} \). The \( P_{\text{sat}} \) and PAE are plotted as a function of \( V_{ds} \) in Fig. 6. For all three gate structures, \( P_{\text{sat}} \) increases for increasing \( V_{ds} \) from 28V to 60V. However, the \( P_{\text{sat}} \) is seen to increase linearly with \( V_{ds} \) for the DG-SR structure, while the increase is sub-linear for both the SR and DG-DR structures. The PAE increases across the drain voltage range for the DG-SR structure while the PAE decreases for the SR and the DG-DR structures.

The observed behavior of the output power and efficiency can be explained by the relationship between the gate geometry and the resulting injection of electrons from the drain edge of the gate. The SG device suffers from the high peak field at the edge of G2. The DG-DR device has the benefit of reduced field at G1, but has high peak electric field at the edge of G2. The DG-SR geometry has the advantage of field shaping, but without the degrading effect of charge injection from the edge of G2. The improvement in field profile without the charge injection from G2 is the reason for the advantageous relationship between PAE and drain voltage for the DG-SR device.

![Figure 5. Large signal loadpull results at \( V_{ds} = 48V \) for (a) dual-gate HEMT with single-recess, (b) dual-gate HEMT with double recess, (c) single-gate recessed HEMT (control device).](image)

**Table 1. Large Signal Power Summary**

<table>
<thead>
<tr>
<th>( V_{ds} ) (V)</th>
<th>( G_t ) (dB)</th>
<th>Peak PAE (%)</th>
<th>( Psat ) (W/mm)</th>
<th>Structure Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>24.9</td>
<td>46.8</td>
<td>4.0</td>
<td>SG</td>
</tr>
<tr>
<td>48</td>
<td>22.0</td>
<td>43.0</td>
<td>6.5</td>
<td>DG-DR</td>
</tr>
<tr>
<td>60</td>
<td>24.5</td>
<td>43.0</td>
<td>4.0</td>
<td>DG-DR</td>
</tr>
<tr>
<td>28</td>
<td>30.3</td>
<td>53.4</td>
<td>2.7</td>
<td>DG-SR</td>
</tr>
<tr>
<td>48</td>
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<td>49.7</td>
<td>4.0</td>
<td>DG-SR</td>
</tr>
<tr>
<td>60</td>
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<td>46.2</td>
<td>4.2</td>
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<td>60</td>
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<td>50.0</td>
<td>8.7</td>
<td>DG-SR</td>
</tr>
</tbody>
</table>

**Figure 6.** Drain bias dependence of key large signal parameters versus \( V_{ds} \).

**Figure 7.** Change in \( P_{out} \) at 60V RF stress at room temperature for dual-gate HEMT with single-recess, and single-gate recessed HEMT (control device).
The impact of increasing electric field as compared to increasing operating temperature was compared for two typical devices with the DG-SR structure. The first device was subject to a stepped RF stress where $V_{ds}$ was stepped up to 60V over a period of 24 hours. Subsequently, the output power was monitored over 250 hours at room temperature. The second device was biased at $V_{ds}=30V$ but the base plate temperature was increased to 200°C and subjected to the same RF stress conditions over 250 hours. The graphs of output power and gain versus time can be seen in Fig. 8. From this comparison, the increase of operating temperature is clearly seen to have a stronger reliability impact as the degradation at higher field and room temperature.

The exact mechanism for this stabilization is under study. The final parameter studied was the impact of a burn-in procedure on the RF output power stability over time. A DG-SR device was put through a thermal and electrical burn-in procedure and then subjected to RF stress at $V_{ds}=30V$ and a base plate temperature of 175°C. The comparison of the device stressed without burn-in at 200°C and the device stressed with burn-in at 175°C can be found in Fig. 9. From this data, the burned-in device appeared to have significantly better output power stability over time. The exact mechanism for this stabilization is under study.

The graphs of output power and gain versus time can be seen in Fig. 9. From this comparison, the burn-in device appeared to have significantly better output power stability over time. The final parameter studied was the impact of a burn-in procedure on the RF output power stability over time. A DG-SR device was put through a thermal and electrical burn-in procedure and then subjected to RF stress at $V_{ds}=30V$ but the base plate temperature was increased to 200°C and subjected to the same RF stress conditions over 250 hours. The graphs of output power and gain versus time can be seen in Fig. 8. From this comparison, the increase of operating temperature is clearly seen to have a stronger reliability impact as the degradation at higher field and room temperature.

Figure 8. RF stress on the DG-SR structure for $V_{ds}=60V$ at room temperature and $V_{ds}=30V$ at baseplate temperature of 200°C.

The second device was biased at $V_{ds}=30V$ and then subjected to RF stress at $V_{ds}=60V$ over a period of 24 hours. Subsequently, the output power was monitored over 250 hours at room temperature. The results of this work support the hypothesis that both device performance and device degradation under stress are strongly affected by the strength of the peak electric field in the gate-drain region of the HEMT. The performance improvement is illustrated by the scaling of PAE with $V_{ds}$ for the DG-SR geometry. This further advantage of this geometry is seen in the limited degradation displayed under RF stress conditions.

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REFERENCES