Parallel Error Coding Decoding for Highly Parallel Memories

ABSTRACT: Optical storage systems offer the potential for drastically increased data transfer rates through the use of parallel access. It is unrealistic however, to devote conventional serial electronic error correction hardware to such a large number (i.e., \(10^3 - 10^6\)) of data channels. We have focused therefore, on the development and evaluation of parallel error correction schemes for use with parallel optical memories. The principal focus of this work has been on the development, evaluation, and demonstration of parallel ECC algorithms and implementations for use with parallel access optical storage media. With volume-holographic parallel access memories in mind, we have developed parallel ECC schemes that demonstrate burst error tolerance and low area overhead (i.e., high code rate). Further, these new schemes map well onto VLSI hardware and efficient electronic parallel implementations have been demonstrated. Specific research results include (1) Extension of conventional serial 1D codes to 2D, (2) Design and fabrication of 2D parallel decoders (electronic and optoelectronic), (3) Optimization of capacity gain achieved through ECC, (4) Characterization of crosstalk noise in holographic storage and development of detection and apodization techniques for its mitigation, (5) A comprehensive study of optical system design issues and their impact on volume storage capacity and density.
[1] COVER SHEET:

Title:  
Parallel Error Coding/Decoding for Highly Parallel Memories

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[2] ABSTRACT: Optical storage systems offer the potential for drastically increased data transfer rates through the use of parallel access. It is unrealistic however, to devote conventional serial electronic error correction hardware to such a large number (i.e., $10^3 - 10^6$) of data channels. We have focused therefore, on the development and evaluation of parallel error correction schemes for use with parallel optical memories. The principal focus of this work has been on the development, evaluation, and demonstration of parallel ECC algorithms and implementations for use with parallel access optical storage media. With volume-holographic parallel access memories in mind, we have developed parallel ECC schemes that demonstrate burst error tolerance and low area overhead (i.e., high code rate). Further, these new schemes map well onto VLSI hardware and efficient electronic parallel implementations have been demonstrated. Specific research results include (1) Extension of conventional serial 1D codes to 2D, (2) Design and fabrication of 2D parallel decoders (electronic and optoelectronic), (3) Optimization of capacity gain achieved through ECC, (4) Characterization of crosstalk noise in holographic storage and development of detection and apodization techniques for its mitigation, (5) A comprehensive study of optical system design issues and their impact on volume storage capacity and density.
[3] TECHNICAL PROJECT SUMMARY: An outline of the research tasks completed during the period of this contract is given below. The detailed results associated with each of these tasks have been reported in numerous journal publications and student theses. A comprehensive list of these is also provided below.

1. Extended conventional serial 1D codes to 1D Parallel.
   (a) Examined various codes and decoding algorithms.
   (b) Established capacity advantage for ECC in holographic storage.
   (c) Quantified costs for parallel decoding.
   (d) Demonstrated candidate parallel 1D decoders (space and spectral).
   (e) Investigated optical accelerations using smart pixel arrays.

2. Scale/Fold 1D solutions into 2D.
   (a) Characterized 2D decoder complexity in terms of time/space/power.
   (b) Investigated 2D optical acceleration.
   (c) Extended parallel ECC application to optical matrix-vector processors.
   (d) Quantified performance of candidate smart pixel solutions.

3. 2D codes and decoding.
   (a) Studied/optimized 2D codes (product codes, array codes, interleaving).
   (b) Developed parallel decoding algorithms.
   (c) Designed optoelectronic implementations using smart pixels and optical interconnects.

4. Volume storage characterization.
   (a) Analyzed optical system design issues in volume storage.
   (b) Executed design optimization for storage density and capacity.
   (c) Identified fidelity impact of storage material quality.
   (d) Quantified pixel-wise and page-wise crosstalk in holographic storage.
   (e) Developed apodization method for mitigating page-wise crosstalk.
   (f) Developed parallel detection method for mitigating pixel-wise crosstalk.

[4] PUBLICATIONS:


DTIC QUALITY IMPROVED


[5] THESES:

