In Fault Modeling and Testing of Complex Systems such as the opto-electronic computing systems, a probabilistic fault model for complex degradable system was proposed. This model has been validated by using an event-driven simulator and fault injector on the representative measures from both replicated and dilated multi-stage interconnection networks. Furthermore, an architecture which integrates the concept of concurrency and distributed test pattern generation for testing complex circuits on a planer layout has been proposed. This approach performs test pattern generation and response analysis concurrently, therefore minimizing testing time for the overall system testing. Circuits are partitioned into segments which can be tested in parallel in testing time bounded by $2^n$ clock cycles, where $n$ is the maximum no. of inputs for the biggest cluster. The impact on the quality of the patterns generated has been found to be negligible. The software package is called Merced, which performs circuit test as well as performance analysis, with full compatibility with commercial tools.
June 15, 1995

Dear Sirs,

This final report serves to summarize all the research and development activities supported by the grant in three sections: research results, student support.

1. Research Results

Our work has matured greatly in the past couple of years. This is not evidence in the quality of the publications but also the number of invited presentations by industry and workshops. I will highlight some of the achievements followed by the list of the papers.

A. Fault Modeling and Testing of Complex Systems

This project has produced an architecture which integrates the concept of concurrency and distributed test pattern generation for testing complex circuits on a planer layout. This approach performs test pattern generation and response analysis concurrently, therefore minimizing testing time for the overall system testing. Circuits are partitioned into segments which can be tested in parallel in testing time bounded by $2^n$ clock cycles, where $n$ is the maximum no. of inputs for the biggest cluster. The impact on the quality of the patterns generated has been found to be negligible. Our software is called Merced, which performs circuit test as well as performance analysis. A list of the papers in this area is in Appendix I.

B. Performance Evaluation of Fault Tolerant Optical Multi-stage Interconnection Network

This project is to set up an evaluation scheme for complex degradable system. An event-driven simulator has been developed to study the corresponding measures as the replicated or
dilated banyans degrade under component failure. A fault-injector is used to inject faults under some given distribution and to degrade the network accordingly. A detailed discussion on the choice for optical network based on these design parameters has been documented in volume I of 'Foundations of Dependable Computing' by Kluwer Academic Publishing. Results on a general N component system were very encouraging for evaluating degradable systems that have uniform components. And simulation results on both the replicated network and the dilated network verify that our modeling techniques were useful. A list of the papers is attached in Appendix II.

You probably will notice that the papers listed in the Appendices go beyond the period of the support. Some papers were extension of the work done after the supporting period. I included the ones that have been accepted here for completeness. Papers still been reviewed, will be augmented later, once accepted.

2. Student Support

Two graduate students have been supported in the past three years under this grant. They have either graduated or on his way to finishing up with the support of this funding. Amiya Bhattacharya is finishing up his thesis work in performability evaluation of complex systems. He has been contacting several research laboratories in possible continuing support of this work at their facilities. Huoy-Yu Liou, who developed the framework for the test architecture, has graduated and is currently working for Tandem Computers. She will oversee that the design of all Tandem computers have the highest testability possible integrated using our framework. We thank the agency for their support over the past three years.

The above summarizes the agency’s support on the project. We are looking at all possibilities to extend this research work to industrial use. If there are suggestions as to who may be interested in this topic, I’ll be happy to accommodate. Thank you very much.

Best regards,

Ting-Ting Y. Lin
(619) 534-4738
Appendix I (Fault Modeling and Testing of Complex Systems)


Appendix II (Performance Evaluation of Fault Tolerant Optical Multi-stage Interconnection Network)


