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ONR Final Report

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Reliable Advanced Electronic Systems Research
July 1, 1988- June 30, 1991

Contract number: N00014-85-K-0600

Project Summary

The SDI Mission requires the production of systems that can operate reliably for long time periods without maintenance. Such systems are feasible only if they can be manufactured and assembled without defects, and run-time errors can be promptly and accurately identified.

The major objectives of this project were (1) new production test methods to eliminate chips with "latent" failures; and (2) fault-tolerance structures designed specifically for temporary as well as permanent failures.

Pseudo-exhaustive test. We have shown that to realize generally accepted quality levels (10-100 DPM) for integrated circuits, it is necessary to have a test technique that will detect at least 99.99% of all possible defects. Such a technique is not feasible by extending current methods that rely on the single-stuck fault model.

The only hope for a sufficiently thorough test technique is some methodology that does not rely on the enumeration of all possible defects and which can detect performance as well as functional faults. In other words, it must be possible to use what we are calling "weak fault models," which are very general fault classes such as all faults that don't introduce state (combinational faults) or all faults that increase supply current, etc. We have developed a design method to ensure that bridging faults in an implementation do not invalidate an exhaustive test due to an increase in state. A supply current monitoring methodology for testing ECL circuits has also been developed.

Our earlier work on bridging faults has now been extended with a technique for detecting delay faults without having to enumerate the faults or network paths.

Another research thrust was the development of a pseudo-exhaustive test methodology that is both thorough and cost-effective. We have written a program to segment arbitrary combinational logic into sufficiently small segments where exhaustive test of each segment is possible. The pseudo-exhaustive test approach is very different from the traditional techniques of either ignoring non single-stuck faults or trying to enumerate and generate tests for other fault models. Since there are too many faults to completely enumerate, such approaches cannot guarantee sufficiently high fault coverage. The risk involved in pursuing pseudo-exhaustive test is that it will not be possible to develop a completely general methodology, but this risk is justified due to the importance of the objective.

Run-time error detection. Run-time error detection is necessary to avoid false actions and to permit the elimination of failed modules. Traditional techniques for detecting run-time errors rely on duplicate subsystems or on the use of embedded checkers and error-detecting codes. Duplication is very expensive not only in terms of cost but also weight. Code methods are effective only for defects that correspond to errors within the capability of the codes used, and require substantial hardware overhead. We have developed a methodology that uses coprocessors called watchdog processors to implement run-time error detection. The watchdog systems are much smaller than duplicate systems and are more general than any of the coding based systems.

Latent failures are initially undetected failures that cause errors after the system is in operation. We have studied the effects on system operation of know failure mechanisms such as oxide breakdown and demonstrated that delay and pattern sensitive faults are important failure modes. Techniques are being developed that will detect these faults.

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We have also demonstrated that the effect of these defects (gate oxide shorts) on system operation depends on voltage and temperature. They can thus cause intermittent faults. We are developing techniques to permit detection of such defects. Designs for error detectors that function correctly in the presence of non-classical faults are being developed.

High-level design for test. To ensure the correctness of a design, the most promising approach is to start with a VERY high level specification and then to automate the design process. In particular, the resulting design should not only meet performance specifications correctly, but should also guarantee good testability at reasonable cost. We are developing a design system that will accept VHDL design specifications and automatically generate a testable implementation. The ingredients in this design system include testable implementations and test protocols for standard macrofunctions such as multiplexers, shifters, comparators, and adders. Self-testing implementations are of particular interest. We have developed a technique for allocating registers to enable effective and cost-efficient BILBO testing. A new BIST structure, called *Orthogonal BIST*, that reduces BIST overhead has been developed.

The only demonstrated solution for on-chip or on-board test response evaluation uses a Linear Feedback Shift Register to compact the test response. The major problem with this technique is the difficulty in determining whether faulty chips will pass the test because of "aliasing" in the signature register and of choosing design parameters to constrain the aliasing to an acceptably low value. While it is possible to simulate the test with the signature register in place, this process is too costly for realistic designs — every fault considered (usually single-stuck faults) must be simulated for all test inputs (fault dropping to reduce simulation cost is not possible when the signature register is included in the simulation). It is also possible to use a probabilistic model to estimate the probability of aliasing, but for typical values of test length and size of the signature register the evaluation of the model is computationally prohibitively expensive. Thus, the only hope is to develop useful bounds on the alias probability. We have developed bounds that permit the alias probability to be estimated very simply as a function of test length and signature register size. Thus, a specification of allowed alias probability can be met by choosing these two parameters according to the bound. Earlier bounds by Ivanov and Williams do not facilitate such a design technique.



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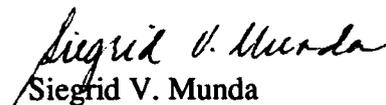
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To Whom it may Concern:

Enclosed is a copy of Prof. Edward J. McCluskey's final report for ONR Contract number: N00014-85-K-0600, Reliable Advanced Electronic Systems Research.

Please call us at (415)723-1258 if you have any questions.

Sincerely,


Siegrid V. Munda
Administrative Assistant
to Prof. McCluskey

encls.

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