FINAL REPORT

STRUCTURE-BASED DESIGN AND ANALYSIS
FOR CONCURRENT ERROR DETECTION AND RECOVERY
IN RELIABLE ELECTRONIC SYSTEMS

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A. Description of the Scientific Research Goals

The complex digital electronic systems necessary for successfully attaining the SDIO mission will be composed of extremely large numbers of fine geometry active devices densely integrated with potentially submicron interconnect. A major problem with the integration of these complex microelectronic circuits on VLSI chips and wafer-scale integration is that they become highly susceptible to physical failures and environmental disturbances, especially intermittent and transient failures. This problem is aggravated when these electronic systems are deployed in harsh environments potentially resulting in erroneous computation due to transient failures as projected in the SDIO mission. Failures can result in disastrous incorrect computational results or complete system shutdown. The purpose of this research has been to develop techniques for the design of highly reliable electronic digital systems based on the concurrent detection of errors and rapid recovery from failures and environmentally induced upsets. Concurrent error detection consistently monitors the correctness of computational results and therefore allows for the detection of errors due to transient environmental upsets as well as permanent failures. Basic scientific results were obtained in this research concerning the derivation of design and analysis principles for concurrent error detection and recovery in electronic systems.

B. Summary of Significant Results

1) Periodic Application of Concurrent Error Detection

A new approach to concurrent error detection was developed called periodic application of concurrent error detection (PACED). The PACED approach utilizes periodic rather than constant application of checking to verify correct results. The approach is parameterized, allowing application to various computational arrays and algorithms, for varying degrees of error coverage. This research resulted in applications of the technique to signal processing algorithms and in detailed simulation and analysis of the error propagation effects with PACED.

2) High Harvest Loop-Based Reconfiguration

A new method of interconnecting good elements in a linear array so that the delay between processing and memory elements is constant was developed in this research. The reconfiguration provides the capability of interconnecting a surprisingly high percentage of the good elements.

3) Reconfigurable Pipelines and Defect-Tolerant Trees

Methods and algorithms for reconfiguring pipeline structures were developed. An accurate method of predicting the percentage of usable pipelines given the defect distribution was developed. A design for large area defect tolerant trees was also proposed. The design allows for defective interconnect and switches and guarantees that an arbitrarily high percentage of the good processing elements can be incorporated into the tree.

4) Simulation and Evaluation

A behavioral simulator was implemented for evaluating the fault coverage of test patterns for integrated circuits. The evaluation is based on the probability of failure derived from the behavioral simulator.
C. List of Publications/Reports/Presentations

1. Papers Published and Submitted to Refereed Journals


2. Non-Refereed Publications and Published Technical Reports

none

3. Presentations

a. Invited


W. K.-Fuchs, "Checkpointing and Recovery in Multiprocessor Systems," Texas A&M University, College Station, Texas, April 1992.

b. Contributed (See list of refereed published conference papers below.)

4. Books (and book chapters)

none supported by SDI

5. Refereed Published Conference Papers (Supported by this Grant)


