Mesa epitaxial and planar implanted InP power MISFET's have been fabricated. At 9.7 GHz CW mesa devices demonstrated 4.5W output with 4 dB gain at 46 percent power-added efficiency with a power density of 4.5W/mm, over three times the highest value ever reported for GaAs FET's. Power output is stable with 2 percent over 167h continuous operation. Planar implanted devices exhibited 3.5W output with 5.4 dB gain, 40 percent power-added efficiency and 3.5W/mm power density at 9.7 GHz.

Presented at Electrochemical Society Meeting, 18-23 October 1987, Honolulu, HI.
features with respect to high mechanical stability, electromechanical efficiency, and positioning accuracy, especially at low temperatures, is a deeper aspect in the influence of cool down-on the electrodynamic behavior of the system.


With the recent emphasis on the characterization of electronic and electro-optical devices and their temperature dependent characteristics, we believe that a survey of available cryogenic apparatus is a valuable reference to the researcher. A comprehensive survey and the advantages of various cryogenic systems are discussed. A survey of state-of-the-art high speed, low noise measurement apparatus is reviewed.

393 The Use of Automated Laboratory Test Equipment for the Characterization of Electronics at Cryogenic Temperatures: C. N. Magoun, R. G. Hansen & Associates, Santa Barbara, CA 93101

Recent developments in the integration of PC computers and automated test controllers with commercially available laboratory cryogenic systems for the characterization of electronic and electro-optic devices for space are discussed. With the recent emphasis on the reliability of electronic systems and components in a "space environment," considerable emphasis is placed on the thermal cycling of electro-optic and electronic equipment with particular emphasis on the reliability of dedicated controllers with programmable temperature indicators and controllers, a vast new capability is available to the researcher. A recent survey of equipment is presented.

394 The Dielectric Chip Probe/Test System (DCP/T): J. G. Tompkins, Teledyne TAC, Woburn, MA 01801

Developed under U.S. Army Manufacturing Methods and Technology Project No. 1060 entitled "Electrical Test and Screening of Monolithic Microwave and Millimeter-Wave Integrated Circuits" the DCP/T is a fully automatic handling system that aligns and tests semiconductor devices from 70 MHz to 300 GHz. It is designed to be the "mount-bond-test approach" where the device could be mounted into a carrier, wire-bonded to metallization on the carrier, and tested at temperature via carrier pin-out interconnections.

DIELECTRICS AND INSULATION/ELECTRONICS

Dielecric Films on Compound Semiconductors


MMC Research at NASA Lewis Research Center is actively involved in the development of monolithic microwave and millimeter wave integrated circuits. The approach of the program is to support basic research in the development of MMC devices, while the technology is under contract, thereby facilitating the transfer of technology to users. Part of the focus of the program has been the extension of technology to higher frequencies. In recent years, the development of 90 GHz devices, particularly for microwave and millimeter wave applications, has been a major undertaking. In this survey, one step that has been made in realizing these devices is the development of high dielectric constant films on compound semiconductors.

396 Effects of Photochemical Treatments on Surface Properties of Dielectric Films: T. Sawada, H. Hasegawa, T. H. Yano, and H. Ohno, Dept. of Electrical Engineering, Faculty of Engineering, Hokkaido University, Sapporo 060, Japan

Photochemical oxidation in water and of photochemical treatment in NH, on surface properties of GaAs are critically investigated by transverse transport, MIS C-V, photoconductivity, and XPS measurements. Photochemical oxidation resulted in enhanced pinning with enhanced PL intensity rather than in "pinning" as previously reported. Treatment in NH, under ArF excimer laser reduced pinning with reduced PL intensity. The result is explained by a rigorous computer simulation showing that higher N, can give enhanced photoconductivity under certain conditions.

397 Silicon Nitride Films Deposited by ECR Plasma CVD for Monolithic Microwave and Millimeter-Wave Applications: M. Sawada, and Y. Harada, Research Center, Sanyo Electric Co., Ltd., 1-12-13 Hashiridani, Hirakata, Osaka 573, Japan

The development of rapid thermal annealing technique for implanted GaAs wafers covered with SiN films is very important for the fabrication of GaAs IC's. The SiN films used in this process play the role of (i) an encapsulation for the annealing, and (ii) through-implantations and encapsulation Films with properties which we believe to be the best, have been developed by ECR Plasma CVD.


Mesa epitaxial and planar implanted InP power MISFET's have been fabricated. At 8 GHz CW mesa devices demonstrated 5.3W output with 4 dB gain at 20% power-added efficiency with a power density of 4.5 W/mm2 over three times the highest value ever reported for GaAs FET's. Power output is stable within 2% over 167th continuous operation. Planar implanted devices exhibited 3.5W output with 5.4 dB gain, 40% power-added efficiency and 3.5 W/mm2 power density at 9.7 GHz.


Germanium nitride (GeN) films were deposited on indium phosphide compound semiconductor substrates using plasma-enhanced chemical vapor deposition with 5% germane in argon, nitrogen, and nitrogen-argon mixtures at 5 mtorr using 13.56 MHz frequency, and a rf power of 100 W. The refractive index of the films was determined by ellipsometry to be in the range of 1.9-2.2. Depth profiles obtained using Auger electron spectroscopy were used to determine the composition of the films. Anodized indium phosphide was used to compare the hydrogen content of the films. MIS capacitors were used to determine the electrical properties of the films. In order to demonstrate the feasibility of germanium nitride as a gate insulator, InP MISFET's were fabricated and exhibited transconductance of 340 mS/mm.

400 Ultrashort Gaps Between Schottky Barriers Formed by Anodization: P. B. Kose* and D. S. Katzer, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221.

Schottky barrier charge-coupled devices with overplating metal electrodes on semi-insulating gallium arsenide: have been demonstrated. The thin dielectric isolation (5000A) on InP/InGaAs implanted wafers was formed by anodication in an ethylene glycol base electrolyte. The overlapping gate structure includes that of the base-packed overlapping and the Schottky gate. The device active channels were formed by ion implantation and rapid thermal annealing with silicon nitride used as a cap. The area oxidation was performed after all high temperature processing steps, including ohmic contact alloying, were complete. Successful deposition of aluminum, palladium, and gold layers were made. Details of the process and device characteristics are presented.

401 Processes in the Fabrication of CCD's on GaAs: P. B. Kose and D. S. Katzer, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221

Two masking requirements exist in the production of CCD's on gallium arsenide: (i) to mask electrical contacts against anodic oxide growth in regions where internal metal contacts are to be made, and (ii) to protect the silicon nitride cap against electrical breakdown at high voltages that are to be applied to the anodic oxide growth process. In both cases, tantalum metal films formed by sputtering have been used as the initial step on protect metal layer. Tantalum films have been found to be particularly well suited to this application because (i) it is an anodizable metal, and (ii) its anodic oxide can be controlled by the thickness of the tantalum layer. Hence, it provides a useful medium for differential masking of aluminum and gallium oxides that are not etched by the CF, plasma. Details of the process and device characteristics are presented.

402 Rapid Thermal Annealing of Ion-Implanted Indium Phosphide: R. D. Biedenbender,* J. V. Rapoor, and D. X. Deng, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221-0030, W. D. Williams, NASA Lewis Research Center, Cleveland, OH 44135

Rapid thermal annealing of ion-implanted indium phosphide has been investigated. The implantation species investigated was silicon, and the encapsulant used was silicon nitride. Substrates were rapid thermal annealed for various times in either nitrogen or hydrogen ambients. The method was demonstrated using Auger electron spectroscopy depth profiling and a sequence of high resolution x-ray photoelectron spectroscopy measurements which concentrate in the secondary ion mass spectrometry. Electrical properties of implanted regions and test structures were analyzed using MISFET's. The sheet resistance of the implanted regions and test structures were measured. Details of the process and device characteristics are presented.

403 Interface Properties of InP-Dielectric Systems: P. Viktorovitch, Laboratoire D'Electronique — UA CNRS 888, Ecole Centrale de Lille, Dept. de Physique, 59037 Lille Cedex, France

The development of appropriate passivation techniques for III-V compound semiconductors is of considerable interest for applications. These high speed, high power devices are used in integrated circuits. In this paper, special attention is given to the device in connection with the fabrication of MISFET's and diodes. The characteristics of the devices are presented along with other applications of high speed, low noise measurement apparatus is reviewed.

404 Recent developments in the integration of PC computers and automated test controllers with commercially available laboratory cryogenic systems for the characterization of electronic and electro-optic devices for space are discussed. With the recent emphasis on the reliability of electronic systems and components in a "space environment," considerable emphasis is placed on the thermal cycling of electro-optic and electronic equipment with particular emphasis on the reliability of dedicated controllers with programmable temperature indicators and controllers, a vast new capability is available to the researcher. A recent survey of equipment is presented.
ABSTRACT
Mesa-type epitaxial and planar fully ion-implanted indium phosphide (InP) n-channel depletion-mode power MISFETs have been fabricated on Fe-doped semi-insulating substrates using SiO\textsubscript{2} as the gate insulator. At 9.7 GHz CW mesa-type epitaxial devices demonstrated 4.5 W output with 4 dB gain at 46% power-added efficiency with a power density of 4.5 W per mm of gate width, over three times the highest value ever reported for GaAs FETs. Power output is stable to within 2% over 167 hours of continuous operation. Also at 9.7 GHz CW the planar fully ion-implanted devices exhibited a power density of 2.9 W per mm of gate width, about twice the highest GaAs FET value.

INTRODUCTION
Recent results on InP MISFETs (1-3) have demonstrated that these devices are very attractive for high frequency power applications. Table I lists a number of advantages of these structures as compared to GaAs FETs. The peak electron drift velocity in InP is approximately 2.2 \times 10^7 cm/sec. as compared to a 1.7 \times 10^7 cm/sec. in GaAs (3). The thermal conductivity of InP is 0.7 W/cm°C compared to 0.5 for GaAs (3). The breakdown field in InP is 530 kV/cm (4) compared to 390 in GaAs (5) for a=10^{-4} cm\textsuperscript{2}. The gate insulator in a MISFET structure constitutes a physical barrier against gate metal diffusion into the channel, an aspect which could prove beneficial in relation to device lifetime and reliability. The gate insulator also makes possible large positive gate voltages, typically greater than 20 V without gate breakdown.

Another advantage of the insulated gate is that it makes possible carrier accumulation in the channel. From capacitance versus voltage measurements on MIS structures it can be seen that for zero gate voltage the InP surface is accumulated at the interface with the SiO\textsubscript{2} gate insulator. This charge accumulation provides the channel
with a carrier density greater than that provided by the doping alone and therefore may be beneficial with regard to mobility. A comparison between ungated channel saturation current before and after deposition of the gate insulator shows roughly a 30% current increase upon insulator deposition. This is presumably attributable to charge carrier accumulation. Of course the application of positive gate voltage will increase this accumulation effect.

The gate leakage current is much lower for an insulated gate device than for such structures as MESFETs, JFETs and heterojunction gate FETs. This gives the InP MISFET an important advantage over devices not having truly insulated gates, including InP MESFETs (6) which exhibit relatively high gate leakage and low source-drain breakdown voltage apparently as a result.

Together the advantages discussed thus far suggest that InP MISFETs should exhibit higher power output per unit gate width (power density) (1-3) than GaAs FETs, a prediction which has been experimentally verified. InP MISFETs (1-3) have demonstrated over three times the highest power density ever reported for GaAs FETs and because of their higher power densities these structures also promise much higher absolute power outputs than have been achieved with GaAs as soon as large enough devices are fabricated. While impressive results are being achieved with large gate width GaAs power MESFETs their low input impedance, which decreases with increasing gate width, leads to difficulties with their utilization in microwave systems (3) and limits the power achievable with such devices. This situation might be greatly improved by the use of a different material or device such as the InP MISFET for instance with higher power density and therefore higher input impedance for a given power output (3).

Table II lists disadvantages of InP power MISFETs as compared to GaAs FETs as well as features not yet known to favor one material or device over the other. InP has a slightly lower bandgap (1.3 eV as compared to 1.4 eV for GaAs at 300 K) is somewhat less mechanically durable and has a lower dissociation temperature than GaAs. Under strictly dc conditions these devices exhibit drain current drift due to charging or discharging of states residing in the neighborhood of the semiconductor/gate-insulator interface. However, when epitaxial InP MISFETs are used as high-frequency amplifiers the drift in power output is
extremely slight. Apparently the presence of an rf signal has a stabilizing effect on the interface states.

In the following section we shall review results from this laboratory concerning InP power MISFET structure, fabrication and performance.

DEVICE PROCESSING

We fabricated two kinds of devices, mesa-type structures fabricated on epitaxial InP layers and planar fully ion-implanted structures. Figure 1 illustrates a schematic cross section of an epitaxial device, an n-channel depletion-mode structure fabricated on an n-type epilayer with an initial thickness of approximately 0.7 μm and a doping density between 5 × 10^{18} and 2 × 10^{17} cm^{-3}. Following mesa definition, alloyed AuGe contact formation and evaporated Au contact pad definition the channels were chemically recessed with a 10% solution of HIO in water to approximately 0.3 μm; the deep channel recess being important (3) for high-voltage high-power device operation.

Next the SiO₂ gate insulator was deposited to a thickness of about 1000 angstroms using remote-plasma-assisted CVD (7) at a temperature of approximately 300 °C using a gas mixture of SiH₄, O₂ and as a carrier gas N₂. Al gates with a thickness of 0.5 μm were then defined by evaporation and liftoff and finally bonding windows were opened in the SiO₂ layer. The source to drain spacing is approximately 4.5 μm and the gate length around 1.4 μm.

Figure 2 shows a cross-sectional representation of a typical ion-implanted device, an n-channel depletion-mode structure fabricated by implanting directly into a substrate of Fe-doped semi-insulating InP having a resistivity of >10⁷ ohm-cm. Contact regions selectively receive a multiple energy n⁺ implant of Si ions using energies ranging from 40 to 360 keV and doses in the range 3 × 10^{13} cm⁻² to 6 × 10^{14} cm⁻². The implant schedule is intended to produce a high-density relatively flat carrier profile from close to the surface to a depth great enough to provide a thorough contact to the implanted channel. High carrier density near the surface may be important for good ohmic contact formation. The precise schedule used is listed in figure 3 which illustrates the implanted impurity density versus depth (assuming Gaussian distributions with their first two moments predicted using Linhard, Scharff, Schiot (LSS) theory) resulting from each
individual energy implant as well as the total predicted density. Also shown in this figure are the results of an electrochemical carrier density profile measurement performed with a Polaron profiler on a semi-insulating Fe-doped InP control wafer which had been implanted with the specified schedule and then activated.

The channel region selectively receives a multiple energy n-type implant of Si which overlaps the n+ contact implanted regions for electrical continuity. Channel implant energies range from 60 to 360 keV with doses from $1 \times 10^{12}$ to $1.5 \times 10^{13} \text{ cm}^{-2}$. In this case the schedule is intended to produce a carrier density in the low $10^{11} \text{ cm}^{-3}$ range with as flat as possible a carrier profile from fairly close to the surface to a depth as great as possible with the maximum implantation energy available to us at the time (360 keV) falling off as abruptly as possible beyond such depth. Carrier density very near the surface is not critical in the channel region since, under the gate, approximately the first 0.3 μm of material is removed in the channel recessing fabrication step. A typical channel implant schedule, the corresponding predicted Si densities versus depth and measured resulting carrier density in an activated control wafer versus depth are shown in figure 4. After implantation the wafers are capped with approximately 2000 angstroms of SiO₂ and then annealed in forming gas at 725 °C for 60 seconds to electrically activate the implant. This activation recipe produced activations of ≈80% and mobilities ≈2000 cm² V⁻¹ sec⁻¹ in Fe-doped InP test wafers which had received 50 keV Si implant doses of $5 \times 10^{12} \text{ cm}^{-2}$.

Figure 5 illustrates one of the device geometries we used for the mesa-type expitaxial devices. For the sake of simplicity and clarity only the ohmic contact and gate metallization regions are shown. The areas marked “D” are isolated drain regions which must be individually wire bonded. The eight individual gate fingers are each 125 μm wide resulting in a total device gate width of 1 mm. Three other similar geometries with from three to five drain regions and from 750 μm to 1 mm total gate widths were also used. The geometries of the implanted devices were basically the same as those of the epitaxial structures.
RESULTS

Figure 6 shows an oscilloscope photograph of the drain characteristics of a representative 1 mm wide epitaxial device with a saturation current of approximately 660 mA per mm of gate width for a gate to source voltage of zero volts. The gate voltage is applied in 80 microsecond pulses. Figure 7 shows the drain characteristics of a typical implanted device.

Table III compares 8-10 GHz CW performance data for implanted and epitaxial InP MISFETs and the best ever reported GaAs FETs (8). The highest power per unit gate width at 4 dB gain for the epitaxial InP devices is 4.5 W/mm, over three times the highest value ever reported for a GaAs FET. The implanted InP MISFETs yielded about twice the best GaAs power density.

As was pointed out for epitaxial devices by Armand, et al. (3), the high power densities of both the InP structures are largely attributable to their high drain bias current per unit gate width, in this case around 330 mA/mm as compared to 127 mA/mm for GaAs (8). This high current per unit gate width arises from the high peak electron drift velocity in InP, the high product of channel thickness and doping density in these devices and from charge carrier accumulation in the channel.

The relatively inferior performance of implanted devices compared to epitaxial devices might be due, at least in part, to the transition between the semi-insulating substrate and the channel being inherently less abrupt in implanted structures as compared to epitaxial ones. Because of this at least part of the implanted channel has a lower than ideal doping density. Another partial cause might be the presence of Fe in device channels formed by direct implantation into the Fe-doped substrate. Possibly just a schedule including a deeper, higher-energy implant might effect an improvement by making possible a deeper channel recess. An advantage of implanted devices, however, is the greater ease, economy and reproducibility with which devices not requiring an epitaxial growth process can be fabricated and monolithically integrated with other devices.

Figure 8 illustrates at 9.7 GHz CW, for the same epitaxial InP MISFET as referred to in Table III, the dependence of power output, power-added efficiency and power gain on drain bias voltage and rf power input.
Optimum values of gate bias varied widely between devices while its effect on device performance was relatively small.

Figure 9 illustrates at the same frequency for a different device the variation of power output as a function of rf power input at a fixed drain bias voltage of 7.5 V; the power gain being 6.8 dB at 20.5 dBm power input. This value of power gain is typical of these devices at this rf power input and drain bias level.

Figure 9 also illustrates that the drain bias current for fixed gate and drain bias voltages is a decreasing function of rf power input (1,3). This effect appears to be due to the influence of the rf voltage applied to the MIS gate on the charge status of states residing in the neighborhood of the semiconductor/gate-insulator interface giving rise to an average channel depletion depth which decreases with increasing rf input power. Consequently, when these devices are operated at high drain bias voltage with no average current limit on the bias supply a large reduction in the rf power input will increase the drain bias current as well as reduce the amount of dc power converted to rf. The device will then have more dc power to dissipate and thermal breakdown will result. For this reason safe operation at high drain bias voltage requires either that the rf input be maintained at a high level (1,3) or that the average drain current be limited. This effect, however, would present no problem for certain applications, for instance applications which don't necessarily require dc power to the device while the rf input is shut off, for example certain radar applications which only require pulses of constant rf power.

Figure 10 illustrates the time dependence of the power output and drain bias current of a representative epitaxial device with its dc drain bias voltage and its rf power input held constant, elapsed time equaling zero when these are first applied. For this device the power output was stable to within 2% over 167 hours of continuous operation despite a 10% drain bias current downward drift.
CONCLUSION

Table IV summarizes the best InP power MISFET results, which are for the epitaxial devices. Power output at 9.7 GHz CW with 4 dB gain is 4.5 W. The power density is 4.5 W/mm, over three times as much as ever reported for a GaAs FET. Maximum power-added efficiency observed is 50% and the power output is stable to within 2% over approximately one week of continuous operation, which is the longest we've looked at these devices so far.

In conclusion, InP power MISFETs promise to substantially advance high frequency power amplification beyond the capabilities of GaAs FETs.

ACKNOWLEDGEMENTS

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REFERENCES


InP POWER MISFET
ADVANTAGES OVER GaAs

HIGHER ELECTRON PEAK VELOCITY
HIGHER THERMAL CONDUCTIVITY
HIGHER BREAKDOWN FIELD
GATE-INSULATOR PREVENTS GATE METAL-DIFFUSION INTO CHANNEL
LARGE POSITIVE FIELD APPLICABLE TO INSULATED GATE
ACCUMULATION IN CHANNEL: (INCREASED CARRIER DENSITY WITHOUT INCREASED DOPING DENSITY)
LOWER GATE LEAKAGE CURRENT
HIGHER POWER PER UNIT GATE WIDTH (POWER DENSITY)
POTENTIALLY HIGHER POWER
HIGHER INPUT IMPEDANCE

Table I. Advantages of InP power MISFETs over GaAs.

InP POWER MISFET
DISADVANTAGES COMPARED TO GaAs

LOWER BANDGAP
LOWER HARDNESS
LOWER DISASSOCIATION TEMPERATURE
CURRENT INSTABILITY (DRIFT)

UNDECIDED FEATURES

ELECTRON VELOCITY OVERSHOOT
NOISE

Table II. InP disadvantages and undecided features.
Figure 1. Mesa-type epitaxial InP power MISFET schematic cross-section.

Figure 2. Planar fully ion-implanted InP power MISFET schematic cross-section.
Figure 3. Contact $n^+$ Si implant data, predicted impurity density vs. depth for each individual implant, total predicted impurity density and carrier density measured on a test sample.
<table>
<thead>
<tr>
<th>Energy (keV)</th>
<th>Dose (cm(^{-2}))</th>
<th>Range ((\mu m))</th>
<th>Std. Dev. ((\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>360</td>
<td>1.1E13</td>
<td>0.355</td>
<td>0.126</td>
</tr>
<tr>
<td>220</td>
<td>7.0E12</td>
<td>0.215</td>
<td>0.091</td>
</tr>
<tr>
<td>120</td>
<td>4.0E12</td>
<td>0.115</td>
<td>0.057</td>
</tr>
<tr>
<td>60</td>
<td>2.0E12</td>
<td>0.056</td>
<td>0.032</td>
</tr>
</tbody>
</table>

Figure 4. Typical channel n-type Si implant data, predicted impurity densities vs. depth for each individual energy implant, total predicted impurity density and carrier density measured on test sample.
Figure 5. Epitaxial InP power MISFET geometry. For clarity only the contact n+ implant and gate metallization regions are shown. Areas marked 'D' are isolated drain regions requiring individual wire bonds. Implanted device geometries were basically the same.

<table>
<thead>
<tr>
<th></th>
<th>Implanted InP MISFET</th>
<th>Epitaxial InP MISFET</th>
<th>Best GaAs MESFET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency</strong></td>
<td>9.7 GHz</td>
<td>9.7 GHz</td>
<td>8 GHz</td>
</tr>
<tr>
<td><strong>Gate Width</strong></td>
<td>0.80 mm</td>
<td>1.0 mm</td>
<td>1.2 mm</td>
</tr>
<tr>
<td><strong>$V_{DS}$</strong> At Max Power Output</td>
<td>16.3 V</td>
<td>18 V</td>
<td>18 V</td>
</tr>
<tr>
<td><strong>$V_{GS}$</strong></td>
<td>-3.0 V</td>
<td>0 V</td>
<td></td>
</tr>
<tr>
<td><strong>$I_{DS}$</strong></td>
<td>269 mA</td>
<td>327 mA</td>
<td>152 mA</td>
</tr>
<tr>
<td><strong>Power Output (4 dB Gain)</strong></td>
<td>2.34 W</td>
<td>4.5 W</td>
<td>1.7 W</td>
</tr>
<tr>
<td><strong>Power-Added Efficiency</strong></td>
<td>31%</td>
<td>46%</td>
<td>37%</td>
</tr>
<tr>
<td><strong>$I_{DS}$/Gate Width</strong></td>
<td>336 mA/mm</td>
<td>327 mA/mm</td>
<td>127 mA/mm</td>
</tr>
<tr>
<td><strong>Power Output/Gate Width</strong></td>
<td>2.9 W/mm</td>
<td>4.5 W/mm</td>
<td>1.4 W/mm</td>
</tr>
</tbody>
</table>

*3.7 dB Gain

Table III. CW power FET technology comparison.
Figure 6. Drain characteristics of a representative 1 mm wide epitaxial InP depletion-mode power MISFET. 100 mA per major vertical division, 500 mV per major horizontal division, 2 V per step.

Figure 7. Drain characteristics of a representative 1 mm wide implanted InP depletion-mode power MISFET. 100 mA per major vertical division, 500 mV per major horizontal division, 2 V per step.
Figure 8. Dependence of power output, power-added efficiency and power gain on drain bias voltage and rf power input for a 1 mm gate width epitaxial InP MISFET. Implanted devices exhibited similar behavior.
Figure 9. Dependence of power output and drain bias current on rf power input for a representative epitaxial InP MISFET.

Figure 10. Time dependence of the power output and drain bias current of a representative 750 m wide epitaxial InP power MISFET with $V_{DS}=9.5$ V, $V_{GS}=-7.5$ V and an input rf power of 0.75 W/mm, all held constant, elapsed time equaling zero when these were first applied.
SUMMARY OF RESULTS

POWER OUTPUT 4.5 W AT 9.7 GHz CW WITH 4 dB GAIN

POWER DENSITY 4.5 WATTS PER MILLIMETER (OVER 3 TIMES THE HIGHEST GaAs VALUE)

POWER-ADDED EFFICIENCY AS HIGH AS 50%

POWER OUTPUT STABLE TO WITHIN 2% OVER 167 HOURS OF CONTINUOUS OPERATION

Table IV. Summary of the best InP power MISFET results, which are for the epitaxial devices.