AUTOMATED SEMICONDUCTOR MODELING

JOHN P. TOBAK

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U. S. ARMY ARMAMENT RESEARCH, DEVELOPMENT AND ENGINEERING CENTER
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INTRODUCTION

The circuit and systems analysis program SUPER*SCEPTRE is a powerful and highly interdisciplinary simulation language. Among its various attributes is its ability to utilize user defined models as circuit or system elements. This report describes a procedure for automating the creation of diode and bipolar transistor (NPN) models used by SUPER*SCEPTRE. While the final models generated appear in SUPER*SCEPTRE format, they can be easily adapted to the format of any nonlinear circuit simulation program. The modeling procedure mentioned begins with the acquisition of semiconductor data by means of an automated test setup. The setup is controlled by a Hewlett Packard 9816S microcomputer in concert with an H.P. 4145B semiconductor parameter analyzer. The data is then transformed by the 9816S into a SUPER*SCEPTRE model. A discussion of the parameters used to describe each model will first be presented followed by a description of the test configurations used to collect parameter data.

DIODE MODEL

The diode model for which the following parameters will be developed is taken from reference 1 and appears in figure 1. Diode model parameter definitions are:

CD = The sum of the diode transition and diffusion capacitances where:

\[
\text{Transition capacitance} = \frac{\text{Co}}{(\text{PHI}-V_{\text{CD}})^N} = \text{C}_J
\]

and

\[
\text{Diffusion capacitance} = \text{KD} (\text{JD} + I_S)
\]

JD = Current generator representing the diode junction current. This generator is a function of the voltage \( V_{\text{CD}} \).

\[
\text{JD} = I_S \left[ \text{EXP}(\text{Theta} \times V_{\text{CD}}) - 1 \right]
\]

I_S = Diode reverse saturation current

Theta = Constant of the diode equation

RB = Diode bulk resistance

Co = Constant of the transition capacitance equation

PHI = Junction contact potential

N = Junction grading constant

KD = Diffusion capacitance constant = \( \frac{\text{Theta}}{(6.28 F)} \)

F = Frequency parameter
\[ V_{CD} = \text{Voltage across capacitor } CD, \text{ which is equal to the diode junction voltage} \]

**Diode Equation Constant and Reverse Saturation Current**

The diode equation constant \( \Theta \) is defined as

\[
\Theta = \frac{q}{(kT)}
\]

where \( q \) is the charge of an electron, \( k \) is Boltzman's constant, and \( T \) is the diode's junction temperature in Kelvins. \( \Theta \) is obtained from the diode junction's measured forward biased characteristic and the assumption that the characteristic can be closely approximated by

\[
J_D = I_S \exp (\Theta V_{CD})
\]

where \( I_S \) represents the diode's saturation current and \( V_{CD} \) its forward junction voltage. Diode D's forward characteristic is measured by using figure 2. The forward junction current and the forward junction voltage are recorded by means of source/monitor units SMU3 and SMU1, respectively, for automatically varied current values of SMU1. Source/monitor units are an integral part of the HP4145B and act as either voltage sources and current monitors or current sources and voltage monitors. In this test, SMU1 consists of a current source in parallel with a voltage monitor, while SMU3 acts as a zero voltage source in series with a current monitor. Physical connections between the diode under test and the HP4145B take place by means of an HP16058A test fixture. The fixture and its connections for the diode case are depicted in appendix A. The typical range of measurements taken are shown in figure 3.

Once obtained, measured data is submitted by means of an HPIB (IEEE-488) interface to a computer program on the Hewlett Packard 9816s microcomputer. The program fits a curve of the form of equation 2 to the data yielding values for \( \Theta \) and \( I_S \). The curve fitting method used is described in appendix B. A comparison plot between typical measured data and its resulting fitted curve is shown in figure 4.

**Bulk Resistance**

Bulk resistance (RB) is obtained from the horizontal difference between the curves of figure 4 for high values of junction current. The migration of measured data to the right of the fitted diode equation is due to the forward voltage drop across RB and can be computed from figure 4 as,

\[
RB = \frac{V_{diff}}{I}
\]

The data used to fit the curve does not include the last few points of measured data. This is done to separate the effects of RB from the proper determination of parameters \( \Theta \) and \( I_S \) as well as legitimizing the calculation of RB by means of equation 3.
Leakage Resistance

Leakage resistance (RS) is obtained from the inverse slope of a curve fit (app B) of the diode's reverse leakage current versus its reverse bias voltage. The following is the assumed form to which the data is fitted:

\[ I = \frac{V}{RS} \]  \hspace{1cm} (4)

The circuit used to obtain the reverse bias data is demonstrated in figure 5. Voltage V is measured across SMU1 while current I is measured by SMU3. Except for the direction of the current generated by SMU1, figure 5 is identical to figure 2. The H.P. 9816S regulates the measurement taking procedure by applying typical currents on the order of a nanoampere and voltages as high as 40 volts.

Diffusion Capacitance Constant

Constant KD is obtained from storage time measurements collected using the circuit of figure 6. A periodic positive and negative pulse is applied to the diode's junction. Forward and reverse values of junction current (IF and IR, respectively) are recorded along with the time (t_s) needed for the junction to discharge and begin to recover to its steady state reverse saturation current (IS). The current seen through the scope monitored 100-ohm resistor is demonstrated in figure 7. A value for KD is obtained using the following equation (refs 1 and 2):

\[ KD = \Theta \left( \frac{t_s}{\frac{I_F}{I_R}} \right) \ln[1 + \left( \frac{I_F}{I_R} \right)] \]  \hspace{1cm} (5)

Transition Capacitance Equation Constants

Transition capacitance equation constants Co, PHI, and N are obtained from a curve fit of transition capacitance (CJ) measured as a function of reverse junction voltage. The H.P. 9816S driven circuit used to obtain the desired data is shown in figure 8. The bias voltage depicted is supplied by the 4145B as directed by the 9816S. Voltage and capacitance values as well as measurement taking instructions are transferred to and from the 9816S microcomputer by means of the HP-IB(IEEE-488) bus. The curve fitting procedure discussed in appendix B assumes the form of the transition capacitance to be

\[ CJ = \frac{Co}{(PHI-V_{CD})^N} \]  \hspace{1cm} (6)

where \( V_{CD} \) represents the diode's junction voltage. A comparison plot between typical values of measured capacitance and a curve fit of the measured data is shown in figure 9.
Diode Model for the 1N457

The procedures described in the previous sections were implemented in the development of the following model and circuit simulation:

MODEL DESCRIPTION
MODEL 1N457(1-3)
ELECTRICAL
CD,1-2=X1(2.3E-11/ABS(.8-VCD)**.874+1.96E-5*(JD+1.58E-10))
RB,2-3=3.45
RS,1-2=7.7E10
JD,1-2=DIODE Q(1.58E-10,22.72)
CIRCUIT DESCRIPTION
ELECTRICAL
R1,2-3=100
R2,5-3=47
E1,1-2=TABLE1
E2,1-5=3
D1,3-6=MODEL 1N457
RV,6-1=100
OUTPUTS
E1,VRV,IRV
CDD1,VCD1
FUNCTIONS
TABLE1
0,4,1E-6,4,1E-6,-7,5E-6,-7
RUN CONTROLS
INTEGRATION ROUTINE=IMPLICIT
RUN INITIAL CONDITIONS
MAX INTEGRATION PASSES = 1E30
MINIMUM STEP SIZE = 1E-30
COMPUTER TIME LIMIT = 1
STOP TIME = 5E-6
END
*END
8

The resulting output appears in figure 10. The results closely match the measured data depicted by figure 7. The only discrepancy is the time needed for the diode current to go to zero after its junction becomes reverse biased. The difference occurs because the model does not include capacitances which exist throughout other parts of the circuit.

TRANSISTOR MODEL

The SCEPTRE transistor model (NPN) to be used is based on the Ebers-Moll model (ref 1) and appears in figure 11. The model parameters are defined as:
\[
CE = \frac{C_{OE}}{(\Phi_{E} - V_{CE})^{N_{E}}} + \Theta_{E} T_{E}(JE + IE_{S})
\]

Emitter transition capacitance  
Emitter diffusion capacitance

\[
CE = \frac{C_{OC}}{(\Phi_{C} - V_{CC})^{N_{C}}} + \Theta_{C} T_{S}(JC + IC_{S})
\]

Collector transition capacitance  
Collector diffusion capacitance

\(C_{OE}\) = Constant of the emitter transition capacitance equation
\(C_{OC}\) = Constant of the collector transition capacitance equation
\(\Phi_{E}\) = Emitter base junction contact potential
\(\Phi_{C}\) = Collector base junction contact potential
\(JE\) = Current generator representing the emitter base junction
\(JC\) = Current generator representing the collector base junction
\(JE = IE_{S}[\exp(\Theta_{E} V_{CE}) - 1]\)
\(JC = IC_{S}[\exp(\Theta_{C} V_{CC}) - 1]\)
\(N_{E}\) = Emitter junction grading constant
\(N_{C}\) = Collector junction grading constant
\(JN\) = Current generator dependent on the emitter base junction current
\(JN = \alpha_{N} JE\)
\(JI\) = Current generator dependent on the collector base junction current
\(JI = \alpha_{I} JC\)
\(IE_{S}\) = Emitter-base saturation current measured in the active region
\(IC_{S}\) = Collector-base saturation current measured in the active region
\(\Theta_{E}\) = Constant of the emitter base junction equation
\(\Theta_{C}\) = Constant of the collector base junction equation
\(TE\) = Time constant of the emitter diffusion capacitance equation
\[ TE = \frac{1}{6.28 \ F_N} \]

\[ TS = \text{Time constant of the collector diffusion capacitance equation} \]

\[ TS = \frac{1}{6.28 \ F_I} \]

\[ F_N = \text{The average } f_r^N \text{ normal} \]

\[ F_I = \text{The average } f_r^I \text{ inverse} \]

\[ TCI = \text{Charge control parameter related to storage time} \]

\[ \alpha_N = \text{Forward current gain} = \frac{I_C}{I_E} \]

\[ \alpha_N \text{ is entered as a function of } J_E \text{ in the SCEPTRE model.} \]

\[ \alpha_I = \text{Inverse current gain} = \frac{I_E}{I_C} \]

\[ \alpha_I \text{ is entered as a function of } J_C \text{ in the SCEPTRE model.} \]

\[ R_B = \text{Base bulk resistance} \]

\[ R_C = \text{Collector bulk resistance} \]

\[ R_{1} = \text{Emitter-base junction leakage resistance} \]

\[ R_{2} = \text{Collector-base junction leakage resistance} \]

**Junction Constants and Saturation Currents**

Constants \( \Theta_E \) and \( \Theta_C \) represent values for the base-to-emitter and base-to-collector junction constants, respectively. Similarly, parameters \( \theta_E^S \) and \( \theta_C^S \) represent base-to-emitter and base-to-collector saturation currents. These values are determined in the same way as in the diode case. The test setup used to obtain the forward characteristic of the base-to-emitter junction is shown in figure 12, while the circuit used to obtain the characteristic of the base-to-collector junction is depicted in figure 13. An active region collector-to-emitter voltage on the order of that seen by the transistor during application should be applied by SMU2 during this test. In this test, SMU2 acts as a voltage source in series with a current monitor. Physical connections between the transistor under test and the HP4145B take place by means of an HP16058A test fixture. The fixture and its connections for the transistor case are depicted in appendix A.
Forward and Inverse Current Gains

Forward current gain ($\alpha_N$) and inverse current gain ($\alpha_I$) are defined by reference 1 as follows:

$$\alpha_N = \frac{I_C}{I_E} \quad \text{and} \quad \alpha_I = \frac{I_E}{I_C} \quad (7 \text{ and } 8)$$

$\alpha_N$ is obtained from the data measured by the circuit of figure 12 while determination of $\alpha_I$ is based on the results of the test setup of figure 13. $\alpha_N$ and $\alpha_I$ are determined for different values of $I_E$ and $I_C$, respectively, allowing them to be described within the model in a tabular way as functions of current.

Emitter and Collector Transition Capacitances

As with the junction constants and saturation currents previously discussed, the emitter and collector transition capacitance parameters ($N_E$, $C_{OE}$, $PHI_E$, $N_C$, $C_{OC}$, $PHI_C$) are also determined as in the diode case. The test circuits for each junction appear in figures 14 and 15.

Base and Collector Bulk Resistance

Bulk resistance ($R_B$) is obtained from the base-to-emitter forward characteristic. Its determination is the same as in the diode case. Collector bulk resistance will be assumed to be typically on the order of 1 ohm. A more precise value for $R_C$ can be obtained by methods described in reference 1.

Junction Leakage Resistances

The base-to-emitter leakage resistance ($R_1$) and collector-to-base leakage resistance ($R_2$) are obtained from the junction reverse bias characteristics. The procedure is the same as in the diode case. The test setups used are described in figures 16 and 17. In these cases, SMU1 acts as a current source and voltmeter while SMU3 supplies a voltage of zero and measures the junction's current.

Time Constant of the Emitter Diffusion Capacitance Equation

Parameter $TE$ is the emitter diffusion time constant and is introduced in an attempt to describe, in terms of a time constant, the capacitive effect which is observed in the transistor's emitter junction as a function of forward base-to-emitter voltage. The development of such a relationship begins by expressing junction voltage in terms of parameter $TE$. This is done by equating the exponential product of $\Theta_{FE}$ and $VC_{PE}$ of the equation for current generator $JE$ to the familiar exponential term of time divided by some time constant. In this case, the time constant will be called $TE$ and will produce the following expression for junction voltage:

$$VC_{PE} = \frac{t}{\Theta_{FE} TE} \quad (9)$$
An expression for the emitter diffusion capacitance (CED) as a function of TE can now be developed. Since capacitance is defined as

\[ C = \frac{1}{\frac{dV}{dt}} \]  

(10)

the derivative of equation 9 with respect to time can be substituted into equation 10 yielding the following expression for capacitance CED:

\[ \text{CED} = \frac{I_{CE_D}}{\Theta_E \cdot \text{TE}} = \text{Theta}_E \cdot \text{TE} \cdot (JE + IE_S) \]  

(11)

The above expression describes the relationship between capacitance CED and parameter TE. Values for CED can now be determined once parameter TE is defined. With this in mind, an expression for TE is next developed from the charge voltage relationship across capacitor CED. Starting with the charge voltage relationship across a capacitor

\[ Q_E = CED \cdot V_{CED} \]  

(12)

where \( Q_E \) is the charge on the junction diffusion capacitance CED with voltage \( V_{CED} \) across it. Since a determination of TE would be most desirable in terms of emitter current, it is necessary to rewrite equation 12 as follows:

\[ Q_E = CED \cdot I_E \cdot RE \]  

(13)

where \( I_E \) is the emitter current of the transistor and \( RE \) is the equivalent emitter junction resistance seen by current generator JE and dimensionally equal to \( 1/\text{Theta}_E(JE + IE_S) \). Differentiating both sides of equation 13 with respect to \( I_E \) yields

\[ \frac{dQ_E}{dI_E} = CED \cdot \frac{IE}{\text{Theta}_E(JE + IE_S)} = \text{TE} \]  

(14)

The term \( \frac{dQ_E}{dI_E} \) has the units of a time constant and can be seen from equation 11 to be equal to the emitter diffusion time constant TE. Through the use of this definition and the equation of charge continuity (eq 15), an expression for TE can be developed in terms of emitter current and time

\[ I_E = \frac{dQ_E}{dt} + \frac{Q_E}{\text{B}} \]  

(15)
The above equation states that the base current of the transistor is made up of the recombination of excess carriers every \( \lambda_B \) seconds and the time varying change in excess carrier distribution. By separating variables and then inverting each side of the equation,

\[
\frac{1}{I_B} = \frac{\text{d}t}{Q_B} \frac{\text{d}Q_E}{\lambda_B}
\]

By multiplying through by \( \text{d}I_E \), substituting \( \frac{\text{d}Q_E}{\text{d}t} \) for \( \text{d}I_E \) on the right side of the equation, and then integrating, a solution for \( \text{TE} \) in terms of \( I_E \) can be obtained as follows:

\[
\begin{align*}
\frac{73\% I_E}{27\% I_E} & = \left( \frac{\text{d}I_E}{\text{d}Q_E} \right) = \left( \frac{\text{d}t}{\lambda_B} \right) \frac{\text{d}Q_E}{\text{d}t} = \left( \frac{\text{d}t}{\text{TE}} \right) \\
\text{TE} & = \frac{\text{d}t}{\lambda_B} \\
\end{align*}
\]

Limit \( t_r \) represents the time it takes for the emitter current to rise from 27% to 73% of its final value. \( I_B \) is assumed to go from zero to \( I_{BL} \) in a stepwise manner. Since \( \frac{Q_B}{\lambda_B} \) represents the d.c. component of the base current, it can be substituted by the d.c. emitter current divided by \( \beta + 1 \) as follows:

\[
\frac{73\% I_E}{27\% I_E} = \left( \frac{\text{d}I_E}{\text{d}Q_E} \right) = \left( \frac{\text{d}t}{\lambda_B} \right) \frac{\text{d}Q_E}{\text{d}t} = \left( \frac{\text{d}t}{\text{TE}} \right) \\
\beta = \frac{\text{d}t}{\text{TE}} (\beta + 1) I_{BL} - I_E
\]

\( \beta \) is the average \( \beta \) for the 27% to 73% collector current transition experienced. Values of \( \beta \) for different values of collector current can be calculated from the \( \alpha_N \) results obtained from equation 7 and the following expression for \( \beta \).

\[
\beta = \frac{\alpha_N}{(1 - \alpha_N)}
\]

Integrating, the following is obtained:

\[
\frac{t_r}{\text{TE}} = -\ln[(\beta + 1) I_{BL} - I_E] \left( \frac{73\% I_E}{27\% I_E} \right)
\]

By evaluating equation 20 over the limits indicated and then substituting \( I_E \) for \( (\beta + 1) I_{BL} \), the following expression for \( \text{TE} \) can be developed:
Therefore, the value of TE for different saturation currents can be obtained by measuring the time necessary for the collector current or collector-to-emitter voltage of the transistor to go from 27% to 73% of its final value. Therefore, TE is expressed within the model in a tabular manner as a function of current generator JE and is obtained from the test setup of figure 18. An example of the oscilloscope trace generated by the test circuit of figure 18 is shown in figure 19.

**Time Constant of the Collector Diffusion Capacitance Equation**

The time constant (TS) of the collector diffusion capacitance equation is determined by observing the depletion of excess charge in the transistor's base region as it is brought out of saturation. By using the equation of charge continuity, reference 3 develops an expression for the transistor's storage time constant as a function of base current and collector saturation current. The expression is as follows:

\[
\lambda_s = \frac{dQ_{BS}}{df_B} = \frac{t_s}{\ln \left( \frac{I_{B1} - I_{B2}}{I_{C}/B - I_{B2}} \right)}
\]

(22)

In the above expression, \( I_{B1} \) represents the base current while the transistor is in saturation; \( I_{B2} \), the base current used to bring the transistor out of saturation; and \( I_C \), the collector saturation current. Parameter \( t_s \) is the storage time needed to deplete the base of excess charge carriers and begin to bring the transistor out of saturation. Values for \( I_{B1}, I_{B2}, \) and \( t_s \) can be obtained by using the circuit of figure 18. The method used to obtain a measurement for \( t_s \) is shown in figure 19. Parameter \( t_s \) is measured from the time when the transistor's base is at its minimum to the time its collector voltage reaches 10% of its final value. The 10% point of reference is used to make it easier to obtain a reading while introducing only a negligible amount of error into the measurement. The result of equation 22 and the inverse mode model components \( IC, CC, \) and \( JJ \) of figure 10 are used to explain saturation region behaviour and develop time constant TS in terms of current generator JC. TS is defined as:

\[
TS = \frac{dQ_{BS}}{df_B} = \frac{t_s}{\ln \left( \frac{I_{B1} - I_{B2}}{I_{C}/B - I_{B2}} \right)} \times \frac{\eta_I}{B_1}
\]

(23)

Parameters \( \lambda_s, \eta, I_C, \) and \( \eta_I \) are all functions of the operating point and are obtained by a SCEPTRE simulation (ref 1). The simulation consists primarily of a constant capacitance steady state model of the transistor which uses all of the parameters obtained up to this point. The model is excited in a common emitter
circuit at different values of collector current. The results produce values from which parameter $TS$ can be expressed in tabular form as a function of the model current generator $JC$.

A Transistor Model for the 2N2222

The procedures described in the previous sections were implemented in the development of a model for the 2N2222 transistor. Tabulated test results used in the determination of parameters $TE$ and $TS$ appear in Tables 1 and 2, respectively. A listing of the model and the SCEPTRE input used to simulate the circuit of figure 18 follow:

MODEL DESCRIPTION
MODEL 2N2222(B-E-C)
ELEMENTS
$CE,1=E=Q1(4.5E-11,.75,VCE,78,28,T3(JE),JE,2.2E-11)$
$CC,1-2=Q1(2.9E-11,.75,VCC,1.03,28.4,T4(1C),1C,2.8E-11)$
$RB,B=1=47$
$RC,C=2=5$
$R1,1-E=3.9E10$
$R2,1-2=1.1E10$
$JE,1-E=DIODE Q(2.2E-11,28)$
$JC,1-2=DIODE Q(2.8E-11,28.4)$
$JN,2-1=TABLE1(JE)*JE$
$JL,1-E=TABLE2(JC)*JC$
FUNCTIONS
$Q1(A,B,C,D,E,F,G,H)=(A/ABS(B-C)**D+E*F*(G+H))$
$TABLE1=0,.9925,5.4E-4,.9925,1.1E-3,.9928,2.35E-3,.9926,1.04E-2,$
$.9926,1.15E-2,.9913,1.37E-2,.992,2E-2,.992$
$TABLE2=0,.36E-2,.2,19E-6,.5,.36E-2,.267E-5,.1028,.5,.135E-5,.138n,$
$.8,.36E-5,.166,1.244E-4,.197,2.6E-4,.2615,3E-4,.2615$
$TABLE3=0,.5E-9,15E-3,.5E-9,20E-3,.42E-9,.40E-3,.5E-9,.40E-3,.813E-9,$
$.1,833E-9$
$TABLE4=0,105,7E-9,5.34E-4,105,7E-9,1.117E-3,1.17E-9,2.44E-1,58,5E-9$
$1.58,5E-9$
CIRCUIT DESCRIPTION
ELEMENTS
$R1,2=3=1E3$
$R2,5=4=100$
$E1,1-2=TABLE1$
$E2,1-5=4$
$T1,3-1=MODEL 2N2222$
$J1,4-1=0$
OUTPUTS
$V11,E1$
FUNCTIONS
$TABLE1$
$0,-1.6,1200E-9,-1.6,1280E-9,1.6,2480E-9,1.6,2520E-9,-1.6,2600E-9,-1.6$
RUN CONTROLS
INTEGRATION ROUTINE=IMPLICIT
RUN INITIAL CONDITIONS
MAX INTEGRATION PASSES = 1E30
MINIMUM STEP SIZE = 1E-30
COMPUTER TIME LIMIT = 1
STOP TIME = 4000E-9
END
*EOR
8
DBEND

Its resulting output appears in figure 20. The results closely match the measured data depicted by figure 19.

CONCLUSIONS

The results obtained in this report confirm the modeling procedures used by Mowers and Sedore and demonstrate a method for successfully automating those procedures using the Hewlett Packard 9816S microcomputer and 4145B semiconductor parameter analyzer.
Table 1. Transistor current rise time parameters for the 2N2222

<table>
<thead>
<tr>
<th>$I_C$ (mA)</th>
<th>$t_r$ (ns)</th>
<th>$T_F$ (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>100</td>
<td>120</td>
</tr>
<tr>
<td>30</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>20</td>
<td>50</td>
<td>120</td>
</tr>
<tr>
<td>15</td>
<td>60</td>
<td>120</td>
</tr>
</tbody>
</table>

Table 2. Transistor storage time parameters for the 2N2222

<table>
<thead>
<tr>
<th>$V_{CE}$ (V)</th>
<th>$V_B$ (V)</th>
<th>$I_{B1}$ (mA)</th>
<th>$I_{B2}$ (mA)</th>
<th>$I_{Cout}$ (mA)</th>
<th>$I_C$ (mA)</th>
<th>$t_s$ (ns)</th>
<th>$t_S$ (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>0.8</td>
<td>0.7</td>
<td>-2.3</td>
<td>40</td>
<td>0.53</td>
<td>20</td>
<td>1.05</td>
</tr>
<tr>
<td>2.0</td>
<td>0.8</td>
<td>1.2</td>
<td>-2.8</td>
<td>40</td>
<td>1.17</td>
<td>20</td>
<td>1.17</td>
</tr>
<tr>
<td>3.0</td>
<td>0.8</td>
<td>2.2</td>
<td>-3.8</td>
<td>40</td>
<td>2.44</td>
<td>30</td>
<td>58.8</td>
</tr>
</tbody>
</table>

$R_S = 124$  $R_I = 0.184$
Figure 1. SCEPTRE diode model

Figure 2. Forward diode characteristic test circuit
Figure 4. Curve fit of the forward characteristic of a 1N457
Figure 5. Reverse diode characteristic test circuit

Figure 6. Diffusion capacitance test circuit
15 ma - IF

2.5 mA/div vertical
500 ns/div horizontal

0.0
IR

-15 ma

\( t_s \)

3.0 \( \mu \)s

Figure 7. Diode (1N457) reverse recovery waveform from the test setup of the diffusion capacitance test circuit

\[ \text{BIAS VOLTAGE} \]

\[ \text{LCR METER} \]

\[ D \]

Figure 8. Transition capacitance test circuit
Figure 9. Transition capacitance of diode IN457 as a function of reverse function voltage.
Figure 10. Simulated diode current of the diffusion capacitance test circuit
Figure 11. SCEPTRE NPN transistor model
Figure 13. Base-to-emitter forward characteristic test

Figure 13. Base-to-collector forward characteristic test
Figure 14. Base-to-emitter transition capacitance test circuit

Figure 15. Base-to-collector transition capacitance test circuit
Figure 16. Base-to-emitter reverse characteristic test setup

Figure 17. Base-to-collector reverse characteristic test setup
Figure 18. Rise time test circuit

Figure 19. Oscilloscope output of rise time test circuit
REFERENCES


APPENDIX A

HP16058A TEST FIXTURE LAYOUTS AND EQUIPMENT LIST
Physical connections between the devices under test and the HP4145B semiconductor parameter analyzer are discussed in this appendix. Connections are made through the use of an HP1605BA test fixture. The wiring layouts used in the diode and transistor tests are demonstrated in figures A-1 and A-2. A general list of the equipment used in this report is shown in table A-1.

While acting as an interface between the HP4145B and the device under test (DUT), the test fixture also provides a means of easily modifying circuit connections with the use of a connection switch. The switch in figures A-1 and A-2 connects the center column nodes (COMM) to the nodes of either columns 1 or 2.

When performing diode related tests, the layout of figure A-1 is used. The connection switch is moved to position 1 when the diode's forward characteristic and leakage resistance are being determined. The switch is moved into position 2 when transition capacitance tests are being performed, but the diode must be removed from the test fixture in this case and connected directly to the LCR meter.

Transistor tests are made using the layout of figure A-2. Once again, the connection switch is used to modify test procedures without disturbing the test fixture. The switch is placed in position 1 when performing the forward NORMAL mode characteristic test and in position 2 when determining the INVERSE mode characteristic. Transition capacitance tests are made using the layout of figure A-1 while remembering that the diode depicted represents the transistor junction under test. Junction leakage resistance tests use the layout of figure A-2 with modifications stipulated by base-to-emitter and base-to-collector reverse characteristic test setups described earlier in this report.
Table A-1. Equipment list

1. Hewlett Packard 9816S microcomputer.
2. Hewlett Packard 4145B semiconductor parameter analyzer.
3. Hewlett Packard 4262A LCR meter.
4. Lambda LE103 FM power supply.
5. Tektronix 5441 storage oscilloscope.
6. Tektronix FG504 function generator.
Figure A-1. Test fixture (H.P. 16058A) diode layout
Figure A-2. Test fixture (H.P. 16058A) transistor layout
APPENDIX B

LEAST-SQUARES CURVE FITTING
The curve fitting method used in this report is known as the least-squares method.* It is based upon the concept that the best line fitted to a set of data points is the one for which the sum of the squares of the deviations between the points and the line is a minimum.

The deviations are squared to eliminate the possible cancelling of positive and negative deviations at different points which could give a false impression of a good fit.

This report maps all of the expressions to be used for fitting purposes to the form of the straight line, \( Y = A + BX \). The sum of the squares of the deviations may be expressed as

\[
\sum (y_c - y_o)^2 = \sum (A + Bx_o - y_o)^2 \tag{B-1}
\]

where \( y_c = A + Bx_o \) is the calculated ordinate for the value of \( x = x_o \).

The values of the constants, \( A \) and \( B \), for which this expression is a minimum may be determined by finding the partial differentiation of equation B-1 with respect to each constant and then setting it equal to zero.

For \( A \):

\[
\frac{\partial}{\partial A} (A + Bx_o - y_o)^2 = 0
\]

\[
2 \cdot y_o - (A + Bx_o - y_o) = 0
\]

\[
(A + Bx_o - y_o) = 0
\]

For \( B \):

\[
\frac{\partial}{\partial B} (A + Bx_o - y_o)^2 = 0
\]

\[
2 \cdot B \cdot x_o + Bx_o^2 - x_o y_o = 0
\]

\[
(Ax_o + Bx_o^2 - x_o y_o) = 0
\]

These two equations can be solved simultaneously for unique values of the quantities \( A \) and \( B \) since values of \( x_o \) and \( y_o \) are available from the original data. The two equations may be written in the form:

* Barnas, Robert E., *Cuvit II - A Curve Fitting Program with Plotting Options*, Management Information Systems Directorate, Picatinny Arsenal, Dover, NJ.
\[
\overline{y_0} = \overline{A} + \overline{Bx_0}
\]

\[
\overline{x_0y_0} = \overline{Ax_0} + \overline{Bx_0^2}
\]

Factoring A and B from the terms gives

\[
\overline{y_0} = N \overline{A} + B \overline{x_0}
\]

\[
\overline{y_0x_0} = A \overline{x_0} + B \overline{x_0^2}
\]

where \(N\) = number of data points and finally

\[
A = \frac{\overline{x_0} \overline{x_0y_0} - \overline{y_0} \overline{x_0^2}}{(\overline{x_0})^2 - N \overline{x_0^2}}
\]

\[
B = \frac{\overline{y_0} \overline{x_0} - N \overline{x_0y_0}}{(\overline{x_0})^2 - N \overline{x_0^2}}
\]

The manner in which assumed data forms were mapped into the straight line form is described in table B-1.
Table B-1. Straight line equation mappings used in the least-squares fit of semiconductor data

<table>
<thead>
<tr>
<th>Equation no.</th>
<th>Original form</th>
<th>Desired form</th>
<th>Mapping</th>
</tr>
</thead>
</table>
| 2            | $I = I_S \exp(\Theta V_{CD})$ | $Y = A + BX$ | $Y = \ln(I)$  
               |               |              | $A = \ln(I_S)$  
               |               |              | $B = \Theta$  
               |               |              | $X = V$ |
| 4            | $I = \frac{V}{RS}$ | $Y = A + BX$ | $Y = I$  
               |               |              | $A = 0$  
               |               |              | $B = \frac{1}{RS}$  
               |               |              | $X = V$ |
| 6            | $C_J = \frac{Co}{((\Phi - V_J)^N)}$ | $Y = A + BX$ | $Y = \ln(C_J)$  
               |               |              | $A = \ln(Co)$  
               |               |              | $B = -N$  
               |               |              | $X = \ln(\Phi - V_J)$ |
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