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SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
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UNCLASSIFIED AFHRL-TR-80-42-PT-2 NL

1 OF 4
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AFHRL-TR-80-42 (Part II)

LEVEL II

(12)

AIR FORCE

HUMAN RESOURCES

SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER SYSTEMS

By

S. J. Clymer
Systems Division
Teledyne Brown Engineering
300 Sparkman Drive
Huntsville, Alabama 35807

OPERATIONS TRAINING DIVISION
Williams Air Force Base, Arizona 85224

February 1981

Final Report

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LABORATORY

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AIR FORCE SYSTEMS COMMAND
BROOKS AIR FORCE BASE, TEXAS 78235

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This final report was submitted by Systems Division, Teledyne Brown Engineering, 300 Sparkman Drive, Huntsville, Alabama 35807, under Contract F33615-78-C-0013, Project 6114, with the Operations Training Division, Air Force Human Resources Laboratory (AFSC), Williams Air Force Base, Arizona 85224. Pat Price was the Contract Monitor for the Labortory.

This report has been reviewed by the Office of Public Affairs (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

MARTY R. ROCKWAY, Technical Director
Operations Training Division

RONALD W. TERRY, Colonel, USAF
Commander

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This report consists of two parts. Part I includes pages 1 through 152. Part II contains pages 153 through 460.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

multiple processors
software partitioning
real-time computational design evaluation
flight simulation
data base management
software design
computer systems

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The overall objective of this study was to design software partitioning techniques that can be used by the Air Force to partition a large flight simulator program for optimal execution on alternative configurations. The results were a mathematical model which defines characteristics for an optimal partition and a manually demonstrated partitioning algorithm design which implements heuristic controls based on the mathematical model statement.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

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APPENDIX C.

FEASIBILITY DEMONSTRATION

Accession For
NTIS GRA&I ☒
DTIC TAB ☐
Unannounced ☐
Justification
By
Distribution/
Availability Codes
A

C.1 VIEWGRAPHS

FINAL BRIEFING

Software Partitioning Schemes

for

Advanced Simulation Computer Systems

CONTRACT F 33615-78-C-0013

CDRL ITEM 6

Prepared by

TELEDYNE BROWN ENGINEERING

AGENDA

- PROJECT SUMMARY
  - SCHEDULE AND APPROACH OBJECTIVES
  - DESIGN GOALS AND ALTERNATIVES
  - RESULTS
- PARTITIONING ALGORITHM DESIGN
  - ORGANIZATION OF DESIGN MATERIALS
  - FEASIBILITY DEMONSTRATION
  - DETAILED DESIGN REVIEW

PROJECT SUMMARY

⇒ ● SCHEDULE AND APPROACH OBJECTIVES

- PROJECT OBJECTIVES
- MILESTONE SCHEDULE
- LITERATURE SEARCH
- FLIGHT TRAINER ANALYSIS
- DESIGN

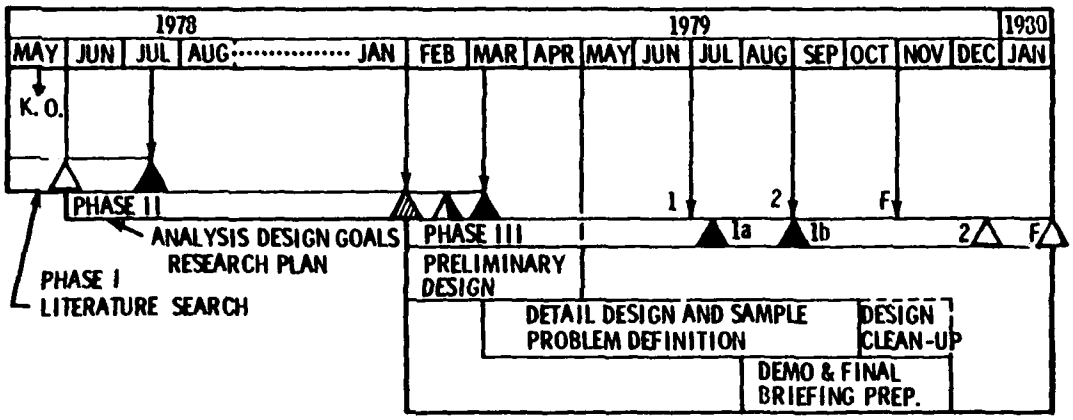
● DESIGN GOALS AND ALTERNATIVES

● RESULTS AND RECOMMENDATIONS

PROJECT OBJECTIVES

- RESEARCH FLIGHT TRAINING SIMULATORS
- ANALYZE FLIGHT TRAINING SIMULATORS
- DESIGN A SOFTWARE PARTITIONING ALGORITHM TAILORED TO FLIGHT TRAINING SIMULATOR PROBLEMS
- DEMONSTRATE THE ALGORITHM'S CAPABILITIES
- RECOMMEND UTILIZATION/AUTOMATION

MILESTONE SCHEDULE



LITERATURE SEARCH

- GOVERNMENT AGENCIES
- MILITARY CONTRACTORS
- COMMERCIAL AIRLINES
- TECHNICAL PUBLICATIONS
- DOD ABSTRACTS
- NASA ABSTRACTS

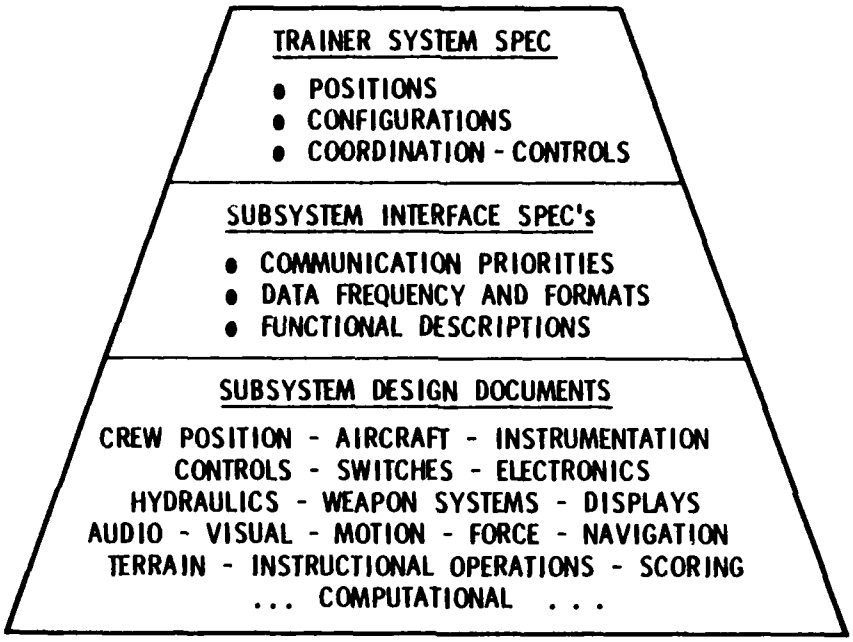
LITERATURE SEARCH

KEY INFORMATION SOURCES

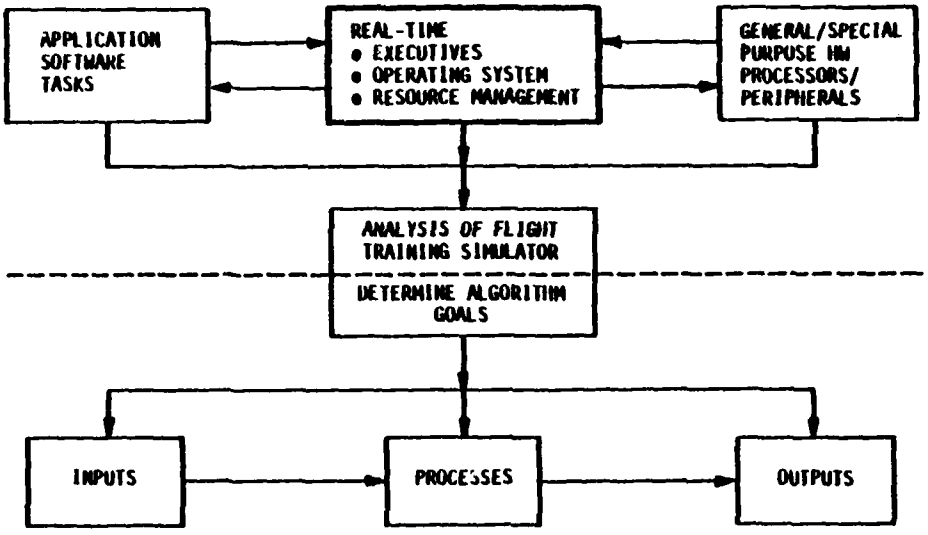
- ASUPT '74 & '76 DOCUMENTS
- ASPT VISUAL SUBSYSTEM EXPANDED PDR
- DEVICE 2E6 TRAINING ENGINEERING DESIGN REPORT
- SPECIFICATION FOR AIR COMBAT MANEUVERING SIMULATOR DEVICE 2E6

LITERATURE SEARCH

HIERARCHY OF FLIGHT TRAINER DOCUMENTS



FLIGHT TRAINER ANALYSIS



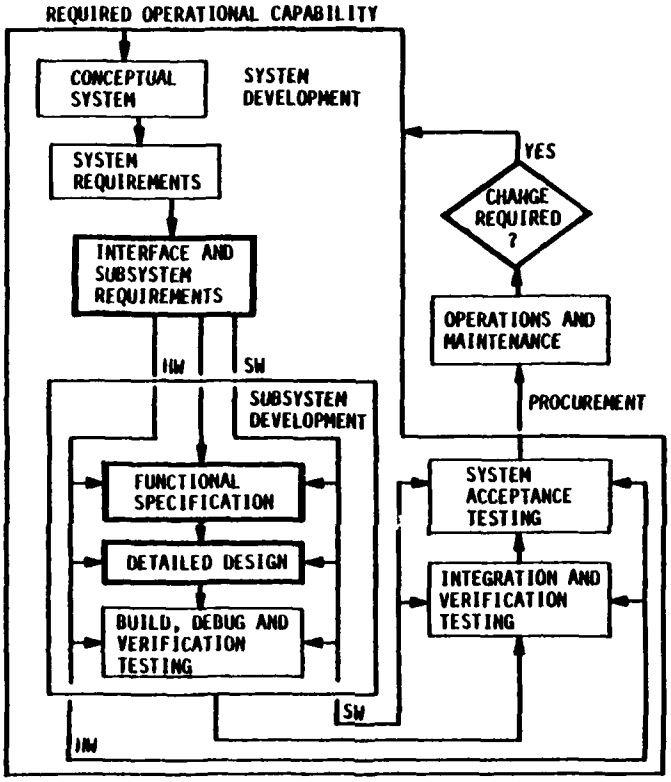
DESIGN CONSIDERATIONS

OPERATIONAL ENVIRONMENT QUESTIONS

- AT WHAT POINT(S) IN THE SYSTEM DEVELOPMENT CYCLE IS THE ALGORITHM TO BE USED?
- WHAT TIME FRAME AND COMPUTER RESOURCES ARE ANTICIPATED FOR CANDIDATE EVALUATIONS?
- WHAT FORMAT AND TO WHAT EXTENT WILL THE SYSTEM REQUIREMENTS BE DOCUMENTED?
- WHAT FORMAT AND TO WHAT EXTENT WILL THE ALTERNATE CANDIDATE DESIGN CONFIGURATIONS BE DOCUMENTED?

DESIGN CONSIDERATIONS

ALGORITHM RELATIONS WITH THE SYSTEM LIFE CYCLE



PROJECT SUMMARY

- SCHEDULE AND APPROACH OBJECTIVES

⇒ • DESIGN GOALS AND CONSIDERATIONS

  - GOALS
  - ALTERNATIVES
  - GOAL PROGRAM ENGLISH STATEMENT
  - HEURISTIC GOAL PROGRAM DECISION MODELS

- RESULTS AND RECOMMENDATIONS

DESIGN GOALS

- PARTITION TASKS TO A USER SPECIFIED MULTIPROCESSOR HARDWARE CONFIGURATION
- IDENTIFY INTERDEPENDENCIES AMONG THE TASKS
- PRECLUDE SYSTEM DEADLOCKS
- BALANCE THE PROCESSING LOAD
- CROSS REFERENCE TASK(S) ASSIGNED TO PROCESSORS
- LIST CRITICAL CONSTRAINTS WHEN A VALID PARTITION IS NOT OBTAINABLE
- PROVIDE A DEVELOPMENT COST ESTIMATE

DESIGN ALTERNATIVES

LINEAR PROGRAMMING
VERSUS
GOAL PROGRAMMING

MIXED INTEGER
VERSUS
CONTINUOUS
SOLUTIONS

OPTIMIZER
VERSUS
HEURISTIC

INITIAL ALLOCATION
USER SUPPLIED
VERSUS
AUTOMATIC GENERATION

GOAL PROGRAM ENGLISH STATEMENT

- COMPETING OBJECTIVES:
  - BALANCE THE PROCESSING LOAD AMONG THE PROCESSORS
  - BALANCE THE MEMORY STORAGE UTILIZATION
  - MINIMIZE DEVELOPMENT COSTS
- SUBJECT TO:
  - REAL-TIME TASK RESOURCE REQUIREMENTS
  - PERFORMANCE SIMULATION FEEDBACK

GOAL PROGRAM SIZING

CASE	CONTROL PARAMETERS						RESULTANT MATRIX		
	T TASKS	P PROC	B BLOCKS	M MEM	I INPUTS	O OUTPUTS	VARIABLES	ROWS	COLUMNS
1	30	2	61	3	3	2	1330	1747	4824
2	30	3	61	4	3	2	2383	3009	8401
3	30	3	120	4	3	3	3038	3608	10224
4	30	3	120	6	3	3	4358	4688	13734
5	60	4	140	6	3	3	10351	12271	34893
PROB 1	5	2	12	3	3	3	264	348	960
PROB 2	7	4	21	6	3	3	1250	1642	4534

VARIABLES = B + P + M + 1 + MB + 3TP + TPM (I + O)

ROWS = B + P + M + 1 + 2T + 2TP (1 + I + O) + TMP (I + O)

COLUMNS = VARIABLES + 2 (ROWS)

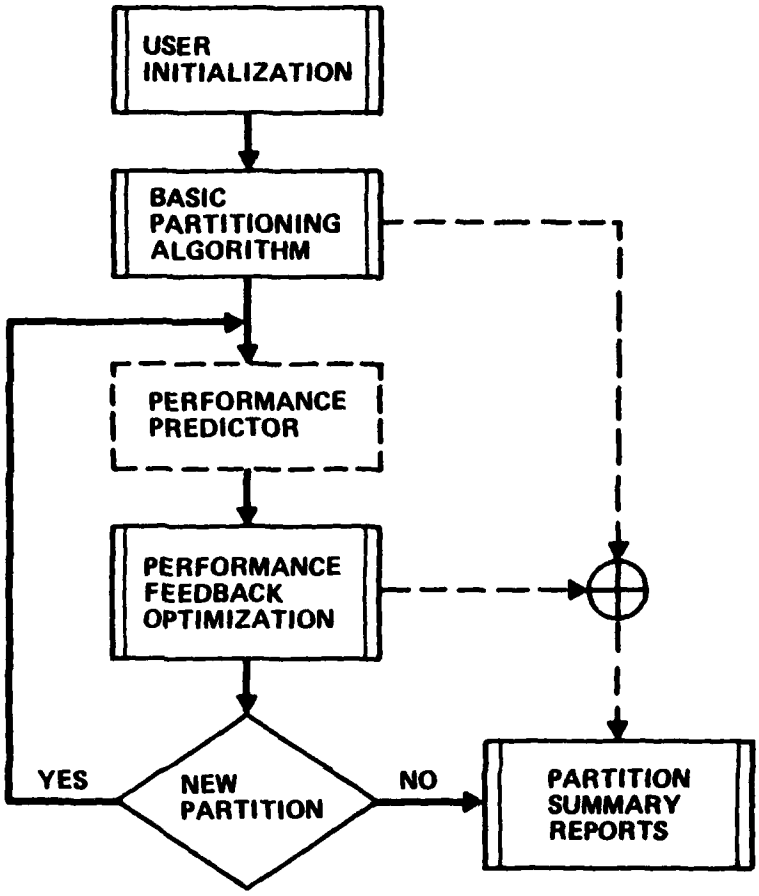
HEURISTIC GOAL PROGRAM DECISION MODELS

- GENERALLY REQUIRE AN INITIAL FEASIBLE ALLOCATION
- TAILORED TO SPECIFIC APPLICATION MODEL RELATIONSHIPS
- SEEK AN "IMPROVED" ALLOCATION SOLUTION WHICH MAY NOT NECESSARILY BE THE GLOBAL OPTIMUM
- PREEMPTIVE PRIORITY TECHNIQUES CAN BE EMPLOYED FOR MULTIPLE OBJECTIVES
- FOR LARGE PROBLEMS (MORE THAN SEVERAL HUNDRED VARIABLES OR CONSTRAINTS) HEURISTICS TEND TO BE COMPUTATIONALLY MORE EFFICIENT THAN A GENERALIZED OPTIMIZER IN PROVIDING ANSWERS TO USERS
- ONLY IMMEDIATE DECISION PARAMETERS ARE REQUIRED "IN MEMORY"

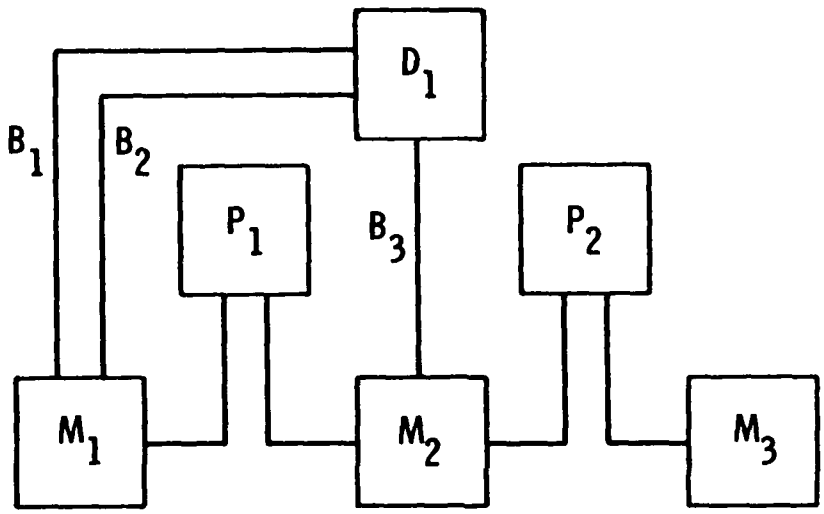
PROJECT SUMMARY

- SCHEDULE AND APPROACH OBJECTIVES
- DESIGN GOALS AND ALTERNATIVES
- ⇒ RESULTS AND RECOMMENDATIONS
  - ALGORITHM COMPUTATIONAL STEPS
  - SIMPLIFIED PROBLEM
  - SOURCE OF INPUTS
  - RECOMMENDED AUTOMATED IMPLEMENTATION TASKS
  - RECOMMENDED IMPLEMENTATION TIMELINE
  - FURTHER STUDY REQUIREMENTS

ALGORITHM COMPUTATIONAL STEPS



SIMPLIFIED PROBLEM CONFIGURATION



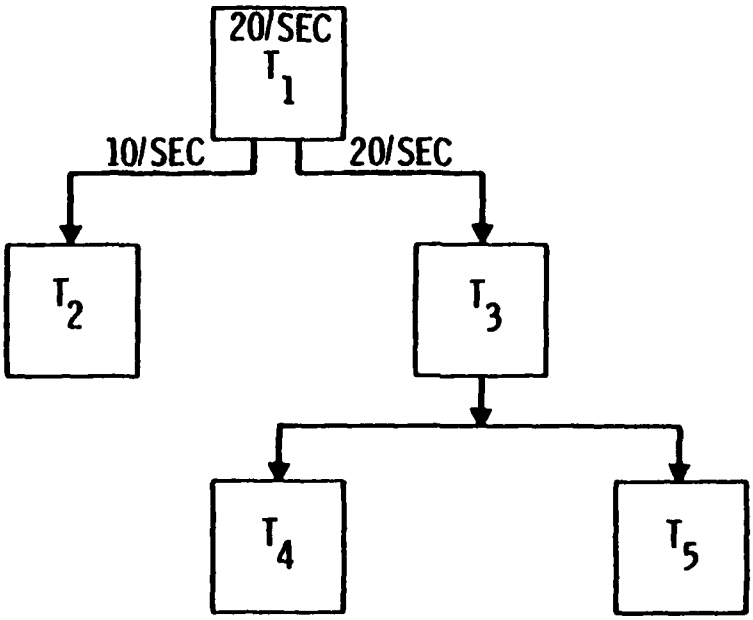
1 DEVICE

3 MEMORIES

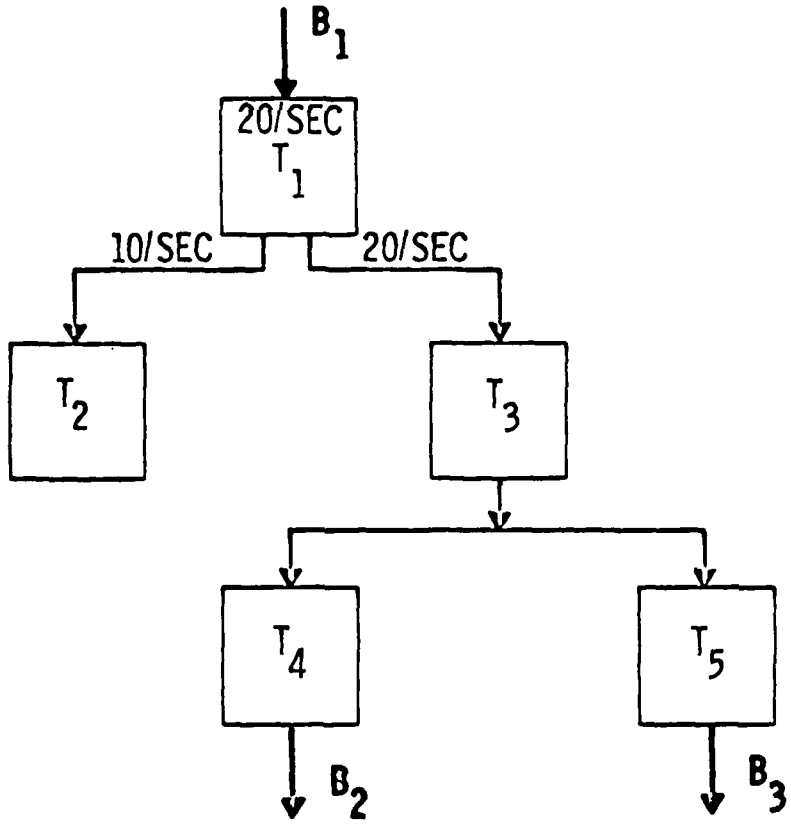
2 PROCESSORS

3 BUFFERS

SIMPLIFIED PROBLEM APPLICATION

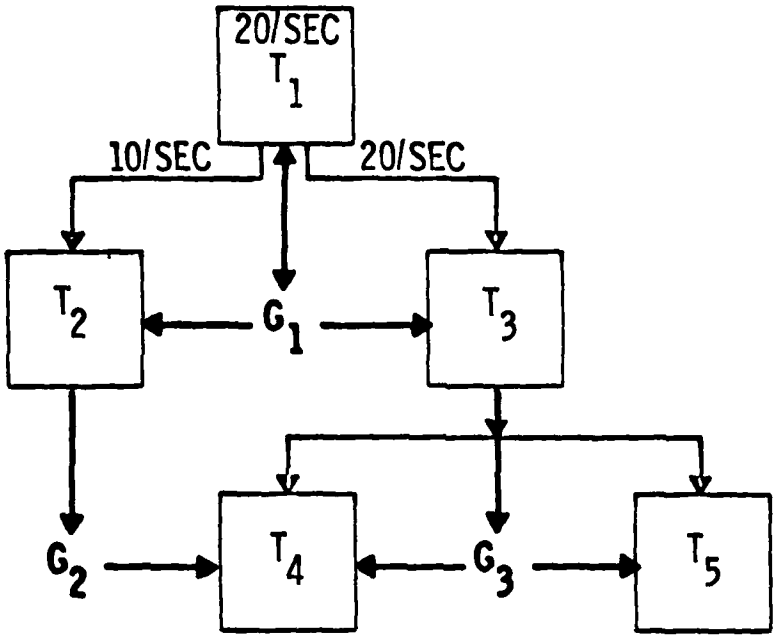


SIMPLIFIED PROBLEM APPLICATION



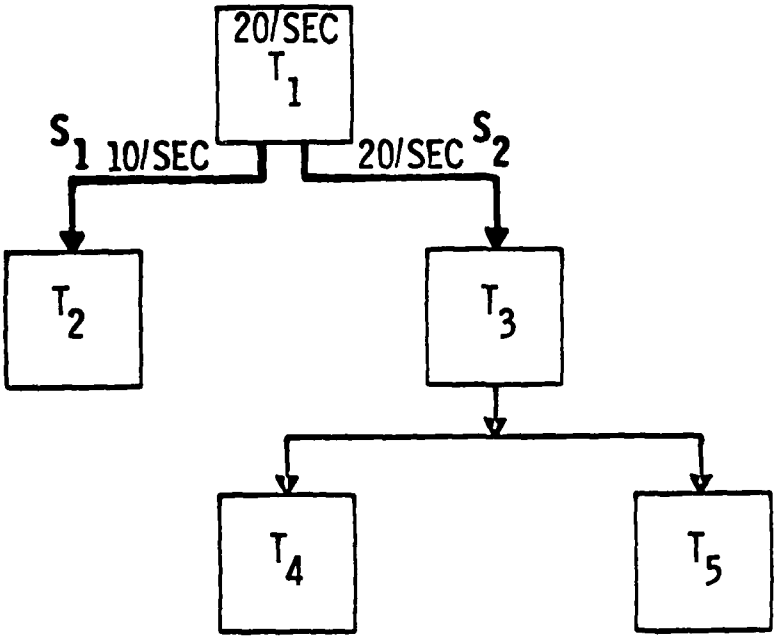
EXTERNAL I/O

SIMPLIFIED PROBLEM APPLICATION



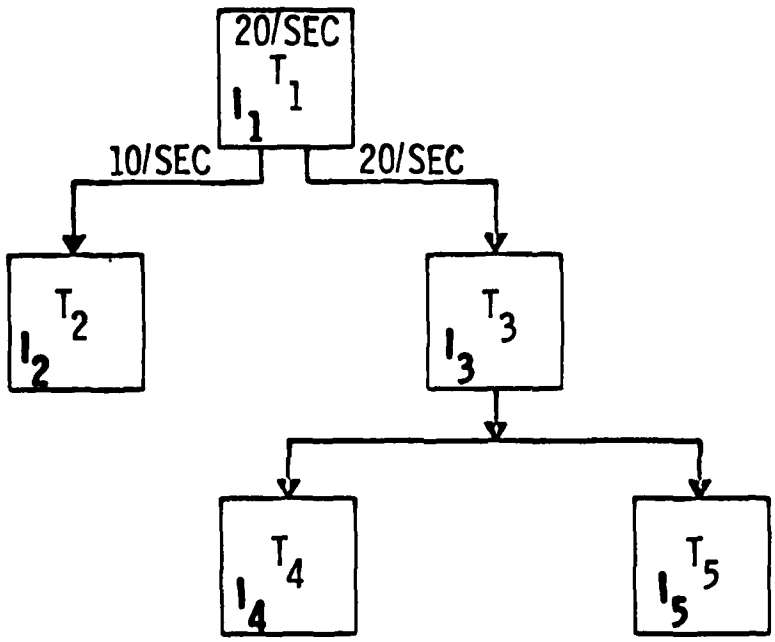
GLOBAL I/O

SIMPLIFIED PROBLEM APPLICATION



SEQUENTIAL I/O

SIMPLIFIED PROBLEM APPLICATION



INSTRUCTION BLOCKS

SIMPLIFIED PROBLEM OUTPUT FORMAT 101

PRIORITY GOAL SUMMARY

MAJOR PRIORITIES				PRIORITY COMPONENTS				
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL / FLAG	COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL / FLAG	
1	PROCESSOR UTILIZATION % BUSY	60.00 5.00%	60.00	P1	60	5.00	60	
				P2	60	5.00	60	
2	DEVELOPMENT COST MANYEARS	5.00 10.00%	5.60 **	T1	.5	10.00	.5	
				T2	1.0	10.00	1.0	
				T3	1.0	5.00	1.5	**
				T4	.5	1.00	.5	
				T5	2.0	10.00	2.0	
3	MEMORY UTILIZATION % ASSIGNED	60.00 5.00%	53.00	M1	60	5.00	66.00	**
				M2	30	2.00	32.00	
				M3	60	5.00	59.00	

PRIORITY GOAL SUMMARY

MAJOR PRIORITIES				PRIORITY COMPONENTS				
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL/FLAG	COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL	FLAG
9	XXXXXXXXXXXXXXX XXXXXXXX	99999.99 99.99	99999.99 FF	XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF
9	XXXXXXXXXXXXXXX XXXXXXXX	99999.99 99.99	99999.99 FF	XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF
9	XXXXXXXXXXXXXXX XXXXXXXX	99999.99 99.99	99999.99 FF	XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF
				XXXXXX9999	99999.99	99.999	99999.99	FF

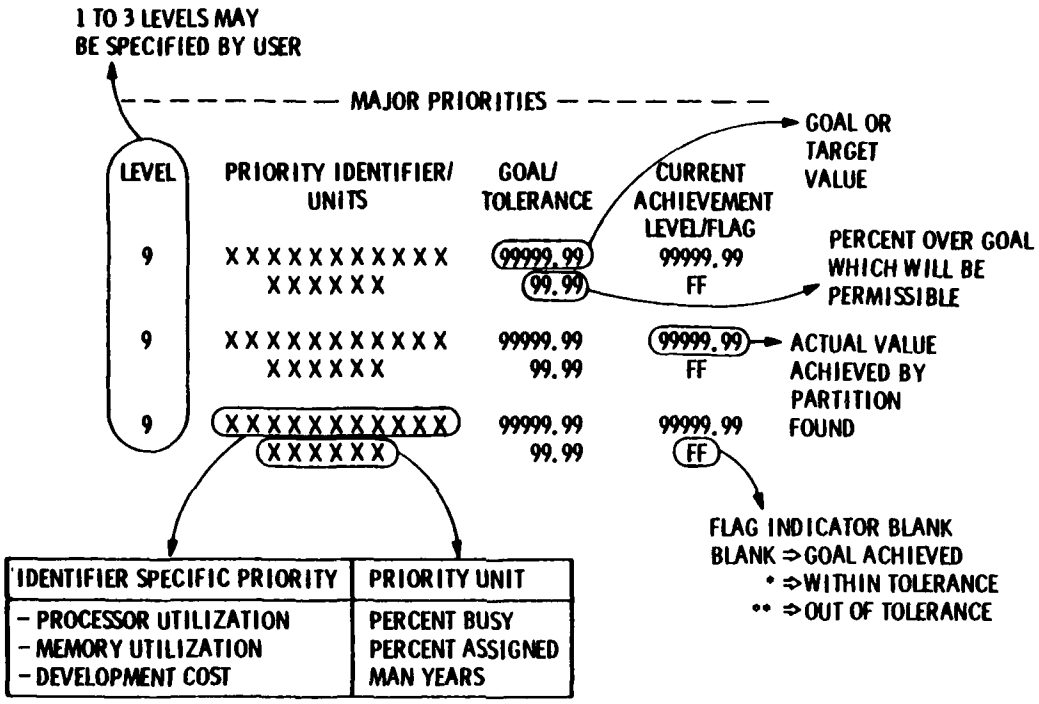
USER SUPPLIED PRIOR TO PARTITIONING

USER IMPLIED PRIOR TO PARTITIONING

USER MAY SUPPLY OR IMPLY PRIOR TO PARTITIONING

RESULTANT PARTITION MEASUREMENT

MAJOR PRIORITY PARAMETERS



IDENTIFIER SPECIFIC PRIORITY	PRIORITY UNIT
- PROCESSOR UTILIZATION	PERCENT BUSY
- MEMORY UTILIZATION	PERCENT ASSIGNED
- DEVELOPMENT COST	MAN YEARS

PRIORITY COMPONENT PARAMETERS

— — — — — — PRIORITY COMPONENTS — — — — — —

COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL	FLAG
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF

ACHIEVEMENT FLAG
* ⇒ ABOVE GOAL BUT WITHIN TOLERANCE
** ⇒ OUT OF TOLERANCE

PROCESSOR ID
MEMORY ID
TASK ID

GOAL OR TARGET DEVELOPMENT FOR GIVEN COMPONENT

MAXIMUM ACCEPTABLE DEVIATION ABOVE TARGET

LEVEL ACTUALLY ACHIEVED BY PARTITIONING ALGORITHMS

SIMPLIFIED PROBLEM OUTPUT FORMAT 102

TASK ALLOCATION					TASK I/O			
TASK	PROCESSOR	EXECUTIONS	TOTAL TIME	FLAG	BLOCK	MEMORY	INPUT	OUTPUT
T1	P1	20/20	.20		I1	M1	✓	✓
					B1	M1	✓	
					G1	M2	✓	✓
					S1	M1		✓
					S2	M2		✓
T2	P1	10/10	.20		I2	M1	✓	
					G1	M2	✓	
					G2	M2		✓
					S1	M1	✓	
T3	P2	20/20	.20		I3	M3	✓	
					G1	M2	✓	
					G3	M2		✓
						M3		✓
					S2	M2	✓	
T4	P1	20/20	.20		I4	M1	✓	
					B2	M1		✓
					G2	M2	✓	
					G3	M2	✓	
T5	P2	20/20	.40		I5	M3	✓	✓
					B3	M2		✓
					G3	M3	✓	

TASK ALLOCATION SUMMARY

TASK ALLOCATION

TASK	PROCESSOR	EXECUTIONS	TOTAL TIME	FLAG	TASK I/O BLOCK	MEMORY	INPUT	OUTPUT
XXXXXX	XXXXXX9999	999/999	9.99999	FF	XXXXXX	XXXXXX9999	9.999999	9.999999
					XXXXXX	XXXXXX9999	9.999999	9.999999
					XXXXXX	XXXXXX9999	9.999999	9.999999
	XXXXXX9999	999/999	9.99999	FF	XXXXXX	XXXXXX9999	9.999999	9.999999
					XXXXXX	XXXXXX9999	9.999999	9.999999
					XXXXXX	XXXXXX9999	9.999999	9.999999
XXXXXX	XXXXXX9999	999/999	9.99999	FF	XXXXXX	XXXXXX9999	9.999999	9.999999
					XXXXXX	XXXXXX9999	9.999999	9.999999

— USER SUPPLIED VIA BASELINE SOFTWARE TASK DESCRIPTIONS, DATA, AND LOAD TO BE PARTITIONED

-- PARTITION ALLOCATION OR RESULTING MEASURE

PROCESSOR ALLOCATION SUMMARY

PROCESSOR	TASK	EXECUTIONS	PROCESSOR UTILIZATION: COMPUTATIONAL TIME	COMPUTATIONAL PERCENT	INPUT/OUTPUT TIME	INPUT/OUTPUT PERCENT	RESOURCE MGMT TIME	RESOURCE MGMT PERCENT	FLAG
XXXXXX9999	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	TOTAL	99999	999.9999	999.99	9.9999	99.99	9.9999	99.99	FF
XXXXXX9999	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF

—— USER SUPPLIED VIA CANDIDATE CONFIGURATION INPUTS

– – PARTITIONING ALLOCATION OR RESULTING MEASURE

SIMPLIFIED PROBLEM OUTPUT FORMAT 103

DATA BLOCK ALLOCATION

BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
B1	M1	1000	3.1	P1		500		
B2	M1	2000	6.2	P1	1000			
B3	M2	4000	12.5	P2	2000			
G1	M2	4000	12.5	P1	✓	✓		
				P2		✓		
G2	M2	1000	3.1	P1	✓	✓		
G3	M2	1000	3.1	P1		✓		
				P2	✓			
	M3	1000	3.1	P2	✓	✓		
S1	M1	256	.8	P1	✓	✓		
S2	M2	256	.8	P1	✓			
				P2		✓		
I1	M1	2000	6.2	P1	✓	✓		
I2	M1	12000	37.8	P1	✓	✓		
I3	M3	8000	25.0	P2	✓	✓		
I4	M1	4000	12.5	P1	✓	✓		
I5	M3	10000	31.2	P2	✓	✓		

DATA BLOCK ALLOCATION SUMMARY

DATA BLOCK ALLOCATION

BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
XXXXXX	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
XXXXXX	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	9999999	FF

—— USER SUPPLIED VIA SOFTWARE TASK BLOCK DESCRIPTIONS

– – PARTITIONING ALLOCATION OR RESULTING MEASURES

MEMORY ALLOCATION SUMMARY

MEMORY ALLOCATION

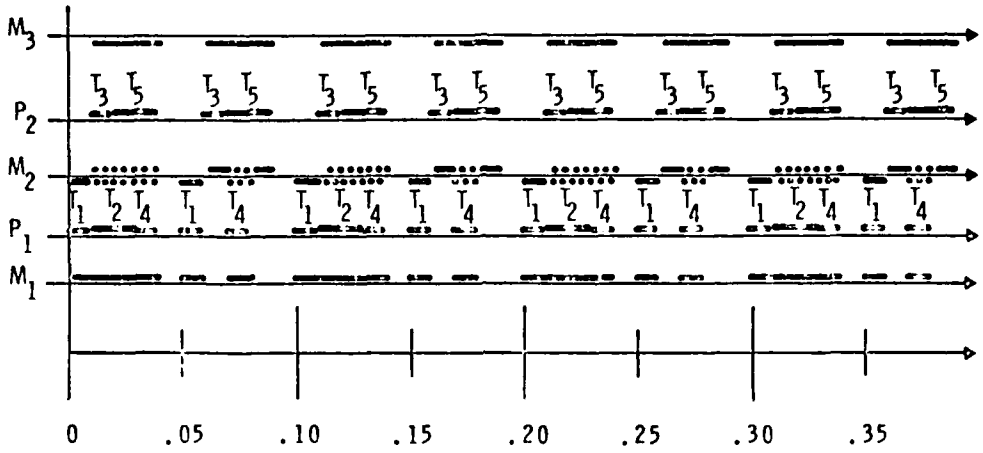
MEMORY	BLOCK	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
XXXXXX9999	XXXXXX	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
	XXXXXX	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
	** TOTAL	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
				**TOT PROC	9999999	9999999	99999999	FF

—— USER SUPPLIED VIA CANDIDATE CONFIGURATION INPUTS

— — PARTITIONING ALLOCATION OR RESULTING MEASURES

SIMPLIFIED PROBLEM UTILIZATION

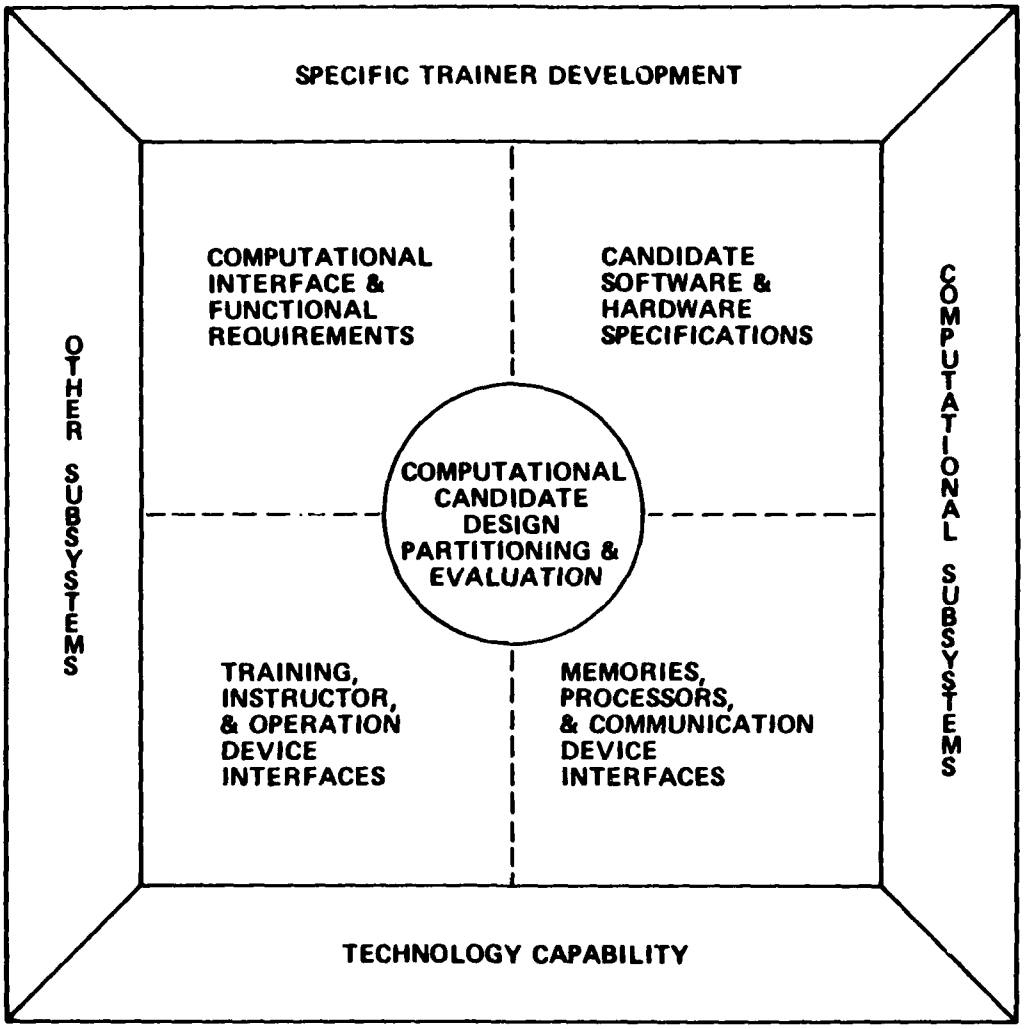
RELATED PERFORMANCE SIMULATION
TYPES OF OUTPUT BASED ON STATIC LOAD



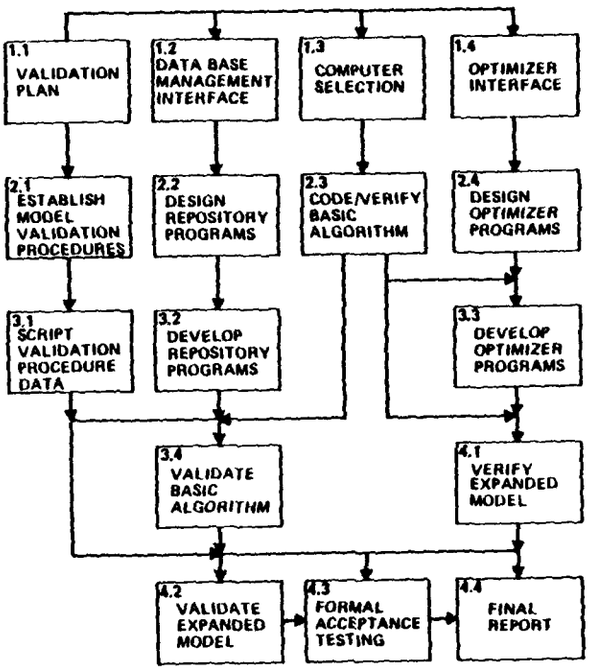
SOURCE OF INPUTS

DOCUMENT(S)	INPUT AREA
COMPUTATIONAL SUBSYSTEM INTERFACE SPECIFICATION	EXTERNAL DEVICE INTERFACES REQUIRED COMPONENTS FUNCTIONAL I/O MAP COMMUNICATION RULES & PRIORITIES BASELINE LOAD(S)
SOFTWARE DESIGN AND DATA BASE SPECIFICATIONS	DATA BLOCK DESCRIPTIONS TASK DESCRIPTIONS TASK THREADS BASELINE LOAD(S) TASKING
HARDWARE CONFIGURATION DESIGN SPECIFICATIONS	PROCESSORS MEMORIES INTERFACES (INTERNAL & EXTERNAL) COMMUNICATION RULES

REPOSITORY SOURCE OF INPUTS



RECOMMENDED AUTOMATED ALGORITHM IMPLEMENTATION TASKS



RECOMMENDED IMPLEMENTATION TIMELINE

PHASE I

	TASK DESCRIPTION	MONTH 1	2	3	4	5	6
1.1	VALIDATION PLAN			△			◇
1.2	DATA MANAGEMENT PLAN			△			◇
1.3	COMPUTER SELECTION			△			◇
1.4	OPTIMIZER INTERFACE			△			◇

PHASE II

	TASK DESCRIPTION	MONTH 7	8	9	10	11	12
2.1	VALIDATION PROCEDURES			△			◇
2.2	DESIGN REPOSITORY PROG.			△			◇
2.3	CODE/VERIFY B.A.			△			◇
2.4	DESIGN OPTIMIZER PROG.			△			◇

PHASE III

	TASK DESCRIPTION	MONTH 13	14	15	16	17	18	19	20	21
3.1	SCRIPT VALIDATION DATA			△			◇			◇
3.2	DEVELOP REPOSITORY PROG.			△			◇			
3.3	DEVELOP OPTIMIZER PROG.			△			◇			
3.4	VALIDATE BASIC ALGORITHM									◇

	TASK DESCRIPTION	MONTH 19	20	21	22	23	24	25	26	27	28	29	30
4.1	VERIFY EXPANDED MODEL			△			◇						
4.2	VALIDATE EXPANDED MODEL						△			◇			
4.3	FORMAL ACCEPTANCE TESTS										○		
4.4	FINAL REPORT								△		△		◇

△ - *INTERIM ON-SITE DEVELOPMENT* PROGRESS REVIEW AND DISCUSSION

◇ - DOCUMENTED PRESENTATION TO AF

○ - INDEPENDENT ASSESSMENT REPORT

FURTHER STUDY REQUIREMENTS

- POTENTIAL EMPLOYMENT AND EXPANSION OF MIXED INTEGER PROGRAM OPTIMIZER

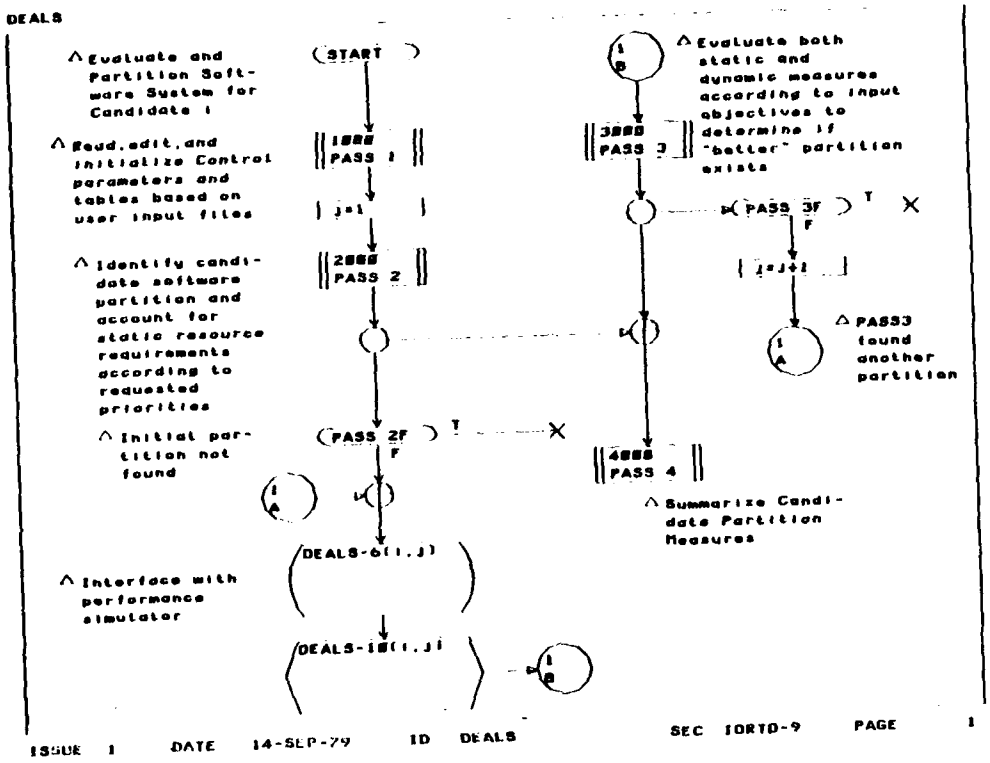
- DEVELOPMENT OF MASTER FLIGHT TRAINING SIMULATOR COMPUTATIONAL SUBSYSTEM DESIGN REPOSITORY WITH AUTOMATED FILES

PARTITIONING ALGORITHM DESIGN

- ORGANIZATION OF DESIGN MATERIALS
- ⇒ FEASIBILITY DEMONSTRATION
  - AREAS ADDRESSED
  - USER INPUT PREPARATION
  - LOAD BALANCE
  - MEMORY BALANCE
  - REDUCE DEVELOPMENT COST
  - PERFORMANCE BOTTLENECK FEEDBACK
  - REPORT GENERATION
- DETAILED DESIGN REVIEW

DEMO AREAS ADDRESSED

- PURPOSE
- PROBLEM
- SOLUTION
- FEASIBILITY ISSUES


DEALS
START
Evaluate and Partition Software System for Candidate 1
1000 PASS 1
Read, edit, and initialize Control parameters and tables based on user input files
J=1
Identify candidate software partition and account for static resource requirements according to requested priorities
2000 PASS 2
PASS 2F
T
F
Initial partition not found
DEALS-6(I,J)
Interface with performance simulator
DEALS-18(I,J)
Evaluate both static and dynamic measures according to input objectives to determine if "better" partition exists
3000 PASS 3
PASS 3F
T
F
J=J+1
PASS3 found another partition
4000 PASS 4
Summarize Candidate Partition Measures
ISSUE 1 DATE 14-SEP-79 ID DEALS SEC IDRTD-9 PAGE 1

INPUT PROCESSING DEMO

PURPOSE: TO PERMIT AND FACILITATE USER PARTITIONING PROBLEM DEFINITION

PROBLEM: PARTITIONING REQUIRES CAREFULLY COORDINATED (YET DIVERSE) SETS OF DATA BASE PARAMETERS

SOLUTION: MODULAR DATA BASE FILES WHICH ARE EASILY CROSS-REFERENCED FOR MINIMIZATION OF REQUIRED AND/OR REDUNDANT USER INPUTS

INPUT PROCESSING DESIGN

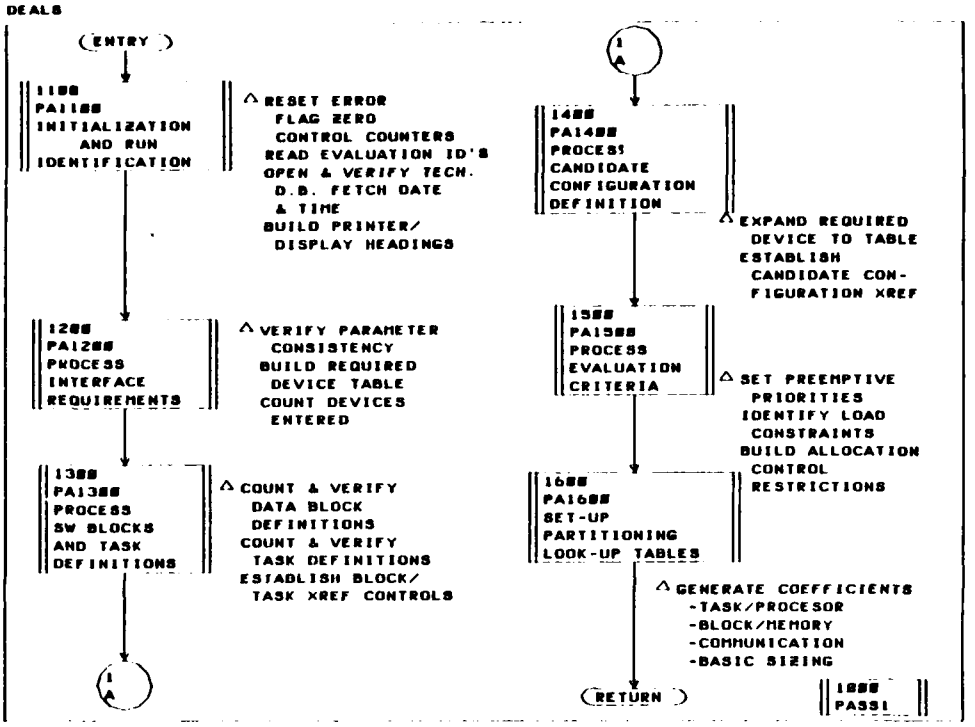
INPUT FILES

- COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS
- BASELINE SOFTWARE TASK/JOB/LOAD CONFIGURATION
- CANDIDATE HARDWARE CONFIGURATION
- TECHNOLOGY DATA BASE
- EVALUATION CRITERIA AND CONSTRAINTS
- INITIAL ALLOCATION

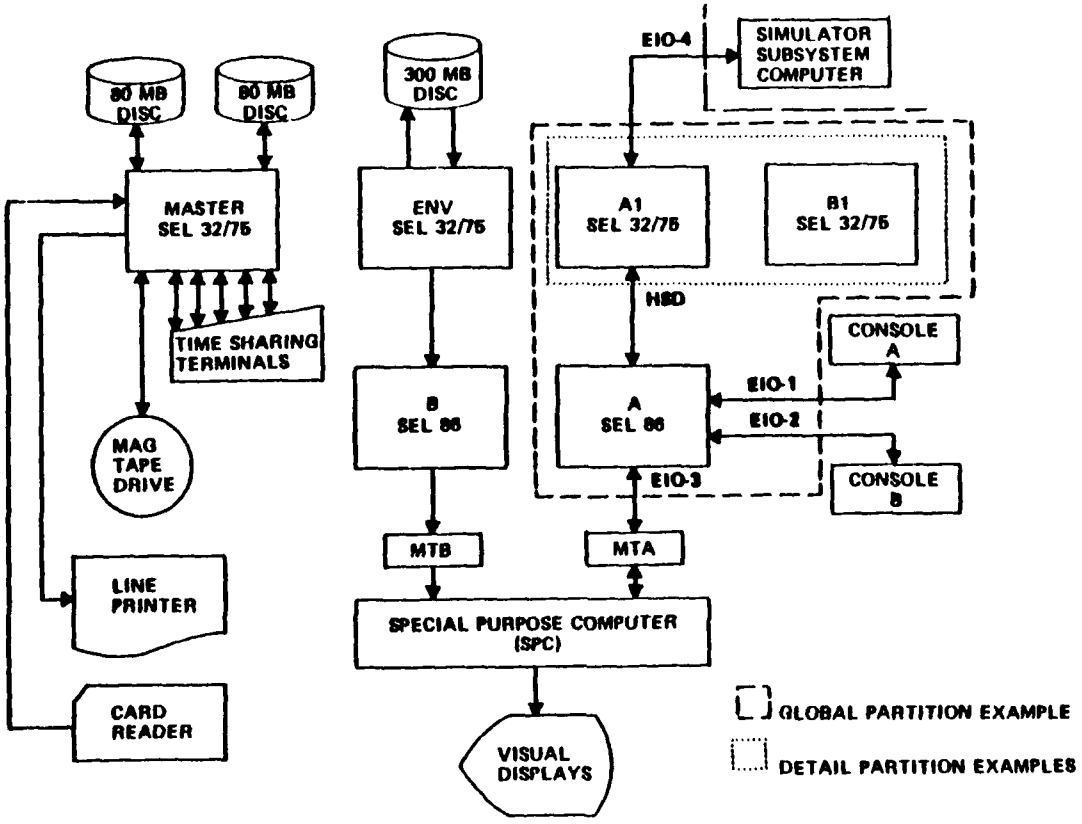
EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

FILE	IDENTIFIER
COMPUTATIONAL INTERFACE REQUIREMENTS	INTERFACE DEFINITION
BASELINE APPLICATION COMPONENTS	SAMPLE APPLICATION
CANDIDATE CONFIGURATION COMPONENTS	SAMPLE CONFIGURATION
BASELINE PARTITIONING LOAD	GLOBAL LOAD EXAMPLE
TECHNOLOGY DATA BASE	HYPOTHETICAL TECH DB

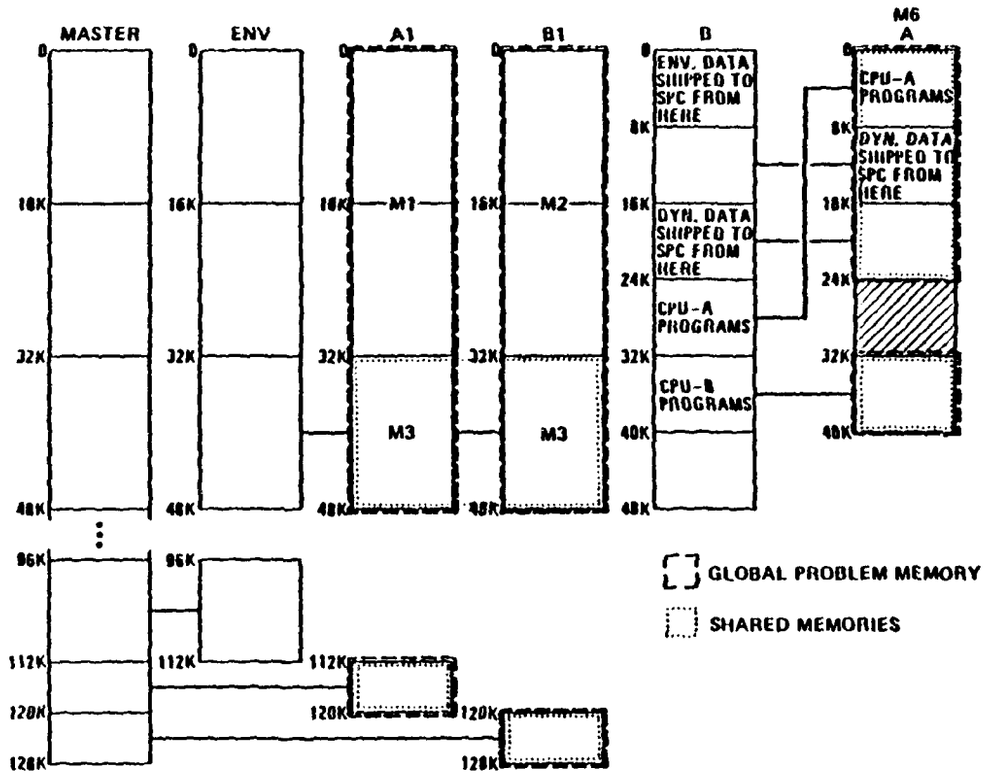
PARTITION LIB


DEALS
(ENTRY)
1100
PA1100
INITIALIZATION
AND RUN
IDENTIFICATION
RESET ERROR
FLAG ZERO
CONTROL COUNTERS
READ EVALUATION ID'S
OPEN & VERIFY TECH.
D.B. FETCH DATE
& TIME
BUILD PRINTER/
DISPLAY HEADINGS
1200
PA1200
PROCESS
INTERFACE
REQUIREMENTS
VERIFY PARAMETER
CONSISTENCY
BUILD REQUIRED
DEVICE TABLE
COUNT DEVICES
ENTERED
1300
PA1300
PROCESS
SW BLOCKS
AND TASK
DEFINITIONS
COUNT & VERIFY
DATA BLOCK
DEFINITIONS
COUNT & VERIFY
TASK DEFINITIONS
ESTABLISH BLOCK/
TASK XREF CONTROLS
1
A
1
A
1400
PA1400
PROCESS
CANDIDATE
CONFIGURATION
DEFINITION
EXPAND REQUIRED
DEVICE TO TABLE
ESTABLISH
CANDIDATE CON-
FIGURATION XREF
1500
PA1500
PROCESS
EVALUATION
CRITERIA
SET PREEMPTIVE
PRIORITIES
IDENTIFY LOAD
CONSTRAINTS
BUILD ALLOCATION
CONTROL
RESTRICTIONS
1600
PA1600
SET-UP
PARTITIONING
LOOK-UP TABLES
GENERATE COEFFICIENTS
-TASK/PROCESOR
-BLOCK/MEMORY
-COMMUNICATION
-BASIC SIZING
(RETURN)
1000
PASS1
ISSUE DATE 13-NOV-79 ID DEALS SEC PPD-1000 PAGE 1

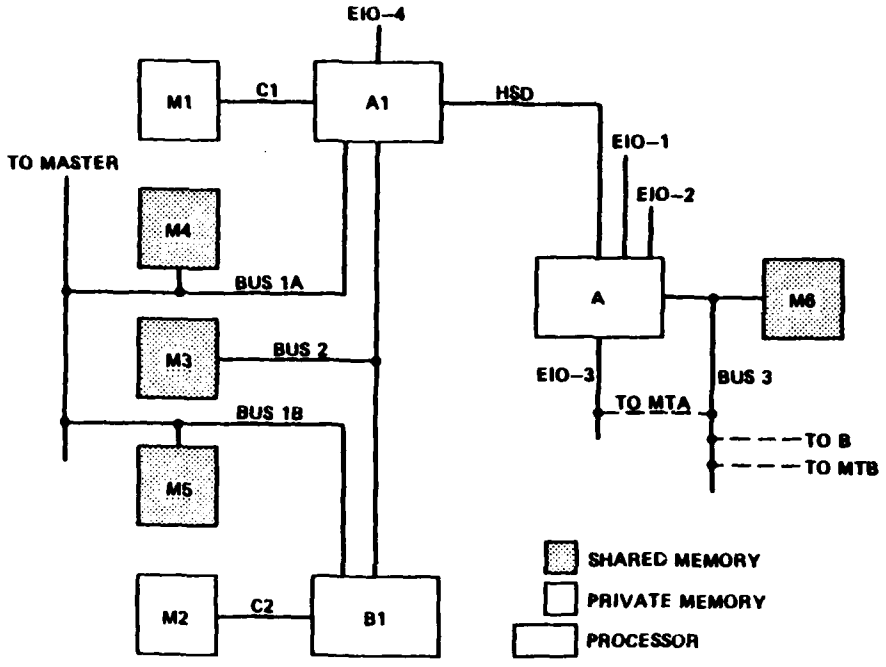
PROCESSOR CONFIGURATION



MEMORY CONFIGURATIONS



SAMPLE CONFIGURATION MEMORY PROCESSOR COMMUNICATIONS



COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
PU	86-PROC	A	8	CUSTOM-VIS	ASSEMBLER	G
			FORTRAN IV	MACRO-ASM		
PU	SPC	SPC	3	ASPT-DIS	MICRO	
IC	VIOC	CONSOLEA				
IC	VIOC	CONSOLEB				
CL	ASYNC-I/O	EIO-1	PU	A		G
			IC	CONSOLEA		
CL	ASYNC-I/O	EIO-2	PU	A		G
			IC	CONSOLEB		
MM	86-MEM	M6	KWRD	48		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 6 - LANGUAGE 3	3 - LANGUAGE 1 8 LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	CUM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONFIGURATION

PROPOSED DEVICES TO COMPLIMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COMLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, --	OPTION 2, 5, 8, --	OPTION 3, 6, 9, --	CONTINUE
TYPE	DEVICE					
PU	XYZ32/75	A1	8	OS-XYZ-2B	FORTRAN IV	C
			JOVIAL J73	ASSEMBLER	FORTRAN 73	
PU	XYZ32/75	B1	3	OS-XYZ-2B	FORTRAN IV	C
			JOVIAL J73	ASSEMBLER		
MM	32-MEM	M1	KWRD	32		
MM	32-MEM	M2	KWRD	32		
MM	32-MEM	M3	KWRD	32		
MM	32-MEM	M4	KWRD	8		
MM	32-MEM	M5	KWRD	8		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

TECHNOLOGY DATA BASE IDENTIFIER: HYPOTHETICAL TECH DB

PROCESSOR: XYZ 32/75 | BYTE = 8 BITS | WORD = 16 BYTES

OPERATING SYSTEM: OS-XYZ-28 | CYCLE TIME: 0.00 μ SAWORD | ACCESS TIME: μ SAWORD

MULTI TASK LEVELS: 64

PRIORITY LEVELS: 64

		SIZING		UNITS	
ADDRESSABLE MEMORY:	4	K	(M)	BYTES	(WORDS)
OPERATING SYS. MEMORY:	48	(K)	M	BYTES	(WORDS)
SUPPORT LIBRARY MEMORY:	20	(K)	M	BYTES	(WORDS)

LANGUAGES

1 ASSEMBLER
2 FORTRAN IV
3 JOVIAL J73
4 FORTRAN 77
5 BASIC
6 COBOL
7 MACRO-ASM
8

MULTI TASKING FEATURES AND RESOURCES

LEVEL (1 to)	MAX TASKS	SERVICED P - PRIORITY R - CIRCULAR F - FIFO	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)			ENABLEMENT RESOURCE MANAGEMENT CIRCLE TYPES(S) TIME	SLAVE	DATA	FREQUENCY TIMES/SECOND	OVERHEAD/ ENABLEMENT
1-54		(R)	(R)	NR	B	T	S	D		
55-63		(F)	R	(NR)	B	T	S	D		
64-64		(F)	R	NR	(B)	T	S	D		
ALL-ALL	255		R	NR	B	(T)	(S)	(D)		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		

TECHNOLOGY DATA BASE IDENTIFIER: HYPOTHETICAL TECH 33

MEMORY DEVICE DEFINITION

IDENTIFIER: 32-MEM

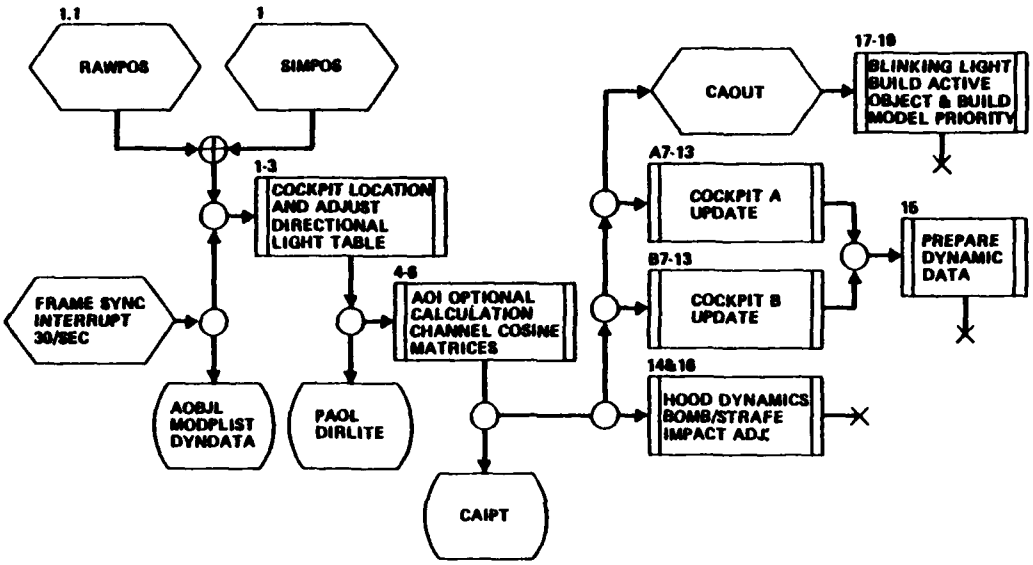
TYPE: ROM RAMM RRAM SM WCS

SINGLE RAM

ADDRESSABLE UNITS

IN	UNIT SIZE		READ (FETCH)			WRITE (STORE)		
	DATA BITS	ERROR BITS	ACCESS (NANO-SEC)	CYCLE (NANO-SEC)	MAX UNITS READ	ACCESS (NANO-SEC)	CYCLE (NANO-SEC)	MAX UNITS WRITTEN
WORD	32	4		900			900	
BYTE	8	1		900			800	
HWRD	16	2		900			800	

SAMPLE APPLICATION



BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

DATA BLOCK DEFINITIONS

ID	LEVEL	DISCIPLINE	SYSTEM INTERFACE DEVICE	MAXIMUM RECORDS	MINIMUM		RECORD SIZE IN WORDS		
					BITS/BYTE	BYTES/WORD	MINIMUM	AVERAGE	MAXIMUM
PAOL	5	RAN	MM-A3	128	8	4	1	1	1
DIALITE	5	RAN	MM-A3	256	8	4	1	1	1
CADUTI	5	CBUF	CL-HSD	2	8	4	128	128	128
ADAIL	5	RAN	CL-HSD	100	8	4	1	1	1
MODPLIST	5	RAN	CL-HSD	20	8	4	1	1	1
CALPT	5	CBUF	CL-HSD	2	8	4	128	128	128
DYNDATA	5	RAN	CL-HSD	8192	8	4	1	1	1
SIMPOS	5	CBUF	CL-EIO-4	2	8	4	128	128	128
RAWPOS	5	CBUF	MM-M1	2	8	4	128	128	128
G1	5	RAN		1024	8	4	1	1	1
ADATA	5	RAN		512	8	4	1	1	1
ADATA	5	RAN		512	8	4	1	1	1
DYNDATA	5	RAN		512	8	4	1	1	1
DYNDATASW	5	RAN	MM-M3	1	8	4	1	1	1

SAMPLE PROBLEM MASTER BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFIER	BRIEF DESCRIPTION
AOI	- AREA OF INTEREST VISUAL COMPUTATIONS
BAOL	- BUILD ACTIVE OBJECT LIST
BLR	- BLINKING LIGHTS ROUTINE
BMBSTRAIMP	- BOMB STRAFE IMPACT TABLE ADJUSTMENT
BMPL	- BUILD MODEL PRIORITY LIST
CADCOSMAT	- COMPUTE CHANNEL ASSIGNMENT DIRECTIONAL COSINE MATRICES
CONIF	- VISUAL CONSOLE OPERATOR INTERFACE

Page 1 of 3

SAMPLE PROBLEM BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFER	BRIEF DESCRIPTION
DRLITADJ	- DIRECTIONAL LIGHT TABLE ADJUSTMENT
FADCOM	- FADING COMPUTATIONS
HOODDYN	- HOOD DYNAMICS
MMP	- MOVING MODEL PRIORITY
MMSADJ	- MOVING MODEL SITE ADJUSTMENT
PDYN	- PREPARE DYNAMIC DATA FOR OUTPUT
PEV	- PSEUDO EDGE VECTOR CALCULATION
RWV	- ROTATE WINDOW VECTORS
RWVM	- ROTATE WINDOW VECTORS MOVING MODEL

Page 2 of 3

SAMPLE PROBLEM MASTER BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFIER	BRIEF DESCRIPTION
SHIPCAIPT	- SHIP CHANNEL ASSIGNMENT INPUT DATA
SIMIF	- SIMULATOR MATH MODEL INTERFACE
TELV	- TERRAIN ELEVATION COMPUTATION
TSMMC	- TRANSFORM SUN VECTOR TO MOVING MODEL COORDINATES
T3	- SHIP POTENTIAL ACTIVE OBJECT LIST (PAOL) AND DIRECTIONAL LIGHT TABLE (DIRLITE)

Page 3 of 3

DASH-ING SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK: T1-3 | QUALIFICATION TYPE: TIME | DASH 0 / MASTER TASK (IF DASH) | MAXIMUM TIME: | OVERLAY: YES (NO) | PRIORITY: 38

INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
SIMPLE	1	1	1	SIMPOS	0	0	ALL		
COUNT	1	0	1	RAMPOS	0	0	0	0	2
DELIGHT	1	1	1	DIRLITE	0	0	0	128	256
T3	1	1	1	PAUL	0	0	128	128	128
				G1	0	0	512	512	1024
				TUNDARA	0	0	ALL		

* CIRCLE ONE FOR ENTRY

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK HORIZON ON PROCESSOR XY232/75

USING _____ OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	1200	208	208	416	1	.01
WORST CASE						
LANGUAGE FACTORS:						
1 [illegible]	1	1	1	1	1	1
2 ASSEMBLER	.8	.7	.7	.7	4.8	1
3						
4						
5						
6						
7						
8						

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

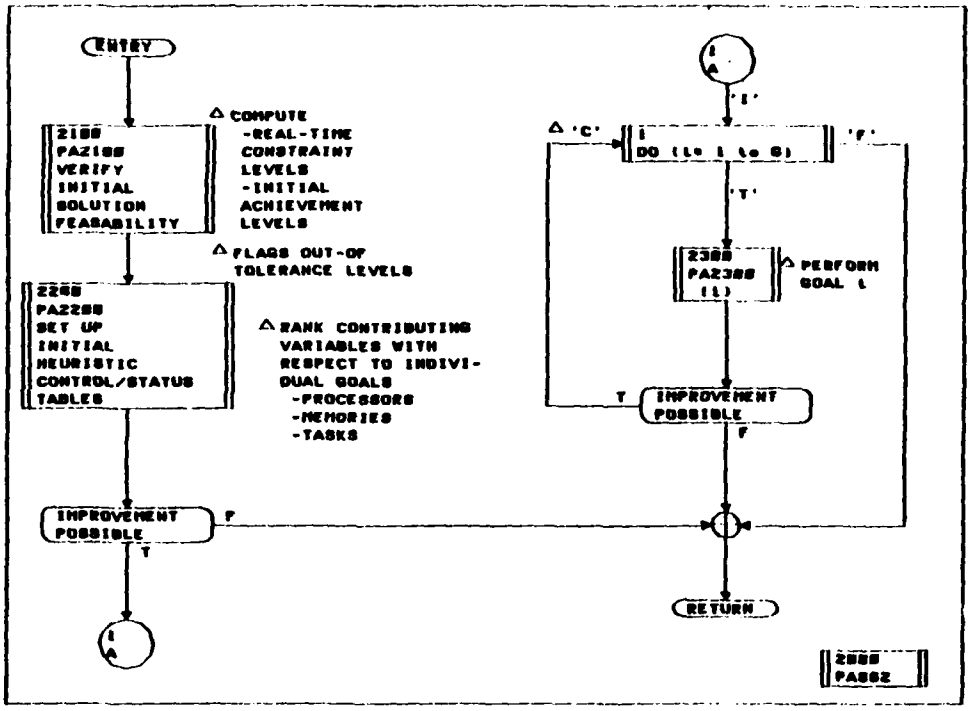
ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER	VALUE IF APP.
F	T	T1-3	A1	30
I	T	T4-5	A1	30
I	T	A7-13	A1	30
I	T	T17-18	A1	30
P	T	T17-18	B1	30
I	T	B7-13	B1	30
I	T	T14&16	B1	30
F	T	T15	B1	15
F	T	T15	A1	15

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT VALUE IF APP.
F	D	PAOL	M3	
F	D	DORLITE	M3	
F	D	CADUTI	M4	
F	D	AOBJL	M3	
F	D	MODPLIST	M3	
F	D	CAIPTI	M4	
F	D	DYNDATA	M3	
F	D	SIMPOS	M1	
F	D	RAWPOS	M1	

DEALS



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PROCESSOR LOAD BALANCE DEMO

PROBLEM: THREEFOLD BALANCE CHARACTERIZATION

(1) NPGTL PROCESSORS OVER ABSOLUTE UTILIZATION LIMIT

(2) NPGTG PROCESSORS ARE ABOVE GOAL UTILIZATION

(3) (NP-NPGTG) PROCESSORS ARE AT OR BELOW GOAL UTILIZATION

PROCESSOR LOAD BALANCE DEMO

QUESTION POSED :

DOES AN IMPROVED ALLOCATION EXIST?

I.E. CAN THE PROCESSORS BELOW GOAL UTILIZATION PERFORM SOME OF THE TASKS CURRENTLY ALLOCATED TO HEAVILY UTILIZED PROCESSORS?

PROCESSOR LOAD BALANCE DEMO

ALGORITHM SOLUTION TECHNIQUE

- RANK PROCESSOR UTILIZATION Up WITH RESPECT TO GOAL Gp USING (Gp-Up) AS MEASUREMENT
- IF Up>Lp (ABSOLUTE LIMIT EXCEEDED) ADD A LARGE NEGATIVE PENALTY TO DIFFERENCE
- RANK RESULTING DIFFERENCES IN DESCENDING ORDER NOTE: LEAST LOADED PROCESSORS WILL APPEAR FIRST
- ATTEMPT TO OFFLOAD PROCESSOR ABOVE LIMIT
- SEE IF LEAST LOADED PROCESSOR CAN RELIEVE ANY OF THE HEAVILY LOADED PROCESSORS

PROCESSOR LOAD BALANCE DEMO

SAMPLE PROBLEM INPUTS

PROCESSOR	COMPONENT TASK	UTIL	U_p	G_p	L_p	$U_p^1 = G_p - U_p$
1	1	50	100	60	75	-140*
	2	10				
	3	25				
	4	15				
2	5	40	40	40	75	0
3	6	20	20	60	75	+40

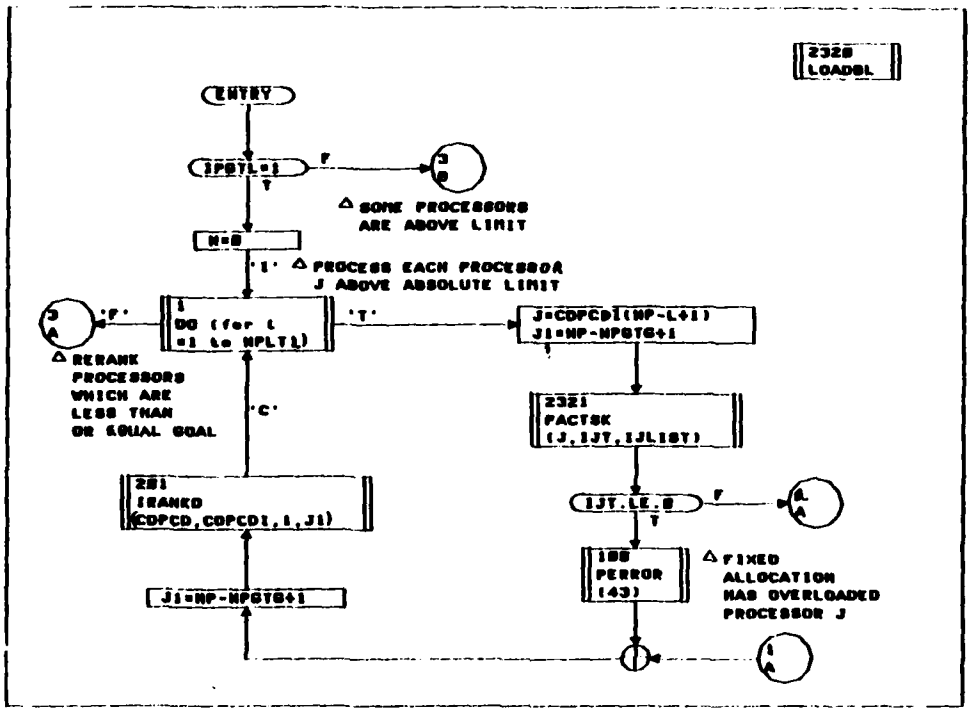
* PENALTY FOR BEING OVER ABSOLUTE LIMIT = 100

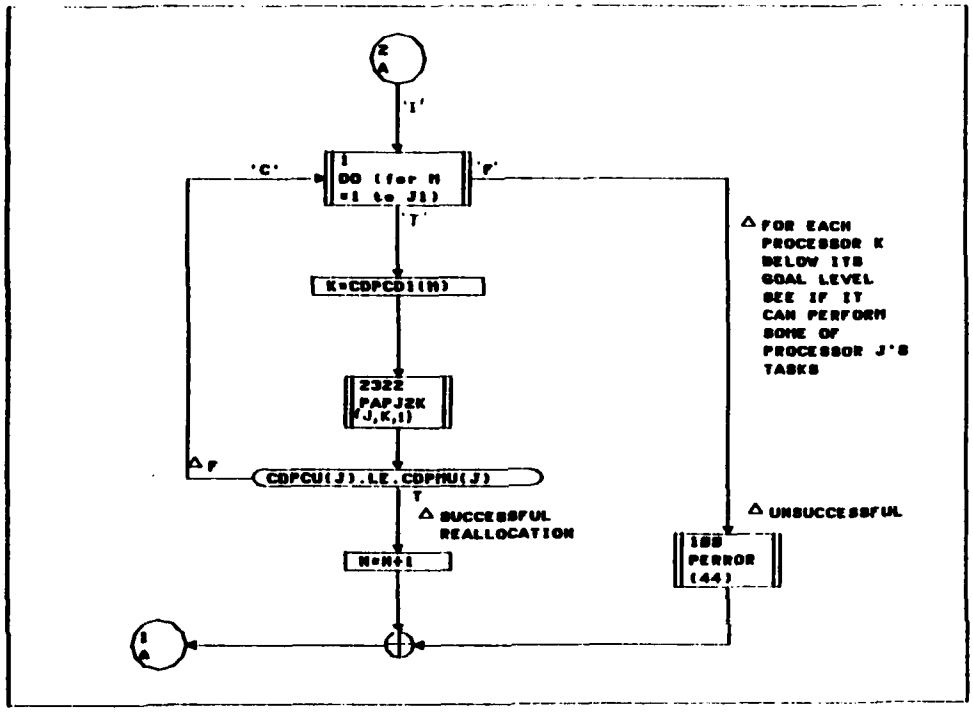
PROCESSOR LOAD BALANCE DEMO

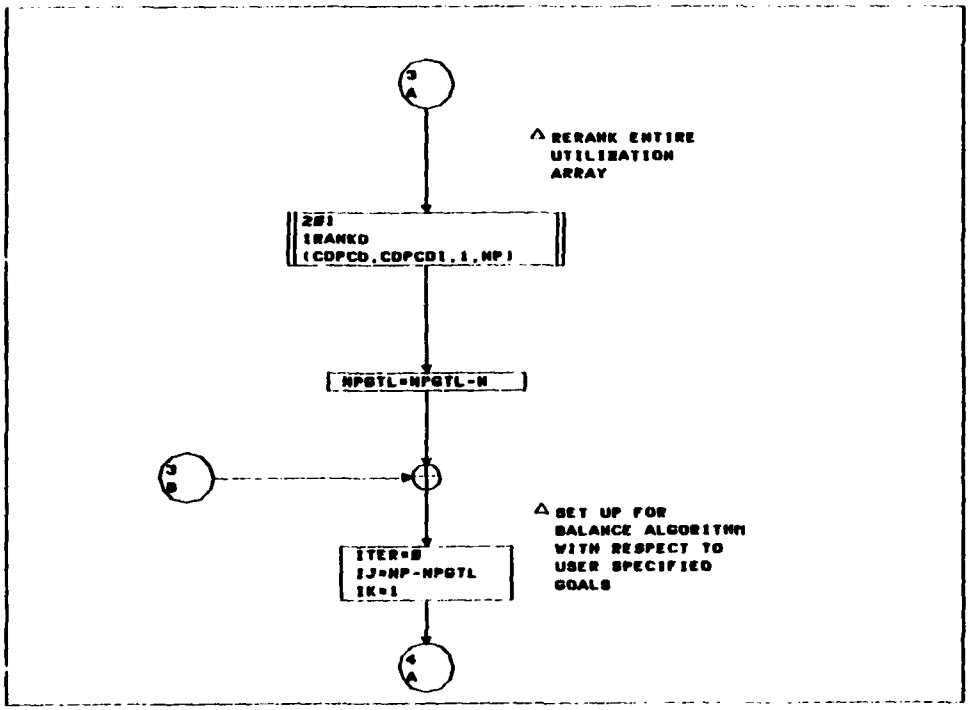
SAMPLE PROBLEM TEST CASES

CASE	DESCRIPTION	RESULTS	
		PROC-TASKS	UTILIZATION
1	IDENTICAL PROCESSORS SHARED MEMORY ALL BLOCKS	P1-T1, T2 P2-T5 P3-T6, T3, T4	60 40 60
2	IDENTICAL PROCESSORS SHARED MEMORY DATA BLOCKS PRIVATE MEMORY INSTRUCTION BLOCKS	P1-T1, T2 P2-T5 P3-T6, T3, T4	60 40 60
3	IDENTICAL PROCESSORS SHARED MEMORY DATA BLOCKS PRIVATE MEMORY INSTRUCTION BLOCKS T3 FIXED ON P1, T1 PROHIBITED ON P3	P1-T1, T3 P2-T5 P3-T6, T4, T2	75* 40 45

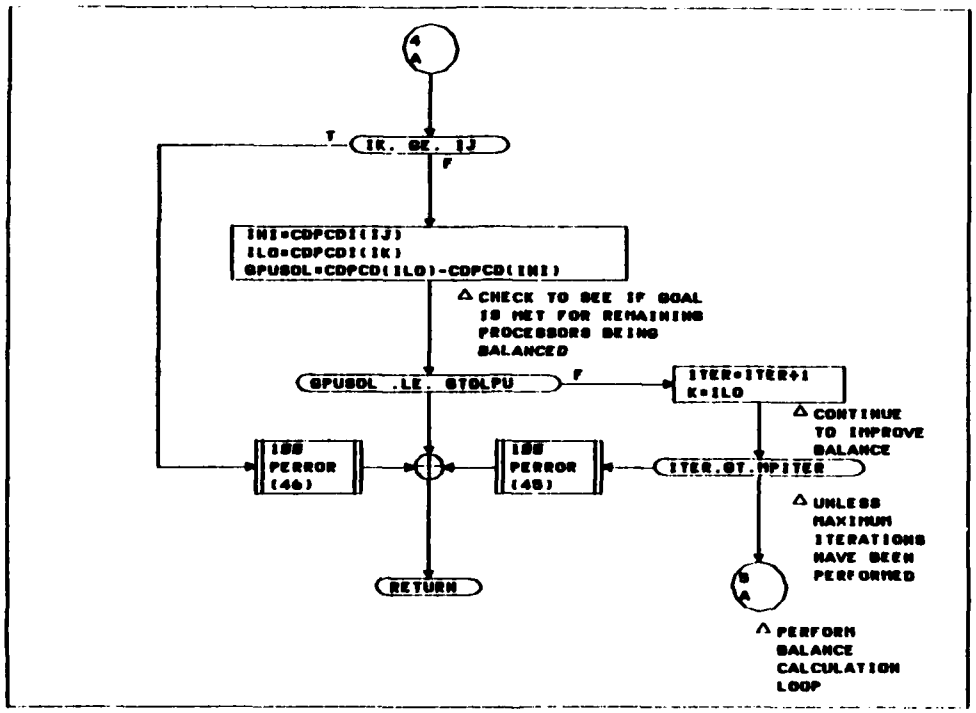
*ABOVE GOAL UNABLE TO OFFLOAD


2328
LOADBL
ENTRY
IPBTL=1
F
T
△ SOME PROCESSORS ARE ABOVE LIMIT
N=0
'I'
△ PROCESS EACH PROCESSOR J ABOVE ABSOLUTE LIMIT
DO (for L =1 to NPLTL)
'F'
'T'
△ RERANK PROCESSORS WHICH ARE LESS THAN OR EQUAL GOAL
'C'
J=CDPCDI(NP-L+1)
J1=NP-NPGTG+1
2321
FACTSK
(J,IJT,IJLIST)
281
IRANKD
(CDPCD,CDPCDI,I,J1)
IJT.LE.0
F
T
188
PERROR
(43)
△ FIXED ALLOCATION HAS OVERLOADED PROCESSOR J
J1=NP-NPGTG+1

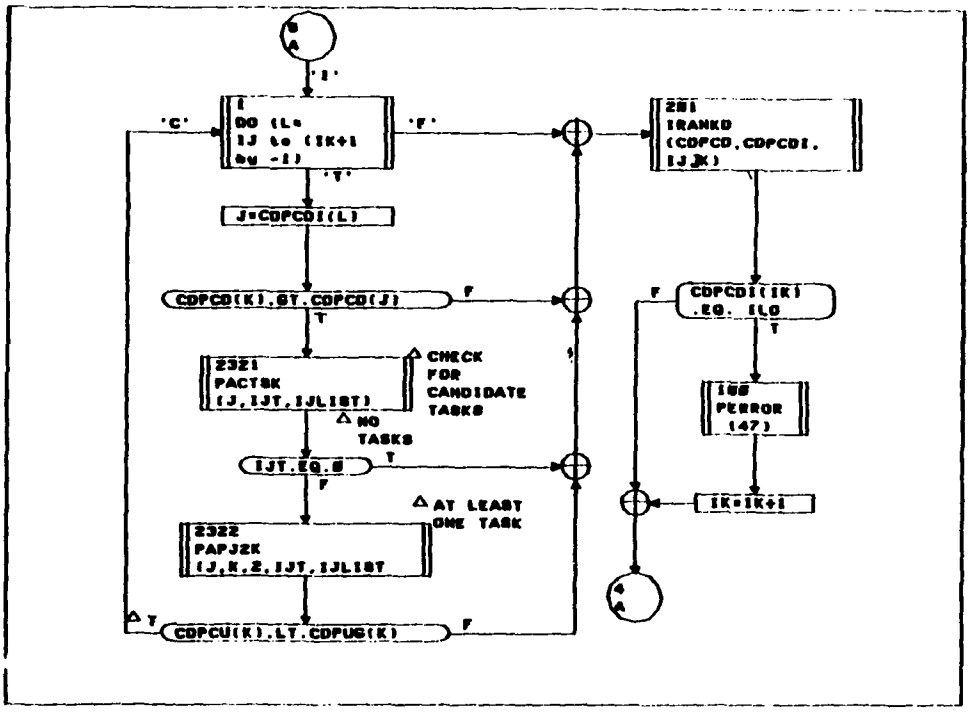

2
A
'I'
'C'
1
DO (for M
=1 to J1)
'F'
'T'
K=CDPCD1(M)
2322
PAPJ2K
(J,K,1)
F
CDPCU(J).LE.CDPMU(J)
T
SUCCESSFUL
REALLOCATION
M=M+1
1
A
FOR EACH
PROCESSOR K
BELOW ITS
GOAL LEVEL
SEE IF IT
CAN PERFORM
SOME OF
PROCESSOR J'S
TASKS
UNSUCCESSFUL
188
PERROR
(44)


3
A
RERANK ENTIRE
UTILIZATION
ARRAY
2#1
IRANKD
(CDPCD,CDPCD1,1,NP)
NPGTL=NPGTL-N
3
B
SET UP FOR
BALANCE ALGORITHM
WITH RESPECT TO
USER SPECIFIED
GOALS
ITER=0
IJ=NP-NPGTL
IK=1
4
A

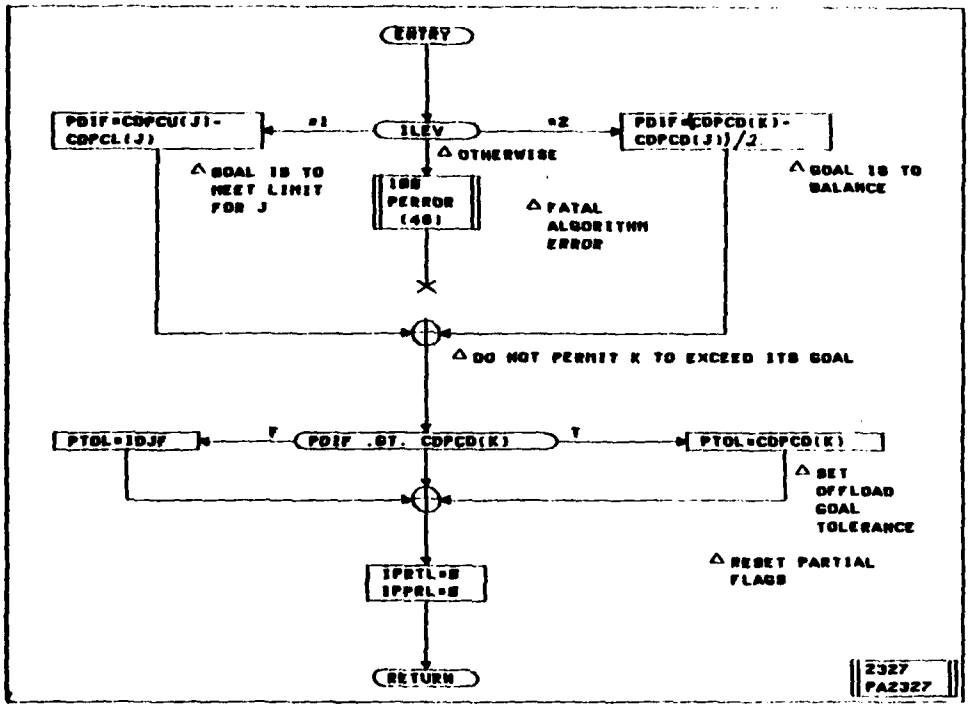
DEALS



ISSUE DATE 19-NOV-79 ID DEALS SEC PPD-2328 PAGE 4


'I'
'C'
'F'
'T'
DO (L=
IJ to (IK+1
by -1)
J=CDPCDI(L)
CDPCD(K).GT.CDPCD(J)
F
T
2321
PACTSK
(J,IJT,IJLIST)
CHECK
FOR
CANDIDATE
TASKS
NO
TASKS
IJT.EQ.0
T
F
AT LEAST
ONE TASK
2322
PAPJ2K
(J,K,2,IJT,IJLIST
T
CDPCU(K).LT.CDPUG(K)
F
281
IRANKD
(CDPCD,CDPCDI,
IJ,K)
F
CDPCDI(IK)
.EQ. ILO
T
100
PERROR
(47)
IK=IK+1

DEAL8



ISSUE DATE 28-NOV-79 ID DEAL8 SEC PPD-2327 PAGE 1

MEMORY ALLOCATION BALANCE DEMO

PROBLEM : THREEFOLD BALANCE CHARACTERIZATION

(1) NMGTL MEMORIES ARE ABOVE ABSOLUTE LIMIT

(2) NMGTG MEMORIES ARE ABOVE GOAL UTILIZATION

(3) (NM-NMGTG) MEMORIES ARE AT OR BELOW GOAL UTILIZATION

MEMORY ALLOCATION BALANCE DEMO

QUESTION POSED :

DOES AN IMPROVED ALLOCATION EXIST?

I.E. CAN THE MEMORIES BELOW GOAL ALLOCATIONS BE ASSIGNED DATA / INSTRUCTION BLOCKS FROM OVER ALLOCATED MEMORIES?

MEMORY ALLOCATION BALANCE DEMO

SOLUTION TECHNIQUE

- RANK MEMORY ALLOCATIONS u_m WITH RESPECT TO GOAL g_m USING $(g_m - u_m)$ AS MEASUREMENT
- MEMORY HEURISTIC CONTROL FLOW IDENTICAL TO PROCESSOR LOAD BALANCE HEURISTIC WITH
  - BLOCKS IN PLACE OF TASKS
  - MEMORIES IN PLACE OF PROCESSORS
- DETAILED CALCULATIONS DIFFER SIGNIFICANTLY

MEMORY ALLOCATION BALANCE DEMO

SAMPLE PROBLEM INPUTS

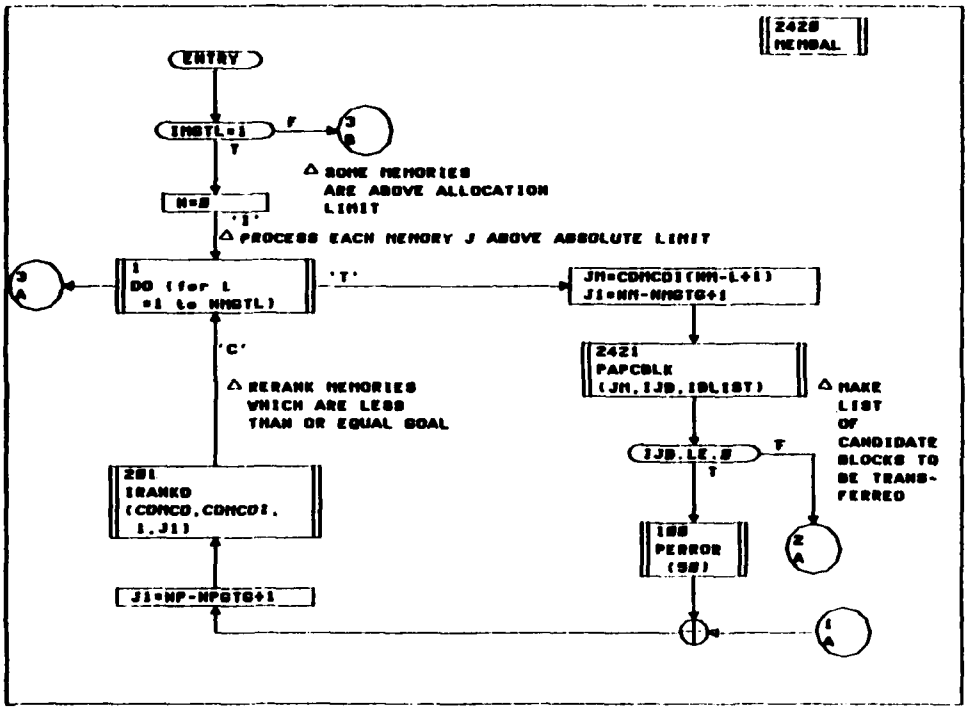
MEMORY	COMPONENT BLOCK	UTIL	U_m	G_m	L_m	$U'_m = G_m - U_m$
1	1	10	80	60	70	-120*
	2	30				
	3	40				
2	4	20	20	60	70	+40

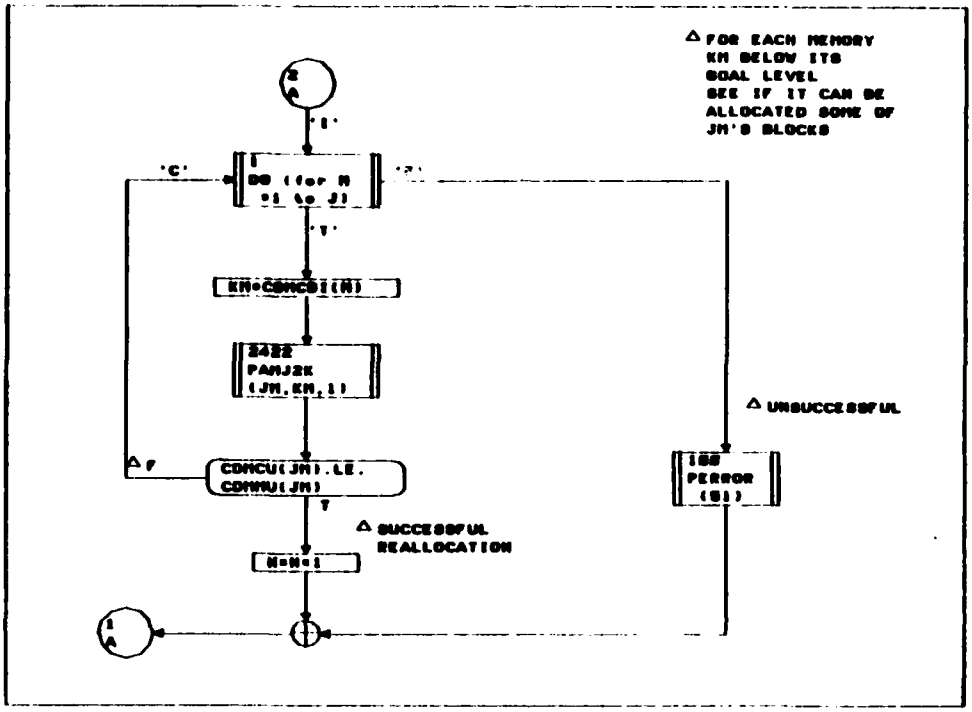
*PENALTY FOR BEING OVER ABSOLUTE LIMIT = 100

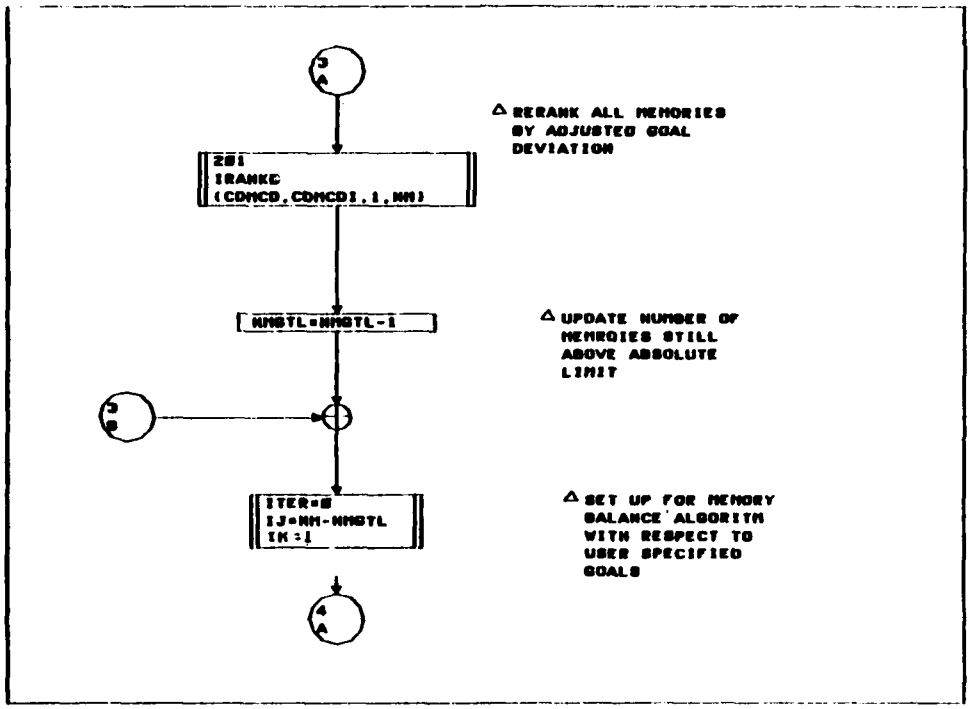
MEMORY ALLOCATION BALANCE DEMO

SAMPLE PROBLEM TEST CASES

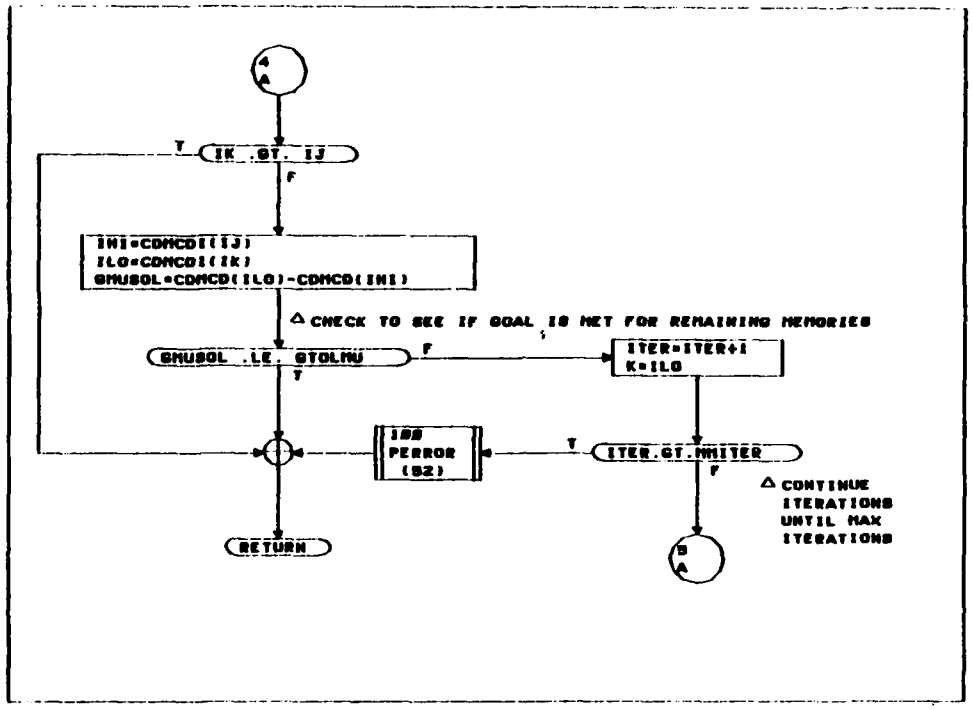
CASE	DESCRIPTION	RESULTS	
		MEMORY-BLOCKS	UTILIZATION
1	BOTH MEMORIES AVAILABLE TO ALL PROCESSORS IDENTICAL MEMORIES	M1 - B3, B1 M2 - B4, B2	50 50
2a	SAME AS CASE 1 EXCEPT B2 FIXED ON M1 WITHOUT SWAP	M1 - B2, B3 M2 B4, B1	70 30
2b	SAME AS CASE 2a EXCEPT SWAP ALGORITHM ADDED	M1 - B2, B4 M2 - B3, B1	50 50
3a	M2 REQUIRES DOUBLE SPACE TO STORE BLOCK 1 AND NO FIXED ASSIGNMENTS NO SWAP	M1 - B2, B3 M2 - B4, B1	70 40
3b	SAME AS CASE 3a EXCEPT SWAP ALGORITHM ADDED	M1 - B1, B3 M2 - B4, B2	50 50


DEALS
2420
MEMBAL
ENTRY
IMGTL=1
F
T
3
B
SOME MEMORIES
ARE ABOVE ALLOCATION
LIMIT
N=0
'I'
PROCESS EACH MEMORY J ABOVE ABSOLUTE LIMIT
3
A
1
DO (for L
=1 to NMGTL)
'T'
JM=CDMCDI(NM-L+1)
J1=NM-NMGTG+1
'C'
RERANK MEMORIES
WHICH ARE LESS
THAN OR EQUAL GOAL
2421
PAPCBLK
(JM,IJB,IBLIST)
MAKE
LIST
OF
CANDIDATE
BLOCKS TO
BE TRANS-
FERRED
IJB.LE.0
F
T
201
IRANKD
(CDMCD,CDMCDI,
1,J1)
100
PERROR
(50)
2
A
J1=NP-NPGTG+1
1
A
ISSUE
DATE
26-NOV-79
ID
DEALS
SEC
PPD-2420
PAGE
1

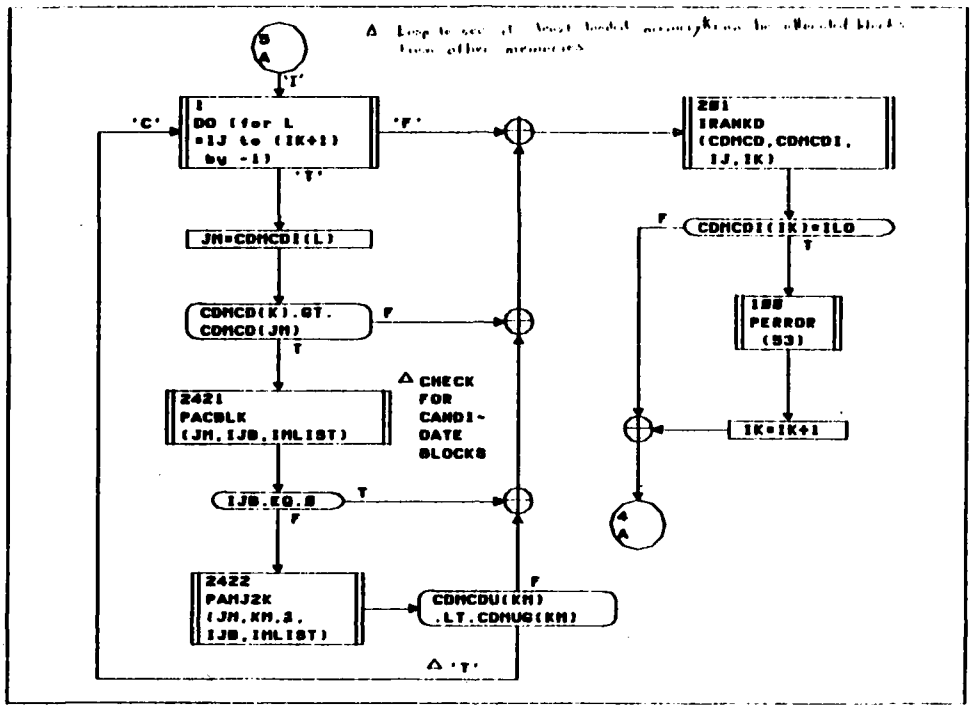

DEALS
FOR EACH MEMORY
KM BELOW ITS
GOAL LEVEL
SEE IF IT CAN BE
ALLOCATED SOME OF
JM'S BLOCKS
'C'
'T'
KM=CDMCBI(M)
2422
PAMJ2K
(JM,KM,1)
UNSUCCESSFUL
CDMCU(JM).LE.
CDMMU(JM)
PERROR
SUCCESSFUL
REALLOCATION
N=N+1
DATE 26-NOV-79 ID DEALS SEC PPD-2428 PAGE 2


DEALS
3 A
RERANK ALL MEMORIES BY ADJUSTED GOAL DEVIATION
201
IRANKC
(CDMCD,CDMCDI,1,NM)
NMGTL=NMGTL-1
UPDATE NUMBER OF MEMROIES STILL ABOVE ABSOLUTE LIMIT
3 B
ITER=0
IJ=NM-NMGTL
IK=1
SET UP FOR MEMORY BALANCE ALGORITM WITH RESPECT TO USER SPECIFIED GOALS
4 A
ISSUE DATE 26-NOV-79 ID DEALS SEC PPD-2420 PAGE 3

DEALS



ISSUE DATE 26-NOV-79 ID DEALS SEC PPD-2428 PAGE 4


5
A
'I'
'C'
I
DO (for L
=IJ to (IK+1)
by -1)
'F'
'T'
JM=CDMCDI(L)
CDMCD(K).GT.
CDMCD(JM)
F
T
2421
PACBLK
(JM,IJB,IMLIST)
CHECK
FOR
CANDI-
DATE
BLOCKS
IJB.EQ.0
T
F
2422
PAMJ2K
(JM,KM,3,
IJB,IMLIST)
CDMCDU(KM)
.LT.CDMUG(KM)
F
'T'
281
IRANKD
(CDMCD,CDMCDI,
IJ,IK)
F
CDMCDI(IK)=ILO
T
188
PERROR
(53)
IK=IK+1
4
A

REDUCE DEVELOPMENT COST DEMO

PROBLEM AREAS:

(1) HOMOGENEOUS VERSUS HETEROGENEOUS CANDIDATE CONFIGURATION COMPONENTS

(2) EXISTING VERSUS NEW SOFTWARE / FIRMWARE CAPABILITIES

(3) SOURCE OF GOOD INPUT ESTIMATES FOR A GIVEN ALLOCATION

REDUCE DEVELOPMENT COST DEMO

QUESTIONS POSED FOR HOMOGENEOUS CASE

(1) CAN A MORE COST EFFECTIVE DEVELOPMENT LANGUAGE BE USED FOR DEVELOPMENT AND STILL MEET REAL-TIME CONSTRAINTS?

(2) IF A TASK IS CURRENTLY ALLOCATED TO MORE THAN ONE PROCESSORS CAN THE NUMBER OF PROCESSORS BE REDUCED AND WHAT IMPACT DOES THIS HAVE ON DEVELOPMENT COST?

REDUCE DEVELOPMENT COST DEMO

QUESTIONS POSED FOR HETEROGENEOUS CASE

(1) ARE ANY TASKS ASSIGNED TO PROCESSORS OF DIFFERENT TYPES?

(2) IF SO, CAN A HOMOGENEOUS ASSIGNMENT BE FOUND FOR THEN TASK ALLOCATION?

REDUCE DEVELOPMENT COST DEMO

ALGORITHM TECHNIQUES

1. DO NOT PERMIT PARTIAL ALLOCATIONS OF TASKS TO HETEROGENEOUS PROCESSORS IN LOADBL UNLESS PRESET CONSTRAINT.

2. DO NOT PERMIT DUPLICATE BLOCKS ON HETEROGENEOUS MEMORIES IN MEMBAL.

3. CREATE A TASK ALLOCATION CHANGE LIST OF TASKS WHICH COULD BE SWAPPED TO REDUCE DEVELOP COST AND STILL MEET REAL-TIME CONSTRAINTS.

4. PROCESS CHANGE LIST TO SEE IF TASK EXCHANGES CAN BE MADE BETWEEN A GIVEN PAIR OF PROCESSORS.

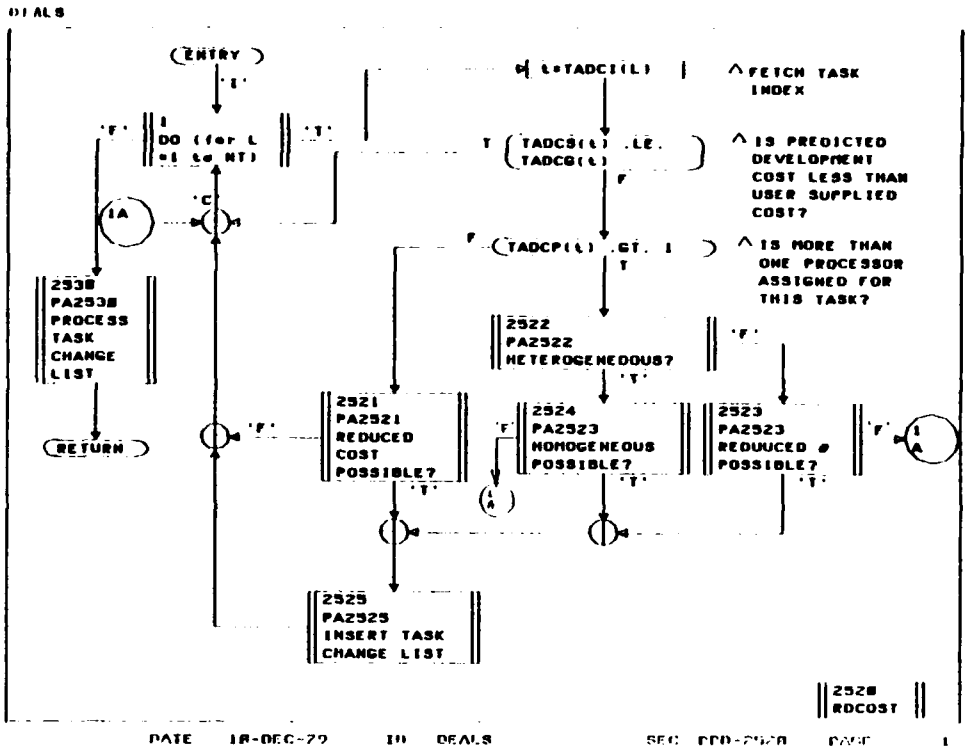
REDUCE DEVELOPMENT COST DEMO

TEST CASES

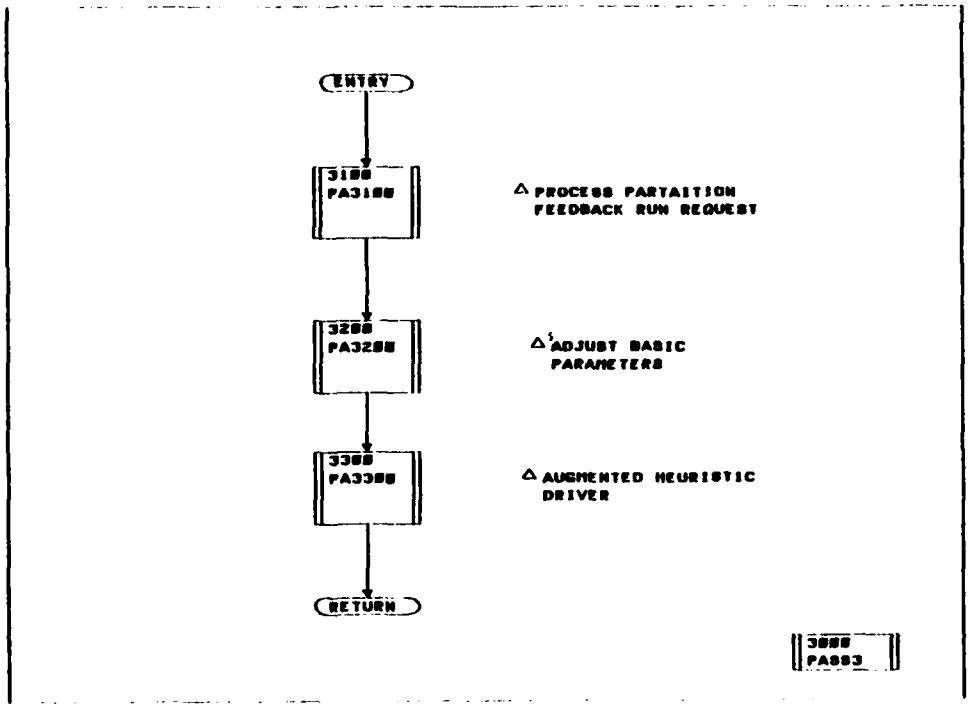
CASE	TASK	PROC1 D.C.	PROC2 D.C.
BASIC INPUTS	T1 T2	5 2	3 4
CASE 1 SWAP CONDITION	T1 T2	✓	 ✓
CASE 2 REDUCE PROCESSOR CONDITION	T1 T2	✓ ✓	✓ ✓

AD-A096 456 TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/G 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
FEB 81 S J CLYMER F33615-78-C-0013
UNCLASSIFIED AFHRL-TR-80-42-PT-2 NL

2 OF 4
AD A
096456

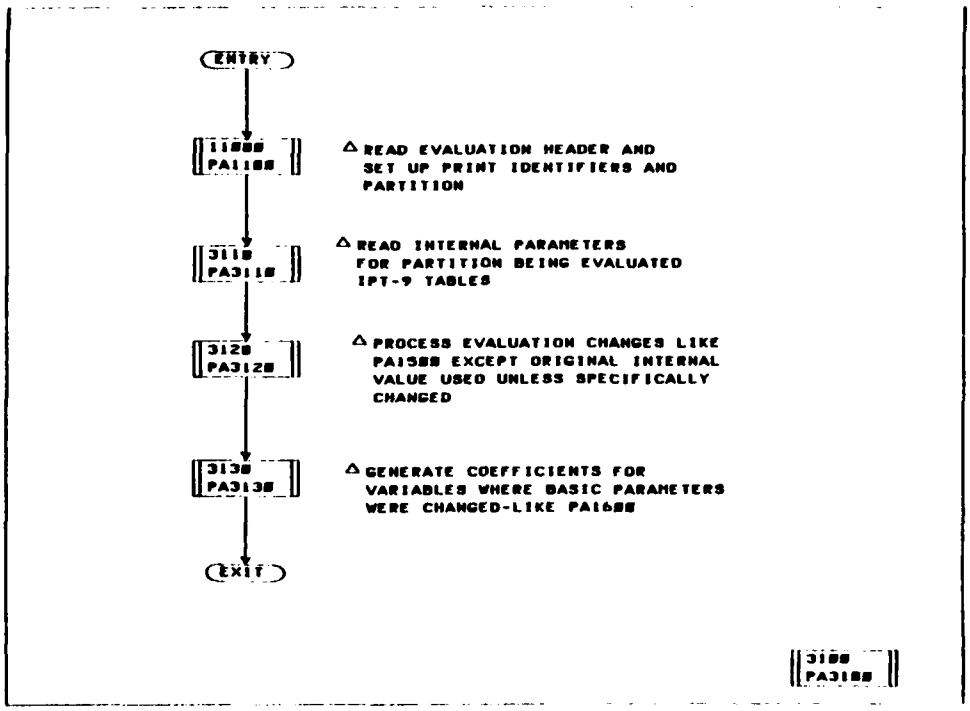

DEALS
ENTRY
'I'
1
DO (for L
=1 to NT)
'F'
'T'
'C'
1A
2530
PA2530
PROCESS
TASK
CHANGE
LIST
RETURN
t=TADCI(L)
FETCH TASK
INDEX
TADCS(t) .LE.
TADCG(t)
IS PREDICTED
DEVELOPMENT
COST LESS THAN
USER SUPPLIED
COST?
TADCP(t) .GT. 1
IS MORE THAN
ONE PROCESSOR
ASSIGNED FOR
THIS TASK?
2522
PA2522
HETEROGENEOUS?
2521
PA2521
REDUCED
COST
POSSIBLE?
2524
PA2523
HOMOGENEOUS
POSSIBLE?
2523
PA2523
REDUUCED #
POSSIBLE?
2525
PA2525
INSERT TASK
CHANGE LIST
2520
RDCOST
DATE 18-DEC-79 ID DEALS SEC PPD-2520 PAGE 1

DEALS

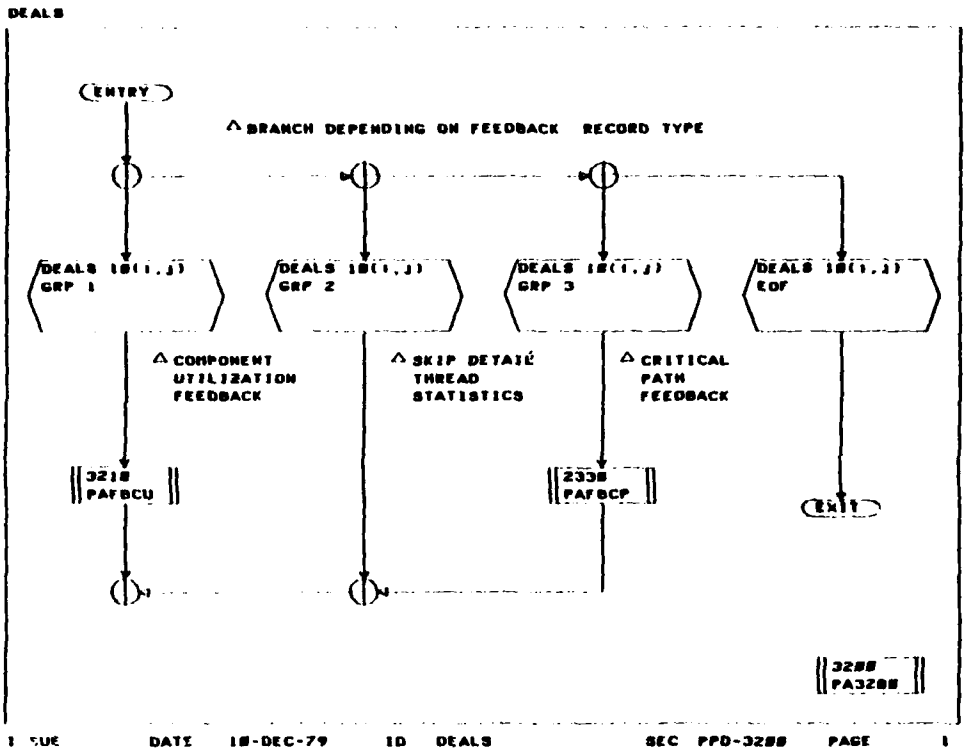


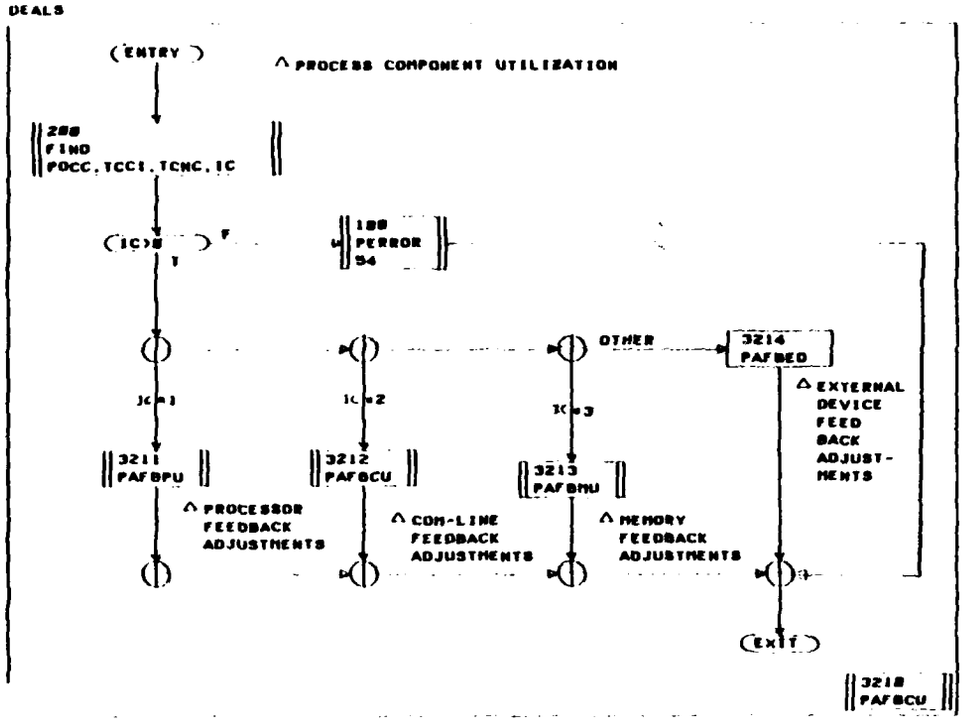
ISSUE DATE 28-NOV-79 ID DEALS SLC PPU-3000 PAGE 1

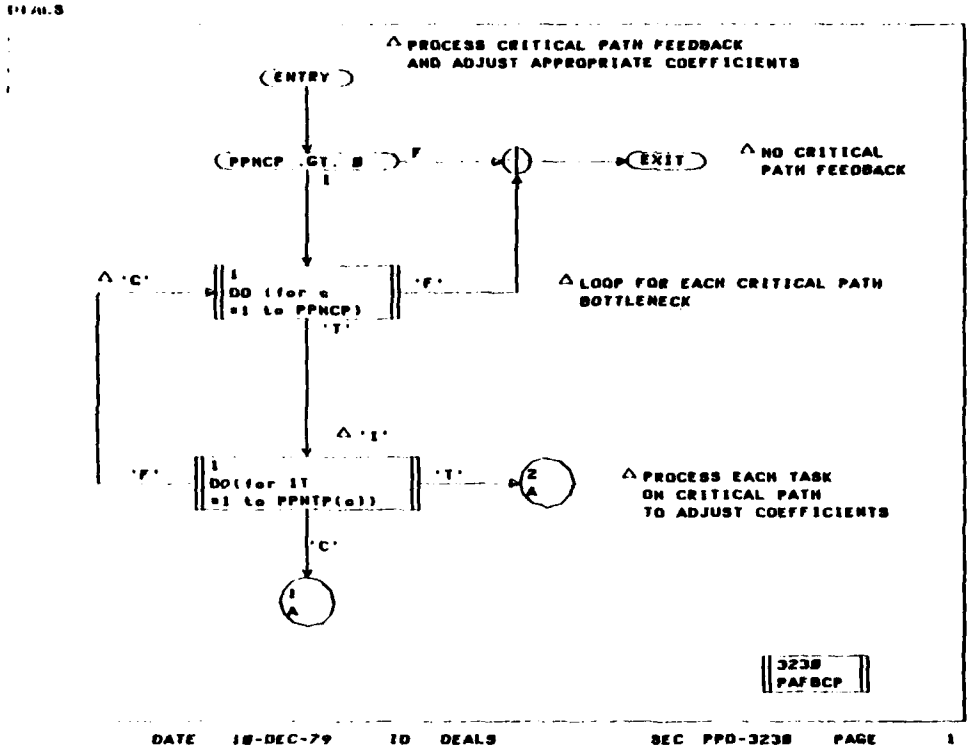
DEALS



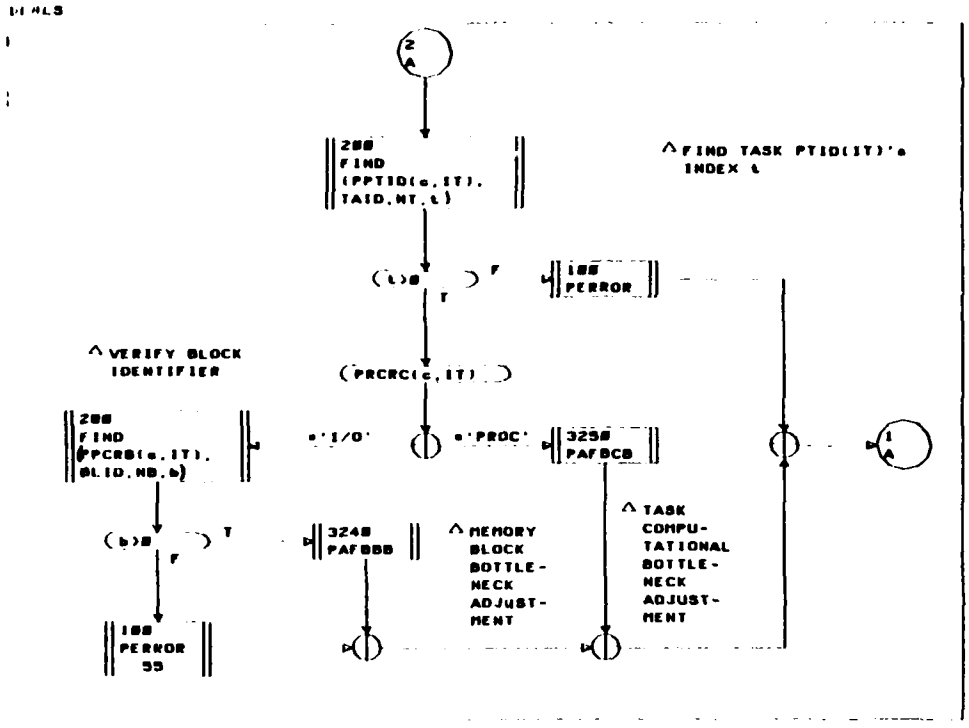
ISSUE DATE 10-DEC-79 ID DEALS SEC PPD-3100 PAGE 1


DEALS
ENTRY
BRANCH DEPENDING ON FEEDBACK RECORD TYPE
DEALS 10(1,J)
GRP 1
DEALS 10(1,J)
GRP 2
DEALS 10(1,J)
GRP 3
DEALS 10(1,J)
EOF
COMPONENT
UTILIZATION
FEEDBACK
SKIP DETAIL
THREAD
STATISTICS
CRITICAL
PATH
FEEDBACK
3210
PAFBCU
2330
PAFBCP
EXIT
3200
PA3200
ISSUE DATE 10-DEC-79 ID DEALS SEC PPD-3200 PAGE 1


DEALS
(ENTRY)
PROCESS COMPONENT UTILIZATION
200
FIND
POCC,TCC1,TCNC,IC
(IC>0)
F
T
100
PERROR
54
IC=1
IC=2
IC=3
OTHER
3214
PAFBED
EXTERNAL
DEVICE
FEED
BACK
ADJUST-
MENTS
3211
PAFBPU
3212
PAFBCU
3213
PAFBMU
PROCESSOR
FEEDBACK
ADJUSTMENTS
COM-LINE
FEEDBACK
ADJUSTMENTS
MEMORY
FEEDBACK
ADJUSTMENTS
(EXIT)
3218
PAFBCU
IE DATE 18-DEC-79 ID DEALS SEC PPD-3218 PAGE 1



DATE 18-DEC-79 ID DEALS SEC PPD-3238 PAGE 1


2
200
FIND
(PPTID(c,IT),
TAID,NT,t)
FIND TASK PTID(IT)'s
INDEX t
(t>0)
F
T
100
PERROR
VERIFY BLOCK
IDENTIFIER
(PRCRC(c,IT))
200
FIND
(PPCRB(c,IT),
BLID,NB,b)
c'I/O'
c'PROC'
3250
PAFBCB
1
(b>0)
T
F
3240
PAFBBB
MEMORY
BLOCK
BOTTLE-
NECK
ADJUST-
MENT
TASK
COMPU-
TATIONAL
BOTTLE-
NECK
ADJUST-
MENT
100
PERROR
55

REPORT GENERATOR DEMO

PURPOSE: TO PRESENT PARTITION SOLUTION FOR USER EVALUATION AND ANALYSIS

PROBLEM: DIFFERENT USERS HAVE DIFFERENT NEEDS

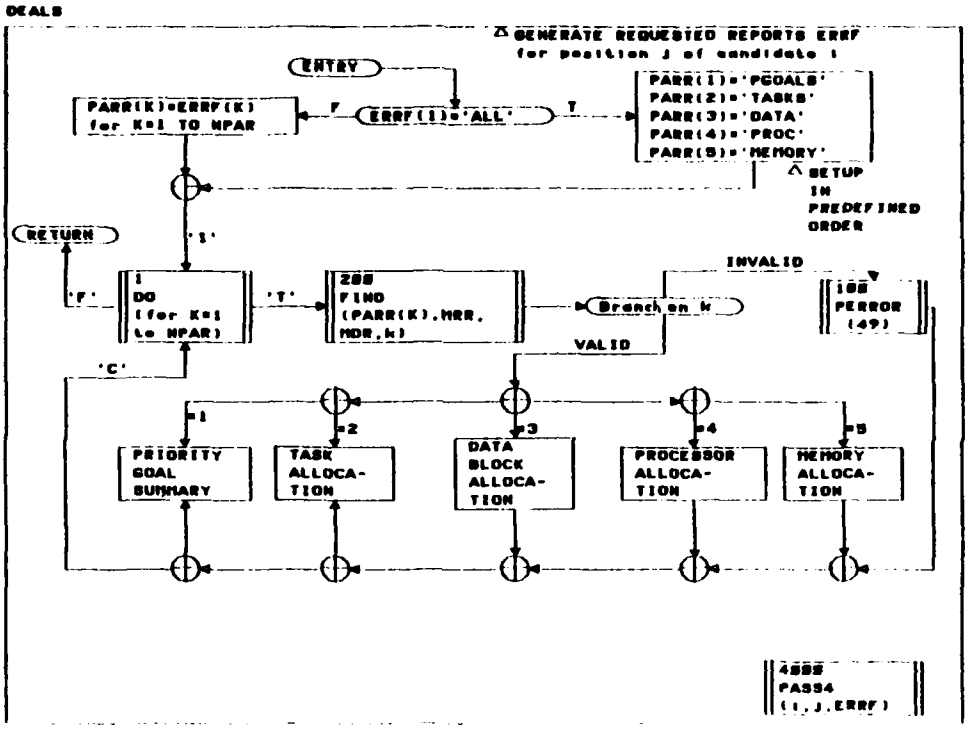
SOLUTION: FLEXIBLE REPORT GENERATOR DESIGN

- MAINTENANCE OF A MASTER SET OF REPORTS
- USER SELECTED AND ORDERED REPORT GENERATION

REPORT GENERATOR DEMO

FEASIBILITY ISSUES

- SOLUTION DATA BASE FORMAT
  - NUMBER OF PARTITIONS SAVED
  - MULTIPLE FILES WITH REORDERED RECORDS VERSUS TEMPORARY FILE SORTS AND/OR CROSS INDEXED LINKED LISTS
- HARDCOPY VERSUS INTERACTIVE DISPLAY


DEALS
GENERATE REQUESTED REPORTS ERRF
for position J of candidate I
ENTRY
PARR(K)=ERRF(K)
for K=1 TO NPAR
F
ERRF(I)='ALL'
T
PARR(1)='PGOALS'
PARR(2)='TASKS'
PARR(3)='DATA'
PARR(4)='PROC'
PARR(5)='MEMORY'
SETUP
IN
PREDEFINED
ORDER
RETURN
'1'
'F'
1
DO
(for K=1
to NPAR)
'T'
200
FIND
(PARR(K),MRR,
MDR,K)
Branch on K
INVALID
100
PERROR
(49)
VALID
'C'
=1
=2
=3
=4
=5
PRIORITY
GOAL
SUMMARY
TASK
ALLOCA-
TION
DATA
BLOCK
ALLOCA-
TION
PROCESSOR
ALLOCA-
TION
MEMORY
ALLOCA-
TION
4000
PASS4
(I,J,ERRF)

REPORT GENERATOR DEMO

INITIAL MASTER REPORT FORMATS

- PRIORITY GOAL SUMMARY
- TASK ALLOCATION
- DATA BLOCK ALLOCATION
- PROCESSOR ALLOCATION
- MEMORY ALLOCATION

PRIORITY GOAL SUMMARY DEMO

PURPOSE: TO PROVIDE MAJOR PARTITION MEASUREMENTS IN TERMS OF EVALUATION GOALS AND PRIORITIES

PROBLEM: CLEARLY INDENTIFY PRIORITIES, UNITS OF MEASURE, TOLERANCES, LEVEL OF ACHIEVEMENT, AND CONTRIBUTING COMPONENTS FOR A GIVEN PARTITION ALLOCATION

TASK ALLOCATION DEMO

PURPOSE: TO PROVIDE PARTITION ALLOCATION OF EACH TASK IN TERMS OF ASSIGNED PROCESSORS AND TASK I/O BLOCK MEMORY SOURCES

PROCESSOR ALLOCATION SUMMARY DEMO

PURPOSE: TO SUMMARIZE PROCESSOR ALLOCATION VIA ASSIGNED TASK MIX AND UTILIZATION PARAMETERS

DATA BLOCK ALLOCATION SUMMARY DEMO

PURPOSE: TO PROVIDE MAPPING OF EACH DATA BLOCK AS ALLOCATED TO MEMORIES OF CANDIDATE CONFIGURATION AND CROSS REFERENCE TO PROCESSOR COMMUNICATIONS

MEMORY ALLOCATION SUMMARY DEMO

PURPOSE: TO SUMMARIZE MEMORY ALLOCATION VIA ASSIGNED DATA BLOCK MIX AND UTILIZATION PARAMETERS

C.2 SAMPLE INPUTS

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITION NUMBER ___Ø

FILE	IDENTIFIER
COMPUTATIONAL INTERFACE REQUIREMENTS	INTERFACE DEFINITION
BASELINE APPLICATION COMPONENTS	SAMPLE APPLICATION
CANDIDATE CONFIGURATION COMPONENTS	SAMPLE CONFIGURATION
BASELINE PARTITIONING LOAD	GLOBAL LOAD EXAMPLE
TECHNOLOGY DATA BASE	HYPOTHETICAL TECH DB

EVALUATION RUN IDENTIFIER GLOBAL PARTITION EX

GLOBAL EVALUATION FACTORS

PRIORITY	ORDER	GOAL	UPPER LIMIT	COEFFICIENT LEVELS	MAXIMUM ITERATIONS
PROCESSOR UTILIZATION (% BUSY)	1	40	60.0	(AVERAGE) WORST CASE	10
MEMORY UTILIZATION (% OCCUPIED)	2	40	60.00	(AVERAGE) WORST CASE	10
DEVELOPMENT COST (PERSON YEARS)	3	3	4.5	AVERAGE (WORST CASE)	5

COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
PU	86-PROC	A	8	CUSTOM-VIS	ASSEMBLER	G
			FORTRAN IV	MACRO-ASM		
PU	SPC	SPC	3	ASPT-DIS	MICRO	
IC	VIOC	CONSOLE A				
IC	VIOC	CONSOLE B				
CL	ASYNC-I/O	EIO-1	PU	A		G
			IC	CONSOLE A		
CL	ASYNC-I/O	EIO-2	PU	A		G
			IC	CONSOLE B		
MM	86-MEM	MG	KWRD	48		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, ···	OPTION 2, 5, 8, ···	OPTION 3, 6, 9, ···	CONTINUE
TYPE	DEVICE					
CL	MTLINK-86	EID-3	PU	A		C
			PU	SPC		
CL	HSD	EID-4				
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONFIGURATION

PROPOSED DEVICES TO COMPLIMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COMLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
PU	XYZ32/75	A1	8	OS-XYZ-2R	FORTRAN IV	C
			JOVIAL J73	ASSEMBLER	FORTRAN 77	
PU	XYZ32/75	B1	3	OS-XYZ-2R	FORTRAN IV	C
			JOVIAL J73	ASSEMBLER		
MM	32-MEM	M1	KWRD	32		
MM	32-MEM	M2	KWRD	32		
MM	32-MEM	M3	KWRD	32		
MM	32-MEM	M4	KWRD	8		
MM	32-MEM	M5	KWRD	8		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONFIGURATION

PROPOSED DEVICES TO COMPLIMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COMLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ···	OPTION 2, 5, 8, ···	OPTION 3, 6, 9, ···	CONTINUE
TYPE	DEVICE					
CL	MBUS	C1	PU	A1		C
			MM	B1		
CL	MBUS	C2	PU	B1		C
			MM	M2		
CL	MBUS	BUS2	PU	A1		C
			PU	B1		C
			MM	M3		
CL	MBUS	BUS1A	PU	C1		C
			MM	M4		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONFIGURATION

PROPOSED DEVICES TO COMPLIMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COMLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ···	OPTION 2, 5, 8, ···	OPTION 3, 6, 9, ···	CONTINUE
TYPE	DEVICE					
CL	MBUS	BUS1B	PU	A1		C
			MM	M5		
CL	HSD	HSD	PU	A1		C
			PU	A		
CL	86MBUS	BUS3	PU	A		
			MM	M6		
CL	HSD	EJD-4	PU	A1		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

PROCESSOR: XYZ32/75 BYTE = 8 BITS WORD = 4 BYTES

OPERATING SYSTEM: OS-XYZ-2B CYCLE TIME: 0.09 μS/WORD ACCESS TIME: μS/WORD

MULTI TASK LEVELS: 64

PRIORITY LEVELS: 64

	SIZING		UNITS	
ADDRESSABLE MEMORY: 4	K	(M)	BYTES	(WORDS)
OPERATING SYS. MEMORY: 48	(K)	M	BYTES	(WORDS)
SUPPORT LIBRARY MEMORY: 20	(K)	M	BYTES	(WORDS)

LANGUAGES

1 ASSEMBLER 6 BASIC
2 FORTRAN IV 8 COBOL
3 JOVIAL J73 7 MACRO-ASM
4 FORTRAN 77 8

MULTI TASKING FEATURES AND RESOURCES

LEVEL (1 to)	MAX TASKS	SERVICED P - PRIORITY C - CIRCULAR F - FIFO	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)			ENABLEMENT RESOURCE MANAGEMENT CIRCLE TYPE(S) TIME	SLAVE	DATA	FREQUENCY TIMES/SECOND	OVERHEAD/ ENABLEMENT
1-54		F	(R)	NR	B	T	S	D		
55-63		F	R	(NR)	B	T	S	D		
64-64		F	R	NR	(B)	T	S	D		
ALL-	255		R	NR	B	(T)	(S)	(D)		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		

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TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

PROCESSOR: 86-PROC

BYTE = BITS

WORD = BYTES

OPERATING SYSTEM: CUSTOM-VIS

CYCLE TIME: μS/WORD

ACCESS TIME: μS/WORD

MULTI TASK LEVELS: 8

PRIORITY LEVELS: 4

	SIZING		UNITS	
ADDRESSABLE MEMORY:	K	M	BYTES	WORDS
OPERATING SYS. MEMORY:	K	M	BYTES	WORDS
SUPPORT LIBRARY MEMORY:	K	M	BYTES	WORDS

LANGUAGES

1 ASSEMBLER
2 FORTRAN IV
3 MACRO-ASM
4
5
6
7
8

MULTI TASKING FEATURES AND RESOURCES

LEVEL 1 to 1	MAX TASKS	SERVICED P – PRIORITY C – CIRCULAR F – FIFO	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)			ENABLEMENT RESOURCE MANAGEMENT CIRCLE TYPE(S) TIME	SLAVE	DATA	FREQUENCY TIMES/SECOND	OVERHEAD/ ENABLEMENT
1-2	1		R	NR	B	T	S	D		
3-4	8	F	R	NR	B	T	S	D		
5-7	8	F	R	NR	B	T	S	D		
8-8	1	F	R	NR	B	T	S	D		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		
-			R	NR	B	T	S	D		

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL.TECH.DB

PROCESSOR: SPC

BYTE = ___ BITS

WORD = ___ BYTES

OPERATING SYSTEM: ASPT-DIS

CYCLE TIME: ___ μS/WORD

ACCESS TIME: ___ μS/WORD

MULTI TASK LEVELS: 3

PRIORITY LEVELS: 3

	SIZING		UNITS	
ADDRESSABLE MEMORY:	K	M	BYTES	WORDS
OPERATING SYS. MEMORY:	K	M	BYTES	WORDS
SUPPORT LIBRARY MEMORY:	K	M	BYTES	WORDS

LANGUAGES

1 MICRO
2
3
4
5
6
7
8

MULTI TASKING FEATURES AND RESOURCES

LEVEL i to j	MAX TASKS	SERVICED P – PRIORITY C – CIRCULAR F – FIFO	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)			ENABLEMENT RESOURCE MANAGEMENT CIRCLE TYPE(S) TIME	SLAVE	DATA	FREQUENCY TIMES/SECOND	OVERHEAD/ ENABLEMENT
1-1	1		R	NR	B	T	S	D		
2-2	2	C	R	NR	B	T	S	D		
3-3	2	C	R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		
			R	NR	B	T	S	D		

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

MEMORY DEVICE DEFINITION

IDENTIFIER: 32-MEM-900

TYPE: ROM (RAMM) RRAM SM WCS

CIRCLE ONE

ADDRESSABLE UNITS

ID	UNIT SIZE		READ (FETCH)			WRITE (STORE)		
	DATA BITS	ERROR BITS	ACCESS (NANO SEC)	CYCLE (NANO SEC)	MAX UNITS READ	ACCESS (NANO SEC)	CYCLE (NANO SEC)	MAX UNITS WRITTEN
WORD	32	4		900			900	
BYTE	8	1		900			900	
HWRD	16	2		900			900	

TECHNOLOGY DATA BASE IDENTIFIER [illegible]

COMMUNICATION LINK DEVICE

DEVICE IDENTIFIER	BASIC TRANSFER [illegible] MAX UNITS MAX RATE (UNITS/SEC)	INTERFACING DEVICE ATTRIBUTES					
		TECH TYPE	DEVICE IDENTIFIER	TRANSMIT UNIT	TRANSMIT RATE	RECEIVE UNIT	RECEIVE RATE
HSD	32 B[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	65.5[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MBUS	32 Bits	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

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BASELINE SOFTWARE APPLICATION IDENTIFICATION [illegible]

DATA BLOCK DEFINITIONS

ID	LEVEL	DISCIPLINE	SYSTEM INTERFACE DEVICE	MAXIMUM RECORDS	MINIMUM		RECORD SIZE IN WORDS		
					BITS/ BYTE	BYTES/ WORD	MINIMUM	AVERAGE	MAXIMUM
PAOL	S	RAN	MM-M3	128	8	4	1	1	1
DIGLITE	S	RAN	MM-M3	256	8	4	1	1	1
CADUT	S	CBUF	CL-HSD	2	8	4	128	128	128
NORJU	S	RAN	CL-HSD	100	8	4	1	1	1
MODPLIST	S	RAN	CL-HSD	20	8	4	1	1	1
CATPT	S	CBUF	CL-HSD	2	8	4	128	128	128
DYNDATA	S	RAN	CL-HSD	8192	8	4	1	1	1
SIMPOS	S	CBUF	CL-EIO-4	2	8	4	128	128	128
RAMPOS	S	CBUF	MM-M1	2	8	4	128	128	128
GL	S	RAN	-	1024	8	4	1	1	1
[illegible]	S	RAN	-	512	8	4	1	1	1
[illegible]	S	RAN	-	512	8	4	1	1	1
[illegible]	L	RAN	-	512	8	4	1	1	1
DYNDATASW	S	RAN	MM-M3	1	8	4	1	1	1
			-						

BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK T1-3 ENABLEMENT TYPE: TIME DATA Q / MASTER TASK: MAXIMUM TIME:

OVERLAY YES (NO) LANGUAGE: MESSEMBLER (IF DATA) (IF SLAVED) FREQUENCY: 30

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
SIMIE	1	1	1	SIMPOS	(I)IO	(S)AE	ALL		
CONIE	1	0	1	RAWPOS	(I)IO	(S)AE	0	0	2
[illegible]	1	1	1	DIRLITE	(I)O	SAE	0	128	256
[illegible]	1	1	1	PAOL	IUO	SAE	128	128	128
				G1	(I)O	SAE	512	512	1024
				DYNDATA	IUO	(S)AE	ALL		
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

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BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK T1-6

OVERLAY: YES (NO)

ENABLEMENT TYPE: SLVD

LANGUAGE: FORTRAN IV

MASTER TASK: T1-3
(IF SLAVED)

MAXIMUM TIME:

FREQUENCY: 33

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]	1	1	1	G1	(I)UO	(S)AE	10	20	40
VIMMA	1	1	1	CAIPT	IU(O)	S(A)E	128	128	256
CADCOSMOT	1	1	1		IUO	SAE			
SALPCAIPT	1	1	1		IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK: A7-13 ENABLEMENT TYPE: SLVD MASTER TASK: T4-6 (IF SLAVED) MAXIMUM TIME:

OVERLAY: YES (NO) LANGUAGE: FORTRAN IV FREQUENCY: 37

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]				DYNDATA	IUO	SAE	1024	2048	4096
[illegible]				G1	IUO	SAE	200	512	512
[illegible]				ADATA	IUO	SAE	200	512	1024
[illegible]				DYNDATASW	IUO	SAE	0	1	1
[illegible]		0			IUO	SAE			
[illegible]					IUO	SAE			
[illegible]					IUO	SAE			
[illegible]					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

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BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK 87-13 ENABLEMENT TYPE: SLVD MASTER TASK: T4-6 (IF SLAVED) MAXIMUM TIME:

OVERLAY: YES (NO) LANGUAGE: FORTRAN FREQUENCY: 5

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]				DYNDATA	IUO	SAE	1024	2048	4096
[illegible]				G1	IUO	SAE	200	512	512
[illegible]				[illegible]	IUO	SAE	200	512	1024
[illegible]				DYNDATASW	IUO	SAE	0		
[illegible]		0			IUO	SAE			
[illegible]					IUO	SAE			
[illegible]					IUO	SAE			
[illegible]					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

BASELINE SOFTWARE APPLICATION IDENTIFICATION [illegible]

TASK DEFINITION

TASK: [illegible] ENABLEMENT TYPE: [illegible] / MASTER TASK: [illegible] (IF SLAVED) MAXIMUM TIME: [illegible]

OVERLAY: YES (NO) FREQUENCY: [illegible]

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	(I)O	(S)AE	[illegible]	[illegible]	[illegible]
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

[illegible] FURNISHED [illegible]

BASELINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

TASK DEFINITION

TASK T14816 ENABLEMENT TYPE: SLVD MASTER TASK: T4-1 MAXIMUM TIME:

OVERLAY: YES (NO) LANGUAGE: FORTRAN IV (IF SLAVED) FREQUENCY:

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]	1	1	1	G1	(IUO)	(SAE)	10	50	100
[illegible]	2	2	10	COMDATA	(IUO)	(SAE)	10	60	120
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

BASELINE SOFTWARE APPLICATION IDENTIFICATION [illegible]

TASK DEFINITION

TASK: [illegible] ENABLEMENT TYPE: [illegible] MASTER TASK: [illegible] (IF SLAVED) MAXIMUM TIME: [illegible]

OVERLAY: YES (NO) FREQUENCY: [illegible]

INSTRUCTION MIX				TASK I/O PER EXECUTION					
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN	AVE	MAX
[illegible]				[illegible]	IUO	SAE	ALL		
[illegible]				AORIL	IUO	SAE		[illegible]	[illegible]
[illegible]				MODPLIST	IUO	SAE	[illegible]	[illegible]	[illegible]
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			
					IUO	SAE			

* CIRCLE ONE PER ENTRY

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EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT VALUE IF APP.
F	T	T1-3	A1	30
I	T	T4-5	A1	30
I	T	A7-13	A1	30
I	T	T17-19	A1	30
P	T	T17-19	B1	30
I	T	B7-13	B1	30
I	T	T14&16	B1	30
F	T	T15	B1	15
F	T	T15	A1	15

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT	
			IDENTIFIER	VALUE IF APP.
F	D	PADL	M3	
F	D	DRLITE	M3	
F	D	CADUT	M4	
F	D	ADBJL	M3	
F	D	MODPLIST	M3	
F	D	CAIPT	M4	
F	D	DYNDATA	M3	
F	D	GIMPOS	M1	
F	D	RAWPOS	M1	

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT VALUE IF APP.
F	D	G1	M3	
I	D	ADATA1	M1	
I	D	BDATA1	M2	
I	D	BOMBDATA	M3	
F	D	DYNDATASW	M3	

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK BAOL ON PROCESSOR XY[illegible]/75

USING [illegible] OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	2000			11111		
WORST CASE				13333		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK BLR ON PROCESSOR XX332/75
USING [illegible] OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	8.00			1.111		
WORST CASE				1.667		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH. DB

INSTRUCTION BENCHMARK AMBSTRAIMP ON PROCESSOR XY7321/75

USING OS-XYP-2P OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	800	31	140	70		
WORST CASE						
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK BMP1 ON PROCESSOR XYZ321/75

USING OS-XYZ-28 OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	3,999			2222.		
WORST CASE						
LANGUAGE FACTORS:						
1				2222.		
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK CATCOSMAT ON PROCESSOR XYZ321/75
USING OS-XYZ-2B OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	3,000			2222		
WORST CASE				2222		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK CONTI ON PROCESSOR XYZ321/75

USING OS-XYZ-23 OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	4800			4444	0	0227
WORST CASE				4444		0050
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK DRLITADD ON PROCESSOR XYZ32/75
USING OS-XYZ-2B OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	800			556	5	16
WORST CASE				556		25
LANGUAGE FACTORS.						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH. DB

INSTRUCTION BENCHMARK FADCOM ON PROCESSOR XYZ32/75

USING OS-XYZ-2P OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	1200			////		
WORST CASE				////		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK HOOTDYN ON PROCESSOR XY7321/75

USING OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	1200	208	208	416	1	.01
WORST CASE						
LANGUAGE FACTORS:						
1 FORTRAN IV	1	1	1	1	1	1
2 ASSEMBLER	.8	.7	.7	.7	4.8	1
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH II

INSTRUCTION BENCHMARK MAP ON PROCESSOR XYZ32/75
USING OS-XYZ-32 OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	800			555		
WORST CASE				555		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH. DB

INSTRUCTION BENCHMARK MMSADN ON PROCESSOR XYZ32/75

USING OS-XYZ-28 OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	800			555		
WORST CASE				555		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK PDYN ON PROCESSOR XY232/75

USING OS-XY2-2B OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURANCE
AVERAGE	800			555		
WORST CASE				555		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK PEV

ON PROCESSOR XYZ32/75

USING OS-XYZ-2B OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURANCE
AVERAGE	120			111		
WORST CASE				111		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK RWK ON PROCESSOR XY7321/75

USING OS-XY7-3F OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURANCE
AVERAGE	3999			2222		
WORST CASE				2222		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH. DB

INSTRUCTION BENCHMARK RWVM

ON PROCESSOR XYZ 32/75

USING OS-XYZ-2A OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURANCE
AVERAGE	3000			2222		
WORST CASE				2222		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK SHIPCAIPT ON PROCESSOR XY732/75

USING OS-XY2-2B OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	120			111		
WORST CASE				111		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH 28

INSTRUCTION BENCHMARK [illegible] ON PROCESSOR [illegible]

USING [illegible] OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	1,000			[illegible]	1	.25
WORST CASE						
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER

INSTRUCTION BENCHMARK 73 ON PROCESSOR

USING OPERATING SYSTEM

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) STORES	FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	30				.9	.05
WORST CASE						
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

C.3 INTERMEDIATE VALUES

PROCESSOR BALANCE CASE 1

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
AL 1a	1	50	5	40	6	20	J = 1, IJT = 4, IJLIST = 1, 3, 4, 2
	2	10					K = 3
	3	25					
	4	15					
							Set Limit PTOL
	U_1 =	100	U_2 =	40	U_3 =	20	1. Amount to offload to meet limit
							$U_J - L_J = 100 - 75 = 25$
							2. Amount which K can take on
							$G_K - U_K = 60 - 20 = 40$
							3. Heuristic decision is to take minimum of
	1	50	5	40	6	30	{J offload amount, K's amount to goal}
	2	10					
	4	15			3	25	= minimum {25, 40} = 25
							Therefore, PTOL = 25
	U_1 =	75	U_2 =	40	U_3 =	45	Process candidate task list
	Note at this point U_1 meets absolute limit branch to general balance algorithm.						1. Find task utilization closest to PTOL. In this case, Task 3 is selected. Verify Task 3 can be performed on processor K = 3; i.e., all real-time constraints are met.
							2. Make full allocation if such a task exists.

AL - above limit heuristic GB - general balance heuristic

ISSUE DATE ID LOADBL SEC CASE 1 PAGE 1/4

PROCESSOR BALANCE CASE 1 CONTINUED

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
GB 1a	1	50	5	40	6	20	IJ = NP - NPGTL = 3 - 0 = 3
	2	10			3	25	IK = 1, ITER = 0
	4	15					CDPCDI = 3, 2, 1 (ranking with respect to goal deviation in descending order)
	U_1	= 75	U_2	= 40	U_3	= 45	
	U_1^1	= -15	U_2^1	= 0	U_3^1	= +15	Compute highest and lowest processor indices
							IHI = CDPCDI (IJ) = 1
							ILD = CDPCDI (IK) = 3
							Compute GPUSOL
							$= U_{ILD} - U_{IHI} = U_3 - U_1 = 15 - (-15) = 30$
							Perform convergence test
							GPUSOL .LE. GTOLPU
							$\Rightarrow 30 \leq 5$
							False continue to iterate
							ITER = ITER + 1 = 1
							Maximum iteration
							ITER .GT. MPITER
							1 .GT. 10
							False implies perform balance loop

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PROCESSOR BALANCE CASE 1 CONTINUED

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
GB 1a Con't	1	50	5	40	6	20	L = 3
	2	10			3	25	J = CDPCDI (L) = 1 processor to be offloaded
	4	15					
	U_1 =	75	U_2 =	40	U_3 =	45	Candidate task list IJT = 3, IJLIST = 1, 4, 2
	U_1^1 =	-15	U_2^1 =	0	U_3^1 =	+15	Set limit to offload = PTOL 1. Amount to balance between processors J and K $= \frac{U_K^1 - U_J^1}{2} = \frac{15 - (-15)}{2} = \frac{30}{2} = 15$ 2. Amount K and take on and not exceed goal $= G_K - U_K = G_3 - U_3^1 = 60 - 45 = 15$ 3. Minimum {balance value, limit value} = 15 Process candidate task list for task closest to 15% utilization on processor J -- in this case, task 4

PROCESSOR BALANCE CASE 1 CONCLUDED

INERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
GB 1a con't	1	50	5	40	6	20	Confirm task 4 can meet all real-time constraints if allocated to processor 3.
	2	10			3	25	
	4	15					If so make allocation.
	U_1 =	75	U_2 =	40	U_3 =	45	This is the case for this example as processors are identical and have one shared memory with no fixed or prohibited allocation of task 4.
	U_1^1 =	-15	U_2^1 =	0	U_3^1 =	+15	
	1	50	5	40	6	20	All processors at goal
	2	10			3	25	GPUSOL = 0
					4	15	RETURN
	U_1 =	60	U_2 =	40	U_3 =	60	
	U_1^1 =	0	U_2^1 =	0	U_3^1 =	0	

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PROCESSOR BALANCE CASE 2

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
AL 1	1	50	5	40	6	20	Same as Case 1 Except instruction block for task 3 must be moved to private memory for processor 3
	2	10					
	3	25					
	4	15					
	1	50	5	40	6	20	
	2	10			3	25	
	4	15					
GB 1a	1	50	5	40	6	20	Same as Case 1 Except instruction block for task 4 must be moved to private memory for processor 3
	2	10			3	25	
	4	15					
	1	50	5	40	6	20	
	2	10			3	25	
					4	15	

ISSUE DATE ID LOADBL SEC CASE 2 PAGE 1/1

PROCESSOR BALANCE CASE 3

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
AL 1a	X1	50	5	40	6	20	Same as Case 1 Except tasks 1 and 3 cannot be allocated to processor 3 and alternate task allocation is sought which is close to 25% (PTOL for AL1)
	2	10					
	X3	25					
	4	15					IJLIST = 4, 2
	U_1 =	100	U_2 =	20	U_3 =	20	IJT = 2
	1	50	5	40	6	20	Task 4 is selected and meets all real-time constraints and its instructions are moved to processor 3's private memory
	2	10			4	15	Note PR1 is still above limit. Continue task search for another potential task offload
	3	25					
	U_1 =	85	U_2 =	40	U_3 =	35	

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PROCESSOR BALANCE CASE 3 CONTINUED

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
A1b	*1	50	5	40	6	20	Reset PTOL - the amount to be offloaded
	2	10			4	15	$= \min\{U_1 - L_1, U_3^1\}$
	*3	25					$= \min\{10, 25\}$
	U_1 =	85	U_2 =	40	U_3 =	35	$= 10$
	U_1^1 =	-110	U_2^1 =	0	U_3^1 =	25	Search remaining candidate tasks for one closest to 10
	*1	50	5	40	6	20	= Task 2
	*3	25			4	15	Confirm task 2 can be performed on Processor 3 by moving instructions to private memory for processor 3
					2	10	Make allocation of task 2 to processor 3
	U_1 =	75	U_2 =	40	U_3 =	45	
	U_1^1 =	-15	U_2^1 =	0	U_3^1 =	+15	
	Note processor 1 is now at limit value. Go to balance loop.						

ISSUE DATE ID LOADBL SEC CASE 3 PAGE 2/4

PROCESSOR BALANCE CASE 3 CONTINUED

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
GB1	1	50	5	40	6	20	Ranks processor wrt goal utilization in descending order
	3	25			4	15	
					2	10	
	U_1 =	75	U_2 =	40	U_3 =	45	CDPCDI = 3, 2, 1
	U_1^1 =	-15	U_2^1 =	0	U_3^1 =	+15	NPGTL = NPGTL = 0
							None of the processors are above their limit
							ITER = 0
							IJ = NP - NPGTL = 3 - 0 = 3
							IK = 1
							Retrieve index to current high and low utilized processors
							IHI = CDPCDI (IJ) = CDPCDI (3) = 1
							ILO = CDPCDI (IK) = CDPCDI (1) = 3
							Check balance between high and low
							GPUSOL = CDPCD (ILO) - CDPCD (IHI) = +15 - (-15) = 30
							Compare with balance tolerance
							GPUSOL $\leq$ 5
							False continue to iterate
							ITER = ITER + 1 = 0 + 1 = 1

ISSUE DATE ID LOADBL SEC CASE 3 PAGE 3/4

PROCESSOR BALANCE CASE 3 CONCLUDED

ITERATION	PR1 TASK	PR1 UTIL	PR2 TASK	PR2 UTIL	PR3 TASK	PR3 UTIL	INTERMEDIATE CALCULATIONS
GB1	*1	50	5	40	6	20	Maximum iteration test
	*3	25			4	15	
					2	10	ITER .GT. 10
	U_1 =	75	U_2 =	40	U_3 =	45	No continue balance process
	U_1^j =	-15	U_2^j =	0	U_3^j =	+15	K = ILO least loaded processor remaining in balance loop
							L = IJ = 3 index to overloaded processor index
							J = CDPCDI (L) = CDPCDI (3) = 1
							CDPCD (K) .GT. CDPCD (J)
							CDPCD (3) .GT. CDPCI (J)
							True continue task offload process
							Build candidate task list to offload from processor j
							T3 fixed
							Leave Task 1
							Task 1 cannot be placed on 3
							Bottleneck condition is diagnosed

ISSUE DATE ID LOADBL SEC CASE 3 PAGE 4/4

MEMORY BALANCE CASE 1

ITERATION	M1 BLOCK	M1 UTIL	M2 BLOCK	M2 UTIL	INTERMEDIATE CALCULATIONS
AL1	1	10	4	20	$U_1 - L_1 = 80 - 70 = 10$ amount to make limit
	2	30			$(U_1 - U_2)/2 = (80 - 20)/2 = 30$ amount to balance
	3	40			$G_2 - U_2 = (60 - 20) = 40$ maximum M2 can take on
					Minimum {10, 30, 40} = 10
	U_1 =	80	U_2 =	20	Transfer block 1
GB1	2	30	4	20	All memories at or below limit switch to balance algorithm
	3	40	1	10	$\frac{1}{2}(U_1 - G_2) = (70 - 30)/2 = 20$ amount to balance
	U_1 =	70	U_2 =	30	$G_2 - U_2 = 60 - 30 = 30$ maximum M2 can take on
					Minimum {20, 30} = 20
					Minimum $\{\overset{\text{block 2}}{\lvert 30 - 20 \rvert}, \overset{\text{block 3}}{\lvert 40 - 20 \rvert}\} = \overset{\text{block 2}}{30}$
					Transfer block 2
GB2	3	40	4	20	$(U_2 - U_1)/2 = (60 - 40)/2 = 10$ amount to balance
			1	10	$G_1 - U_1 = 60 - 40 = 20$ maximum M1 can take on
			2	30	Minimum {10, 20} = 10
	U_1 =	40	U_2 =	60	Select block 1 to go to M1
	3	40	4	20	$U_2 - U_1 = 0$ implies "perfect" balance
	1	10	2	30	
	U_1 =	50	U_2 =	50	

AL - above limit iterations GB - memory goal balance iterations

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MEMORY BALANCE CASE 2

ITERATION	M1 BLOCK	M1 UTIL	M2 BLOCK	M2 UTIL	INTERMEDIATE CALCULATIONS
AL1	1	10	4	20	Same as Case 1
	2	30			
	3	40			
	U_1 =	80	U_2 =	20	
GB1	2	30*	4	20	$(U_1 - U_2)/2 = (70 - 30)/2 = 20$ balance amount
	3	40	1	10	$G_2 - U_2 = 60 - 30 = 30$ maximum to take on
	U_1 =	70	U_2 =	30	Minimum (20, 30) = 20
					Note: Block 2 cannot be transferred Block 3 will cause M2 to exceed goal hence a bottleneck situation appears to be encountered.
AL1 - SWAP	2	30	3	40	
	4	20	1	10	Swap check
	U_1 =	50	U_2 =	50	

	NET	M1	NET	M2
2 ⟷ 4	-30 + 20	-10	-20 + 30	+10
*2 ⟷ 1	-30 + 10	-20	-10 + 30	+20
*3 ⟷ 4	-40 + 20	-20	-20 + 40	+20
3 ⟷ 1	-40 + 10	-30	-10 + 40	+30

Alternate optimal swaps of 20 units added to M2

MEMBAL CASE 2 1/1

MEMORY BALANCE CASE 3

ITERATION	M1 BLOCK	M1 UTIL	M2 BLOCK	M2 UTIL	INTERMEDIATE CALCULATIONS
AL1	1	10	4	20	$U_1 - L_1 = 80 - 70 = 10$ amount to make limit
	2	30			$(U_1 - U_2)/2 = (80 - 20)/2 = 30$ amount to balance
	3	40			
	U_1 =	80	U_2 =	20	$G_2 - U_2 = (60 - 20) = 40$ maximum M2 can take on
					minimum {10, 30, 40} = 10
					Transfer Block 1
GB1	2	30	4	20	$(U_1 - U_2)/2 = (70 - 40)/2 = 15$
	3	40	1	20	$(G_2 - U_2) = (60 - 40) = 20$
	U_1 =	70	U_2 =	40	Minimum {15, 20}
					Without swap neither block can be moved
GB1 - SWAP	1	10	4	20	With swap trades
	3	40	2	30	
	U_1 =	50	U_2 =	50	

	NET	M1	NET	M2
2⟷4	-30 + 20 =	-10	-20 + 30 =	+10
*2⟷1	-30 + 10 =	-20	-20 + 30 =	+10
3⟷4	-40 + 20 =	-20	-20 + 40 =	+20
3⟷1	-40 + 10 =	-30	-20 + 40 =	+20

MEBAL CASE 3 1/1

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
A_{ti}	TARRF(t,i) of DEALS IPT-9 GRP-11	F10.5	= fraction of information input for task t from block i $= \frac{\text{TARR}(t,i,k)}{\text{BLMXR (TAIOB}(t,i))} = \frac{\text{Records Read}}{\text{Maximum Records for Block i}}$ Example: TASK: T1-3 BLOCK: DIRLITE RECORDS REFERENCED = 120 for average case MAXIMUM RECORDS = 256 $\text{TARRF}(t,i) = \frac{128}{256} = 0.5$ NOTE: It is permissible for values to exceed 1 when multiple references are made by a task.

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MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
a_{mpti}	MPSOL (m,p,e,3)	Nonnegative integer	= the number of times input block i of task t is input for task t on processor p from memory m This is a function of the current solution variables: TPMAP(t,p,1) of DEALS IPT9 GRP8 MPMAP(m,p,1) of DEALS IPT9 GRP9 MBMAP(m,b,1) of DEALS IPT9 GRP10 where b = TAIOB(t,i) of DEALS IPT9 GRP12 Actual implementation should consider a subroutine which computes this value for active solution entries as needed for decision making. The computation is more complex if duplicate blocks.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
α_{mp}		0,1	= 1 if access from memory m to processor p exists, i.e., there is at least one access link q for m and p = 0 if otherwise This switch may be computed by testing α_{mp} as follows: If ($\alpha_{mp} > 0$) Then $\alpha_{mp} = 1$ Else $\alpha_{mp} = 0$ NOTE: α_{mp} is design variable MPMAP(m,p,1) of DEALS IPT9 GRP9.

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
α_{mp}	MPMAP (m,p,l) of IPT9 GRP9	Real ≥ 0	= bits/sec transfer rate from memory m to processor p based on statistical composite of access links for p and m

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
B	NB of DEALS IPT9 GRP2	Positive Integer $1 \leq NB \leq MB$ where MB is maximum number of blocks as defined in DEALS IPT9 GRP1	= number of distinct storage blocks to be allocated to memories This variable is computed by PASS1 PPD-1310 ADDBLK. It includes all data and task instruction blocks.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
β	MB of DEALS IPT9 GRPI	Positive Integer	= maximum number of input and/or output blocks per task Specific algorithm implementation should provide a fixed upper limit or a dynamic computed upper limit as a function of the other major sizing variables P, T, B, Q, M

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
C_{tk}			= portion of task t which must be completed before the next dependent task in thread k may be enabled

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
c_{tp}	TPVAL(t,p,1) of DEALS IPT9 GRP8	Real > 0	= time for task t execution on processor p in seconds maintained to an accuracy of nanoseconds

Formula in English

$$= \text{Cycle Time} * \sum \left[\begin{array}{l} \text{Benchmark} \\ \text{instruction} \\ \text{mix (computa-} \\ \text{tional +} \\ \text{fetch wait +} \\ \text{store wait)} \\ \text{cycles} \end{array} \right] + \text{Time Enablement Overhead} + \text{Data Enablement Overhead} + \text{Slaved Enablement Overhead} + \text{Overlay Overhead}$$

Example from Sample Problem 2
Tasks T14 and 16 on Processor A1

$$= 9 * 10^{-7} * \left[1 * \overbrace{\left(\underset{416}{\text{Comp}} + \underset{208}{\text{Fetch}} + \underset{208}{\text{Store}} \right)}^{\text{HOODDYN}} + 2 * \overbrace{\left(\underset{70}{\text{Comp}} + \underset{31}{\text{Fetch}} + \underset{140}{\text{Store}} \right)}^{\text{BMBSTRAIMP}} \right] + 0 + 0 + 1 \times 10^{-6} + 0$$

$$= 0.0011836 \text{ sec}$$

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
D_t	TADCS(t)	Real ≥ 0	= development cost for task t in manyears $= \sum_{p=1}^{P} [d_{tp}\, x_{tp}$ one time development $+ \delta_{tp}\, x_{tp}$ resource management development $- d_{tp}\, y_{tp}]$ duplicate utilization This parameter is computed for the initial solution and recomputed for each change that is made by the heuristic tradeoffs.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
d_{tp}	TPVAL(t,p,4) of DEALS IPT9 GRP8	Real ≥ 0	= the cost coefficient for developing task t to run on processor p (independent of allocation) in manyears exclusive of duplicated charges and one-time charges d_{tp} may be calculated as needed as follows: TANIM(t) $= \sum_{i=1} (TAIMX(t,i,j) * TPDC(p,I,2,\ell))$ where TANIM(t) of DEALS IPT9 GRP12 = number of benchmark instruction for task t TAIMX(t,i,j) of DEALS IPT9 GRP12 = number of specification instruction i references; j = 2 → average number, j = 3 → worstcase number TPDC(p,I,2,ℓ) of DEALS IOPT-5 = development cost per instruction reference in language ℓ on processor p I = TAIMX(t,i,1) of DEALS IPT9 GRP12 ℓ = TASC(t) of DEALS IPT9 GRP12

EXAMPLE:

AVERAGE COST FOR TASK T1-3
ON PROCESSOR A1

i	BENCHMARK id	AVERAGE COUNT	PROCESSOR COST
1	SIMIF	1	0.2500
2	CONIF	0	0.0027
3	DRLITADJ	1	0.1600
4	T3	1	0.0500

Development Cost = 0.4600

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
D	GDCSOL of DEALS IPT9 GRP3	F10.2	= total partition development cost estimate in manyears $= \sum_{t=1}^{N_t} D_t$

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MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
δ_{tp}			= the cost coefficient for resource management of task t development on processor p. This is a function of the current partition solution and the established technology data base parameters for the processor and task enablement type. For example, a processor may currently limit the maximum number of tasks it can handle. If the solution tries to exceed this number, an additional development cost penalty must be added. This applies to enablement type disciplines as well. Those parameters related to development cost are in IOPT5 GRP3 as a function of processor and operating system.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
e_{tp}	TPMAP(t,p,1) of DEALS IPT9 GRP12	Integer .GE.0 .LE.TAFRQ(t) of DEALS IPT9 GRP12	= the number of task t executions on processor p for evaluation problem time period This is a major output of PASS2/PASS3.

MATH SYMBOL	DESGIN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
F_k	BLTIN(K,*) of DEALS IPT9 GRP13	Positive integers	= a task thread defined as a group of serially dependent tasks with the following notation: $F_k = \{f_{k1}, \ldots, f_{kG_k}\}$ where $f_{kg} \equiv$ BLTIN(k,g) of IPT9 GRP13 thread k task g's index for g = 1 to G_k $G_k \equiv$ BLTNT(k) of IPT9 GRP13 is the number of tasks in thread k

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
G_p	CDPGU(p) of DEALS IPT9 GRP4	Positive real 0 .LT. G_p .LE. 1.00	= goal utilization for processor p

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMEERS
g_m	CDMGU(m)	Positive real 0 .LT. g_m .LE. 1	= goal allocation for memory m

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
h_b		Integer ≥ 1 $\leq$ MH of IPT 9 GRP 1	= number of memories where block b is stored $= \sum_{m=1}^{NM} MBMAP(m,b,1)$ MBMAP is probably best handled as a linked list (for each block) of active allocation due to anticipated sparse density. MBMAP of IPT9 GRP10

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
I_t		Nonnegative integer	= number of distinct input blocks for task t $= \sum_{i=1}^{TANIO(t)} f(TAHBR(t,i))$ where $f(TAHBR(t,i)) \begin{cases} = 1 \text{ if } TAHBR(t,i) = 1 \\ = 1 \text{ if } TAHBR(t,i) = 3 \\ = 0 \text{ otherwise} \end{cases}$ TAHBR(t,i) and TANIO(t) are in IPT9 GRP12.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
i_{ti}	TAIOB(t,i) of IPT9 GRP12	Positive integer	= global data block index for task t input block i provided that TAHBR(t,i) = 1 or 3 TAHBR(t,i) of IPT9 GRP12

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
L_m	CDMSZ(m) of DEALS IPT9 GRP5	Real > 0	= length of memory m in bits CDMSZ(m) = TMAUP(m,u,2) * CDMSA(m) where u = CDMSU(m) of DEALS IPT9 GRP5 = index to unit of measure for memory m's sizing TMAUP(m,u,2) of DEALS IOPT5 GRP5 = bits per unit u CDMSA(m) of DEALS IPT9 GRP5 = number of u units available on memory m

Example:

MEMORY: MT DEVICE: 32-MEM
UNIT: 8BB AMOUNT: 32768

L_m = 8 * 32768 = 262144

TMAUP CDMSA

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
ℓ_{mb}	MBVAL(m,b) of IPT9 GRP10		= length in bits of block b when stored in memory m = BLMXR(b) maximum records * BLRW(b,3) maximum generic words/record * ⌈(BLRBI(b) ceiling of bits per byte * BLRBY(b)) bytes per word } = bits/word divided by addressable unit which can best handle the load /TMAUP(k,u,2)⌉ where I = ⌈x⌉ = ceiling of x x → I i.e., 0.9 1 1.0 1 1.1 2 BLMXR, BLRW, BLRBI, and BLRBY of IPT9 GRP11 TMAUP(k,u,2) of IOPT5 GRP5 k is memory device associated with memory m u is addressable unit best suited

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
M	NM of IPT9 GRP2	Positive integer ≤ MM of IPT9 GRP1	= number of memories This is accumulated by PASS1 in DEALS PPD 12, 13 ADDMM (add memory definition). In Sample Problem: 1 NM = 3 2 NM = 6

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
N_t			= number of times task t is to be executed during the evaluation interval τ for which partitioning is being done = TAFRQ(t) * BLPER where TAFRQ(t) of IPT9 GRP12 is iteration of task t per sec BLPER of IPT9 GRP13 is evaluation period in sec Sample Problem No. 2 TAFRQ(1) = iteration rate for task T1-3 = 30 BLPER = 1 sec N_t = TAIT(t) * BLPER

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
O_t		Nonnegative integer	= number of distinct output data blocks for task t $= \sum_{o=1}^{TANIO(t)} f(TAHBR(t,o))$ where $f(TAHBR(t,o)) \begin{cases} = \text{ if } TAHBR(t,o) = 2 \\ = 1 \text{ if } TAHBR(t,o) = 1 \\ = 0 \text{ otherwise} \end{cases}$ TAHBR(t,o) and TANIO(t) are in IPT9 GRP12.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
O_{to}	TAIOB(t,i) of IPT9	Positive integer	= global data block index for task t output block o = TAIOB(t,i) provided that TAHBR(t,i) = 2 or 3 TAHBR of IPT9 GRP12

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
P	NP of IPT9 GRP2	Positive integer ≤ MP of IPT9 GRP1	= number of processors NP is accumulated by PASS1 in DEALS PPD 1211 ADDPU (add processor unit definition). In sample problems No. 1 NP = 2 No. 2 NP = 4

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
Q	NQ of IPT9 GRP2	Positive integer	= number of communication links NQ is accumulated in PASS1 by DEALS PPD 1212 ADDCL (add communication link).

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MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
R_{tp}	TPOSM(p,9) of DEALS IOPT5 GRP3	Real	= resource task management coefficient for task t on processor p which is independent of enablement rate prorated for a second of processor time

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
r_{tp}		Real	= resource task management per task t execution on processor p in seconds with accuracy to nanoseconds dependent on task enablement discipline if time enabled r_{tp} = TPOSM(p,4) of IOPT5 GRP3 if data enabled r_{tp} = TPOSM(p,6) of IOPT5 GRP3 if slaved r_{tp} = TPOSM(p,8) of IOPT5 GRP3

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINTIION AND RELATED PARAMETERS
S_t	TAMET(t) of IPT9 GRP12	Real	= maximum time limit per task t execution in seconds with accuracy to microseconds

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
s_{mb}	MBMAP(m,b,1) of IPT9 GRP10	0,1	= 1 if memory storage m contains block b = 0 otherwise This is a major output of PASS2 and PASS3.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
T	NT of IPT9 GRP2	Positive integer ≤MT of IPT9 GRP12	= number of tasks to be allocated to processors NT is accumulated by PASS1 DEALS PPD 1320 ADDTSK (add task definition).

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
τ	BLPER of IPT9 GRP13	REAL >0	= time period for which partition is being allocated in seconds

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
U_p	CDPCU(p) of IPT9 GRP4	Positive real	= current allocation utilization estimate for processor p
			$= \frac{1}{T} \sum_{t=1}^{T} [(c_{tp} + r_{tp})\, e_{tp}$ — task computation and resource management time
			$+ \sum_{i=1}^{I_t} A_{ti} \sum_{m=1}^{m} \omega_{mp}^{-1}\, \rho_{mti}\, a_{mpti}$ — task input processing
			$+ \sum_{o=1}^{O_t} \Omega_{to} \sum_{m=1}^{M} \omega_{mp}^{-1}\, \rho_{mto}\, w_{mpto}$ — task output processing
			$+ R_{tp}\, x_{tp}]$ — task resource management

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
u_m	CDMCU(m) of IPT9 GRP5	Postive real	= current partition solution estimate for memory m's allocated storage $= \frac{1}{L_m} \sum_{b=1}^{B} \ell_{mb} \, s_{mb}$

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
w_{mpto}	MPSOL(m,p,e,4)	Nonnegative integer	= the number of times output block o of task t is written or updated by task t on processor p to memory m This is a function of the current partition variables TPMAP(t,p,1) of DEALS IPT9 GRP8 MPMAP(m,p,1) of DEALS IPT9 GRP9 MBMAP(m,b,1) of DEALS IPT9 GRP10 where b = TAIOB(t,0) of DEALS IPT9 GRP12 block b is either an update or output (i.e., TAHBR(t,0) = 2 or 3 in DEALS IPT9 GRP12) Actual automated implementation should consider a function *or subroutine for current partitioning decision and* measures. If block b is stored in replicate locations, this becomes more complex.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
ω_{mp}		0,1	= 1 if processor p is permitted to change contents memory m; i.e., there is at least one write access link q from p to m = 0 if otherwise ω_{mp} can be computed as follows: = 1 if MPMAP(m,p,2) > 0 = 0 otherwise MPMAP(m,p,2) of IPT9 GRP9

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
Ω_{to}	TARWF(t,o) of IPT9 GRP12	Positive real	= percent of information output from task t to block o dependent on task/block evaluation level: minimum, average, worst-case (k = 1, 2, 3, respectively) TARWF(t,o) = TARW(t,i,k)/BLMXR(b) where TARW(t,i,k) is in IPT9 GRP12 and is set by PASS1 DEALS PPD 1630 PACLC.

MATCH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
ω_{mp}	MPMAP (m,p,2) of IPT9 GRP9	Real ≥ 0	= bits/sec transfer rate from processor p to memory m based on statistical composite of write access links for p and m.

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
x_{tp}		0,1	= 1 if task is assigned to execute on processor p = 0 otherwise x_{tp} is a function of the current partition solution as follows: = 1 if TPMAP(t,p,1) > 0 = 0 otherwise where TPMAP is in IPT9 GRP8

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
y_{tp}			= duplicate development cost to implement task t on processor p as currently partitioned if task t is on more than one processor = 0 for p = 1 = maximum (λ_{ipt} x_{ti} for i = 1 to p - 1) for p > 1 where λ_{ipt} = 1. if common language available on processor i and p ($i \neq p$) for task t = .25 if different languages are to be used ($i \neq p$) = 0 if i = p. Other values may be assigned as a function of the master language list. Note this is the amount by which development cost is reduced due to duplicate effort not needed for additional processors.

SAMPLE PROBLEM OUTPUT FORMAT 1

MM/DD/YY HH:MM:SS EVALUATION GLOBAL PARTITION EX CANDIDATE SAMPLE CONFIGURATION PASS PAGE 1

SYSTEM INTERFACE DEFINITION TECHNOLOGY HYPOTHETICAL TECH DB SOFTWARE SAMPLE APPLICATION

FORMAT 1. STANDARD RUN IDENTIFICATION

SAMPLE PROBLEM OUTPUT FORMAT 2

HARDWARE COMPONENT SUMMARY

CATEGORY/DEVICE		IDENTIFIER	REQUIRED
PU	86-PROC	A	YES
PU	SPC	SPC	YES
PU	XYZ32/75	A1	CAND
PU	XYZ32/75	B1	CAND
MM	86-MEM	M6	YES
MM	32-MEM	M1	CAND
MM	32-MEM	M2	CAND
MM	32-MEM	M3	CAND
MM	32-MEM	M4	CAND
MM	32-MEM	M5	CAND
CL	ASYNC-IO	EIO-1	YES
CL	ASYNC-IO	EIO-2	YES
CL	M7LINK-86	EIO-3	YES
CL	HSD	EIO-4	YES
CL	MBUS	C1	CAND
CL	MBUS	C2	CAND
CL	MBUS	BUS2	CAND
CL	MBUS	BUS1A	CAND
CL	MBUS	BUS1B	CAND
CL	HSD	HSD	CAND
CL	86MBUS	BUS3	CAND

SAMPLE PROBLEM OUTPUT FORMAT 3

DATA BLOCK SUMMARY AND EXTERNAL SOURCE/DESTINATION

BLOCK	IDENTIFIER	LEVEL -FLAG	DISCIPLINE -FLAG	MAXIMUM RECORDS	BITS/ BYTE	BYTES/ WORD	WORDS-PER-RECORD MIN	AVE	MAX	EXTERNAL IDENTIFIER	COMPONENT FREQUENCY
1	PAOL	S	RAN	128	8	4	1	1	1		
2	DIRLITE	S	RAN	256	8	4	1	1	1		
3	CAOUT	S	CBUF	2	8	4	128	128	128	HSD	30
4	AOBJL	S	RAN	100	8	4	1	1	1	HSD	30
5	MODPLIST	S	RAN	20	8	4	1	1	1	HSD	30
6	CAIPT	S	CBUF	2	8	4	128	128	128	HSD	30
7	DYNDATA	S	RAN	8192	8	4	1	1	1	HSD	30
8	SIMPOS	S	CBUF	2	8	4	128	128	128	EIO-4	30
9	RAWPOS	S	CBUF	2	8	4	128	128	128		
10	G1	G	RAN	1024	8	4	1	1	1		
11	ADATA	G	RAN	512	8	4	1	1	1		
12	BDATA	G	RAN	512	8	4	1	1	1		
13	BOMBDATA	L	RAN	512	8	4	1	1	1		
14	DYNDATASW	S	RAN	1	8	4	1	1	1	AIS	30

SAMPLE PROBLEM OUTPUT FORMAT 4

TASK SUMMARY

TASK	IDENTIFIER	LANGUAGE	INPUT BLOCKS	OUTPUT BLOCKS	ENABLEMENT DISCIPLINE	FREQ 1	FREQ 2	FREQ 3
1	T13	ASSEMBLER	SIMPOS RAWPOS DIRLITE G1	DIRLITE PAOL G1 DYNDATA	TIME	30		
2	T46	FORTRAN IV	G1	CAIPT	SLVD		30	
3	A713	FORTRAN IV	G1 ADATA	DYNDATA ADATA	SLVD		30	
4	B7-13	FORTRAN IV	G1 BDATA	DYNDATA BDATA	SLVD		30	
5	T14&16	FORTRAN IV	G1 BOMBDATA	BOMBDATA	SLVD		30	
6	T15	MACRO ASM	DYNDATA	DYNDATA	SLVD			30
7	T17-19	FORTRAN IV	CAOUT AOBJL MODPLIST	AOBJL MODPLIST	DATA			30

SAMPLE OUTPUT FORMAT 6 (Sheet 1 of 2)

EVALUATION ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE	COMPONENT ASSIGNED	APPLICATION COMPONENT IDENTIFIER	CONFIGURATION COMPONENT IDENTIFIER	VALUE WHEN APPLICABLE
Fixed	Task	T1-3	A1	30
Initial	Task	T4-5	A1	30
Initial	Task	A7-13	A1	30
Initial	Task	T17-19	A1	30
Prohibited	Task	T17-19	B1	30
Initial	Task	B7-13	B1	30
Initial	Task	T14&16	B1	30
Initial	Task	T15	B1	15
Initial	Task	T15	A1	15
Fixed	Data	PAOL	M3	15
Fixed	Data	DIRLITE	M3	
Fixed	Data	CAOUT	M4	
Fixed	Data	AOBJL	M3	

SAMPLE OUTPUT FORMAT 6 (Sheet 2 of 2)

EVALUATION ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE	COMPONENT ASSIGNED	APPLICATION COMPONENT IDENTIFIER	CONFIGURATION COMPONENT IDENTIFIER	VALUE WHEN APPLICABLE
Fixed	Data	MODPLIST	M3	
Fixed	Data	CAIPT	M4	
Fixed	Data	DYNDATA	M3	
Fixed	Data	SIMPOS	M1	
Fixed	Data	RAWPOS	M1	
Fixed	Data	G1	M3	
Initial	Data	ADATA	M1	
Initial	Data	BDATA	M2	
Initial	Data	BOMBDATA	M3	
Fixed	Data	DYNDATASW	M3	

SAMPLE PROBLEM OUTPUT FORMAT 7

EVALUATION PRIORITIES

MAJOR PRIORITIES				
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE LIMIT	COEFFICIENT LEVEL &	MAX ITER
1	Processor Utilization (% Busy)	40. 60.	A	10
2	Memory Utilization (% Occupied)	40. 60.	A	10
3	Development Cost (Person Years)	3 4.5	W	5

PRIORITY COMPONENTS			
COMPONENT	GOAL	TOLERANCE PERCENT	COEFFICIENT LEVEL
A1	50.	10.	W
B1	30.	10.	A
SPC	40.	20.	A
A	40.	60.	A
M1	60.	10.	A
M2	60.	10.	A
M3	60.	0.	A
M4	60.	0.	A
M5	60.	0.	W
M6	60.	5.	A
T1-3			W
T4-6			A
A7-13			A
B7-13			A
T14&16			W
T15			A
T17-19			A

SAMPLE PROBLEM OUTPUT FORMAT 8

BASIC PARTITIONING PROBLEM SIZE

7 TASKS	4 PROCESSORS
14 DATA BLOCKS	6 MEMORIES
2 PRIORITIES SELECTED	

SIMPLIFIED PROBLEM OUTPUT FORMAT 101

PRIORITY GOAL SUMMARY

MAJOR PRIORITIES				PRIORITY COMPONENTS				
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL / FLAG	COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL / FLAG	
1	PROCESSOR UTILIZATION % BUSY	60.00 5.00%	60.00	P1	60	5.00	60	
				P2	60	5.00	60	
2	DEVELOPMENT COST MANYEARS	5.00 10.00%	5.60 **	T1	.5	10.00	.5	
				T2	1.0	10.00	1.0	
				T3	1.0	5.00	1.5	**
				T4	.5	1.00	.5	
				T5	2.0	10.00	2.0	
3	MEMORY UTILIZATION % ASSIGNED	60.00 5.00%	53.00	M1	60	5.00	66.00	**
				M2	30	2.00	32.00	
				M3	60	5.00	59.00	

SIMPLIFIED PROBLEM OUTPUT FORMAT 102

TASK ALLOCATION								
					TASK I/O			
TASK	PROCESSOR	EXECUTIONS	TOTAL TIME	FLAG	BLOCK	MEMORY	INPUT	OUTPUT
T1	P1	20/20	.20		I1	M1	✓	✓
					B1	M1	✓	
					G1	M2	✓	✓
					S1	M1		✓
					S2	M2		✓
T2	P1	10/10	.20		I2	M1	✓	
					G1	M2	✓	
					G2	M2		✓
					S1	M1	✓	
T3	P2	20/20	.20		I3	M3	✓	
					G1	M2	✓	
					G3	M2		✓
						M3		✓
					S2	M2	✓	
T4	P1	20/20	.20		I4	M1	✓	
					B2	M1		✓
					G2	M2	✓	
					G3	M2	✓	
T5	P2	20/20	.40		I5	M3	✓	✓
					B3	M2		✓
					G3	M3	✓	

SIMPLIFIED PROBLEM OUTPUT FORMAT 103

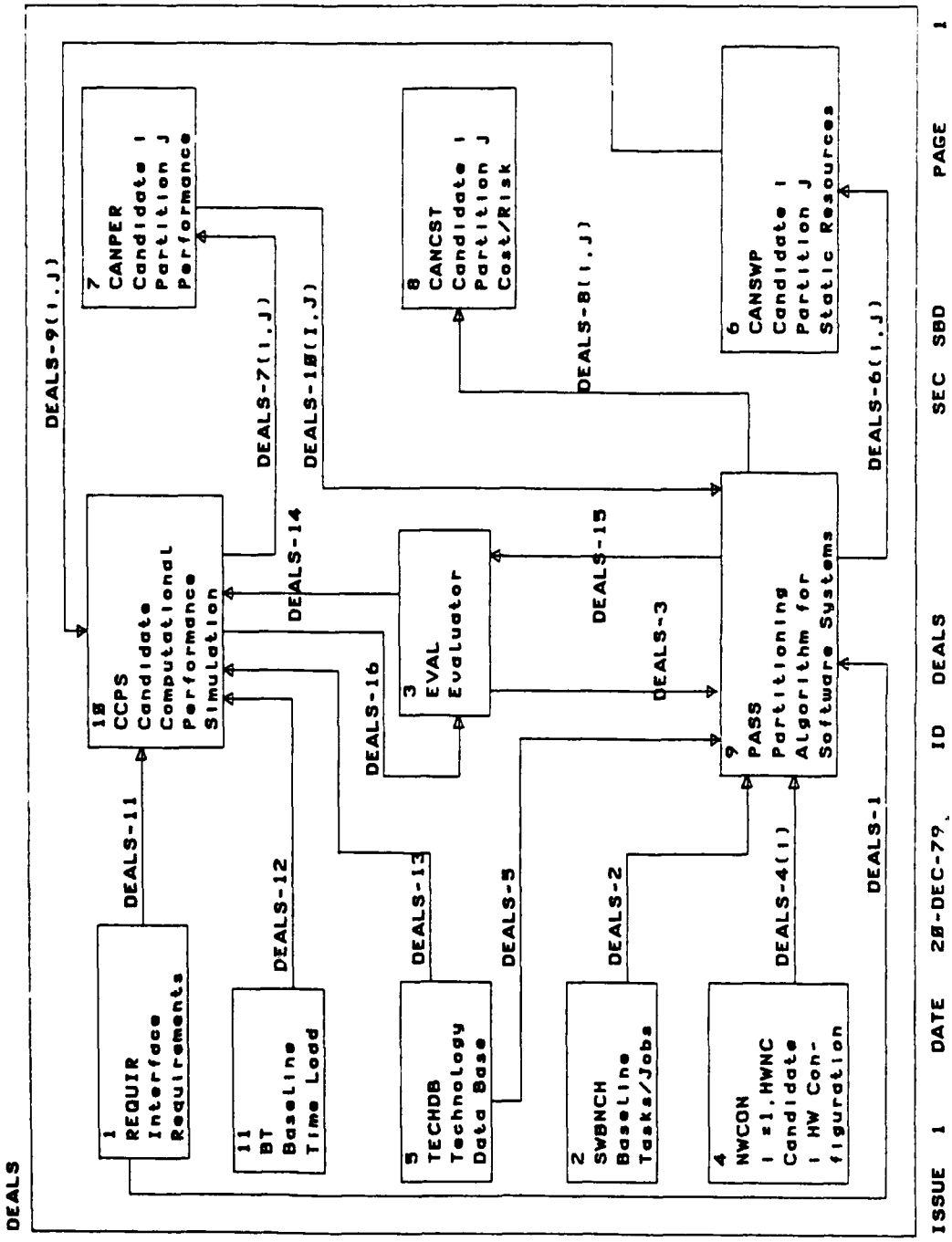
DATA BLOCK ALLOCATION

BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
B1	M1	1000	3.1	P1		500		
B2	M1	2000	6.2	P1	1000			
B3	M2	4000	12.5	P2	2000			
G1	M2	4000	12.5	P1	✓	✓		
				P2		✓		
G2	M2	1000	3.1	P1	✓	✓		
G3	M2	1000	3.1	P1		✓		
				P2	✓			
	M3	1000	3.1	P2	✓	✓		
S1	M1	256	.8	P1	✓	✓		
S2	M2	256	.8	P1	✓			
				P2		✓		
I1	M1	2000	6.2	P1	✓	✓		
I2	M1	12000	37.8	P1	✓	✓		
I3	M3	8000	25.0	P2	✓	✓		
I4	M1	4000	12.5	P1	✓	✓		
I5	M3	10000	31.2	P2	✓	✓		

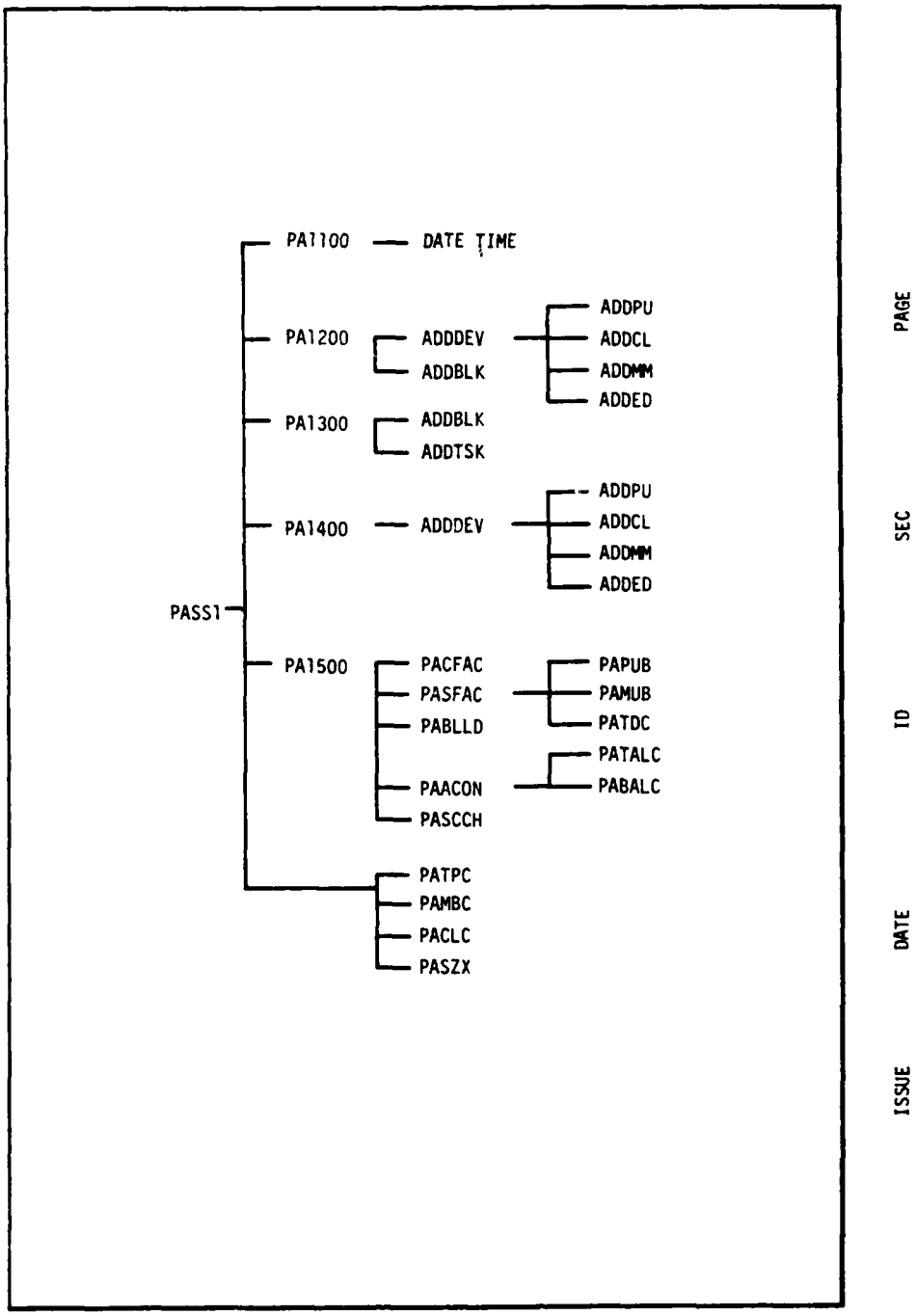
APPENDIX D.

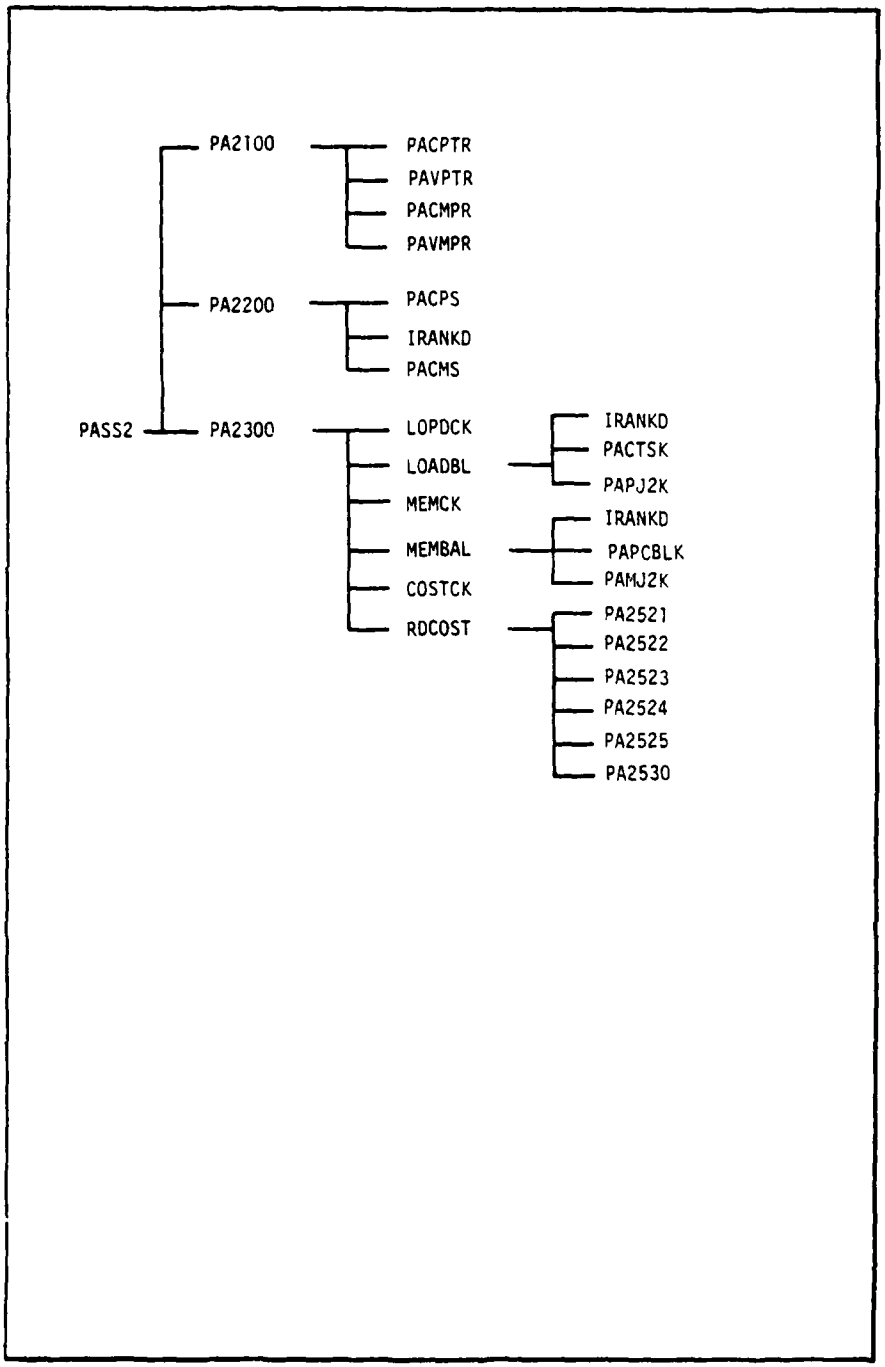
DETAILED DESIGN

D.1 SYSTEM INTERFACE



D.2 HIERARCHICAL STRUCTURE





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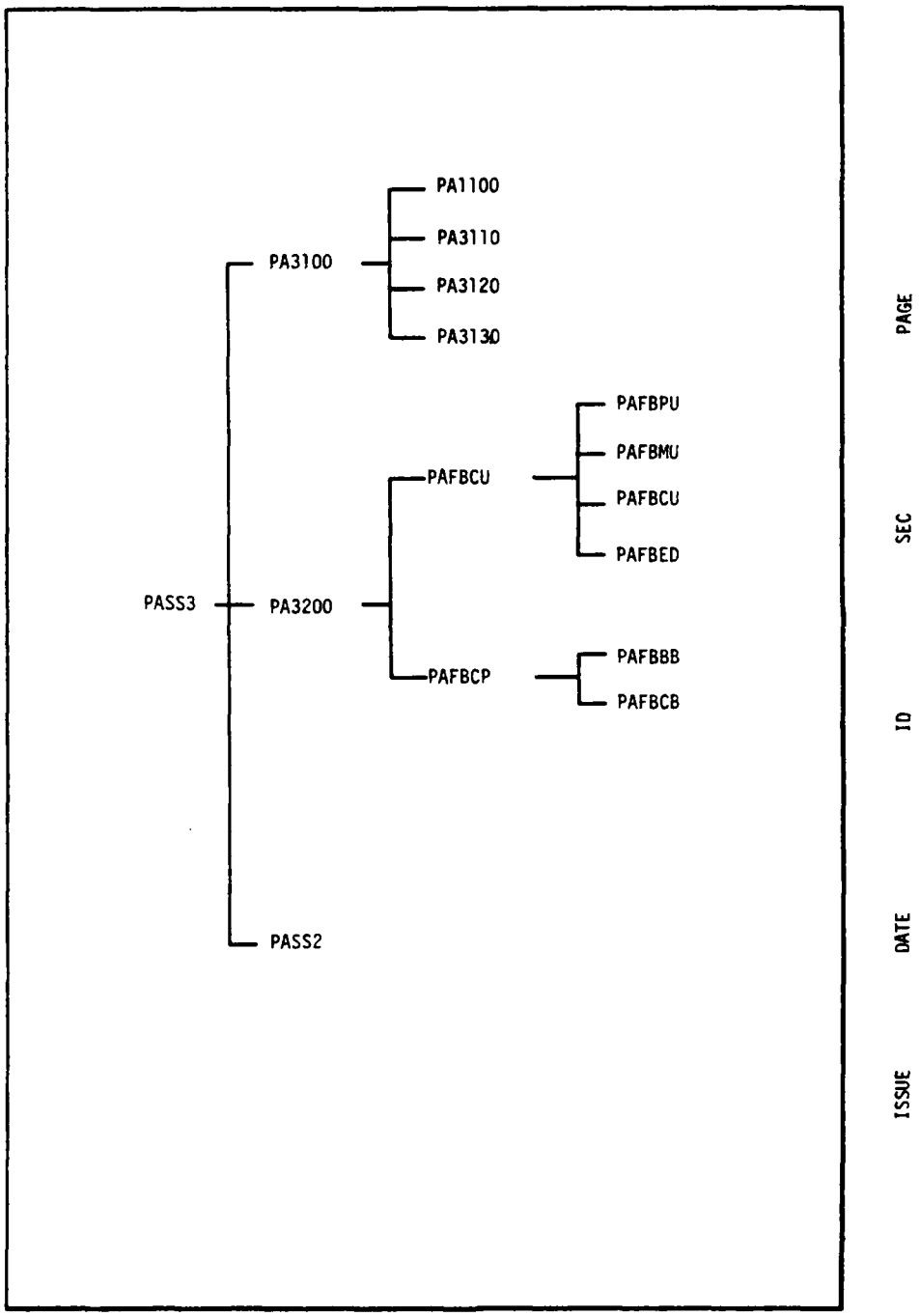
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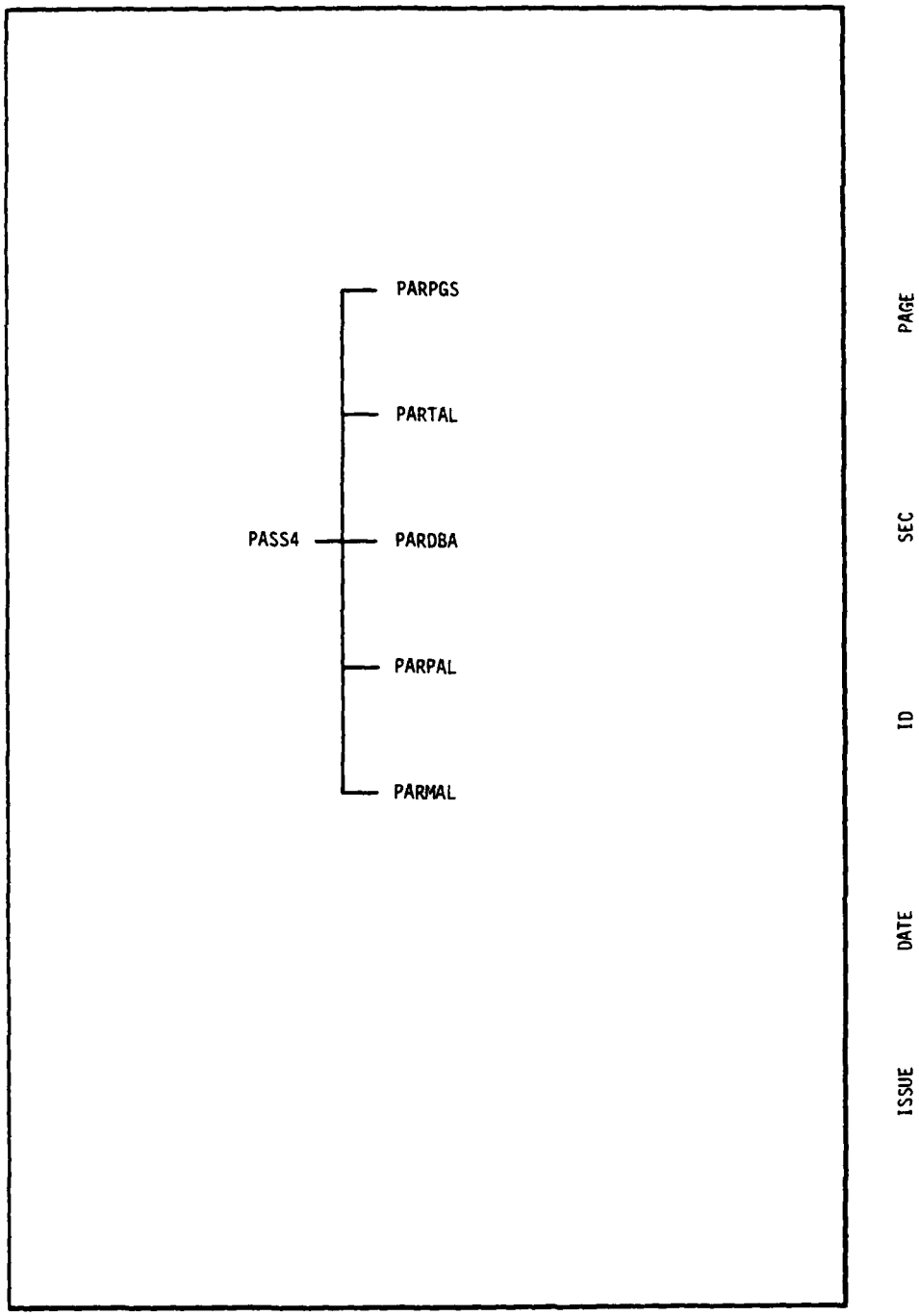
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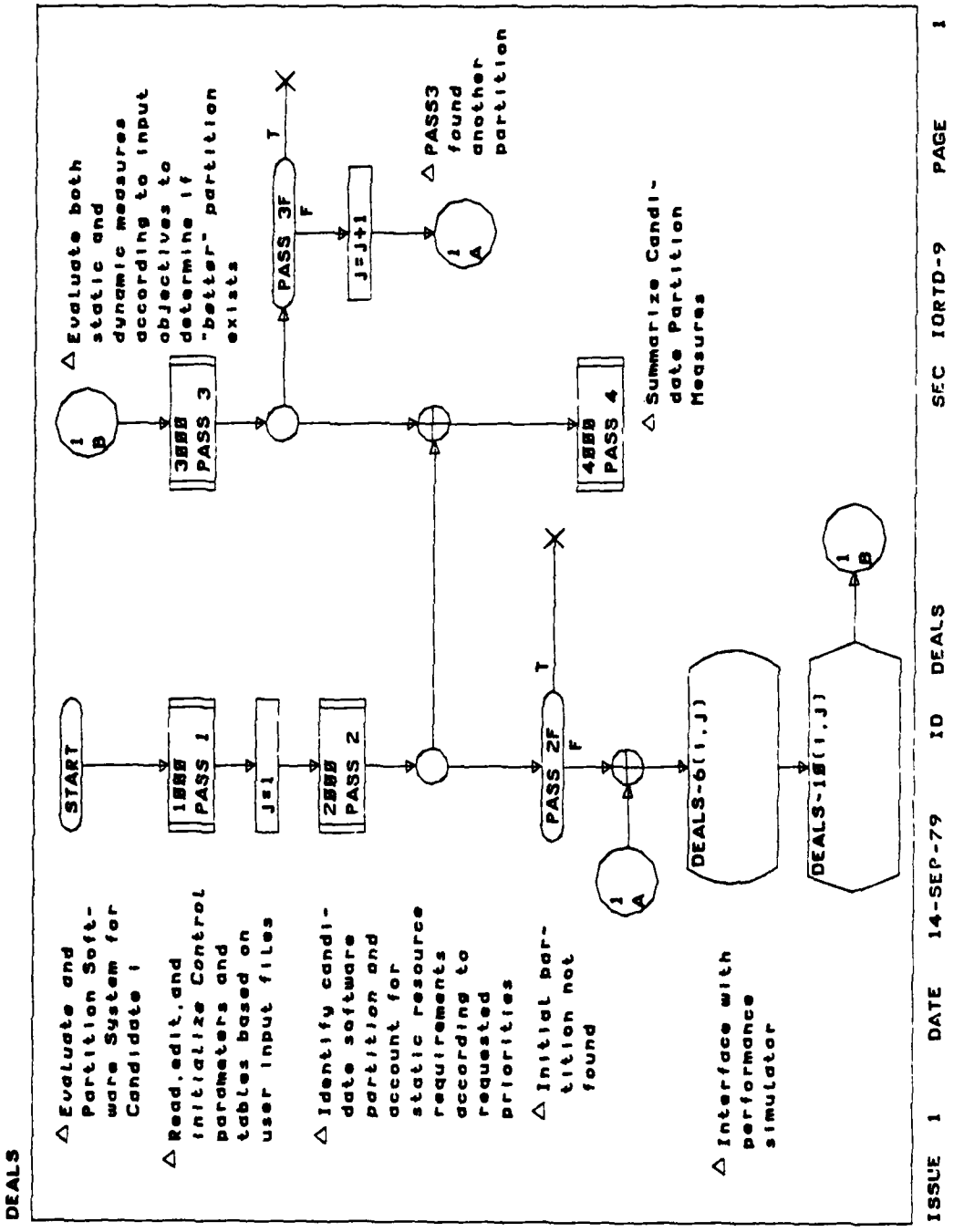
D.3 FLOW DIAGRAMS



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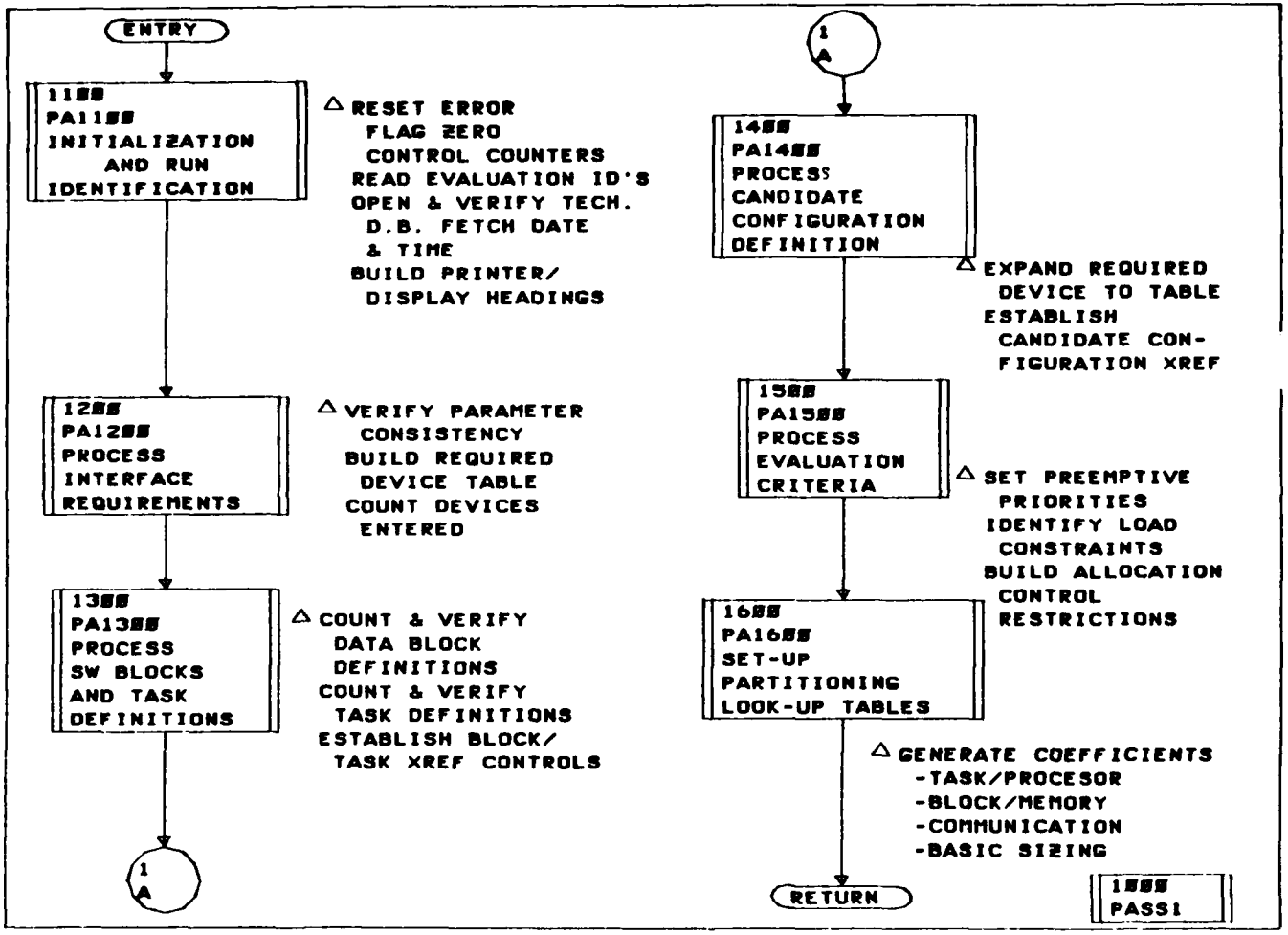

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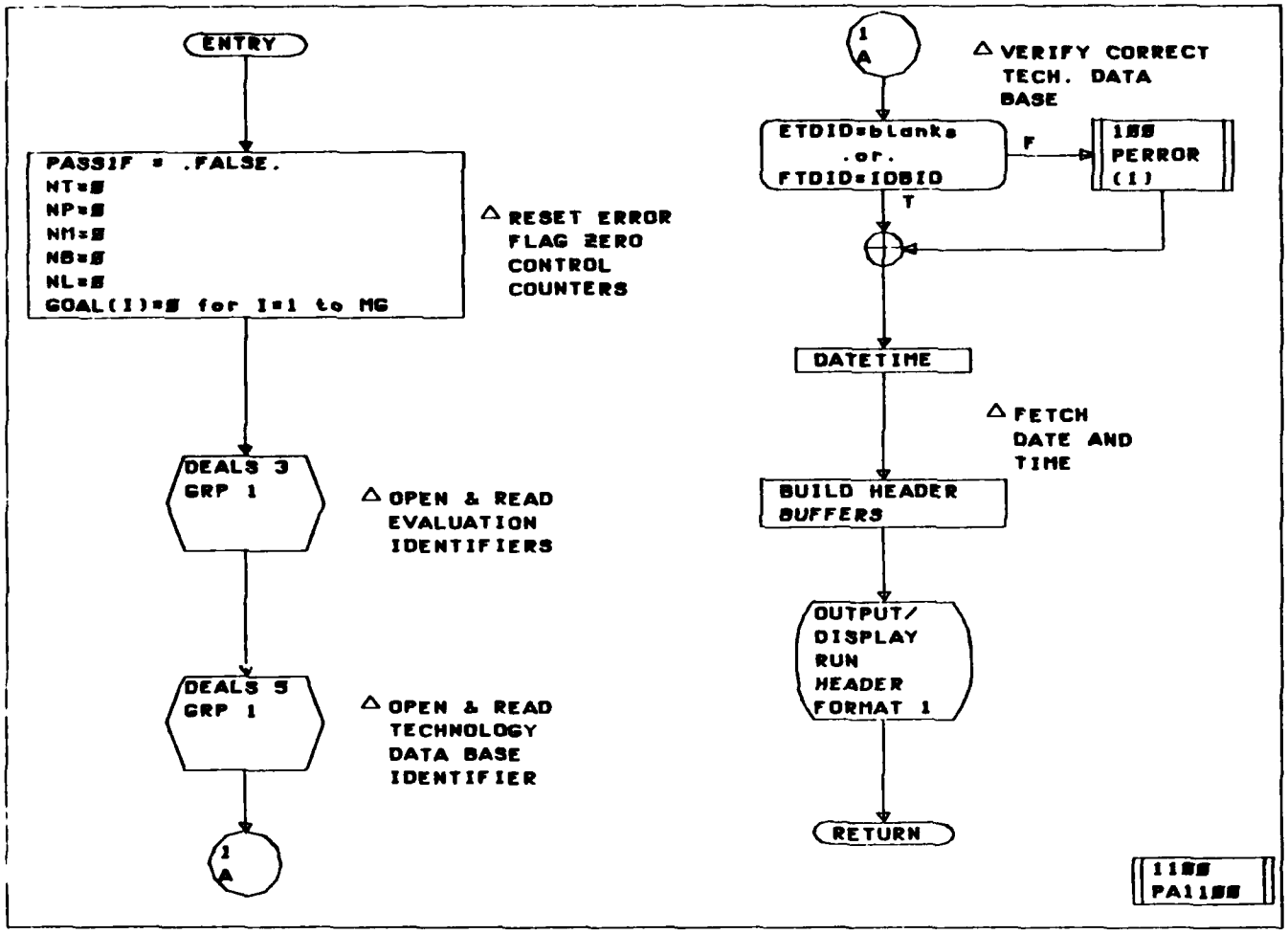
DEALS



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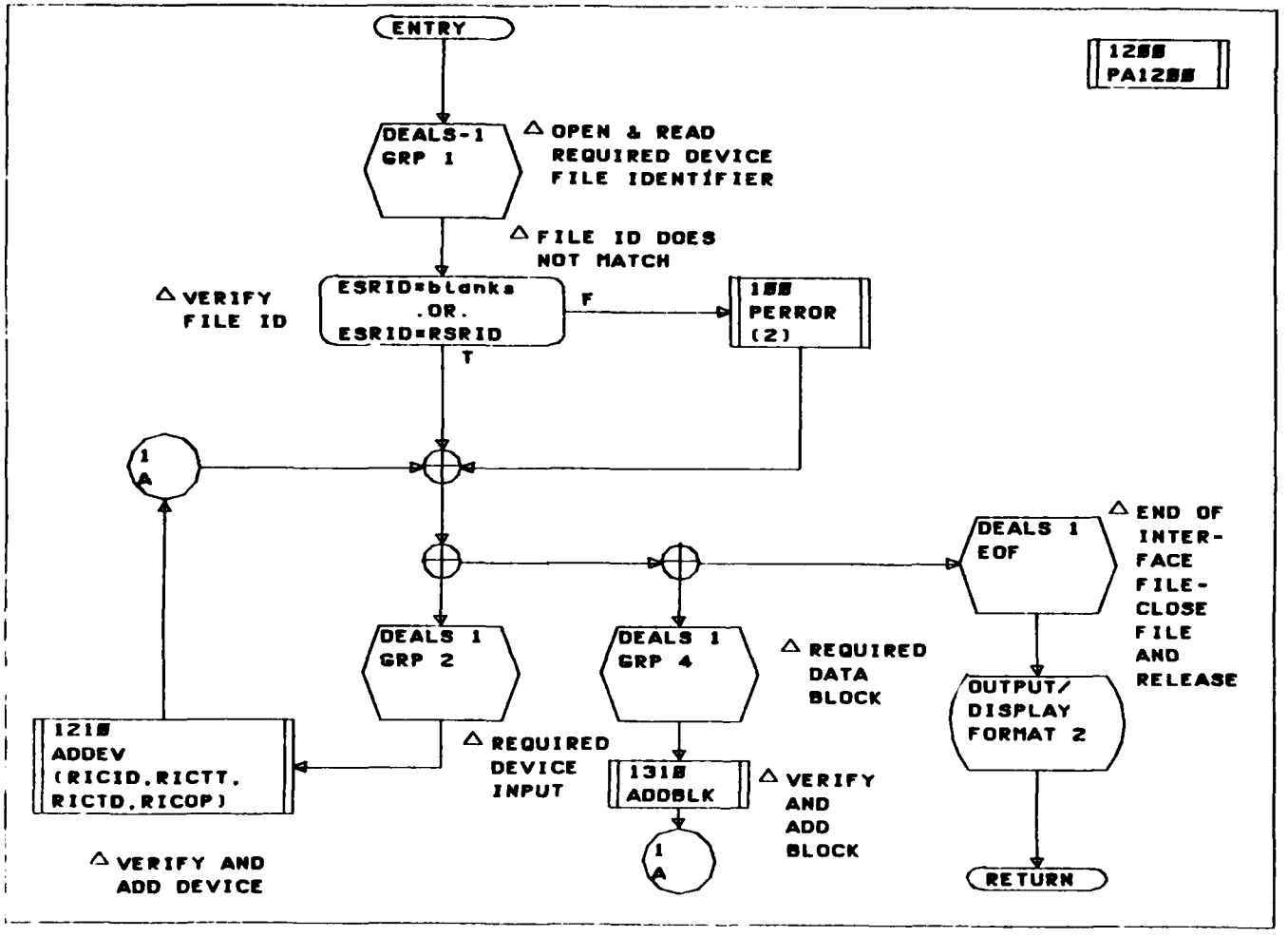
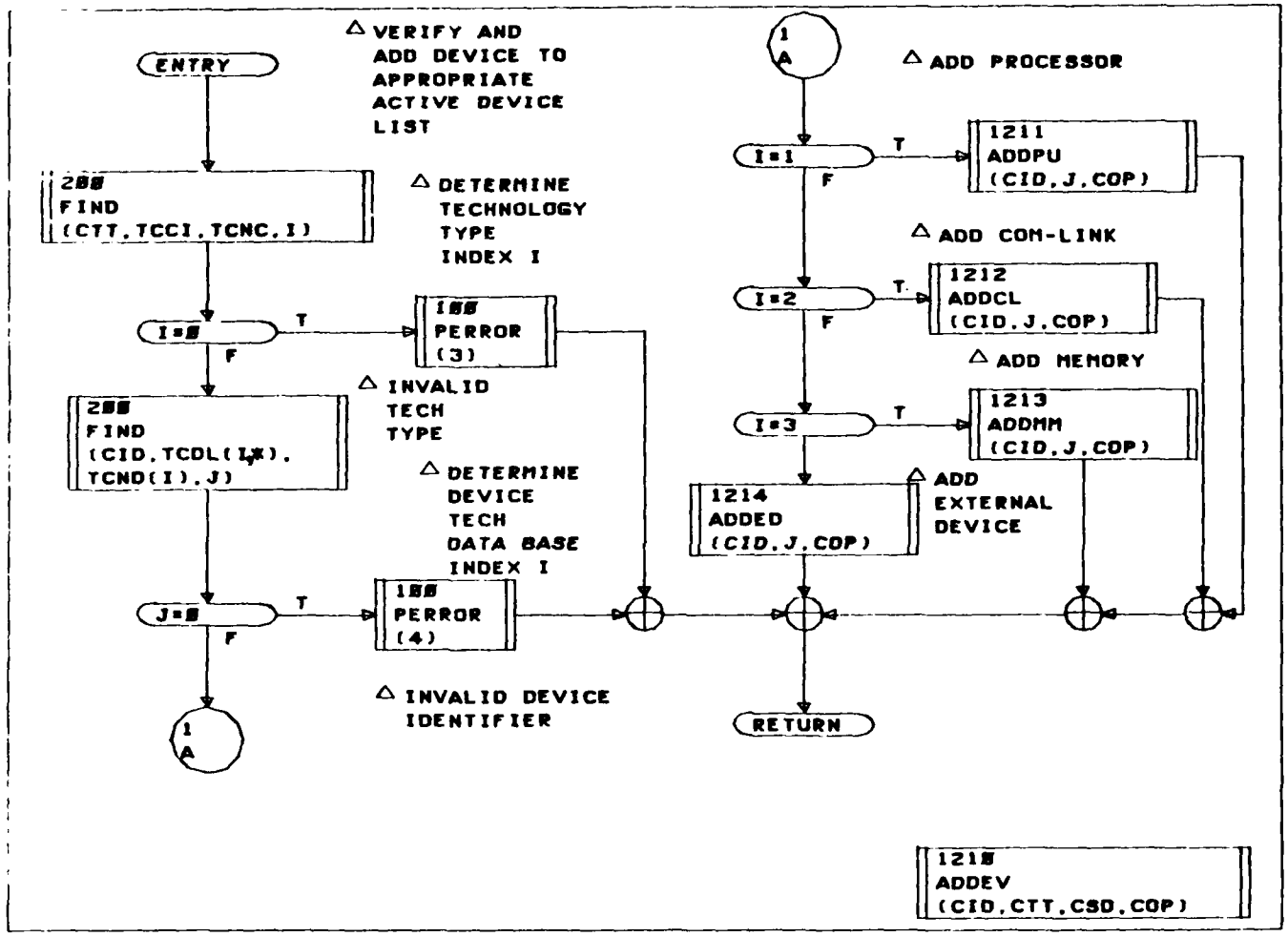
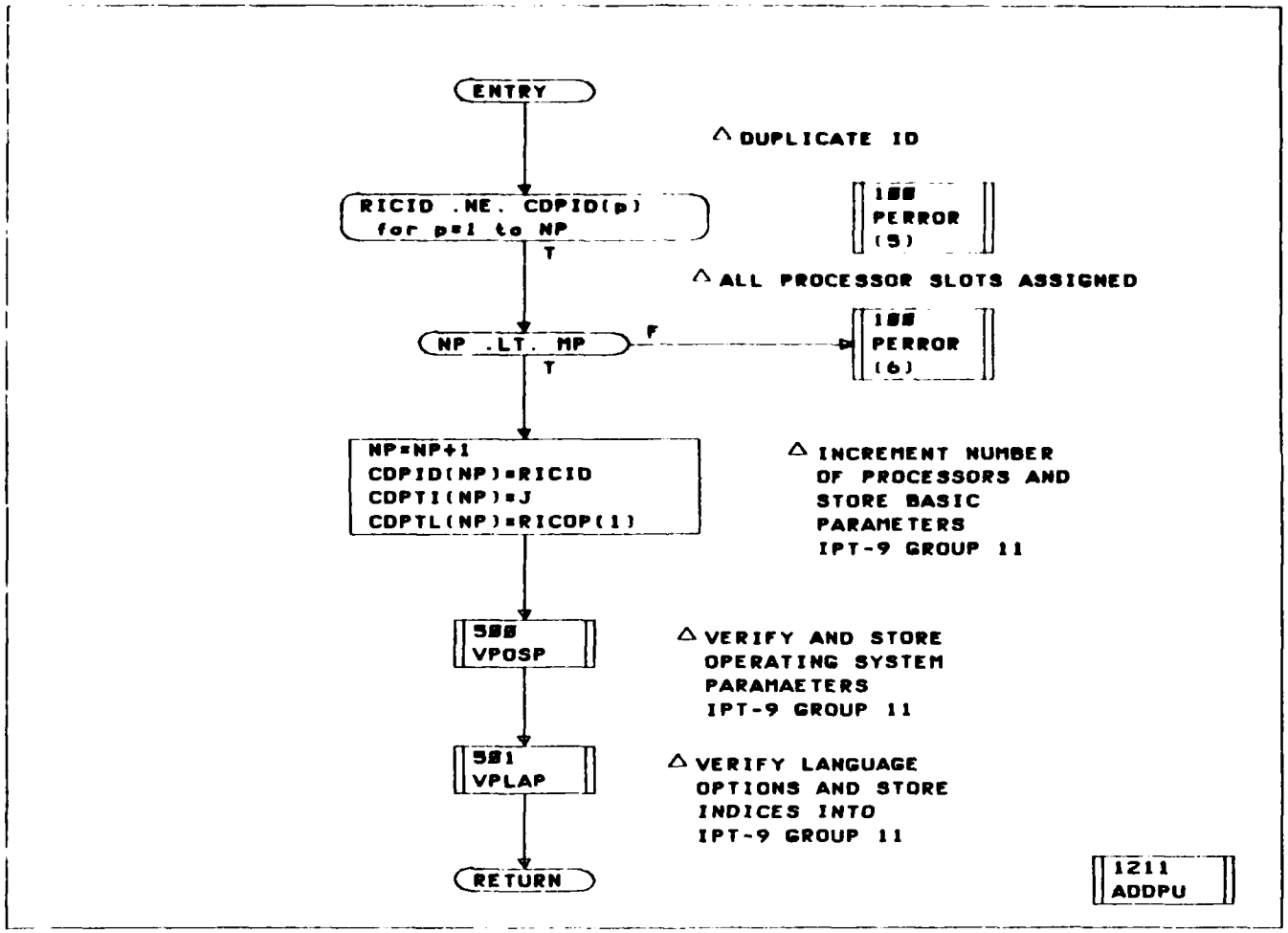
DEALS



ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1200 PAGE 1


ENTRY
△ VERIFY AND ADD DEVICE TO APPROPRIATE ACTIVE DEVICE LIST
200 FIND (CTT,TCCI,TCNC,I)
△ DETERMINE TECHNOLOGY TYPE INDEX I
I=0
T
F
100 PERROR (3)
△ INVALID TECH TYPE
200 FIND (CID,TCDL(I,*), TCND(I),J)
△ DETERMINE DEVICE TECH DATA BASE INDEX I
J=0
T
F
100 PERROR (4)
△ INVALID DEVICE IDENTIFIER
1 A
1 A
△ ADD PROCESSOR
I=1
T
F
1211 ADDPU (CID,J,COP)
△ ADD COM-LINK
I=2
T
F
1212 ADDCL (CID,J,COP)
△ ADD MEMORY
I=3
T
1213 ADDMM (CID,J,COP)
△ ADD EXTERNAL DEVICE
1214 ADDED (CID,J,COP)
RETURN
1210 ADDEV (CID,CTT,CSD,COP)

DEALS



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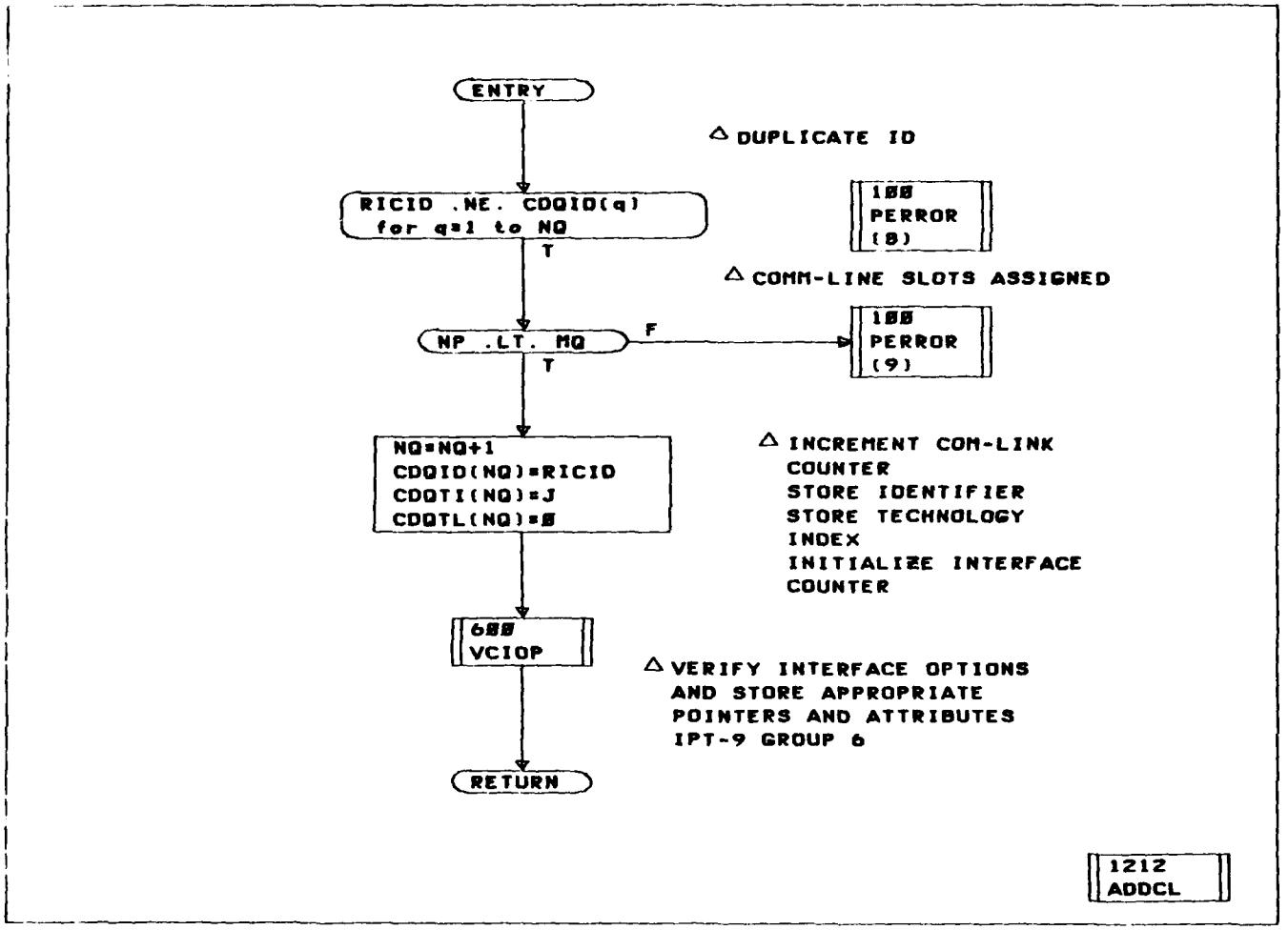
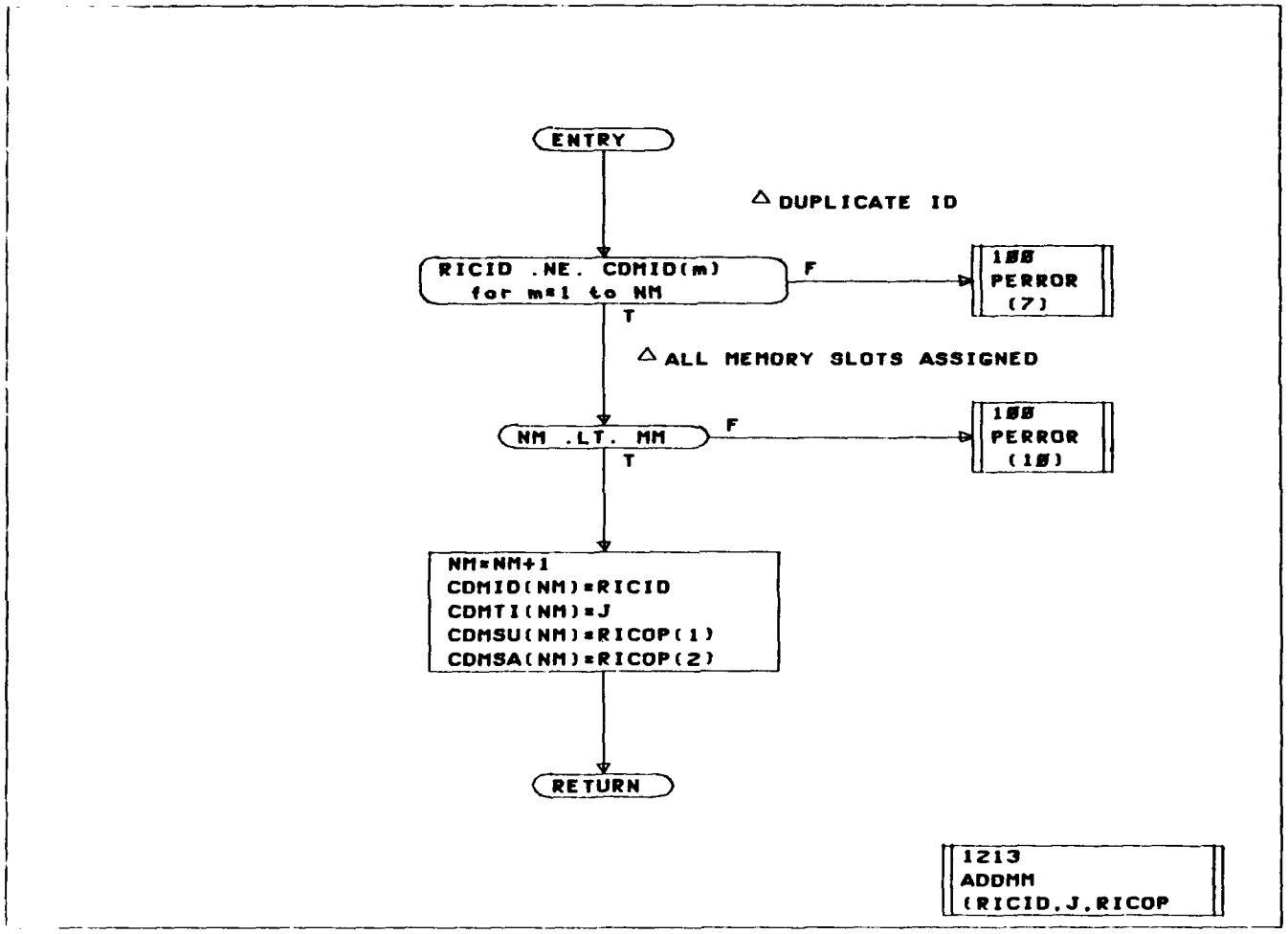
DEALS

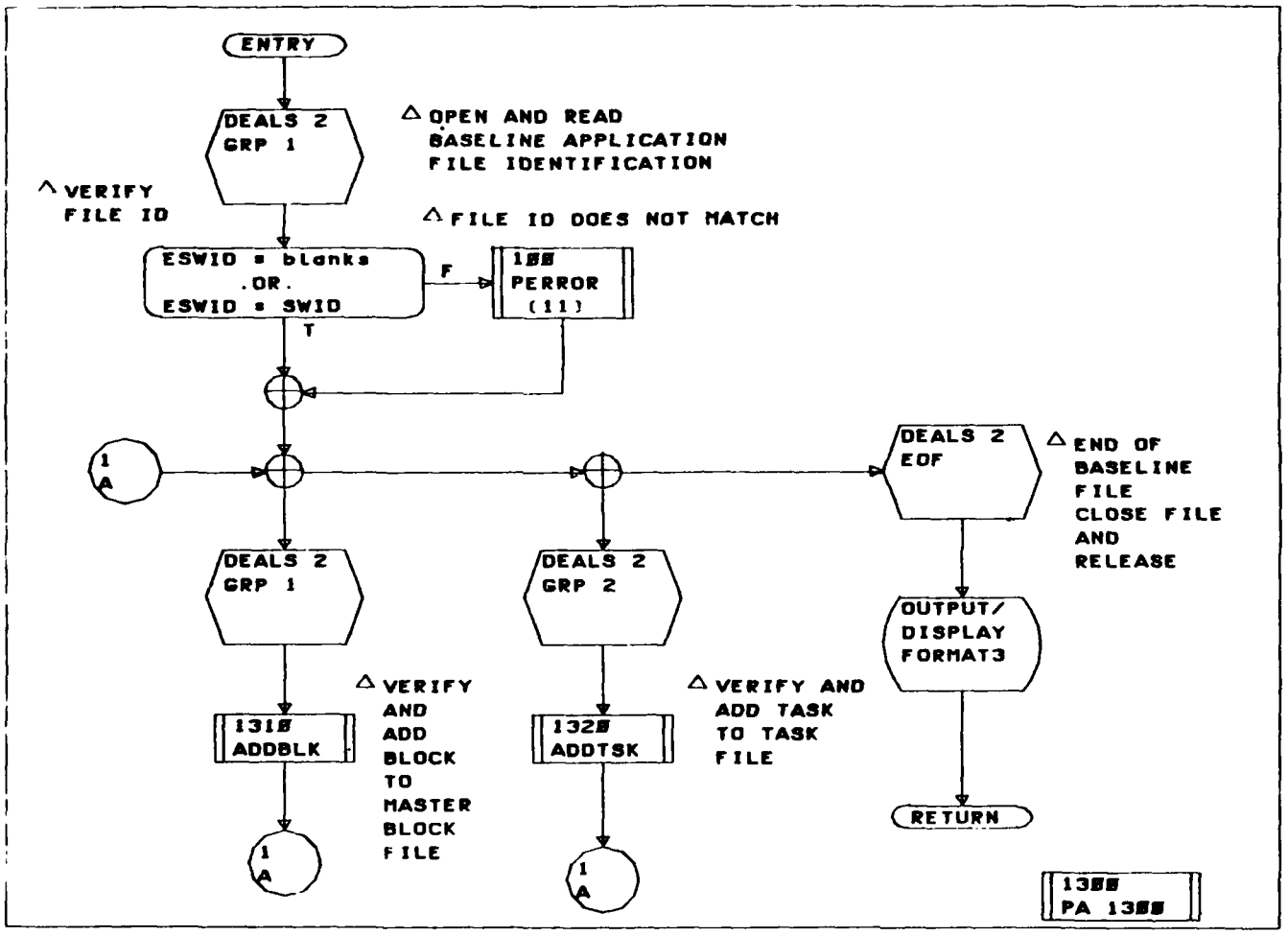


ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1212 PAGE 1

DEALS


ENTRY
△ DUPLICATE ID
RICID .NE. CDMID(m)
for m=1 to NM
F
T
100
PERROR
(7)
△ ALL MEMORY SLOTS ASSIGNED
NM .LT. MM
F
T
100
PERROR
(10)
NM=NM+1
CDMID(NM)=RICID
CDMTI(NM)=J
CDMSU(NM)=RICOP(1)
CDMSA(NM)=RICOP(2)
RETURN
1213
ADDMM
(RICID,J,RICOP

DEALS



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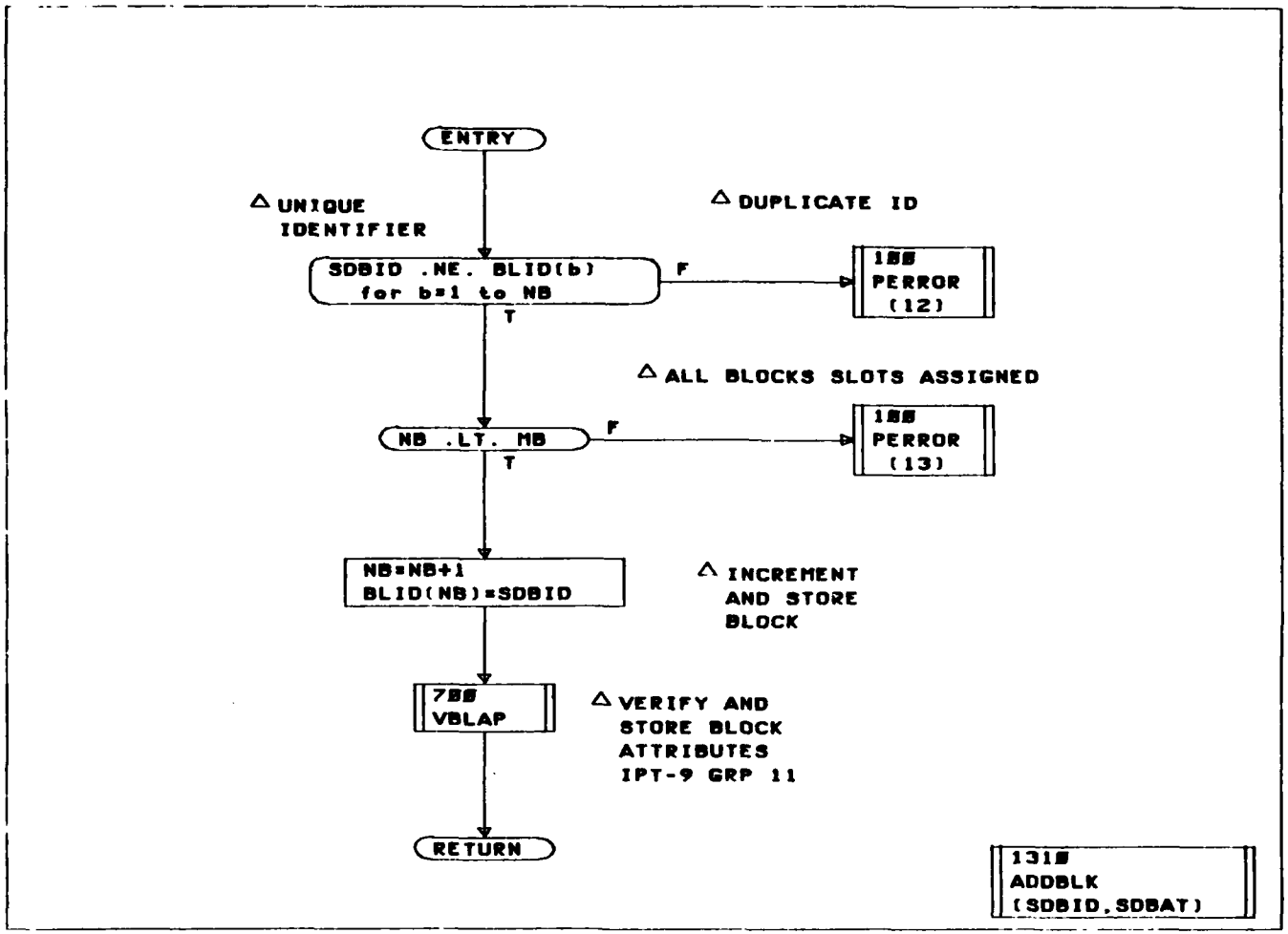
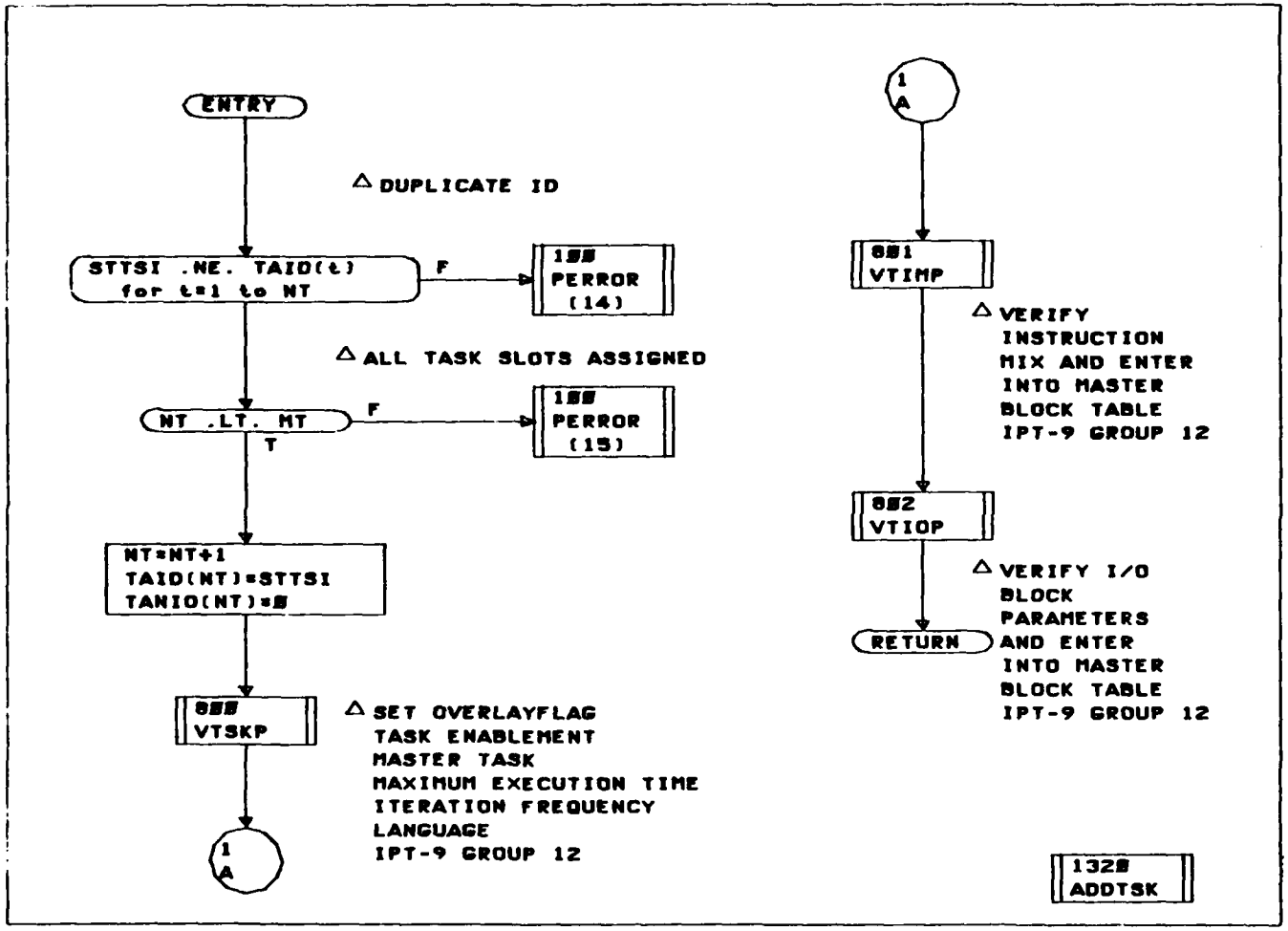
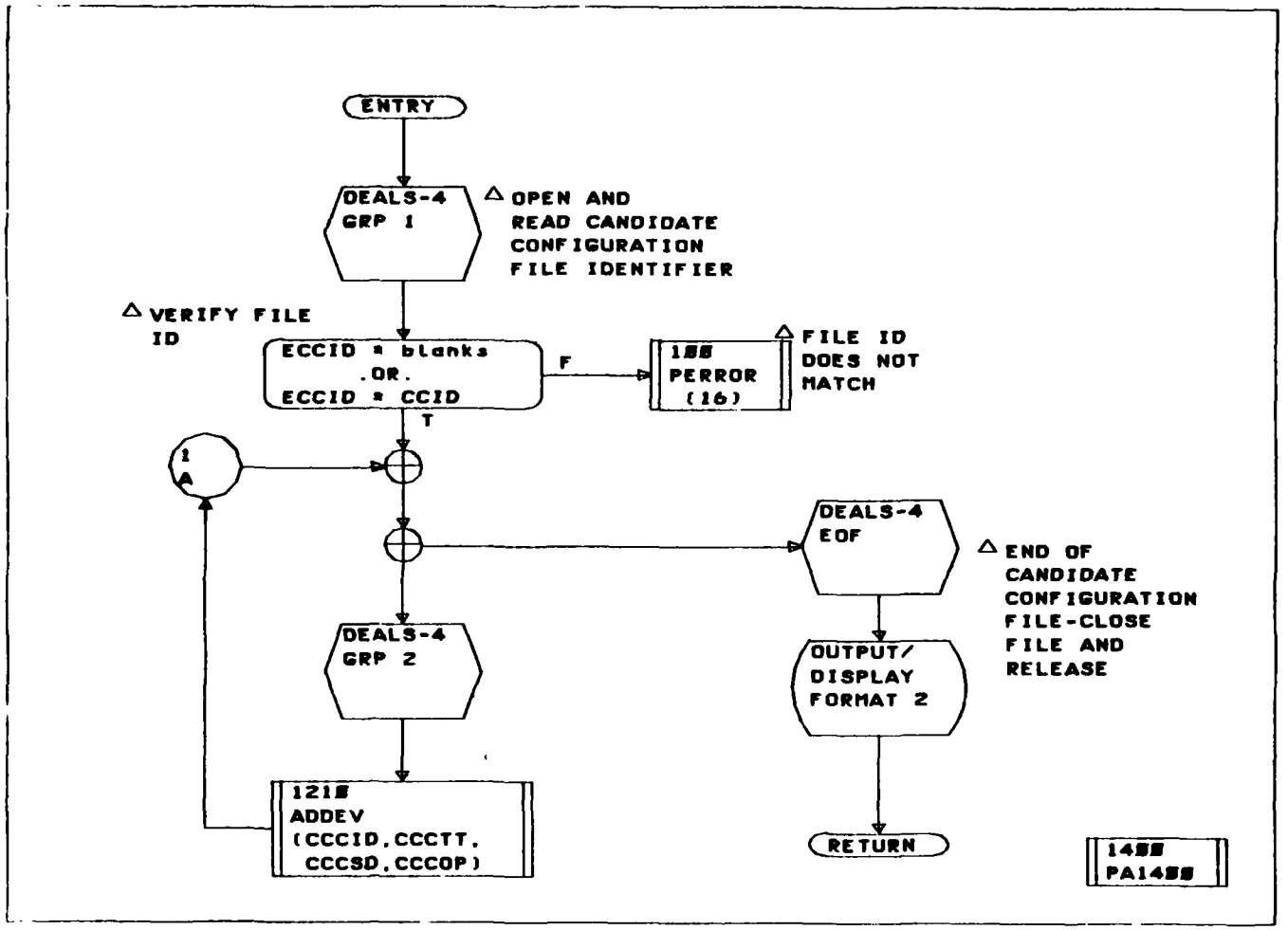
DEALS


ENTRY
△ UNIQUE IDENTIFIER
△ DUPLICATE ID
SDBID .NE. BLID(b) for b=1 to NB
F
T
100 PERROR (12)
△ ALL BLOCKS SLOTS ASSIGNED
NB .LT. MB
F
T
100 PERROR (13)
NB=NB+1
BLID(NB)=SDBID
△ INCREMENT AND STORE BLOCK
700 VBLAP
△ VERIFY AND STORE BLOCK ATTRIBUTES IPT-9 GRP 11
RETURN
1310 ADDBLK (SDBID,SDBAT)

DEALS


ENTRY
△ DUPLICATE ID
STTSI .NE. TAID(t)
for t=1 to NT
F
1##
PERROR
(14)
△ ALL TASK SLOTS ASSIGNED
NT .LT. MT
F
T
1##
PERROR
(15)
NT=NT+1
TAID(NT)=STTSI
TANIO(NT)=#
8##
VTSKP
△ SET OVERLAYFLAG
TASK ENABLEMENT
MASTER TASK
MAXIMUM EXECUTION TIME
ITERATION FREQUENCY
LANGUAGE
IPT-9 GROUP 12
1
A
1
A
8#1
VTIMP
△ VERIFY
INSTRUCTION
MIX AND ENTER
INTO MASTER
BLOCK TABLE
IPT-9 GROUP 12
8#2
VTIOP
△ VERIFY I/O
BLOCK
PARAMETERS
AND ENTER
INTO MASTER
BLOCK TABLE
IPT-9 GROUP 12
RETURN
132#
ADDTSK

DEALS



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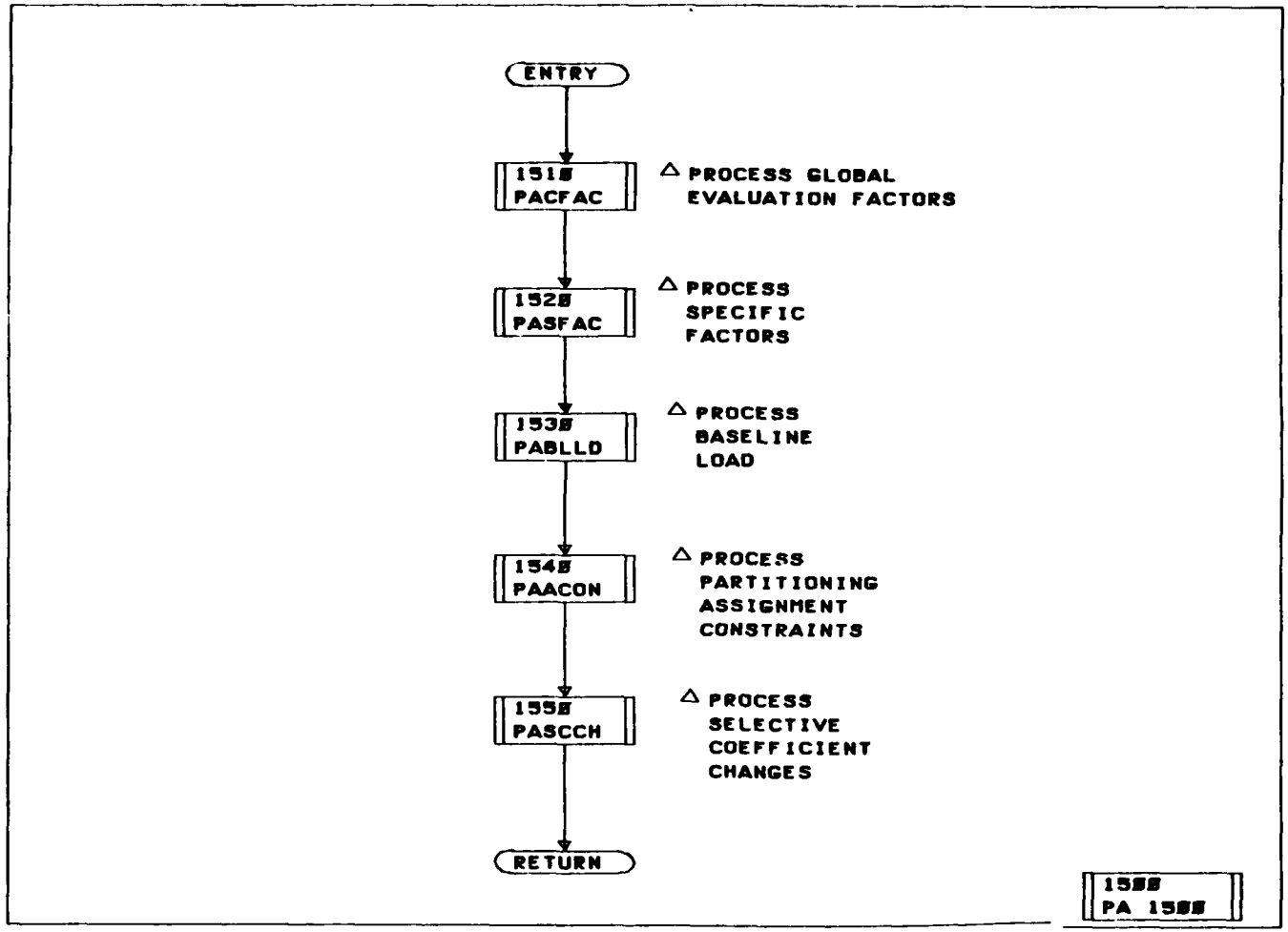
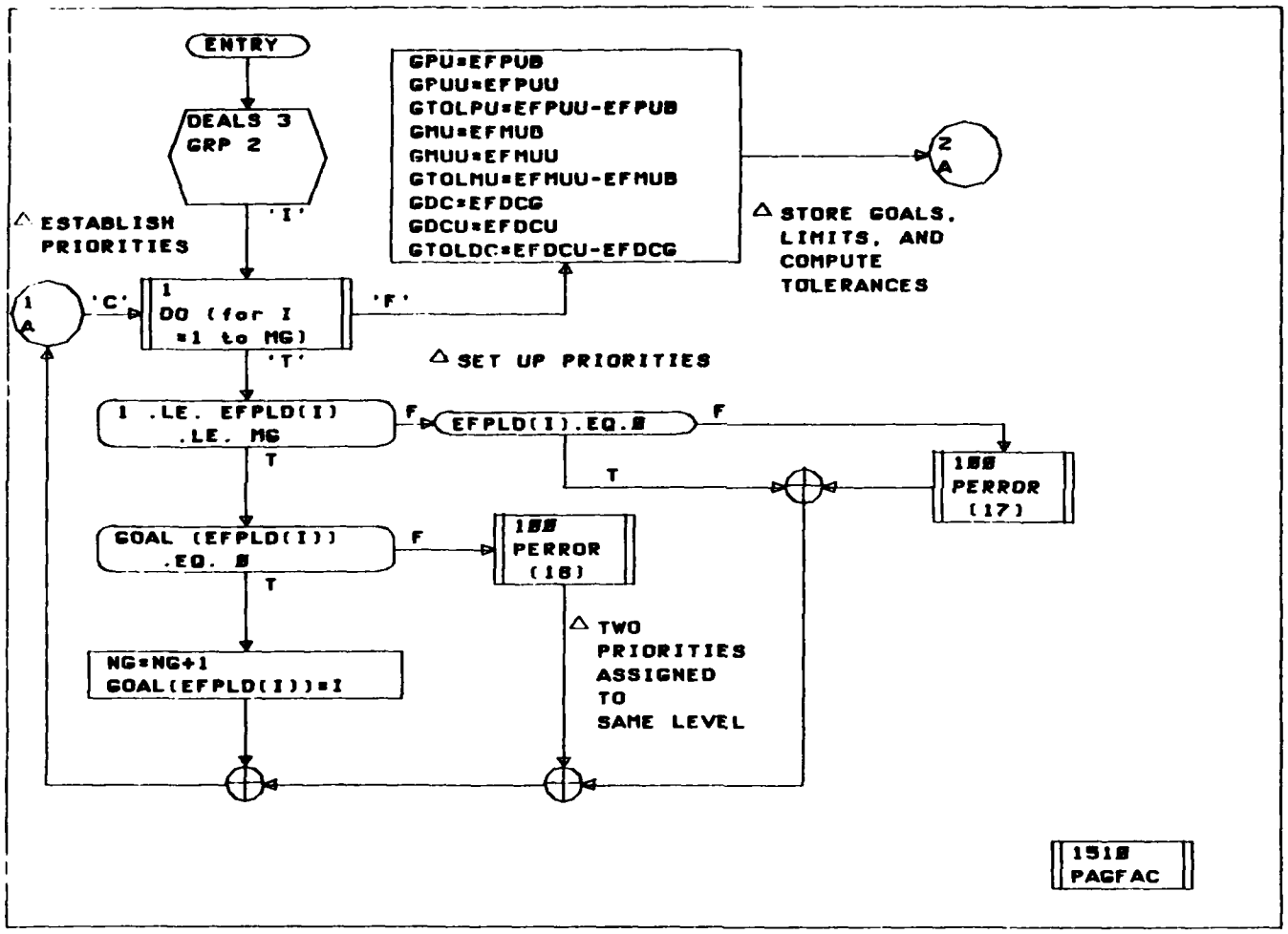
DEALS


ENTRY
1510
PACFAC
△ PROCESS GLOBAL EVALUATION FACTORS
1520
PASFAC
△ PROCESS SPECIFIC FACTORS
1530
PABLLD
△ PROCESS BASELINE LOAD
1540
PAACON
△ PROCESS PARTITIONING ASSIGNMENT CONSTRAINTS
1550
PASCCH
△ PROCESS SELECTIVE COEFFICIENT CHANGES
RETURN
1500
PA 1500

DEALS



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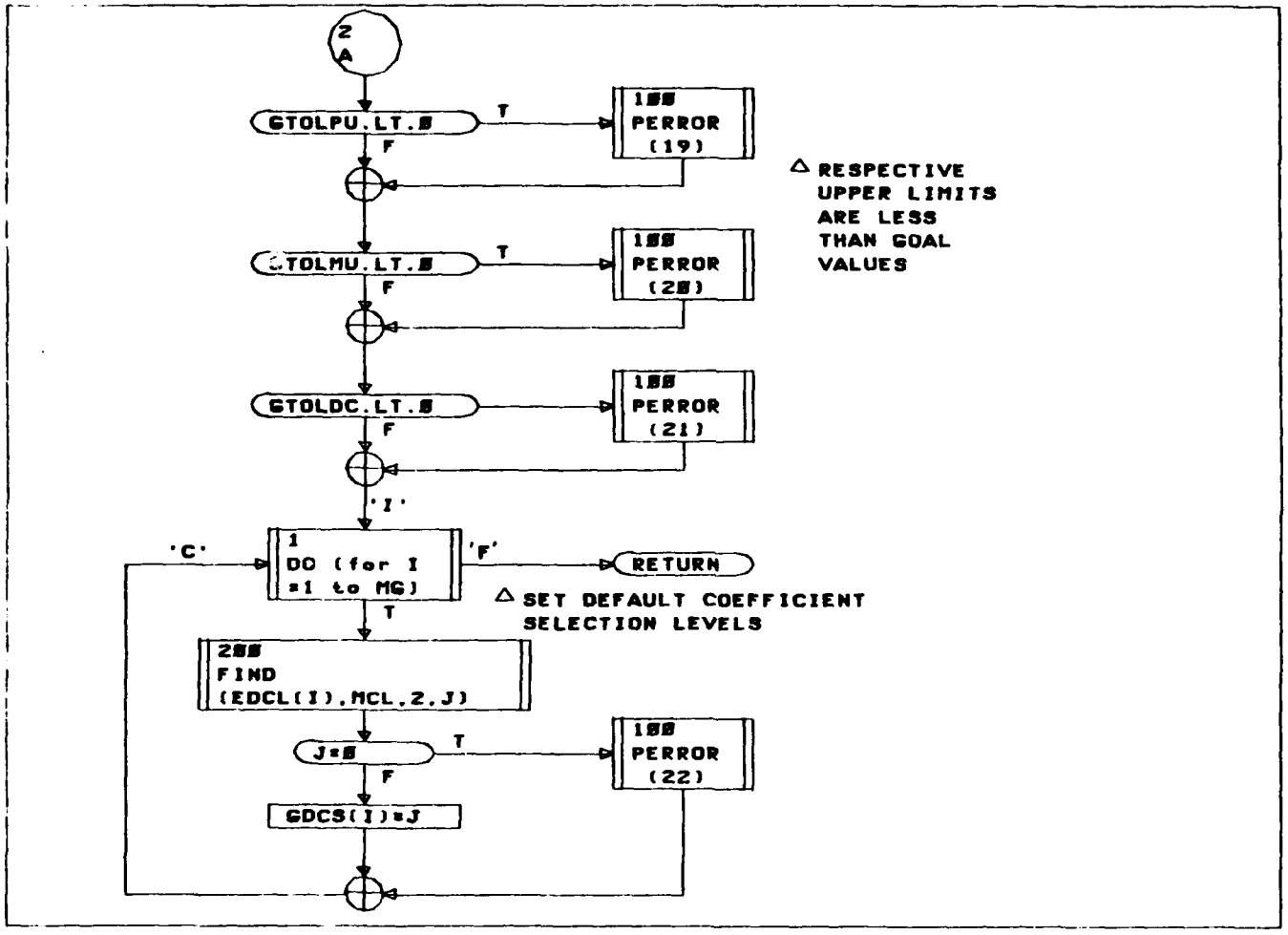
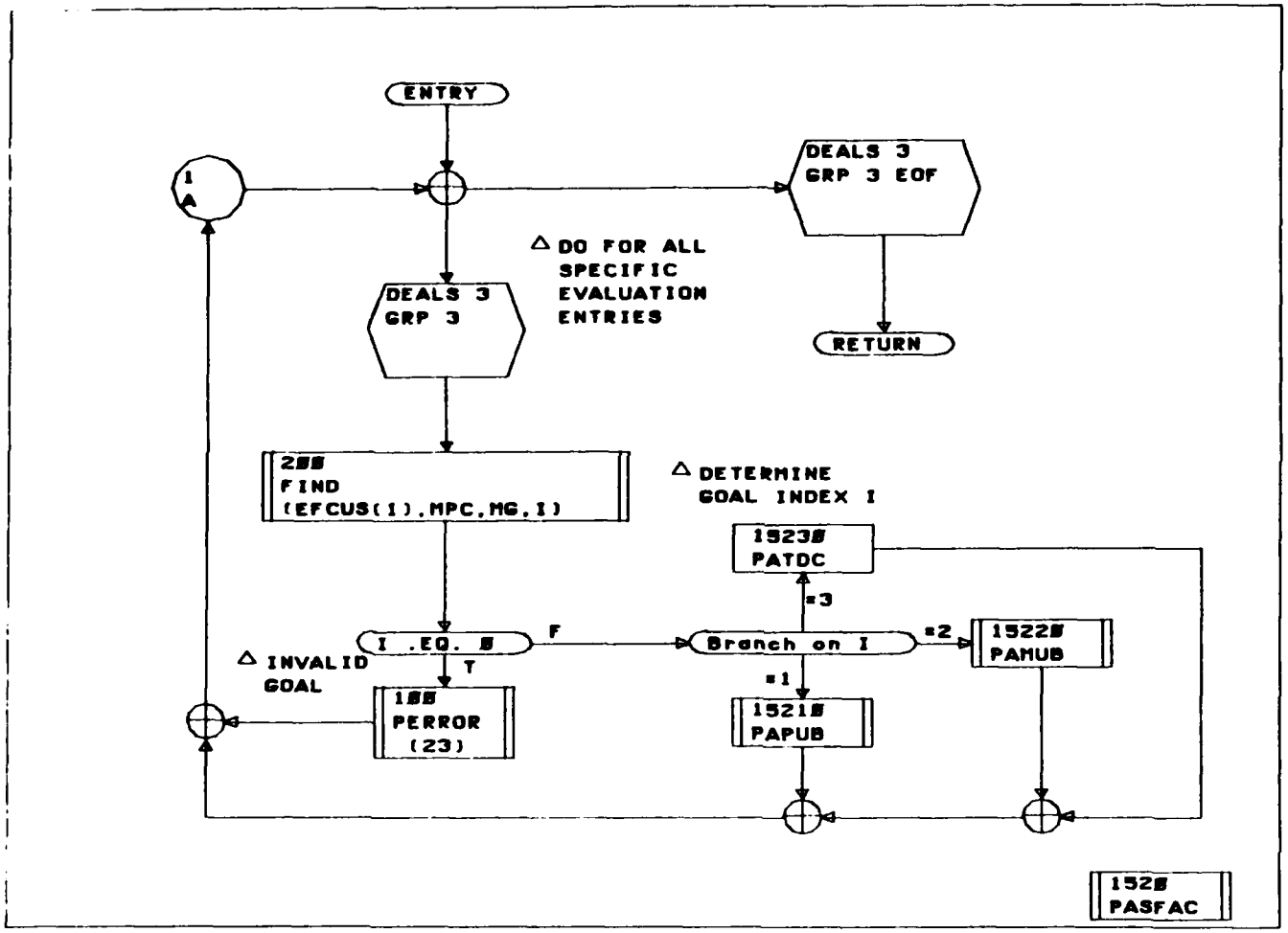
DEALS


2
A
GTOLPU.LT.0
T
F
100
PERROR
(19)
GTOLMU.LT.0
T
F
100
PERROR
(20)
GTOLDC.LT.0
F
100
PERROR
(21)
'I'
'C'
1
DO (for I
=1 to MG)
'F'
RETURN
T
200
FIND
(EDCL(I),MCL,2,J)
J=0
T
F
100
PERROR
(22)
GDCS(I)=J
△ RESPECTIVE UPPER LIMITS ARE LESS THAN GOAL VALUES
△ SET DEFAULT COEFFICIENT SELECTION LEVELS

DEALS



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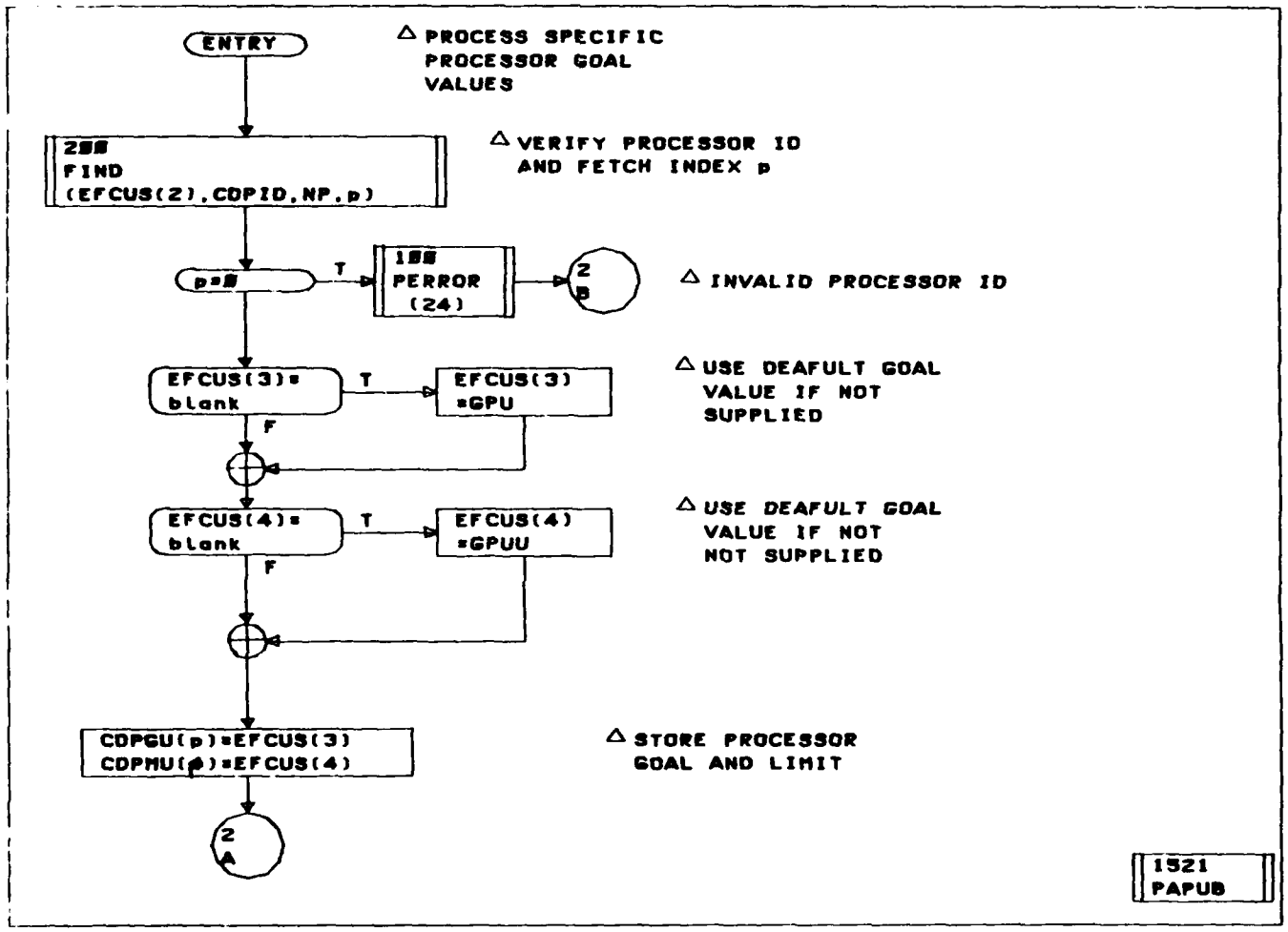
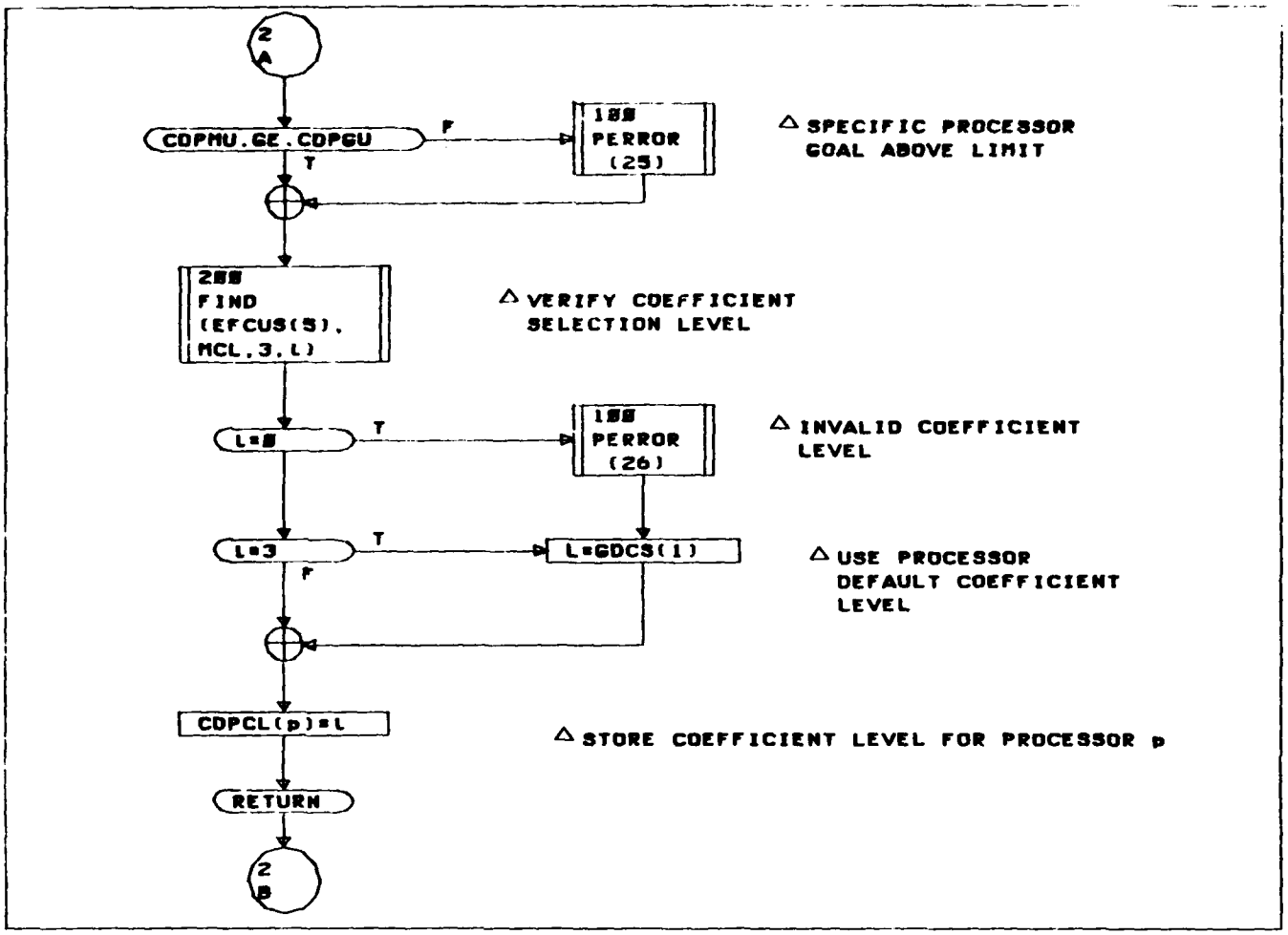
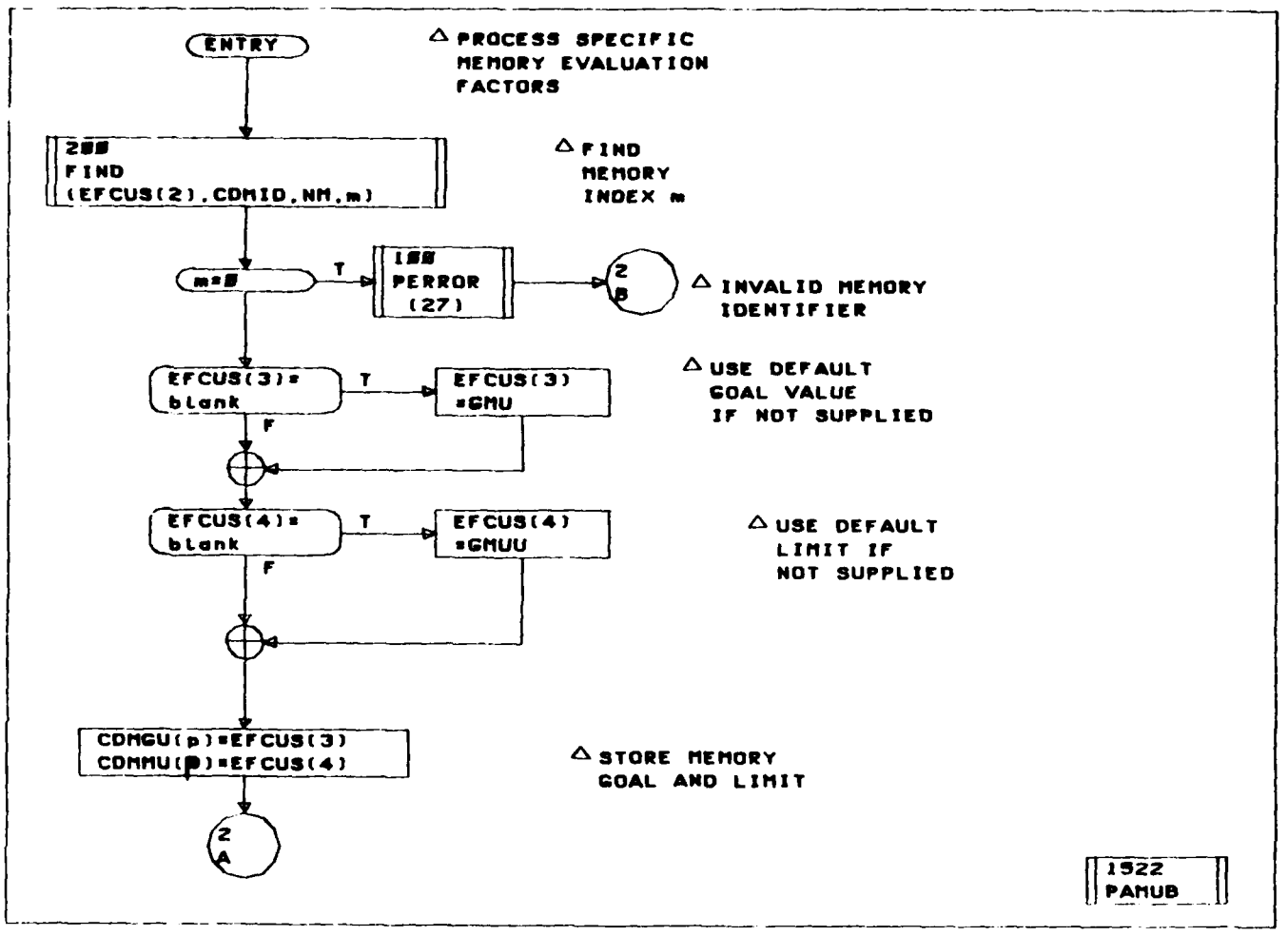
DEALS


ENTRY
△ PROCESS SPECIFIC PROCESSOR GOAL VALUES
200 FIND (EFCUS(2),CDPID,NP,p)
△ VERIFY PROCESSOR ID AND FETCH INDEX p
p=0
T
100 PERROR (24)
2 B
△ INVALID PROCESSOR ID
EFCUS(3)= blank
T
EFCUS(3) =GPU
F
△ USE DEAFULT GOAL VALUE IF NOT SUPPLIED
EFCUS(4)= blank
T
EFCUS(4) =GPUU
F
△ USE DEAFULT GOAL VALUE IF NOT NOT SUPPLIED
CDPGU(p)=EFCUS(3)
CDPMU(p)=EFCUS(4)
△ STORE PROCESSOR GOAL AND LIMIT
2 A
1521 PAPUB

DEALS


2
A
CDPMU.GE.CDPGU
F
T
100
PERROR
(25)
△ SPECIFIC PROCESSOR GOAL ABOVE LIMIT
200
FIND
(EFCUS(S),
MCL,3,L)
△ VERIFY COEFFICIENT SELECTION LEVEL
L=0
T
100
PERROR
(26)
△ INVALID COEFFICIENT LEVEL
L=3
T
F
L=GDCS(I)
△ USE PROCESSOR DEFAULT COEFFICIENT LEVEL
CDPCL(p)=L
△ STORE COEFFICIENT LEVEL FOR PROCESSOR p
RETURN
2
B

DEALS



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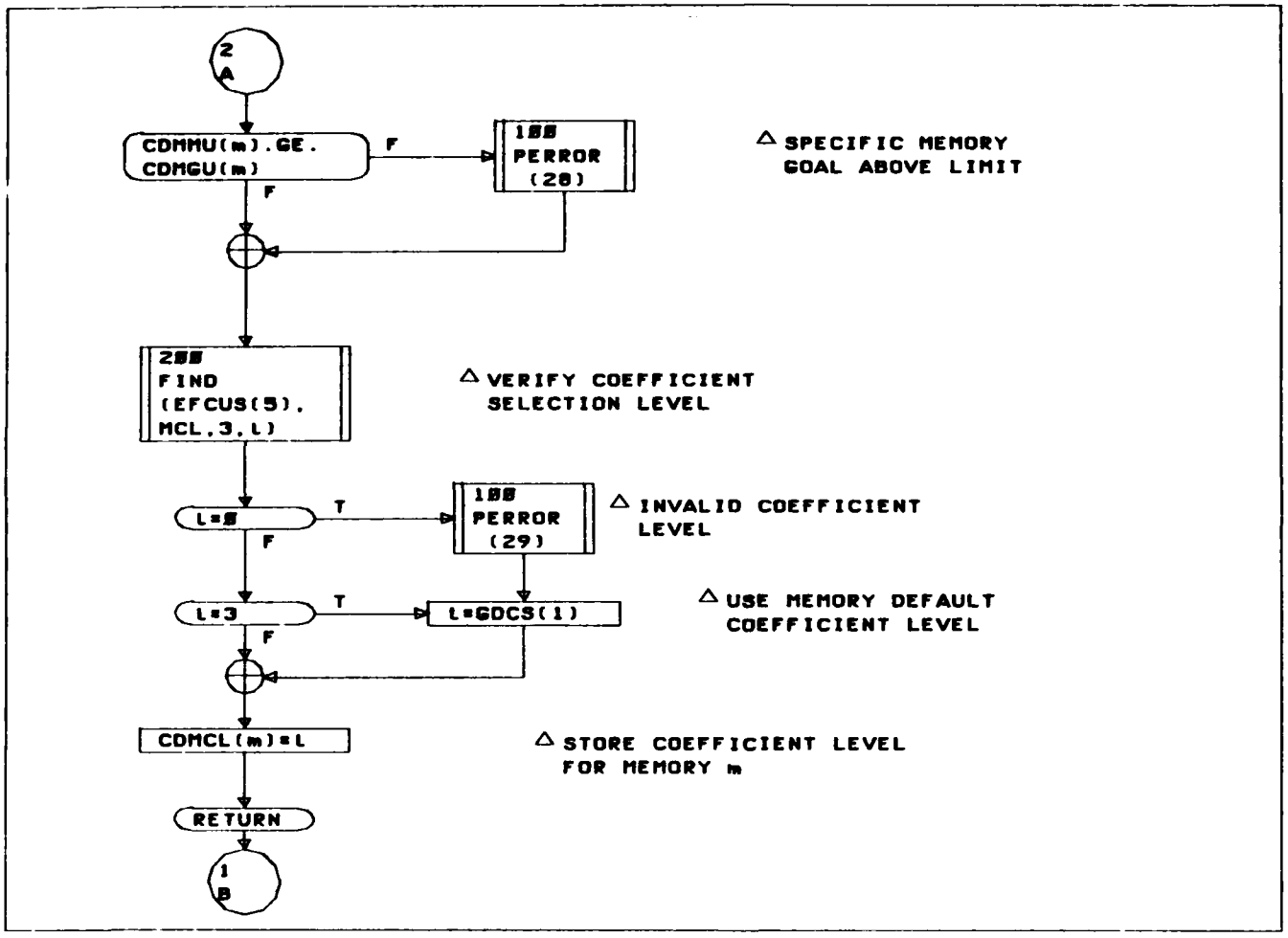
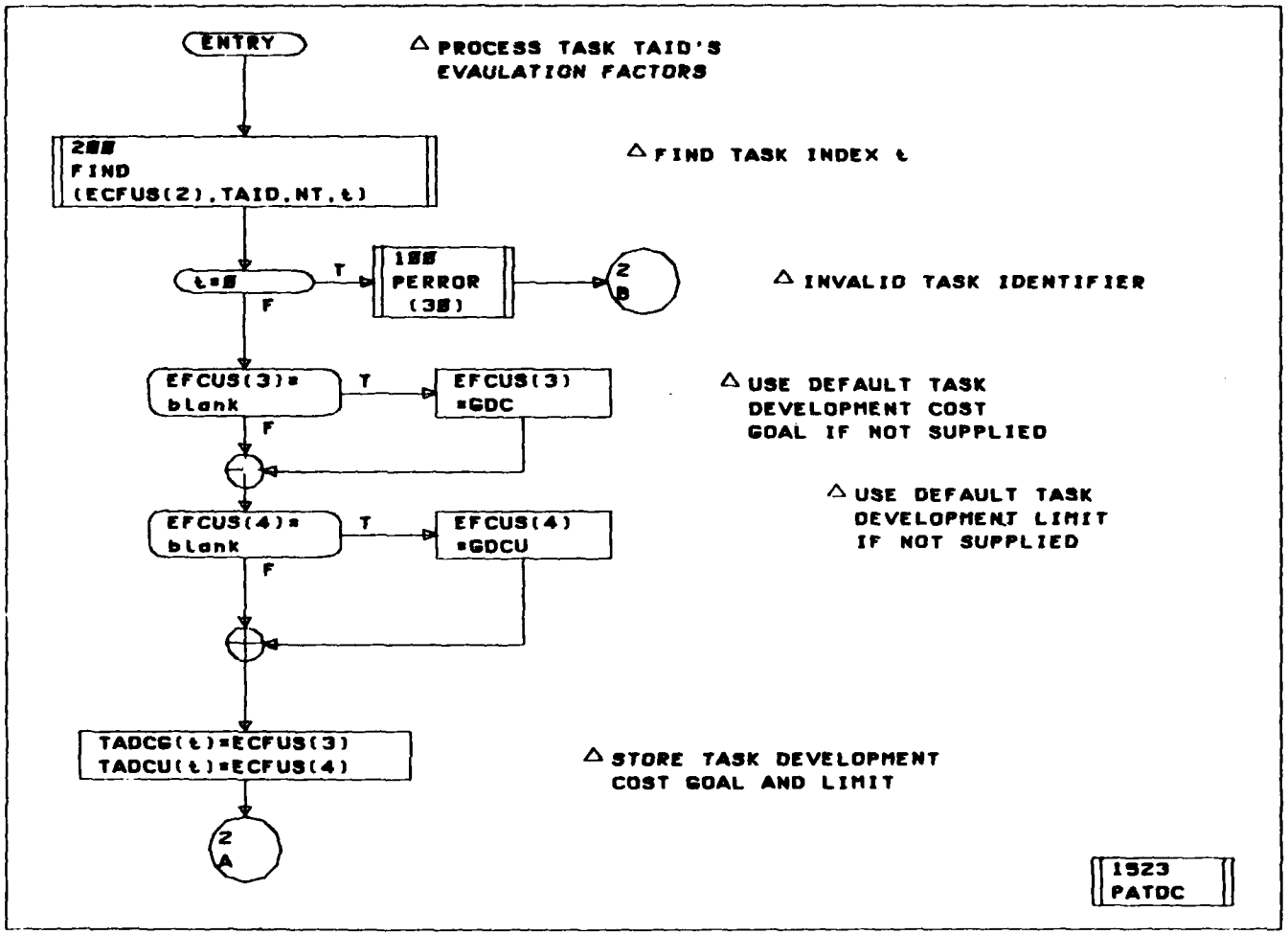
DEALS



ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1522 PAGE 2

DEALS



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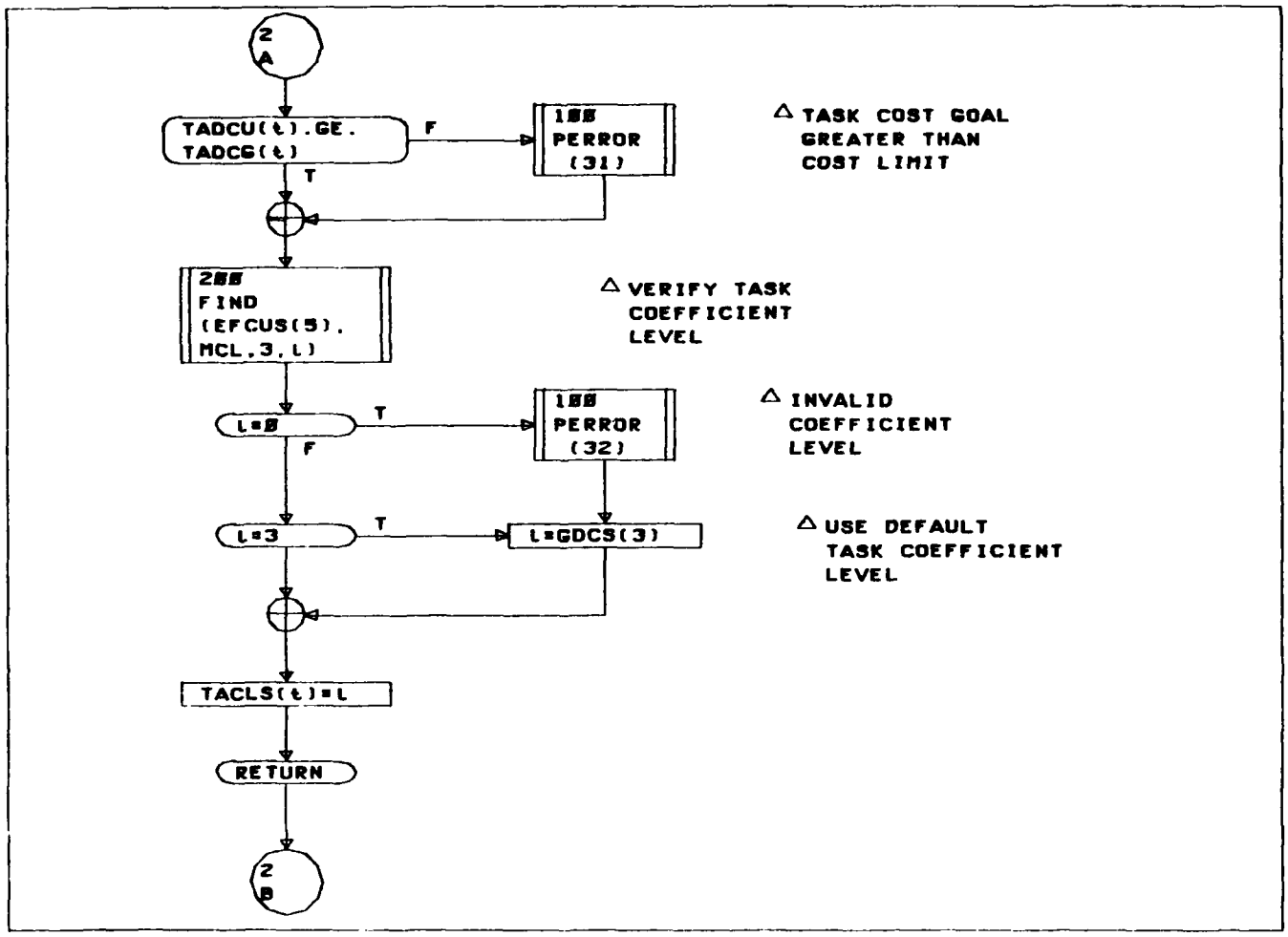
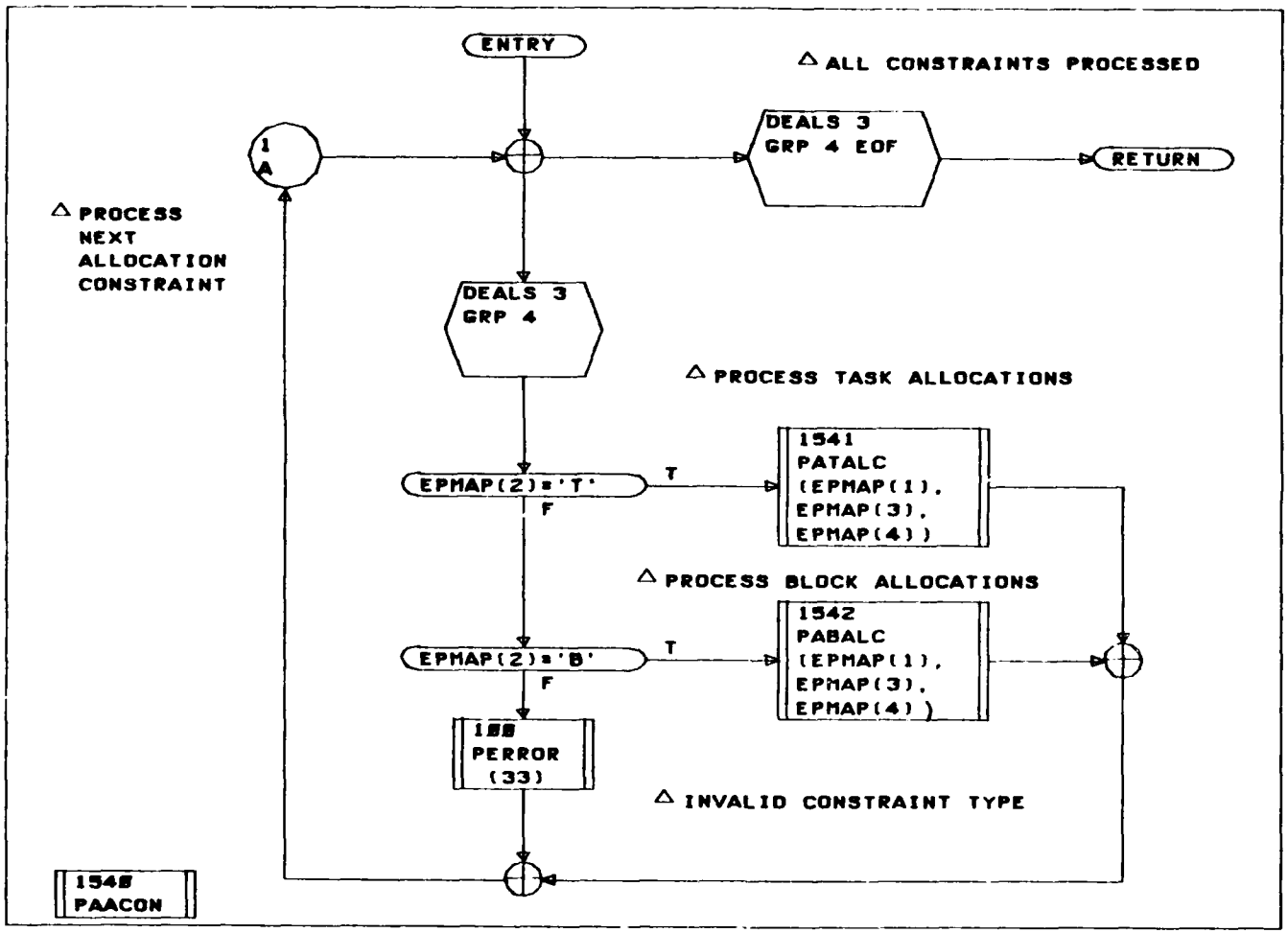
DEALS

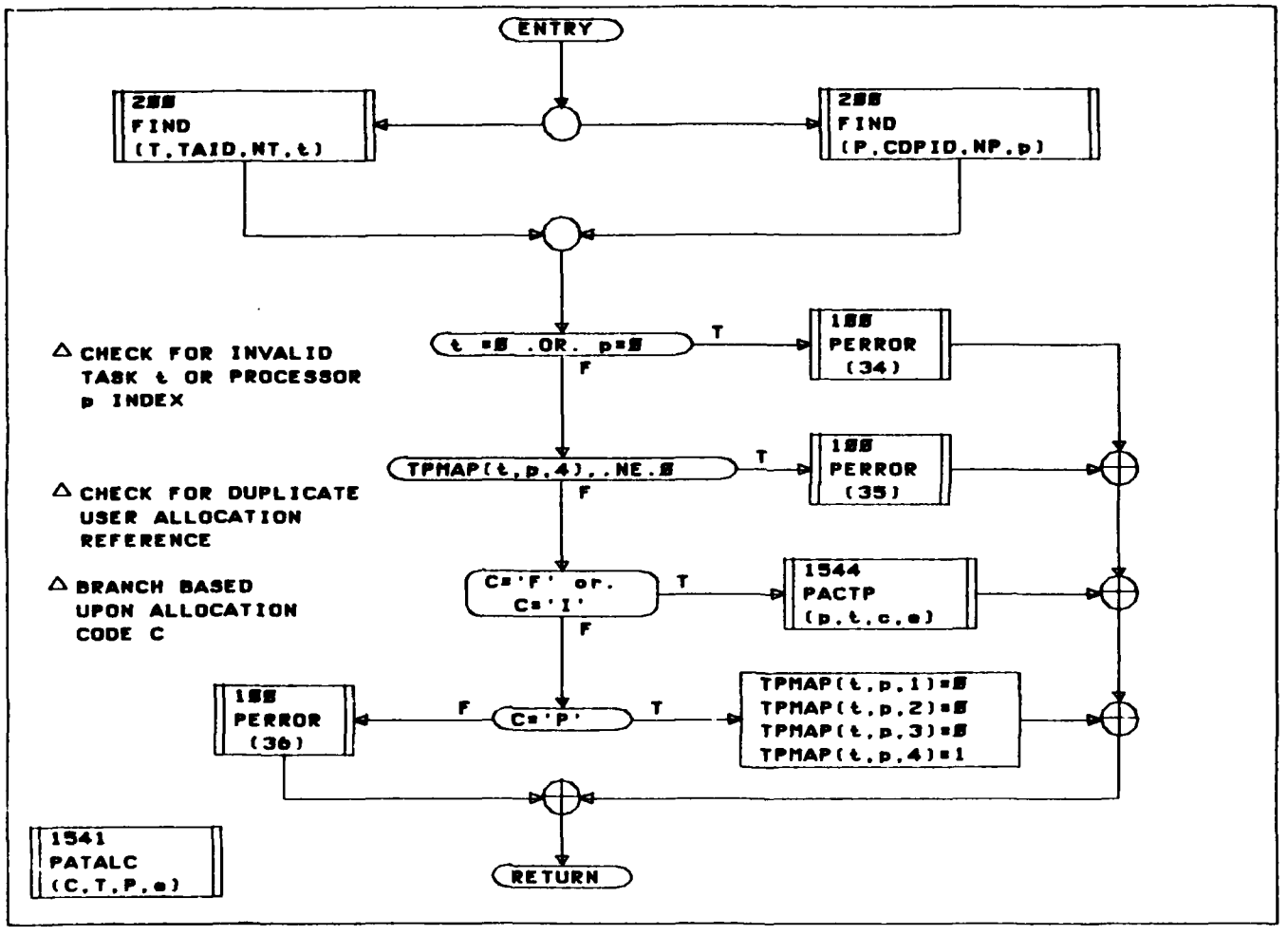

2
A
TADCU(t).GE.
TADCG(t)
F
T
100
PERROR
(31)
△ TASK COST GOAL
GREATER THAN
COST LIMIT
200
FIND
(EFCUS(5),
MCL,3,L)
△ VERIFY TASK
COEFFICIENT
LEVEL
L=0
T
F
100
PERROR
(32)
△ INVALID
COEFFICIENT
LEVEL
L=3
T
L=GDCS(3)
△ USE DEFAULT
TASK COEFFICIENT
LEVEL
TACLS(t)=L
RETURN
2
B

DEALS

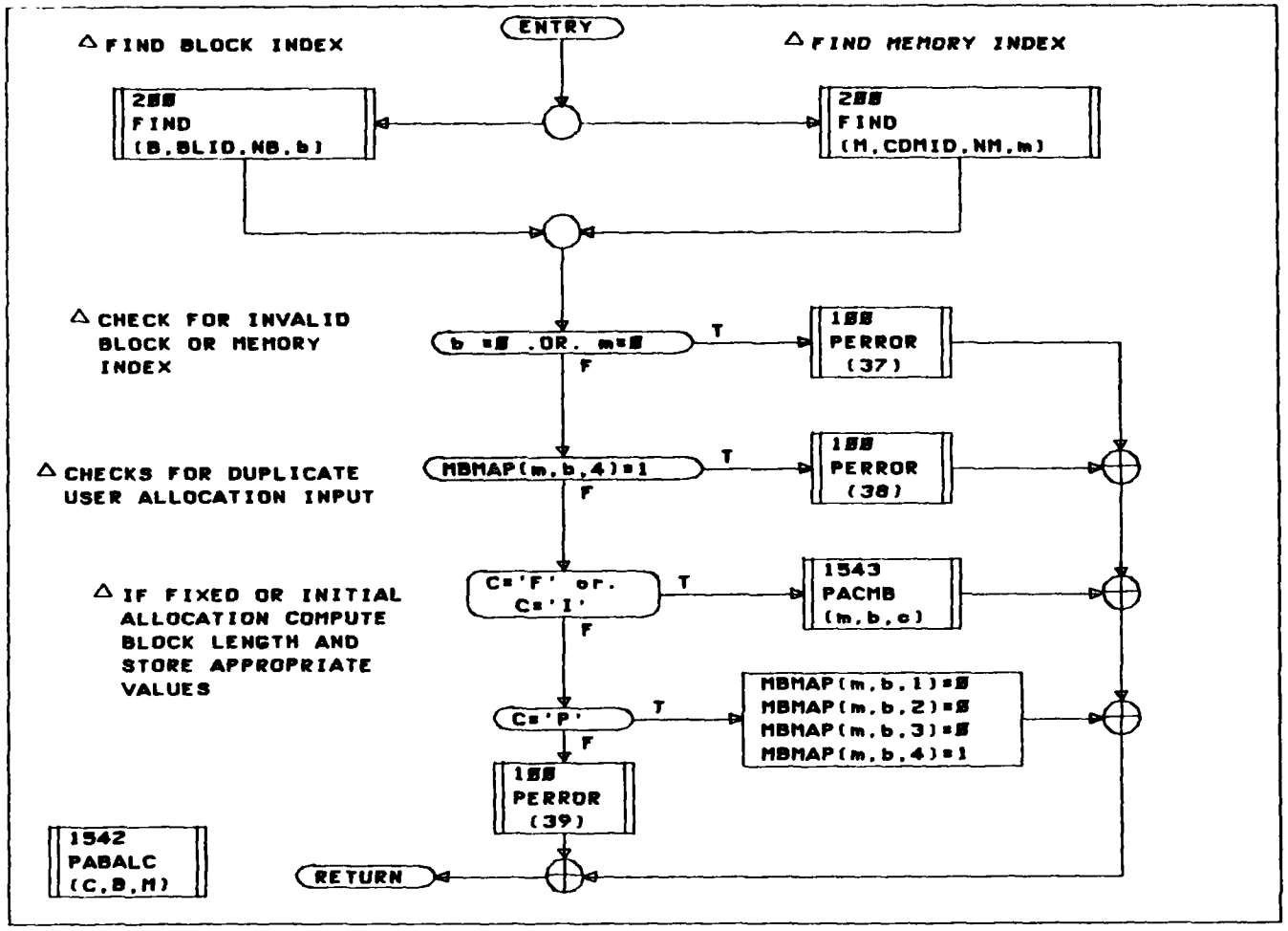


ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1540 PAGE 1

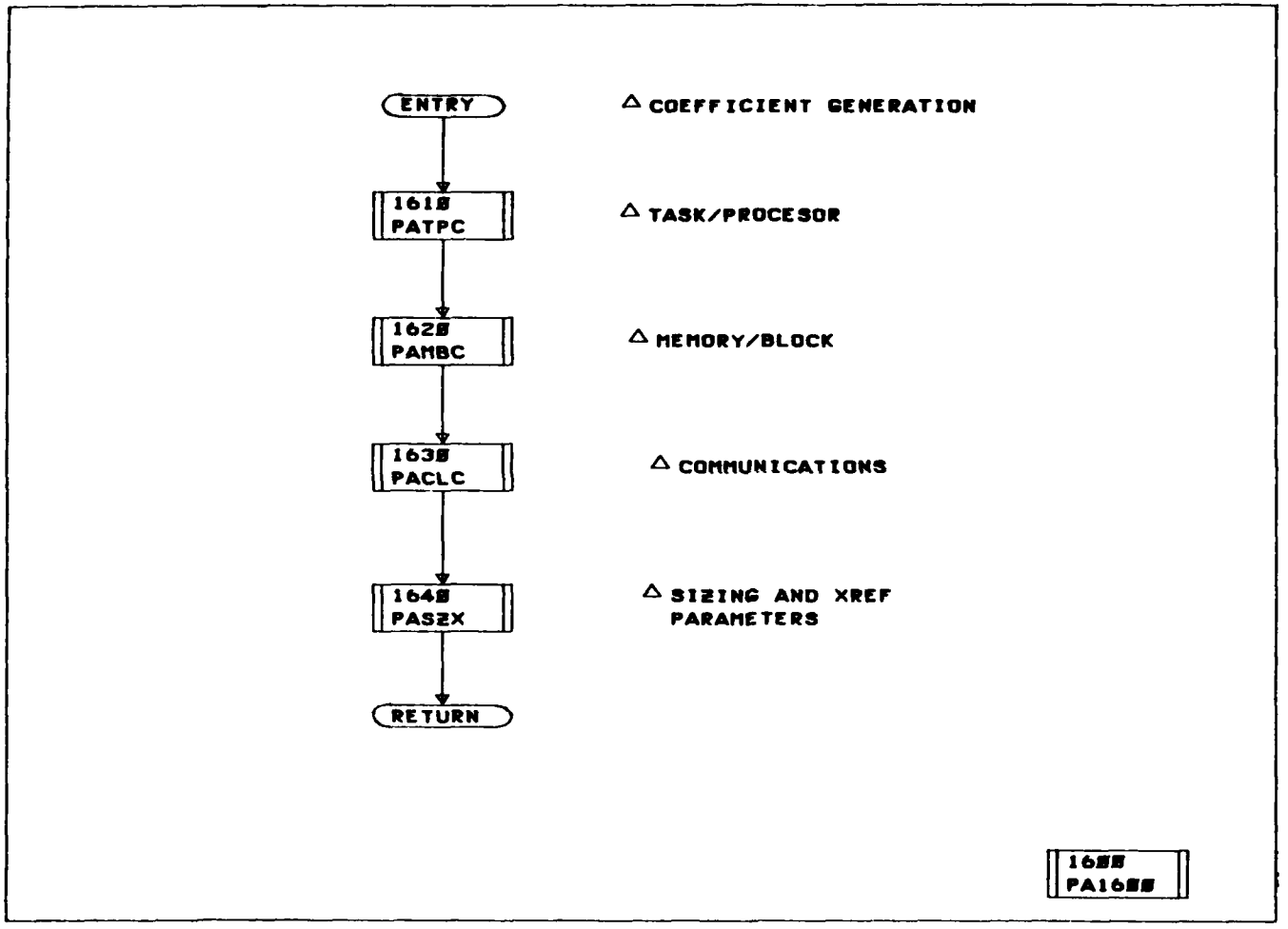
DEALS


ENTRY
200
FIND
(T,TAID,NT,t)
200
FIND
(P,CDPID,NP,p)
t =0 .OR. p=0
T
F
100
PERROR
(34)
TPMAP(t,p,4),.NE.0
T
F
100
PERROR
(35)
C='F' or.
C='I'
T
F
1544
PACTP
(p,t,c,e)
C='P'
F
T
100
PERROR
(36)
TPMAP(t,p,1)=0
TPMAP(t,p,2)=0
TPMAP(t,p,3)=0
TPMAP(t,p,4)=1
△ CHECK FOR INVALID TASK t OR PROCESSOR p INDEX
△ CHECK FOR DUPLICATE USER ALLOCATION REFERENCE
△ BRANCH BASED UPON ALLOCATION CODE C
1541
PATALC
(C,T,P,e)
RETURN

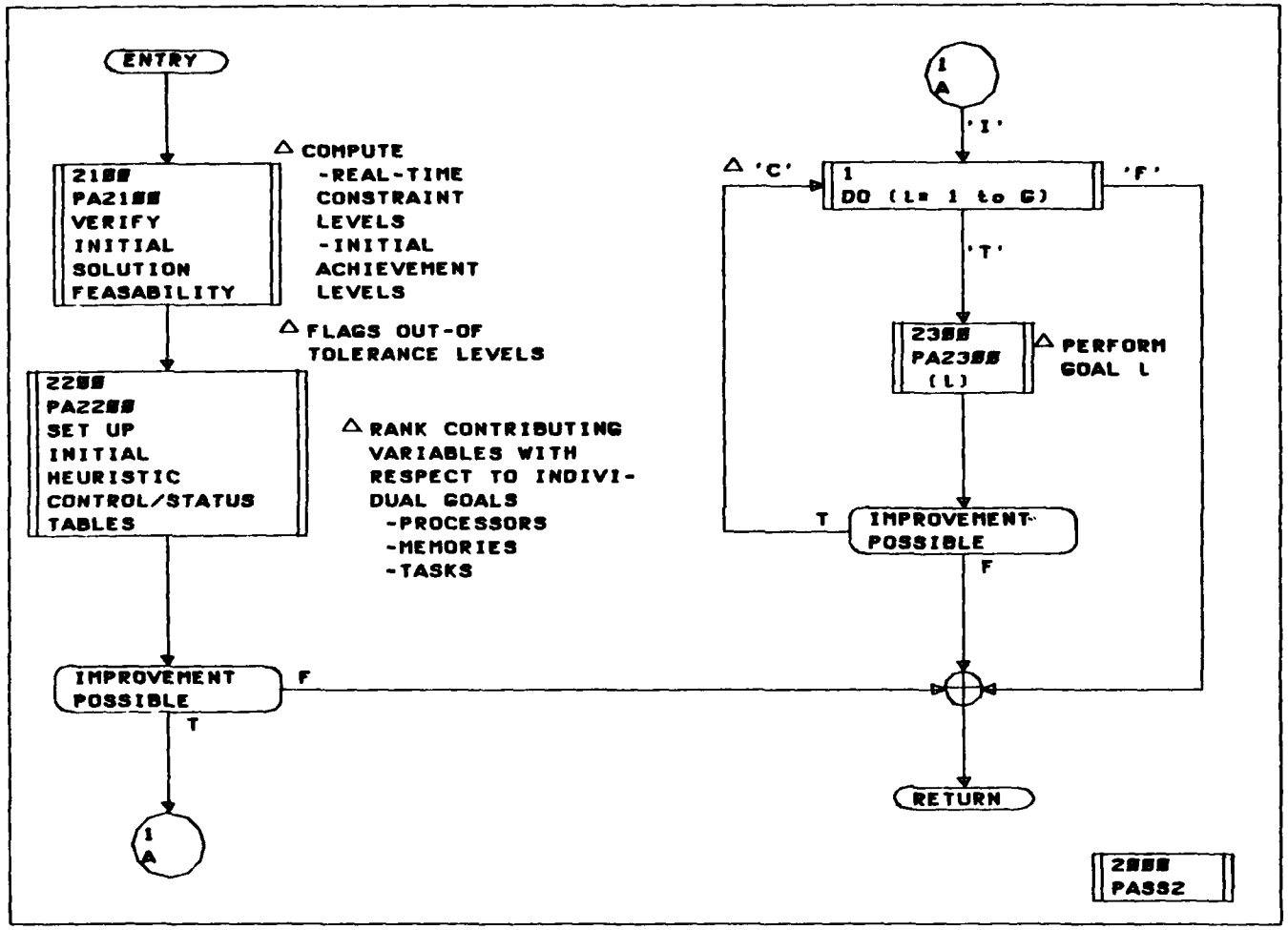
DEALS


ENTRY
△ FIND BLOCK INDEX
200
FIND
(B,BLID,NB,b)
△ FIND MEMORY INDEX
200
FIND
(M,CDMID,NM,m)
△ CHECK FOR INVALID BLOCK OR MEMORY INDEX
b =0 .OR. m=0
T
F
100
PERROR
(37)
△ CHECKS FOR DUPLICATE USER ALLOCATION INPUT
MBMAP(m,b,4)=1
T
F
100
PERROR
(38)
△ IF FIXED OR INITIAL ALLOCATION COMPUTE BLOCK LENGTH AND STORE APPROPRIATE VALUES
C='F' or. C='I'
T
F
1543
PACMB
(m,b,c)
C='P'
T
F
MBMAP(m,b,1)=0
MBMAP(m,b,2)=0
MBMAP(m,b,3)=0
MBMAP(m,b,4)=1
100
PERROR
(39)
1542
PABALC
(C,B,M)
RETURN

DEALS


ENTRY
1610
PATPC
1620
PAMBC
1630
PACLC
1640
PASZX
RETURN
△ COEFFICIENT GENERATION
△ TASK/PROCESOR
△ MEMORY/BLOCK
△ COMMUNICATIONS
△ SIZING AND XREF PARAMETERS
1600
PA1600

DEALS



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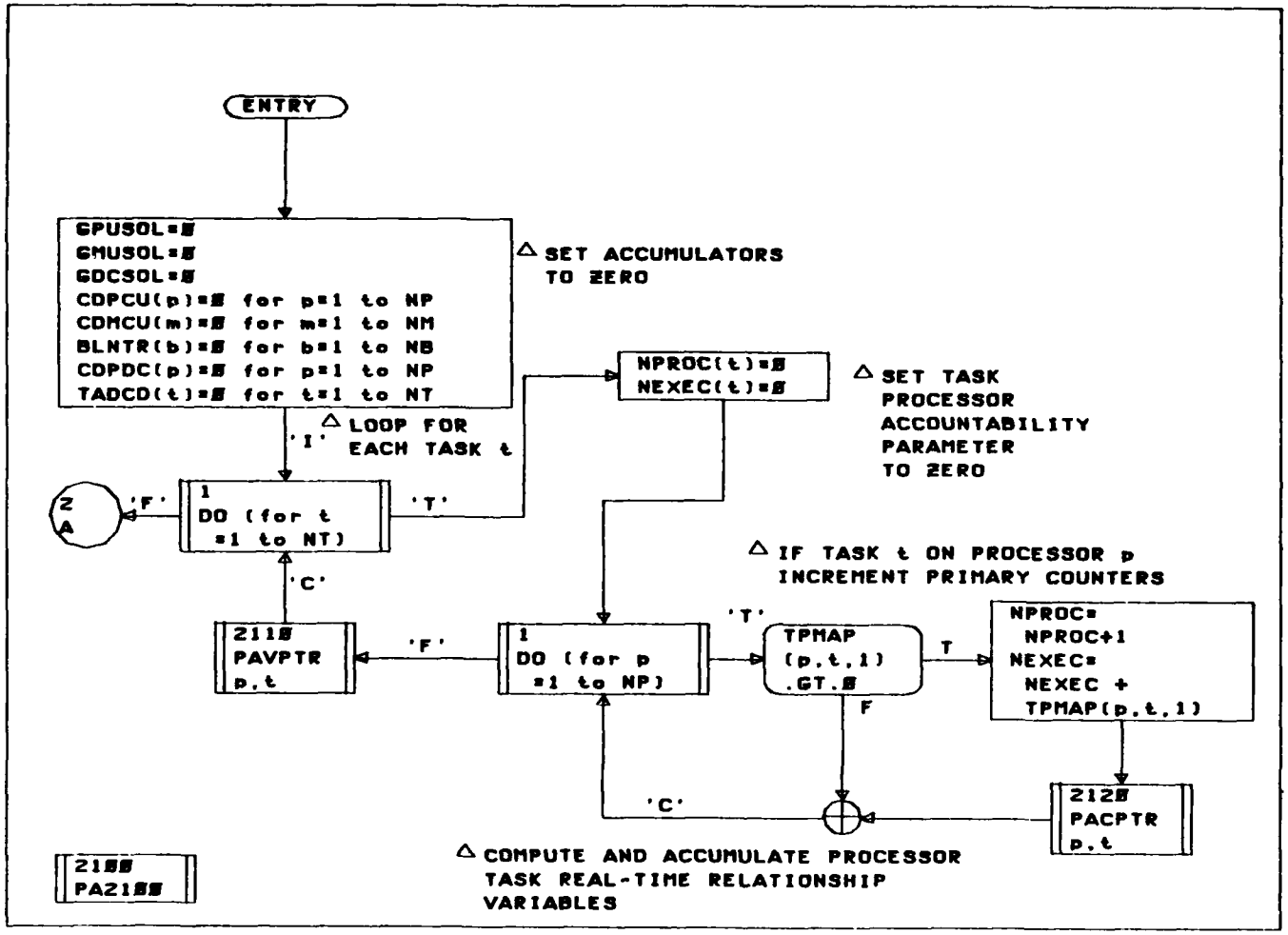
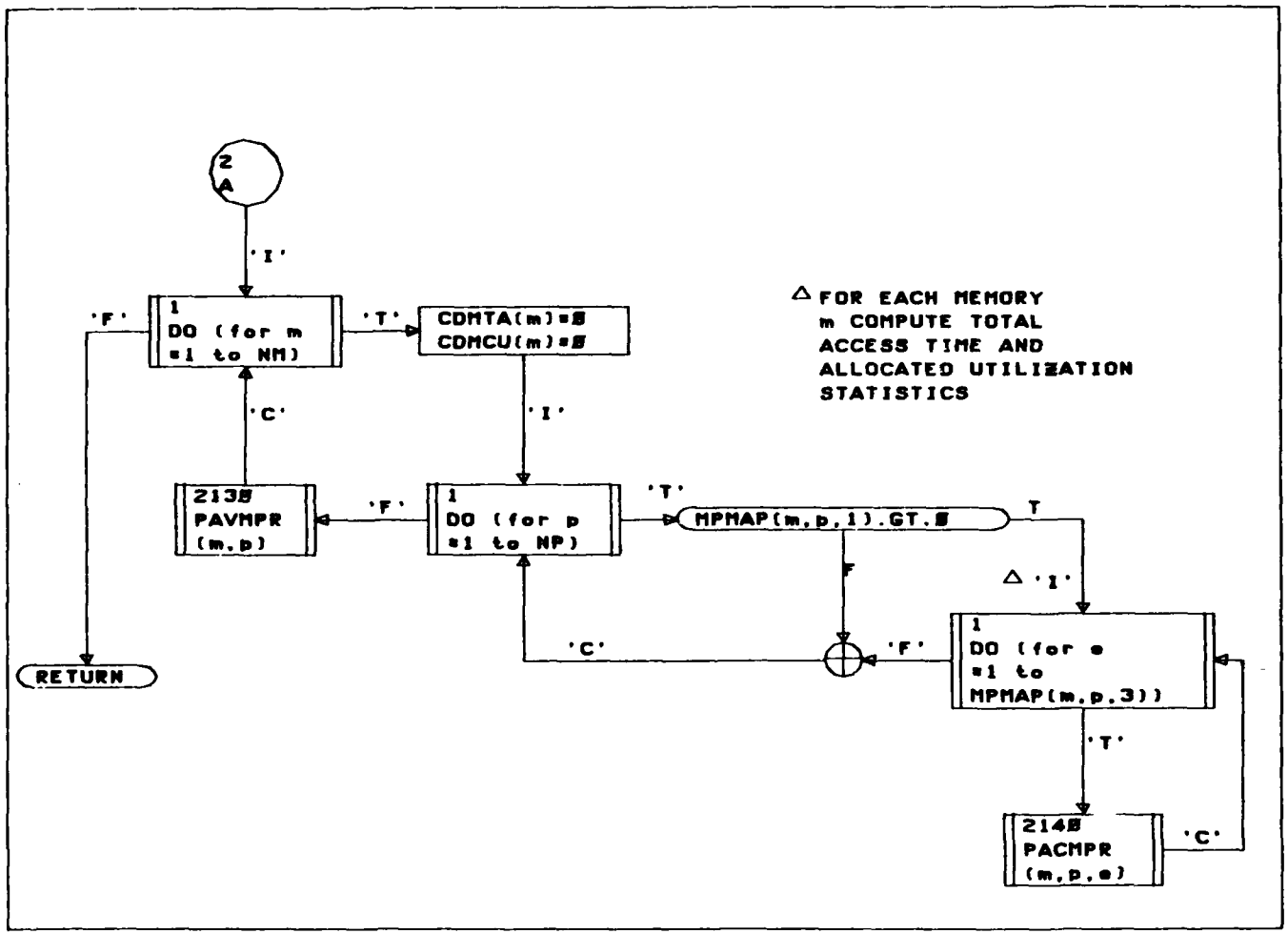
DEALS



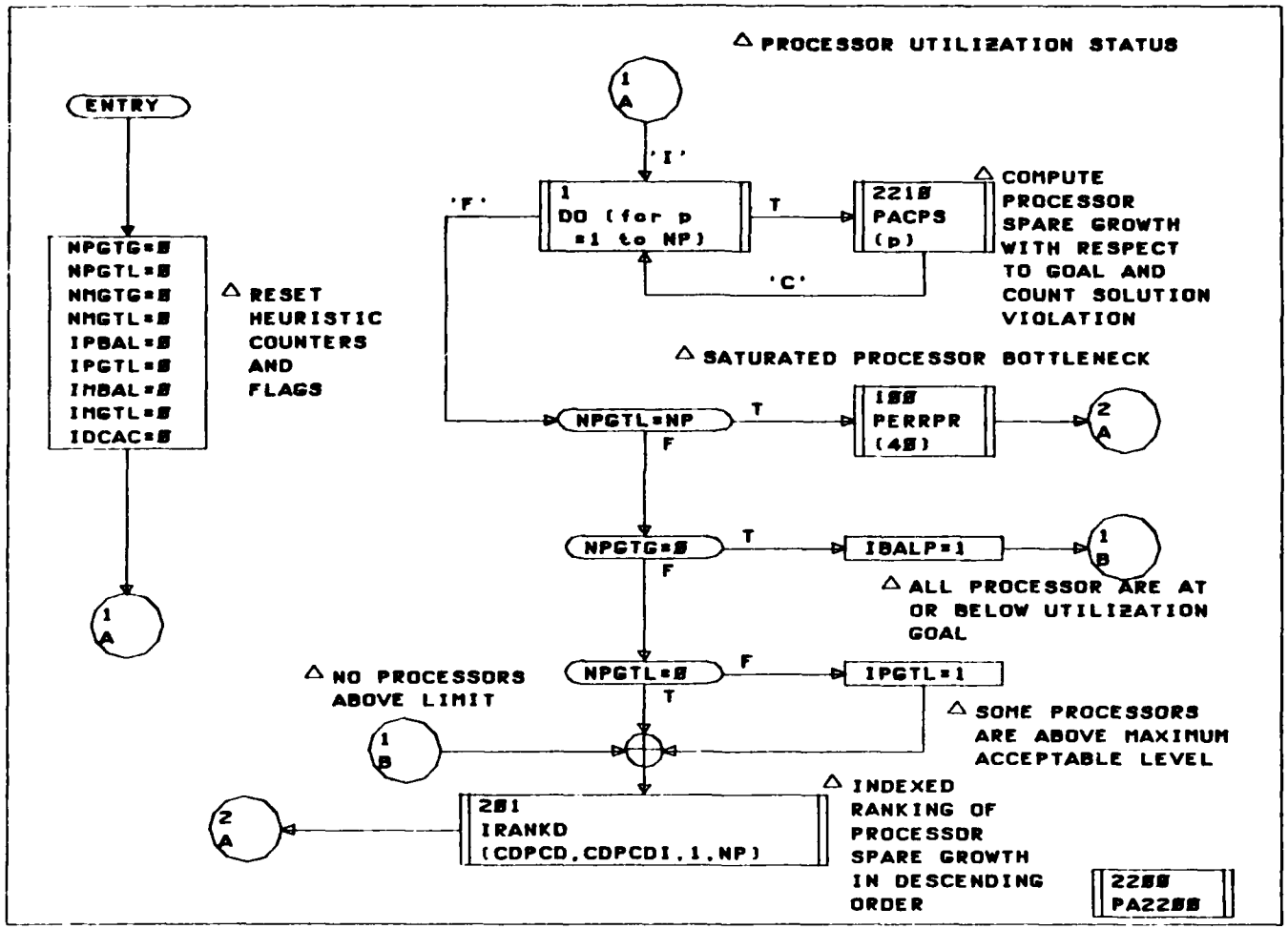
ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-2100 PAGE 1

DEALS

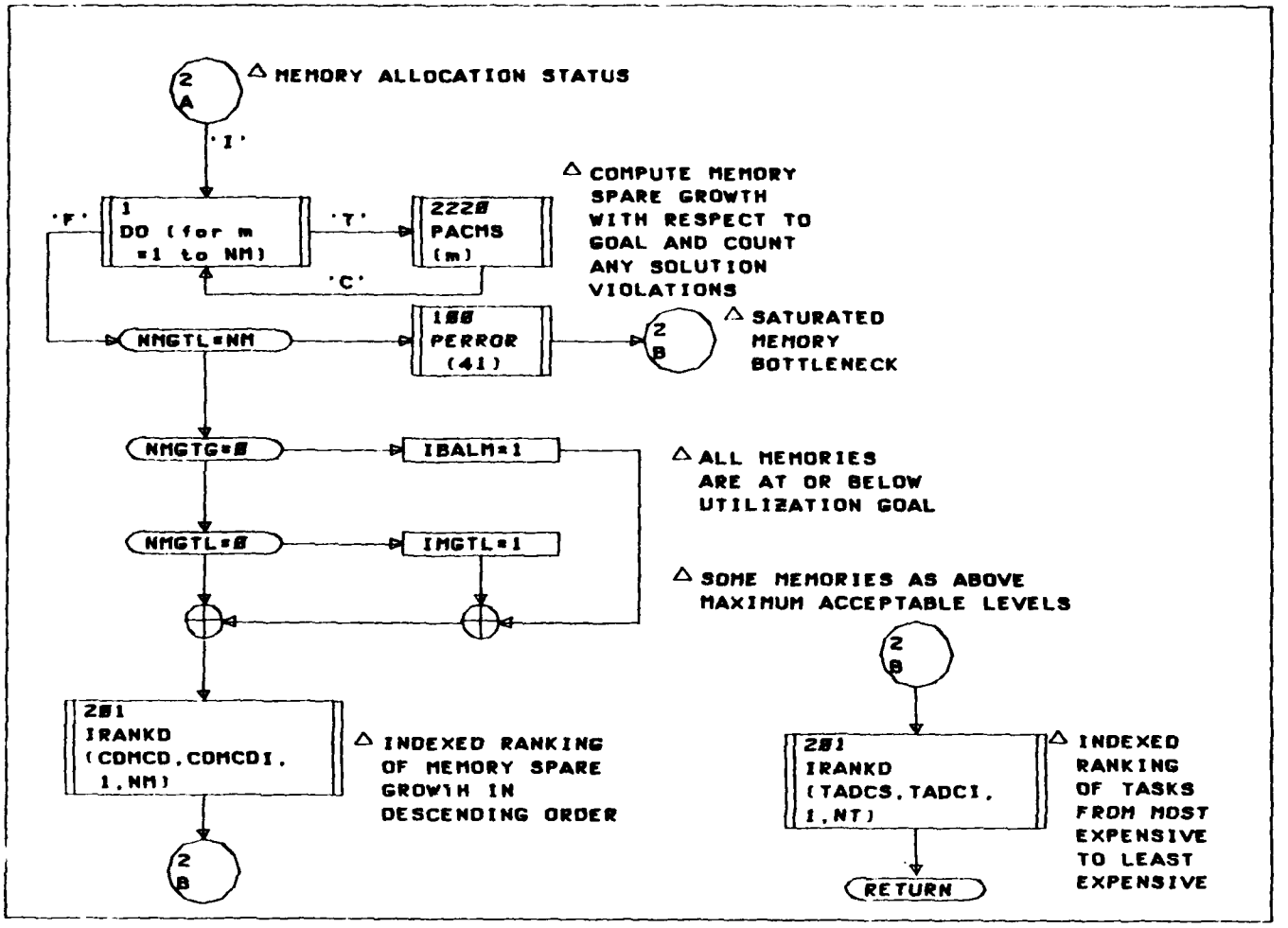


ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-2100 PAGE 2

DEALS


△ PROCESSOR UTILIZATION STATUS
ENTRY
NPGTG=0
NPGTL=0
NMGTG=0
NMGTL=0
IPBAL=0
IPGTL=0
IMBAL=0
IMGTL=0
IDCAC=0
△ RESET HEURISTIC COUNTERS AND FLAGS
1 A
'I'
'F'
1
DO (for p =1 to NP)
T
2210
PACPS
(p)
△ COMPUTE PROCESSOR SPARE GROWTH WITH RESPECT TO GOAL AND COUNT SOLUTION VIOLATION
'C'
△ SATURATED PROCESSOR BOTTLENECK
NPGTL=NP
T
100
PERRPR
(40)
2 A
F
NPGTG=0
T
IBALP=1
1 B
△ ALL PROCESSOR ARE AT OR BELOW UTILIZATION GOAL
F
NPGTL=0
F
IPGTL=1
T
△ NO PROCESSORS ABOVE LIMIT
1 B
△ SOME PROCESSORS ARE ABOVE MAXIMUM ACCEPTABLE LEVEL
2 A
201
IRANKD
(CDPCD,CDPCDI,1,NP)
△ INDEXED RANKING OF PROCESSOR SPARE GROWTH IN DESCENDING ORDER
2200
PA2200

DEALS



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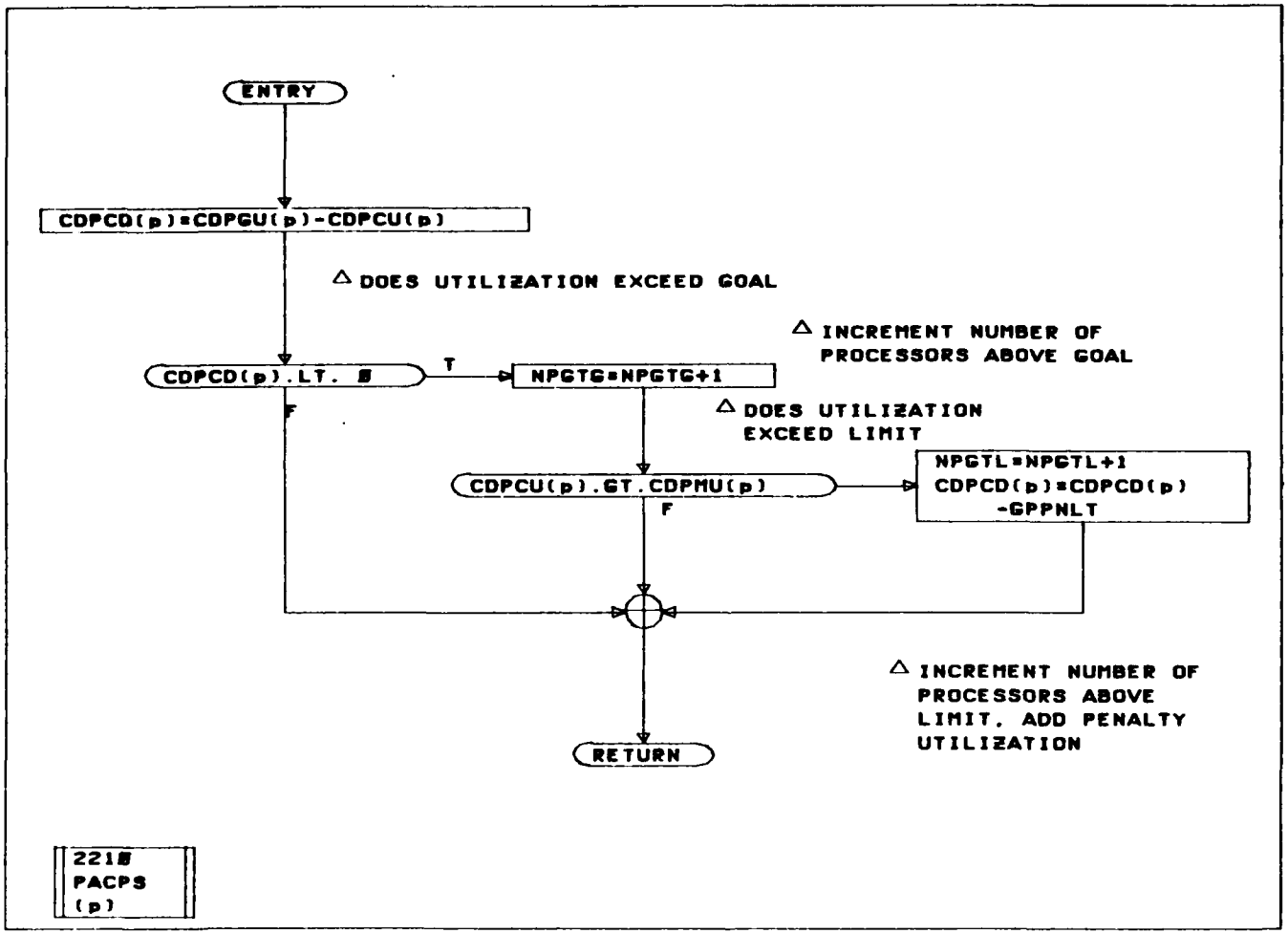
DEALS



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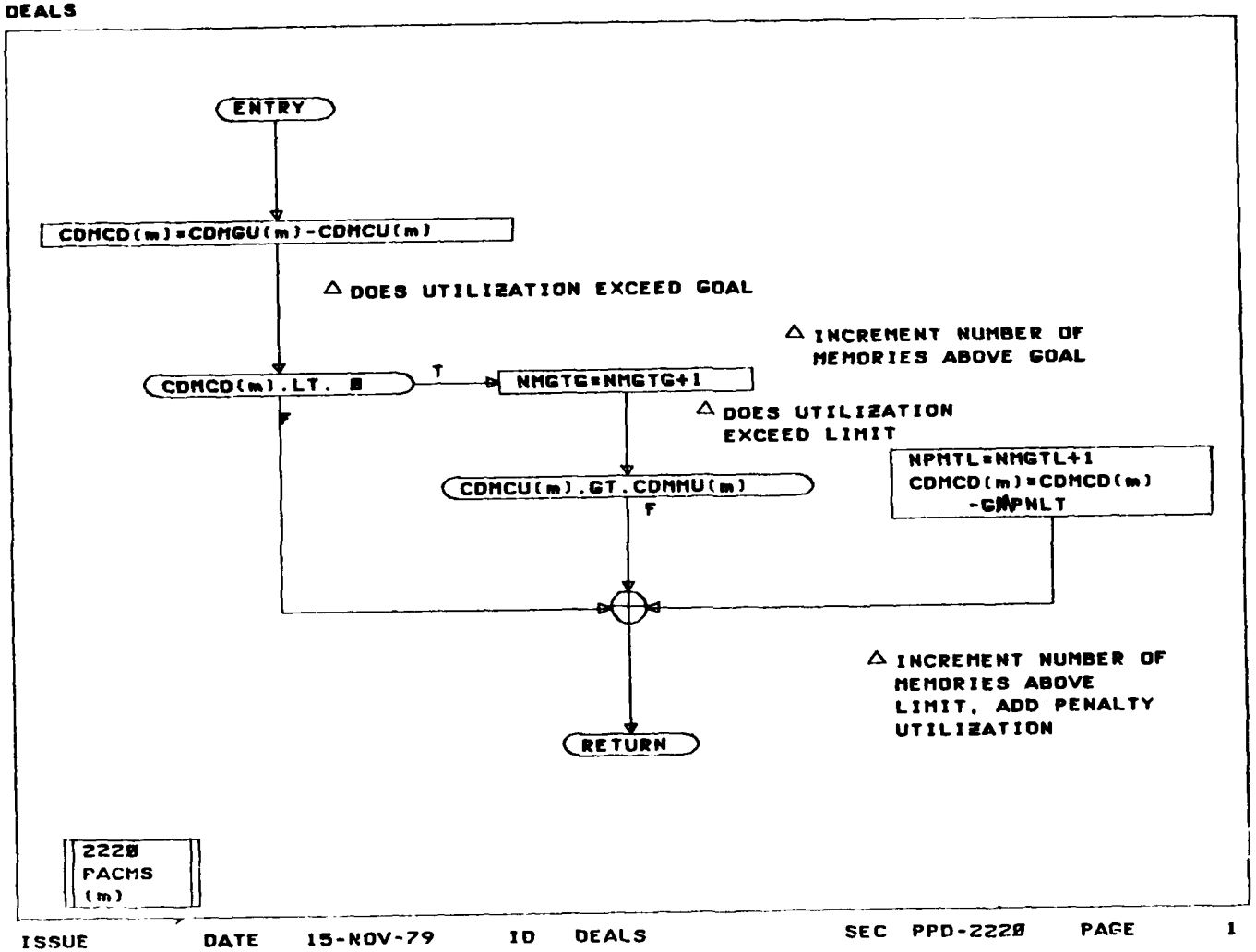
DEALS



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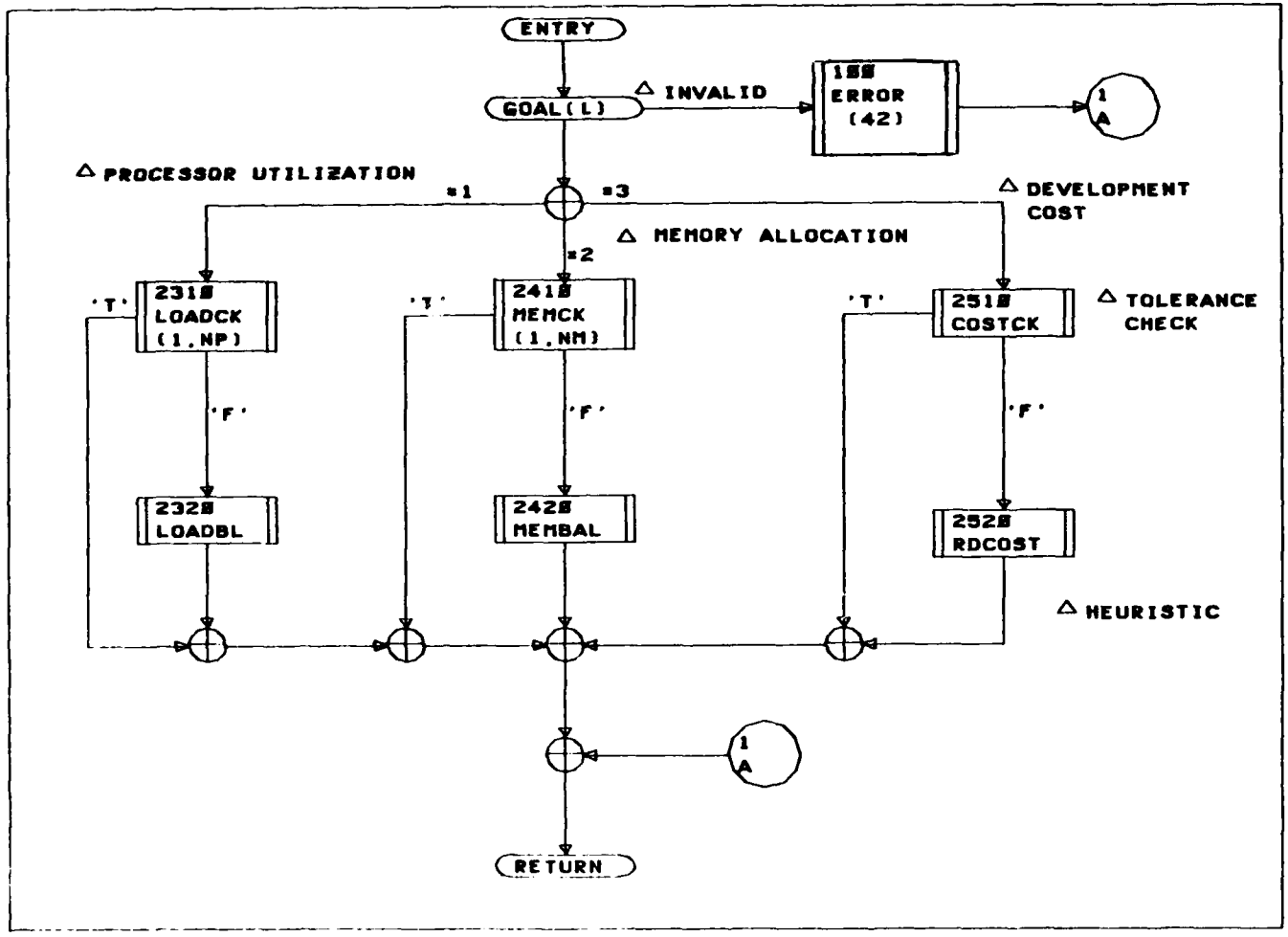
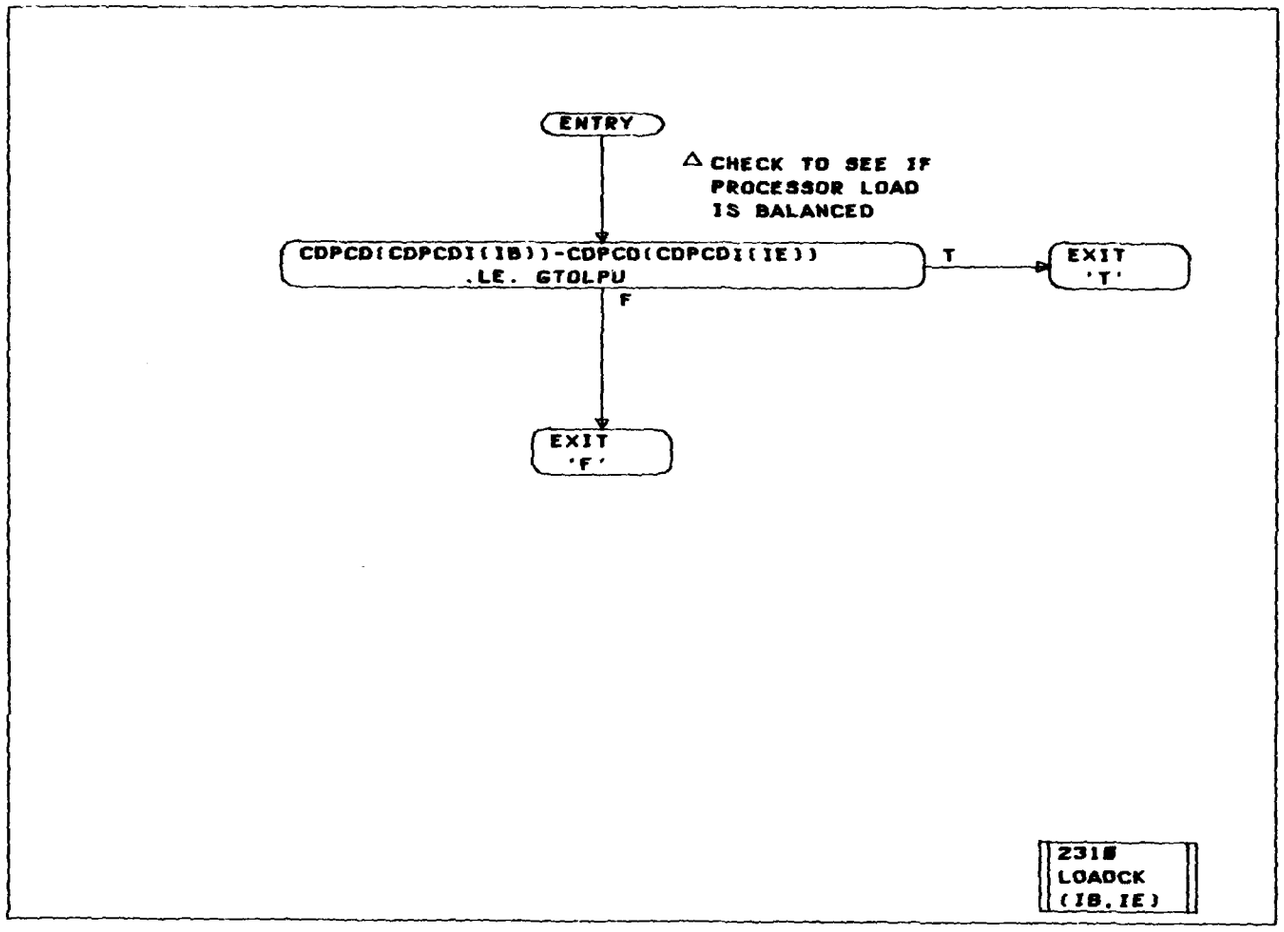
DEALS

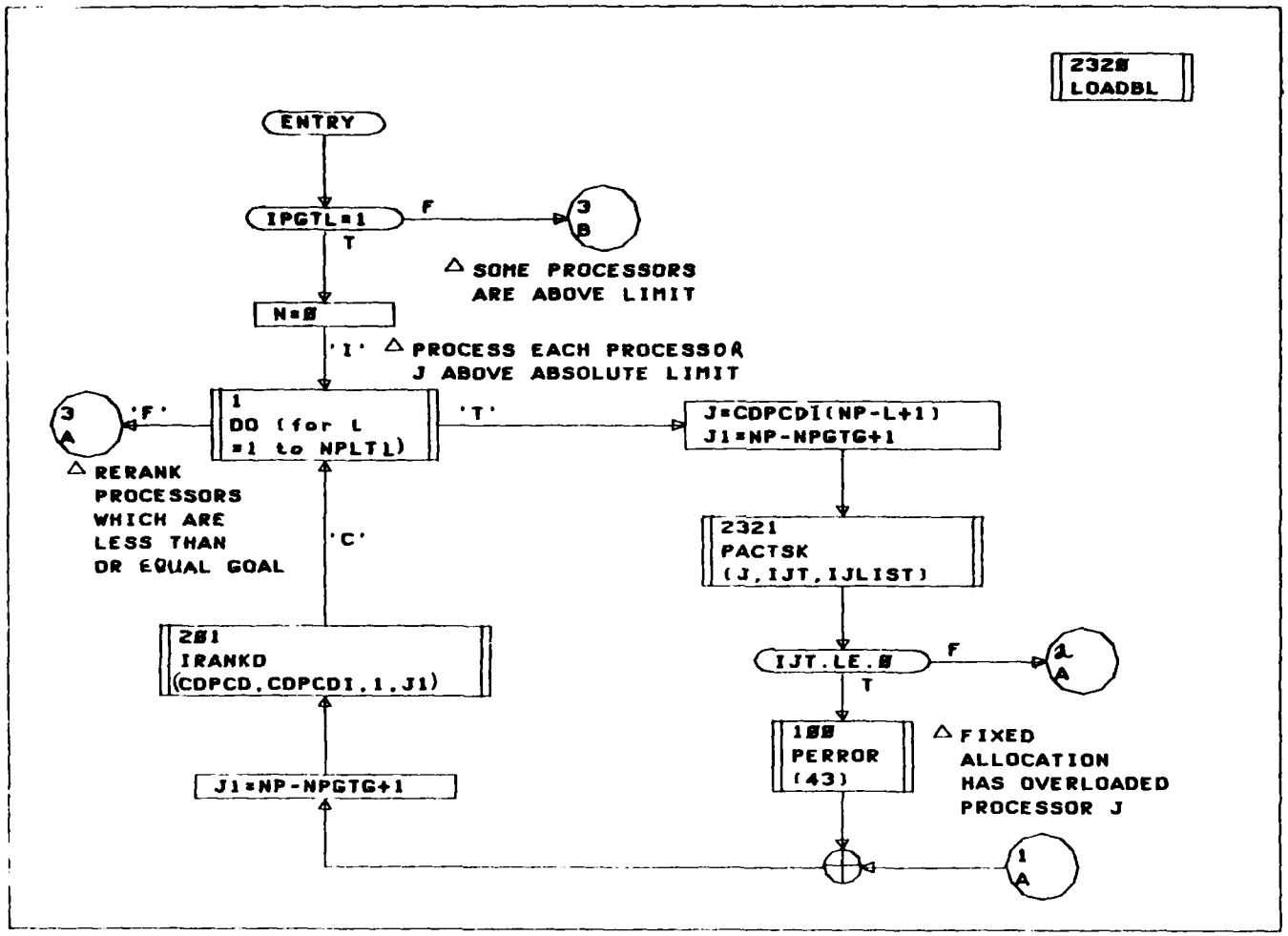


ISSUE DATE 19-NOV-79 ID DEALS SEC PPD-2300 PAGE 1

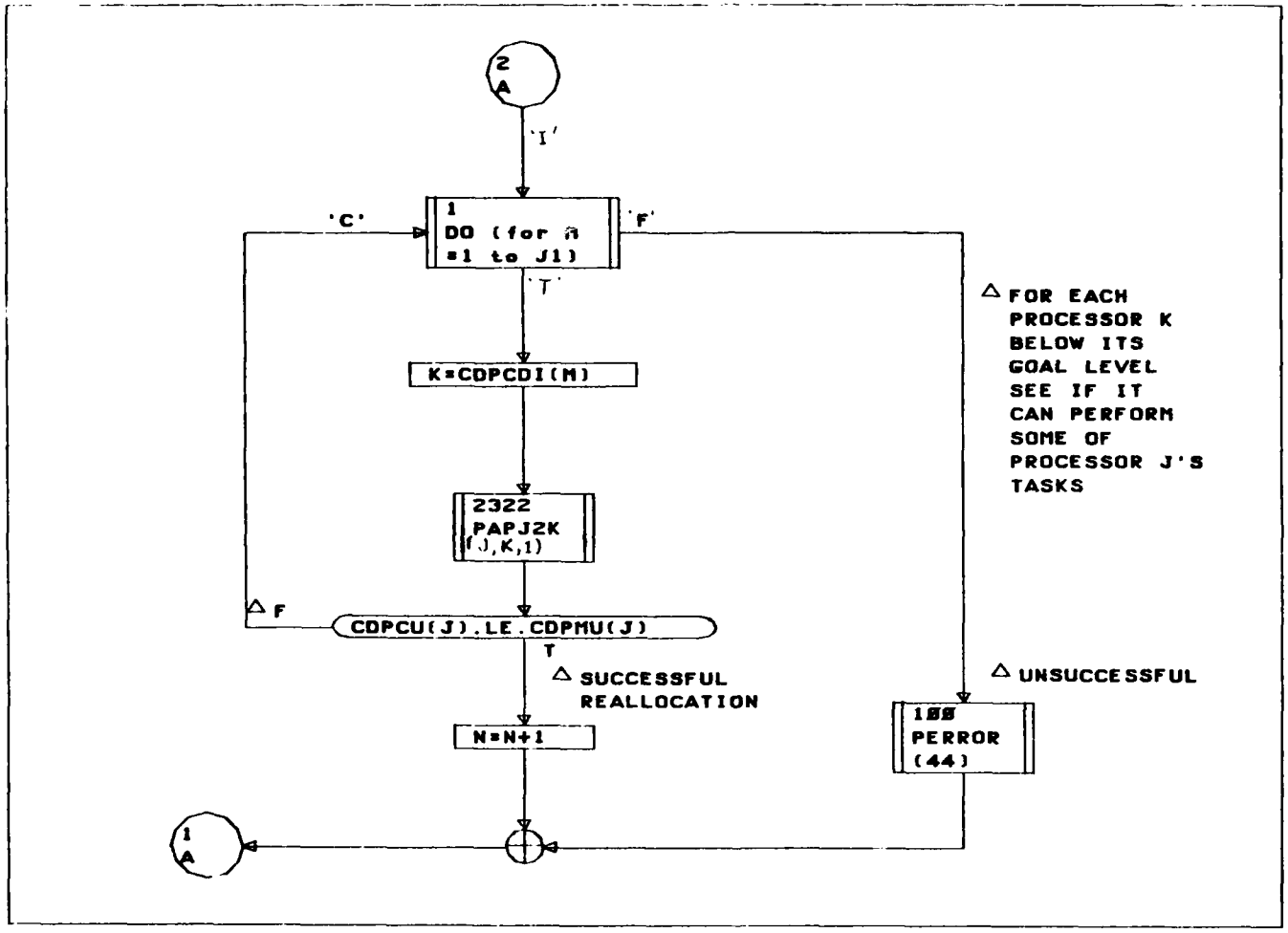
DEALS



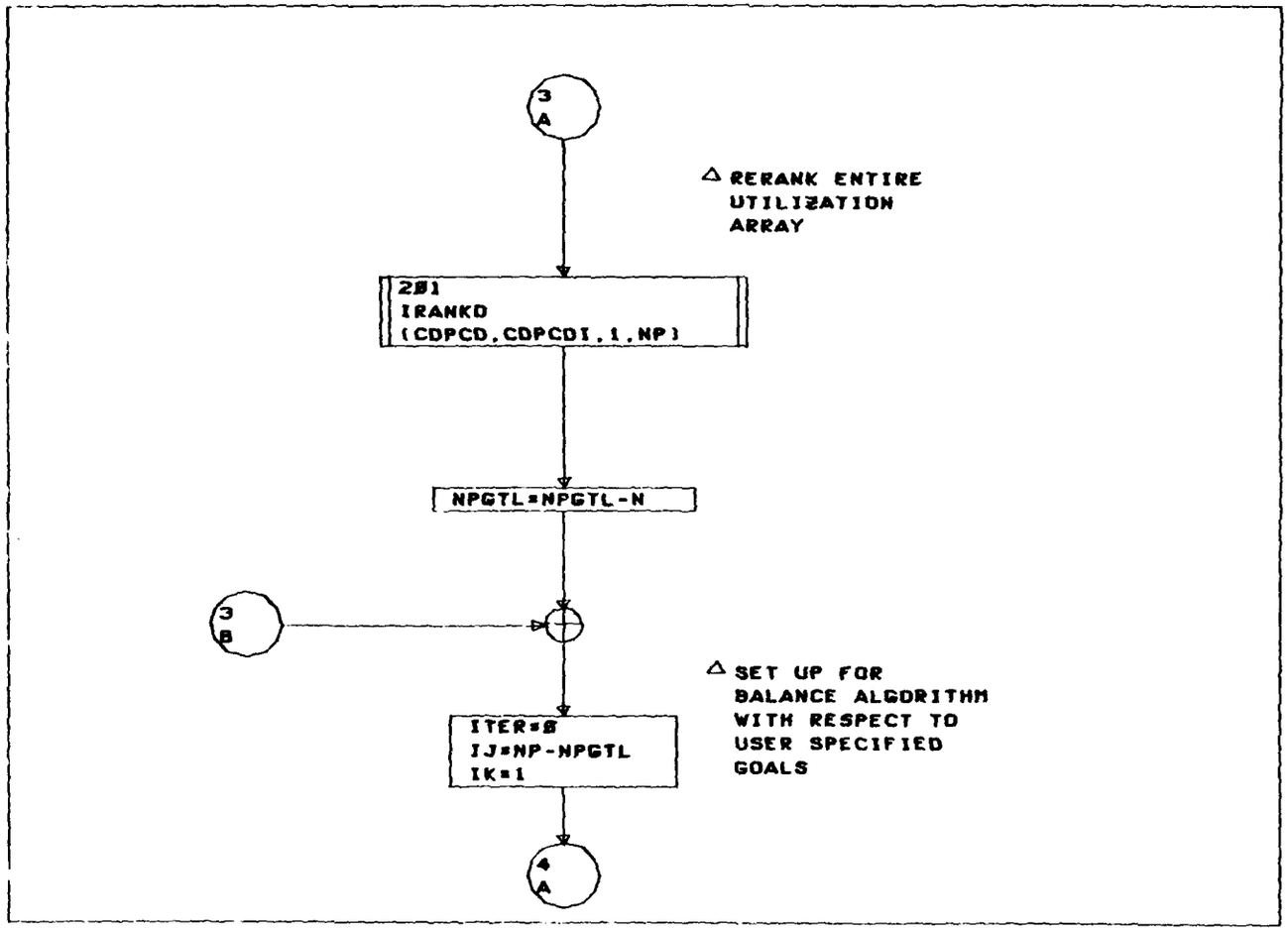
ISSUE DATE 28-NOV-79 ID DEALS SEC PPD-2318 PAGE 1


2320
LOADBL
ENTRY
IPGTL=1
F
T
3
B
△ SOME PROCESSORS
ARE ABOVE LIMIT
N=0
'I'
△ PROCESS EACH PROCESSOR
J ABOVE ABSOLUTE LIMIT
1
DO (for L
=1 to NPLTL)
'F'
3
A
△ RERANK
PROCESSORS
WHICH ARE
LESS THAN
OR EQUAL GOAL
'T'
J=CDPCDI(NP-L+1)
J1=NP-NPGTG+1
2321
PACTSK
(J,IJT,IJLIST)
IJT.LE.0
F
T
2
A
100
PERROR
(43)
△ FIXED
ALLOCATION
HAS OVERLOADED
PROCESSOR J
1
A
'C'
201
IRANKD
(CDPCD,CDPCDI,1,J1)
J1=NP-NPGTG+1

DEALS

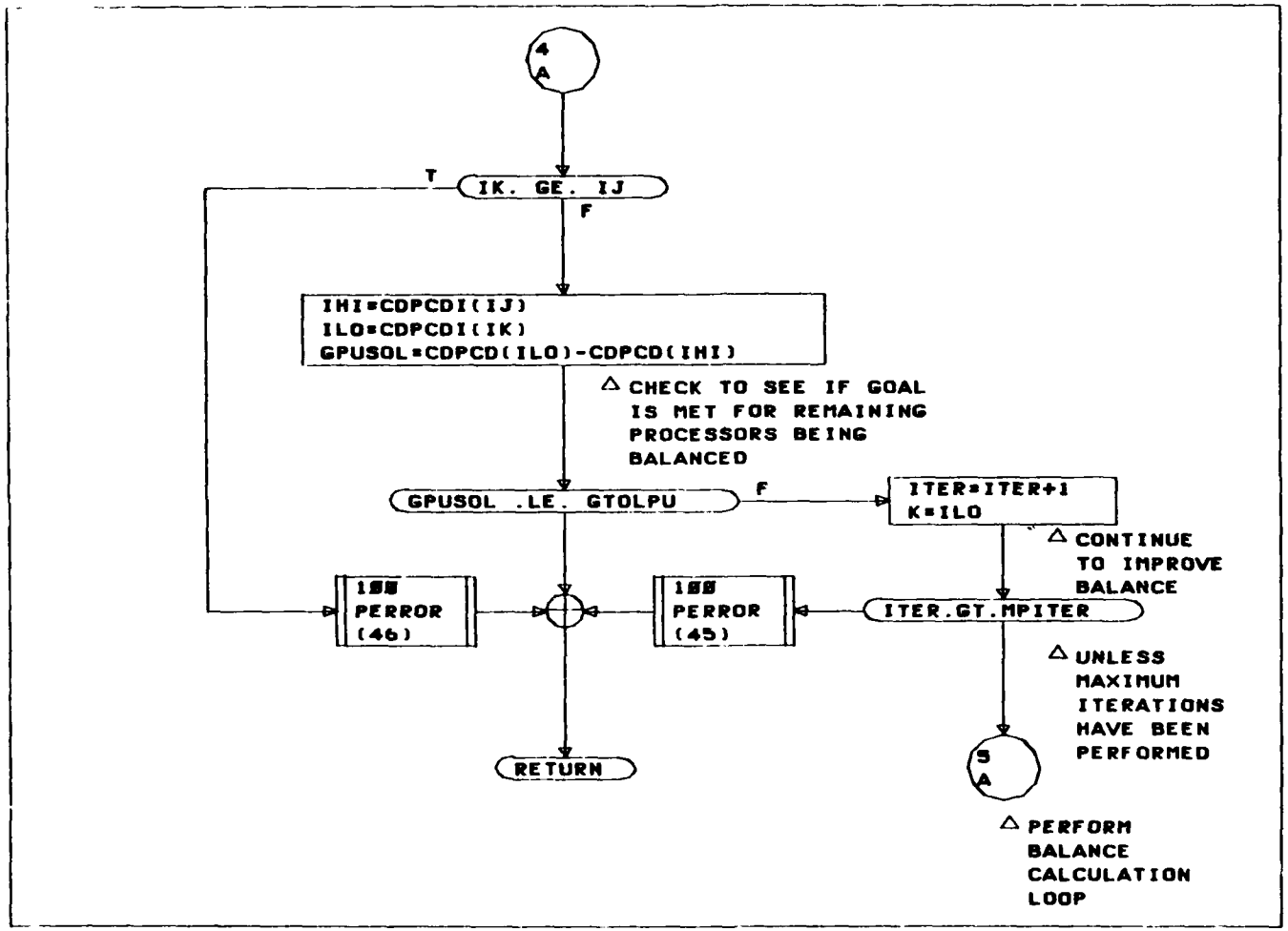

2
A
'I'
1
DO (for n
=1 to J1)
'C'
'F'
'T'
K=CDPCDI(M)
2322
PAPJ2K
(J,K,1)
F
CDPCU(J).LE.CDPMU(J)
T
SUCCESSFUL
REALLOCATION
N=N+1
1
A
FOR EACH
PROCESSOR K
BELOW ITS
GOAL LEVEL
SEE IF IT
CAN PERFORM
SOME OF
PROCESSOR J'S
TASKS
UNSUCCESSFUL
100
PERROR
(44)

DEALS

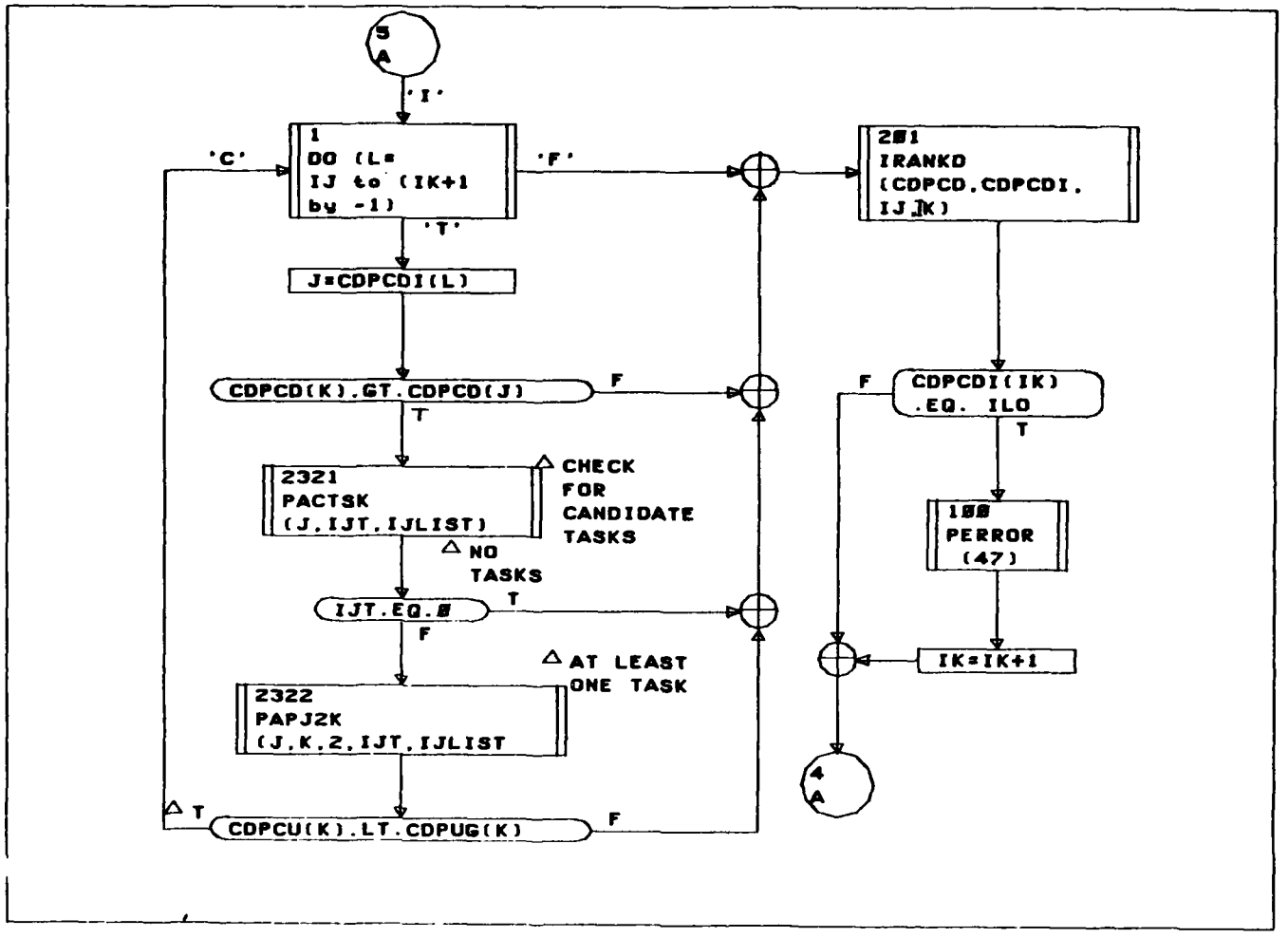


ISSUE DATE 19-NOV-79 ID DEALS SEC PPD-232Ø PAGE 3

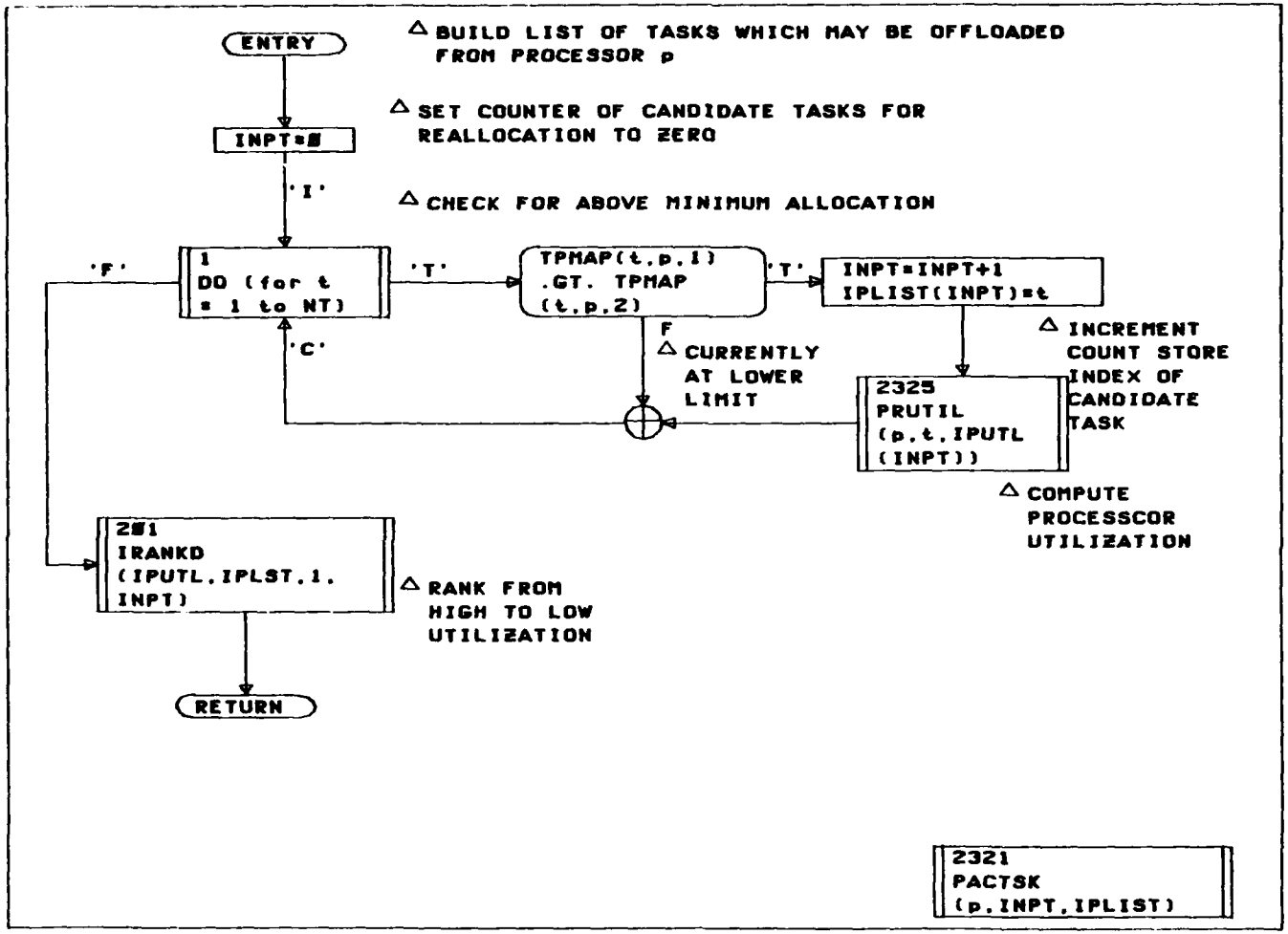
DEALS


4
A
IK. GE. IJ
T
F
IHI=CDPCDI(IJ)
ILO=CDPCDI(IK)
GPUSOL=CDPCD(ILO)-CDPCD(IHI)
△ CHECK TO SEE IF GOAL IS MET FOR REMAINING PROCESSORS BEING BALANCED
GPUSOL .LE. GTOLPU
F
ITER=ITER+1
K=ILO
△ CONTINUE TO IMPROVE BALANCE
100 PERROR (46)
100 PERROR (45)
ITER.GT.MPITER
△ UNLESS MAXIMUM ITERATIONS HAVE BEEN PERFORMED
RETURN
5
A
△ PERFORM BALANCE CALCULATION LOOP

DEALS

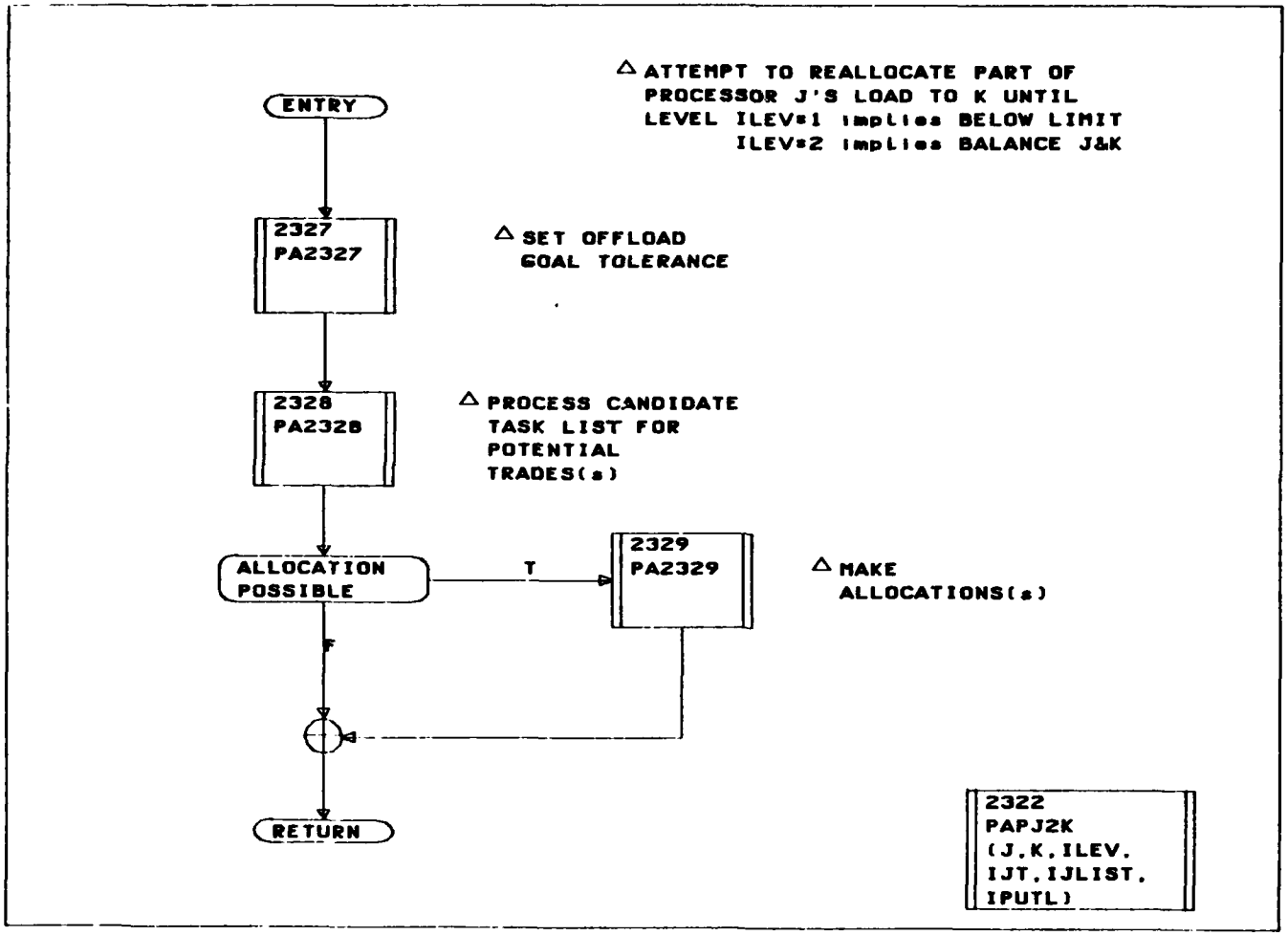

5
A
'I'
1
DO (L=
IJ to (IK+1
by -1)
'C'
'F'
'T'
J=CDPCDI(L)
CDPCD(K).GT.CDPCD(J)
F
T
2321
PACTSK
(J,IJT,IJLIST)
CHECK
FOR
CANDIDATE
TASKS
NO
TASKS
IJT.EQ.0
T
F
AT LEAST
ONE TASK
2322
PAPJ2K
(J,K,2,IJT,IJLIST
T
CDPCU(K).LT.CDPUG(K)
F
201
IRANKD
(CDPCD,CDPCDI,
IJ,IK)
F
CDPCDI(IK)
.EQ. ILO
T
100
PERROR
(47)
IK=IK+1
4
A

DEALS



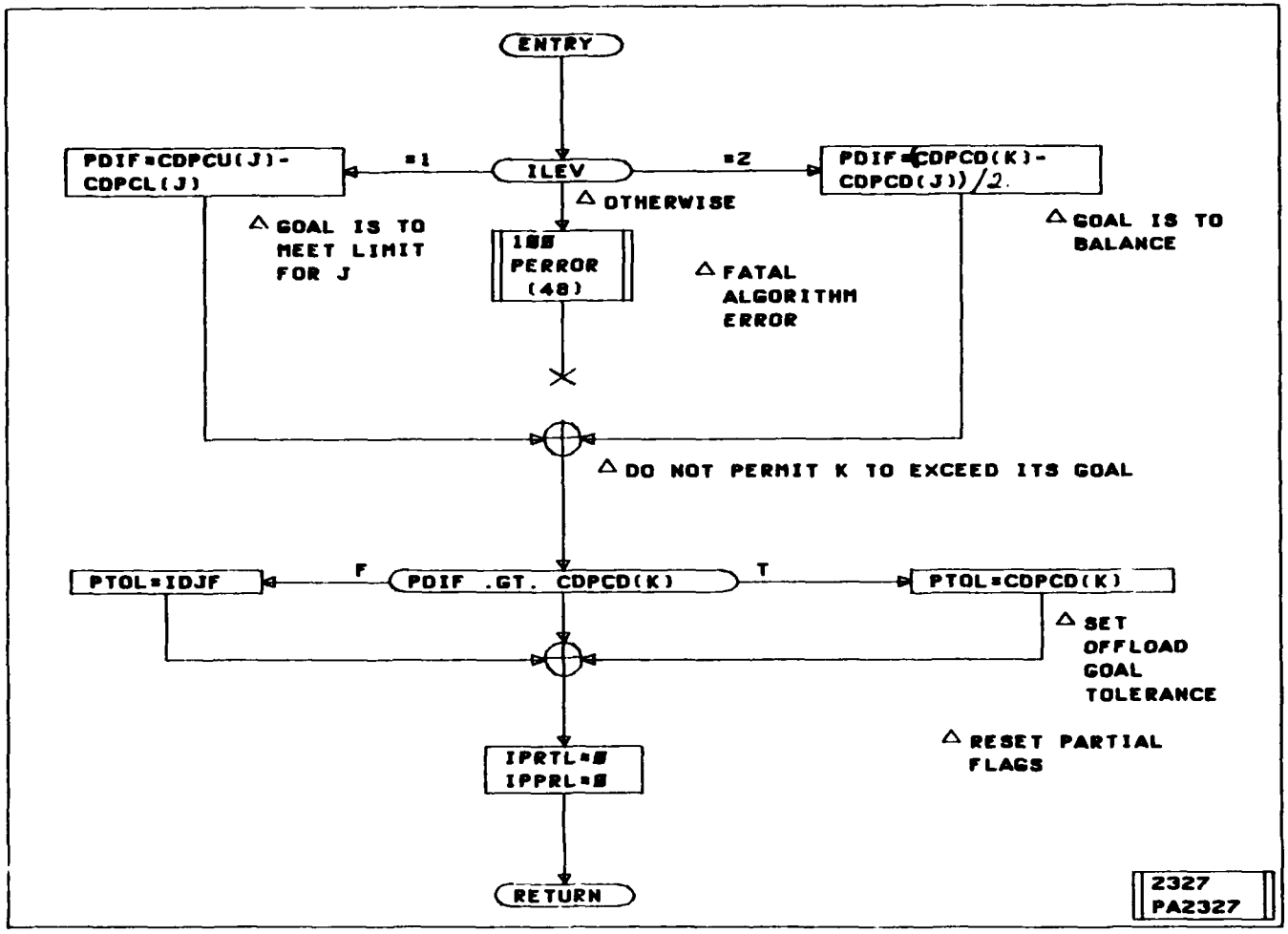
ISSUE DATE 20-NOV-79 ID DEALS SEC PPD-2321 PAGE 1

DEALS



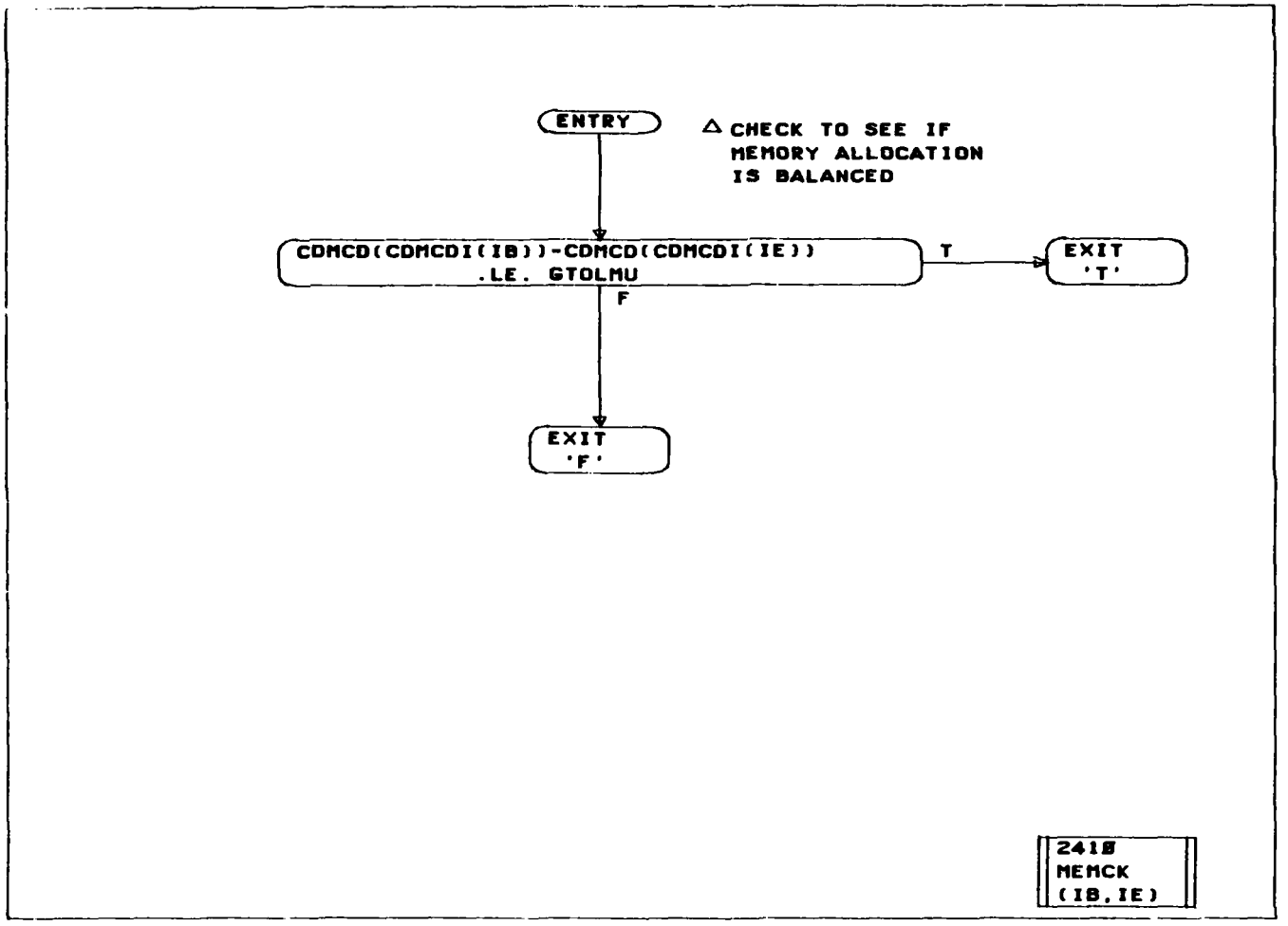
ISSUE DATE 28-NOV-79 ID DEALS SEC PPD-2322 PAGE 1

DEALS

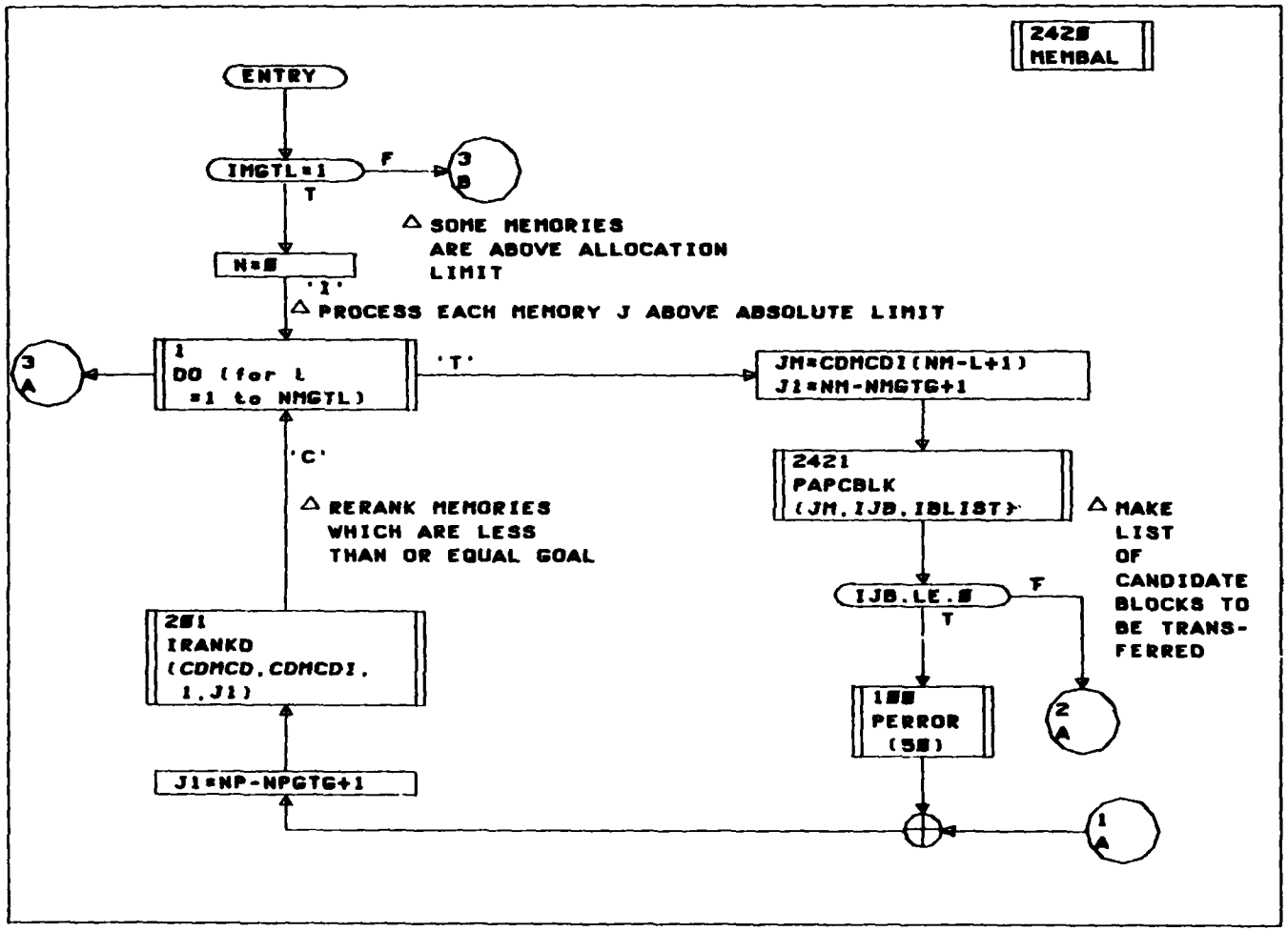


ISSUE DATE 20-NOV-79 ID DEALS SEC PPD-2327 PAGE 1

DEALS

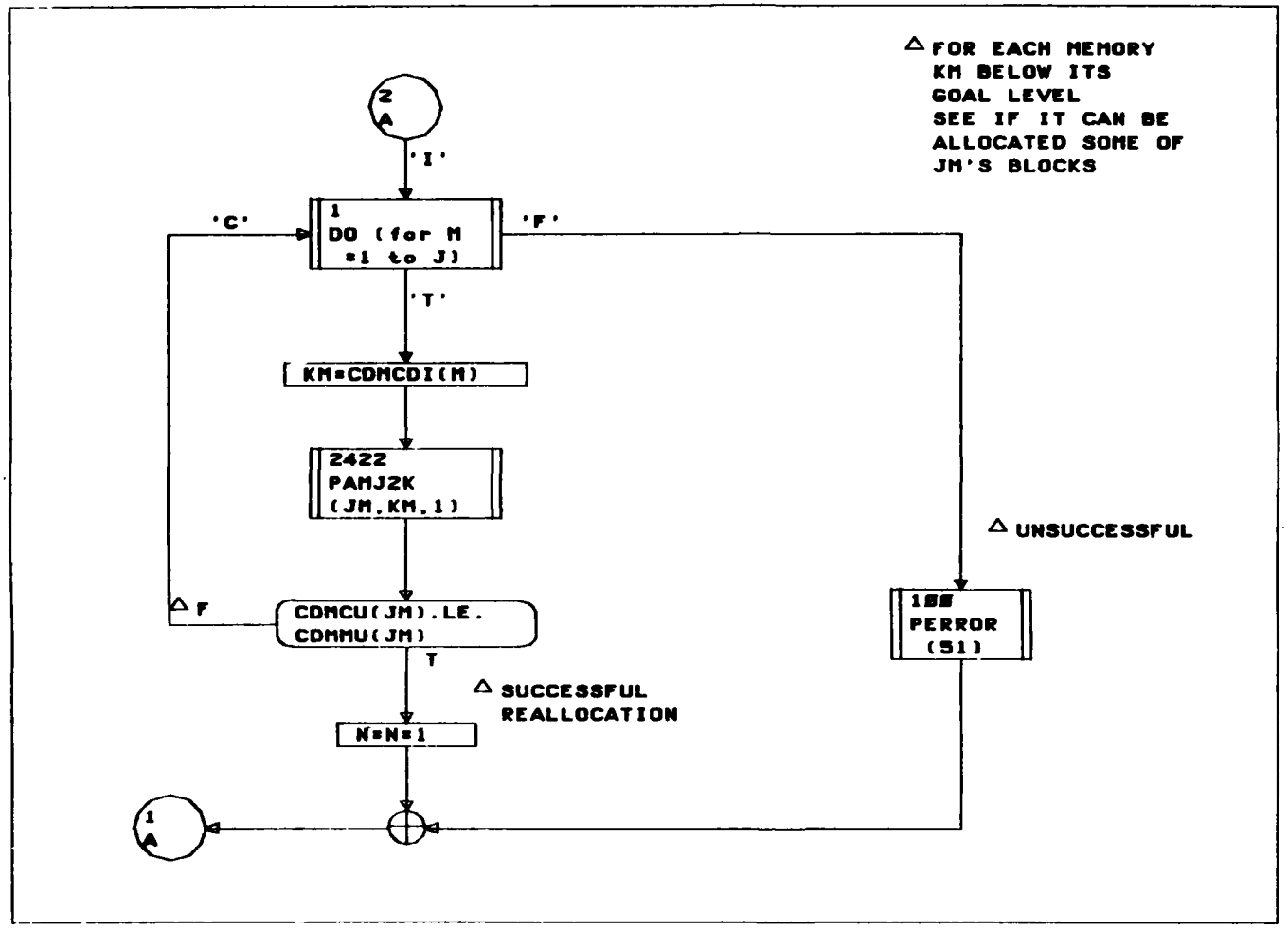

ENTRY
△ CHECK TO SEE IF MEMORY ALLOCATION IS BALANCED
CDMCD(CDMCDI(IB))-CDMCD(CDMCDI(IE)) .LE. GTOLMU
T
EXIT 'T'
F
EXIT 'F'
2410 MEMCK (IB,IE)

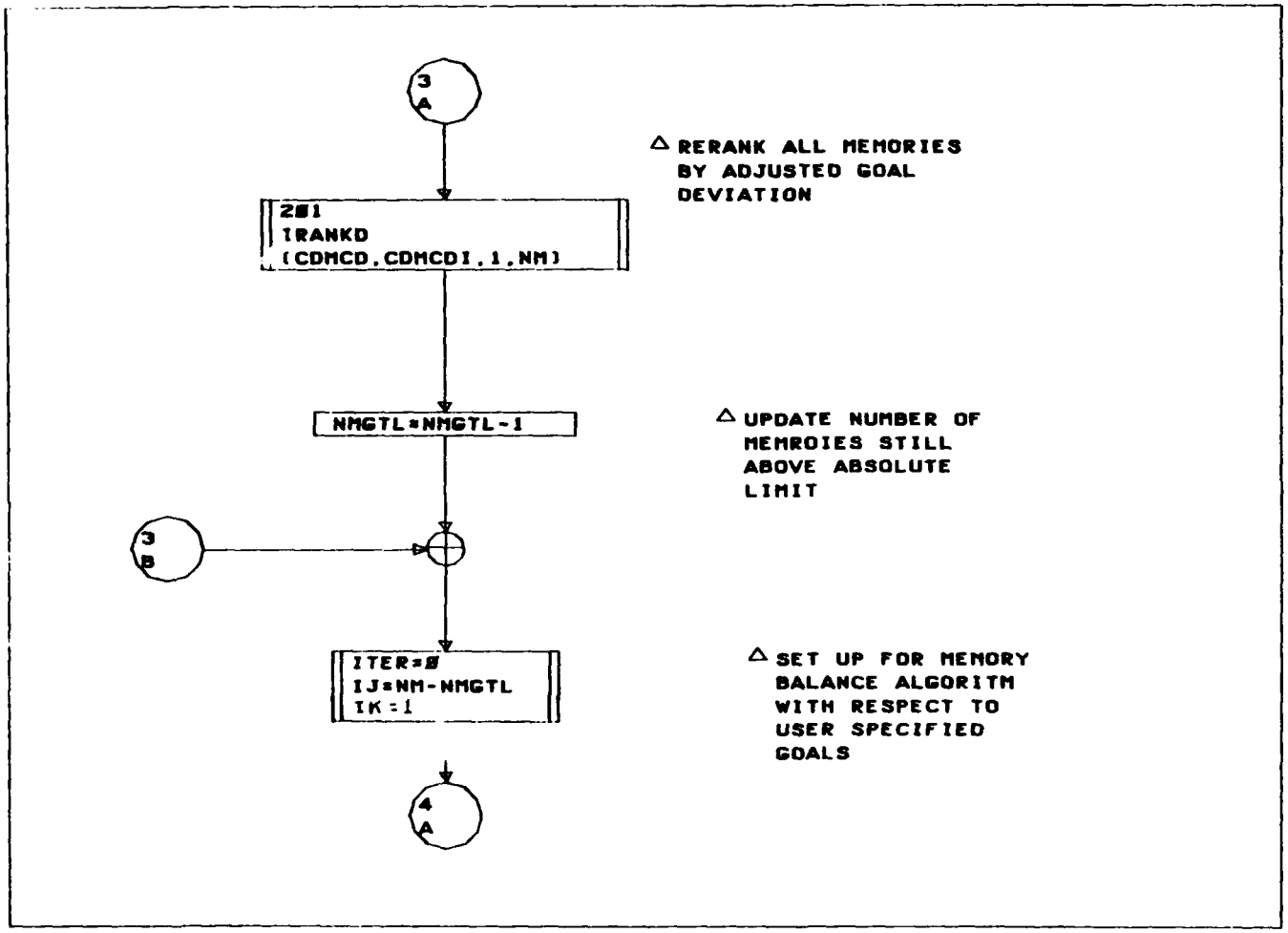
DEALS



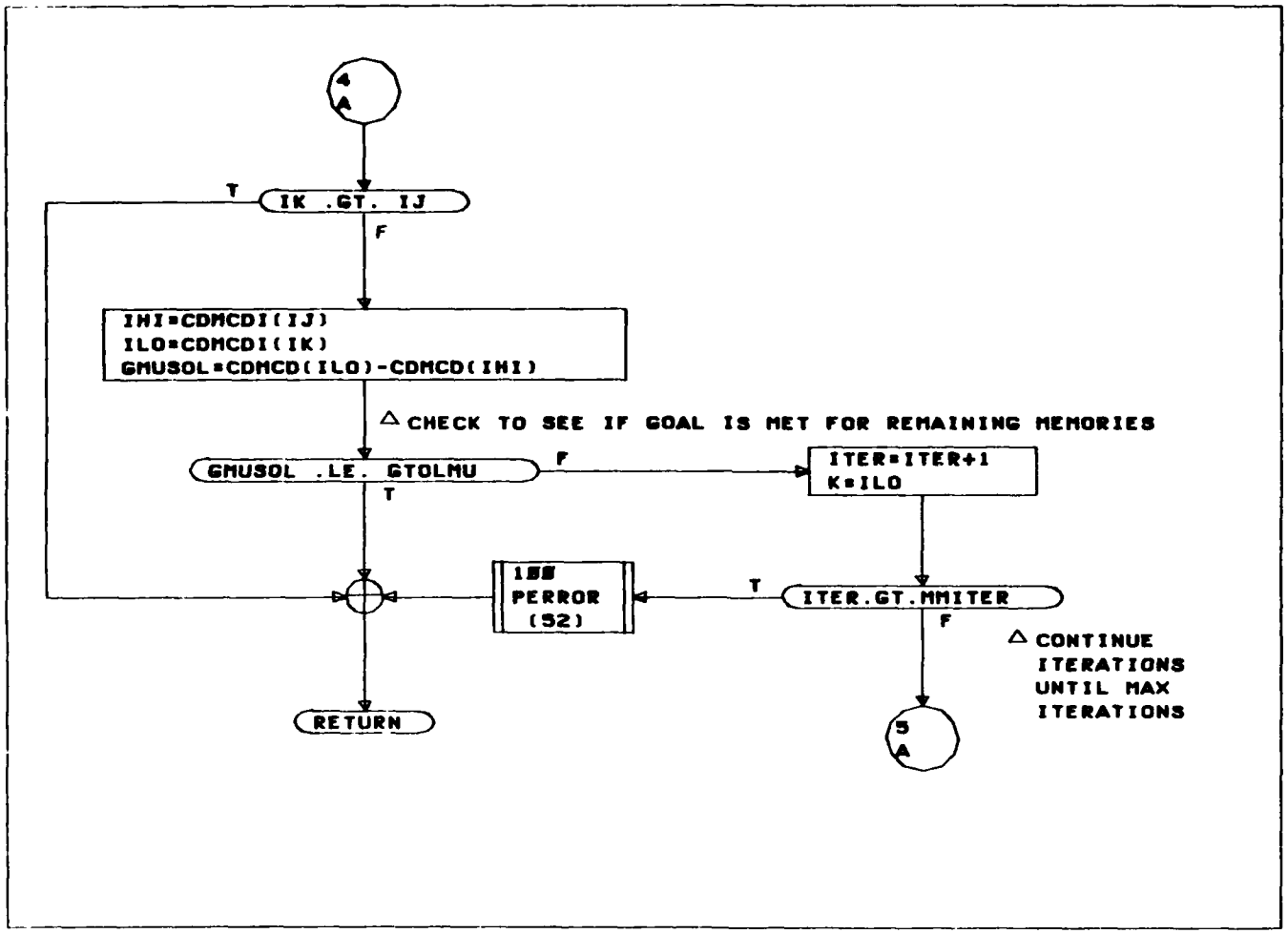
ISSUE DATE 26-NOV-79 ID DEALS SEC PPD-2420 PAGE 1

DEALS

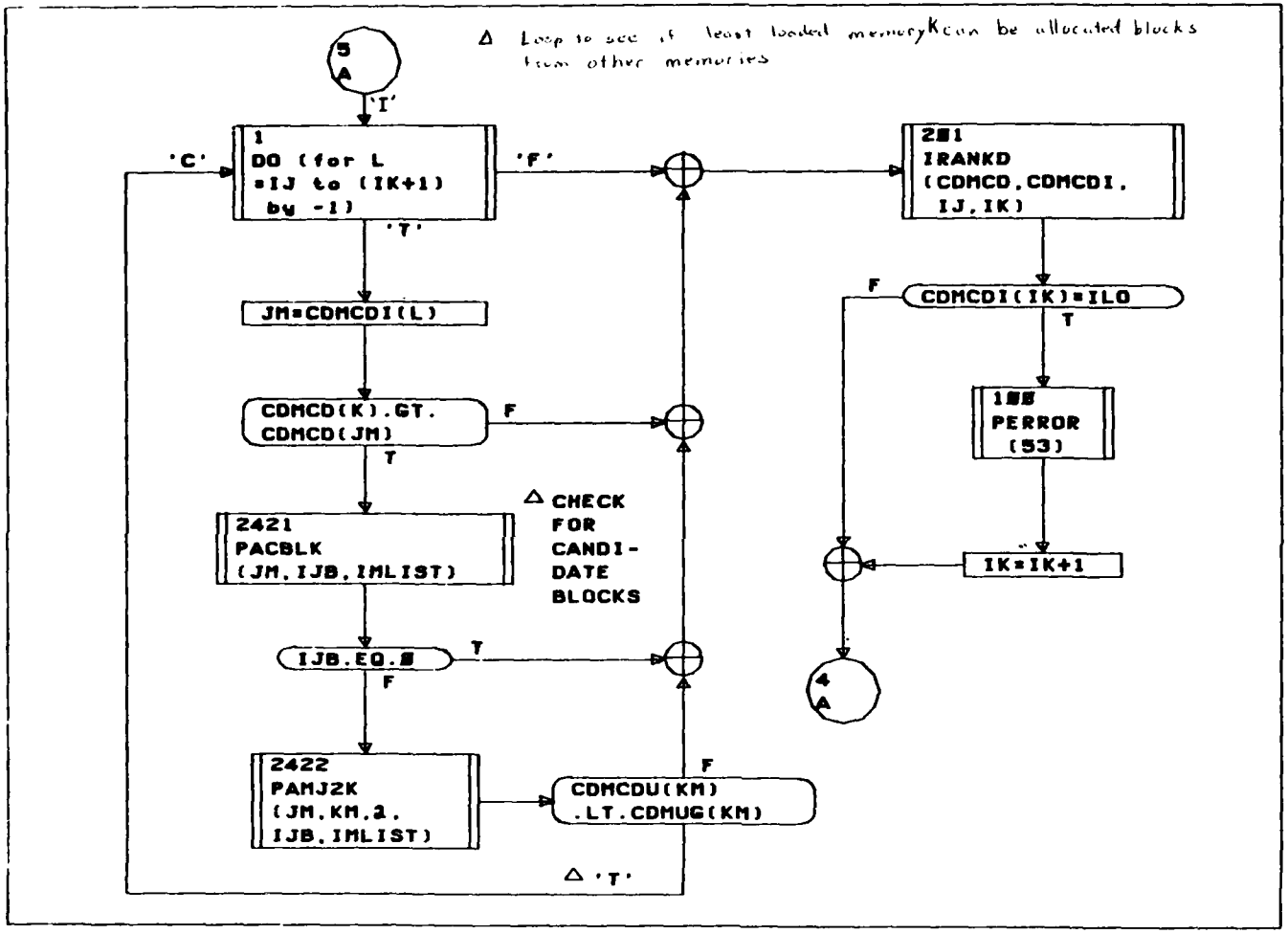

△ FOR EACH MEMORY KM BELOW ITS GOAL LEVEL SEE IF IT CAN BE ALLOCATED SOME OF JM'S BLOCKS
2
'I'
1
DO (for M =1 to J)
'C'
'F'
'T'
KM=CDMCDI(M)
2422
PAMJ2K
(JM,KM,1)
△ UNSUCCESSFUL
△ F
CDMCU(JM).LE.
CDMMU(JM)
T
100
PERROR
(51)
△ SUCCESSFUL REALLOCATION
N=N+1
1


3
A
2#1
IRANKD
(CDMCD,CDMCDI,1,NM)
△ RERANK ALL MEMORIES BY ADJUSTED GOAL DEVIATION
NMGTL=NMGTL-1
△ UPDATE NUMBER OF MEMROIES STILL ABOVE ABSOLUTE LIMIT
3
B
ITER=#
IJ=NM-NMGTL
IK=1
△ SET UP FOR MEMORY BALANCE ALGORITM WITH RESPECT TO USER SPECIFIED GOALS
4
A

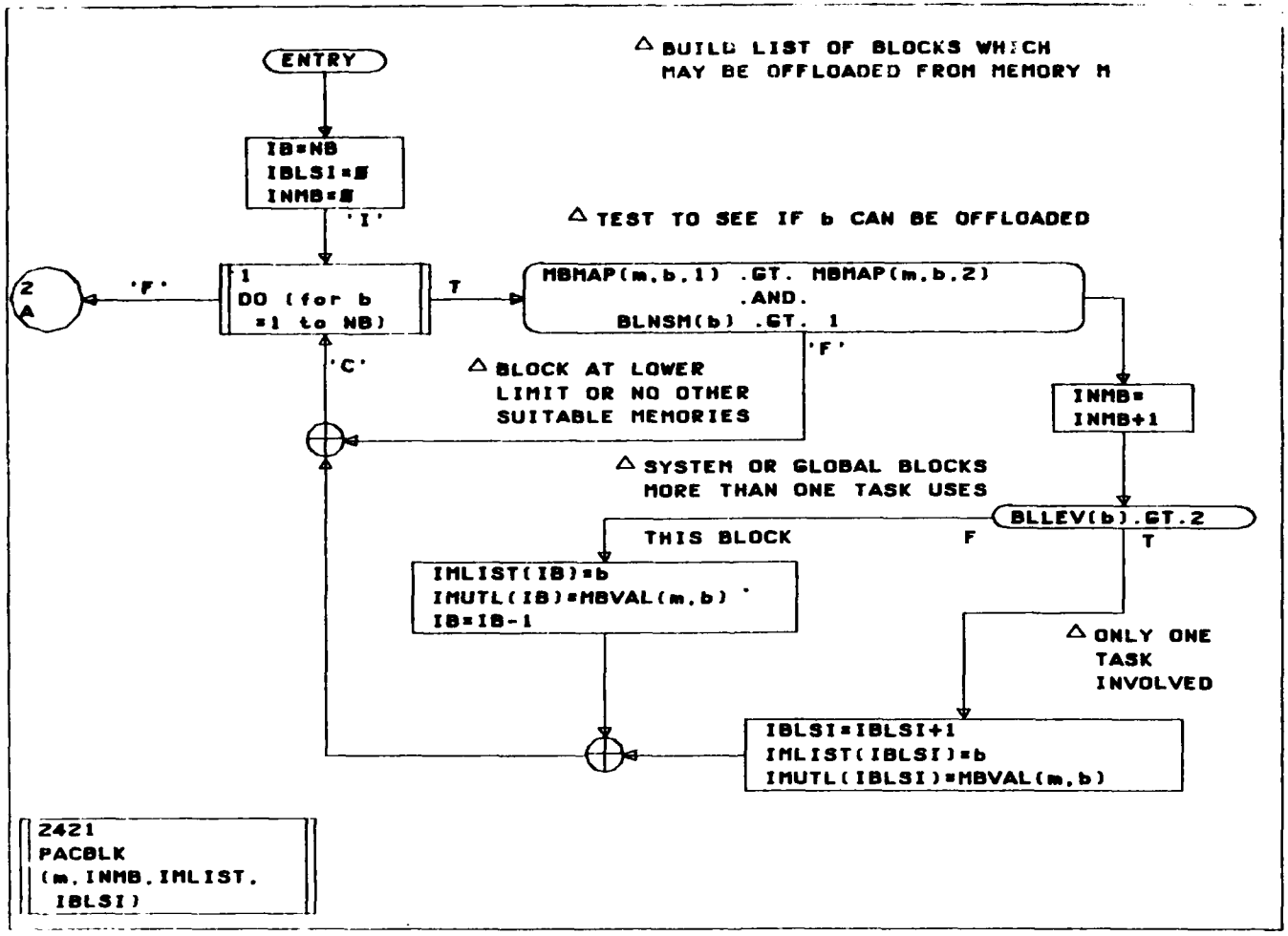
DEALS

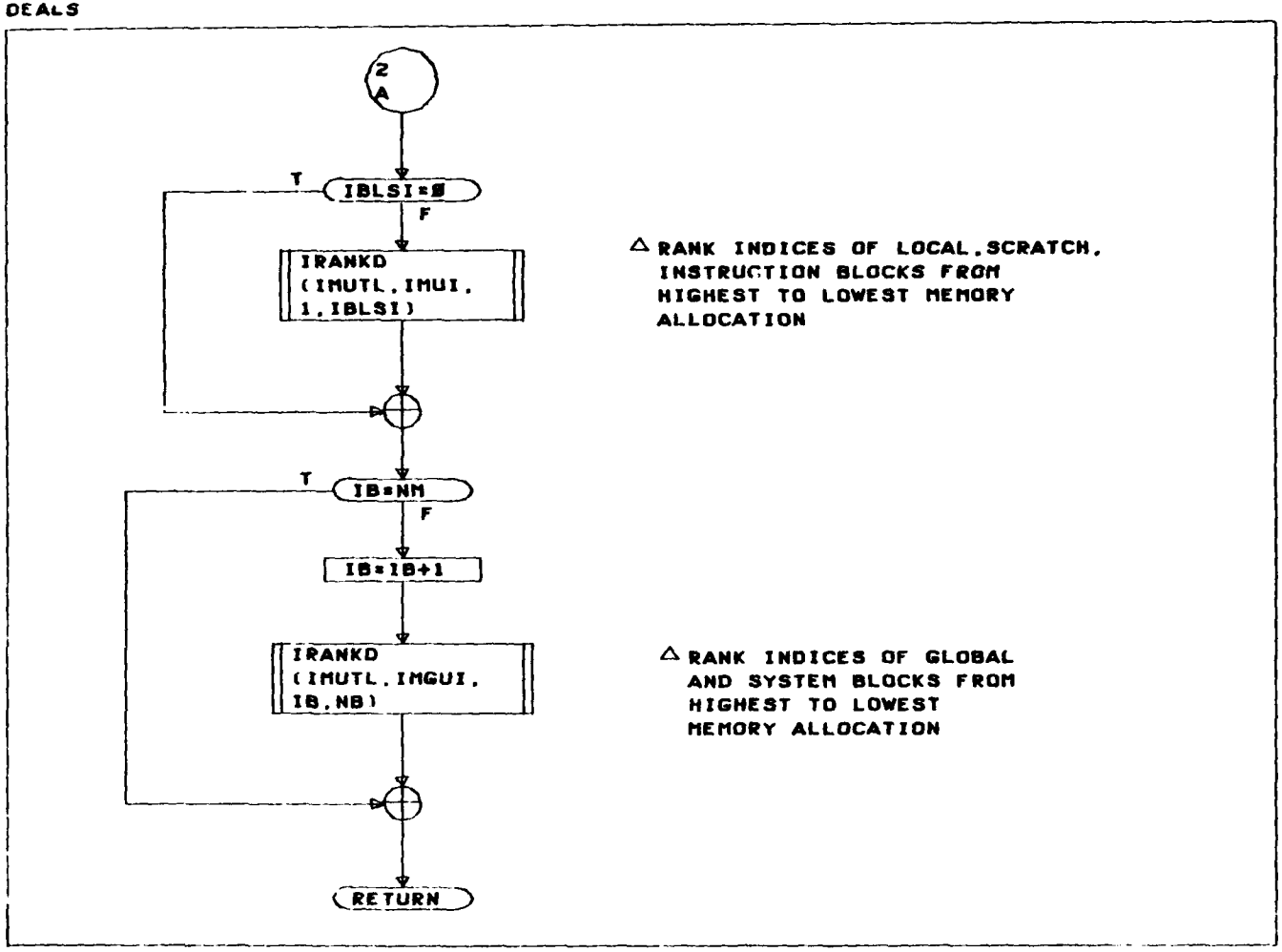

4
A
IK .GT. IJ
T
F
IHI=CDMCDI(IJ)
ILO=CDMCDI(IK)
GMUSOL=CDMCD(ILO)-CDMCD(IHI)
△ CHECK TO SEE IF GOAL IS MET FOR REMAINING MEMORIES
GMUSOL .LE. GTOLMU
F
T
ITER=ITER+1
K=ILO
100
PERROR
(52)
T
ITER.GT.MMITER
F
△ CONTINUE
ITERATIONS
UNTIL MAX
ITERATIONS
RETURN
5
A

DEALS


Δ Loop to see if least loaded memory K can be allocated blocks from other memories
5 A
'I'
1
DO (for L =IJ to (IK+1) by -1)
'C'
'F'
'T'
JM=CDMCDI(L)
CDMCD(K).GT. CDMCD(JM)
F
T
2421
PACBLK
(JM,IJB,IMLIST)
Δ CHECK FOR CANDI-DATE BLOCKS
IJB.EQ.0
T
F
2422
PAMJ2K
(JM,KM,2, IJB,IMLIST)
CDMCDU(KM) .LT.CDMUG(KM)
F
Δ 'T'
201
IRANKD
(CDMCD,CDMCDI, IJ,IK)
CDMCDI(IK)=ILO
F
T
100
PERROR
(53)
IK=IK+1
4 A

DEALS

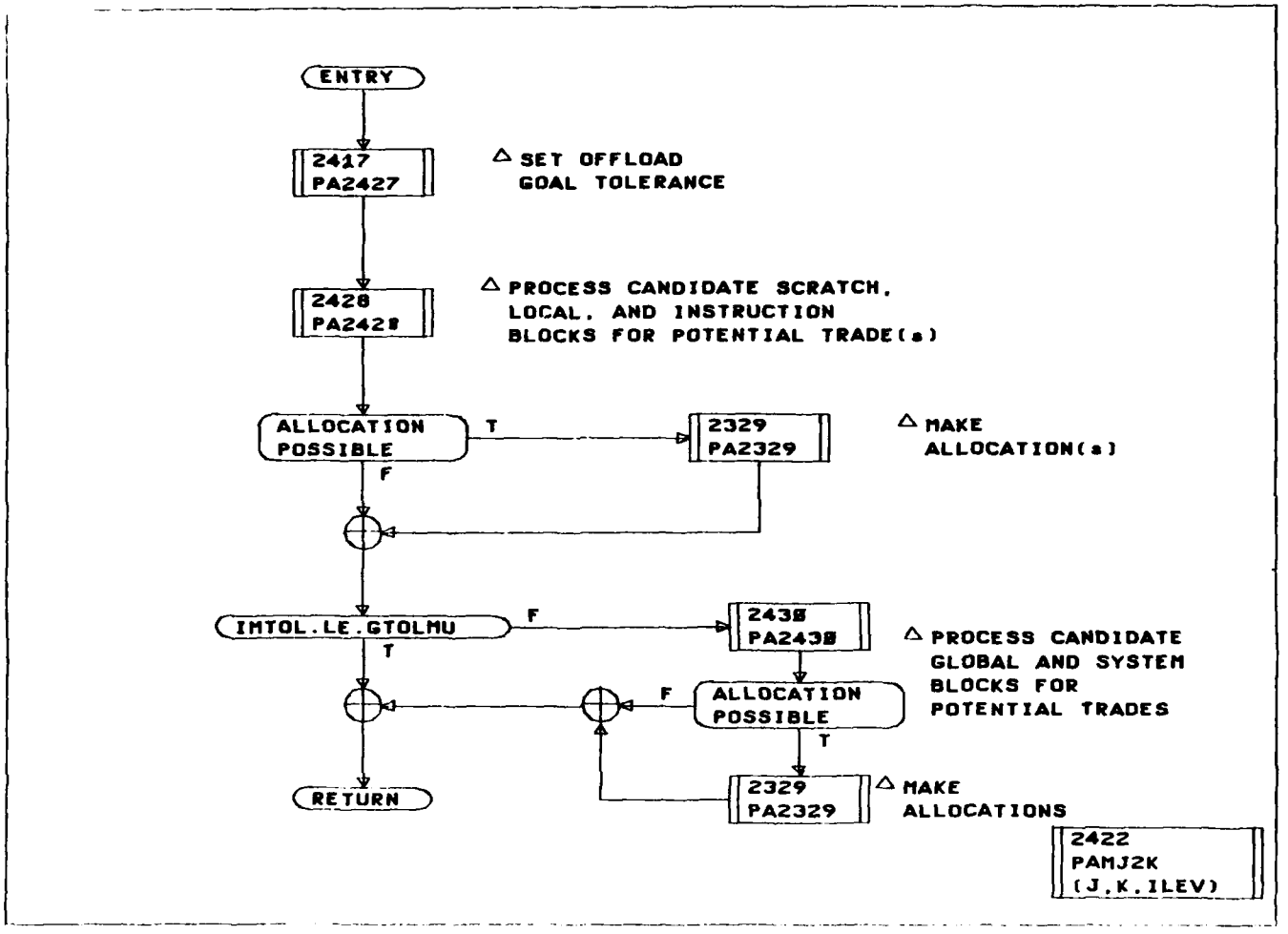

ENTRY
IB=NB
IBLSI=0
INMB=0
'I'
△ BUILD LIST OF BLOCKS WHICH MAY BE OFFLOADED FROM MEMORY M
△ TEST TO SEE IF b CAN BE OFFLOADED
2 A
'F'
1 DO (for b =1 to NB)
T
MBMAP(m,b,1) .GT. MBMAP(m,b,2) .AND. BLNSM(b) .GT. 1
'F'
'C'
△ BLOCK AT LOWER LIMIT OR NO OTHER SUITABLE MEMORIES
INMB= INMB+1
△ SYSTEM OR GLOBAL BLOCKS MORE THAN ONE TASK USES THIS BLOCK
BLLEV(b).GT.2
F
T
IMLIST(IB)=b
IMUTL(IB)=MBVAL(m,b)
IB=IB-1
△ ONLY ONE TASK INVOLVED
IBLSI=IBLSI+1
IMLIST(IBLSI)=b
IMUTL(IBLSI)=MBVAL(m,b)
2421
PACBLK
(m,INMB,IMLIST, IBLSI)



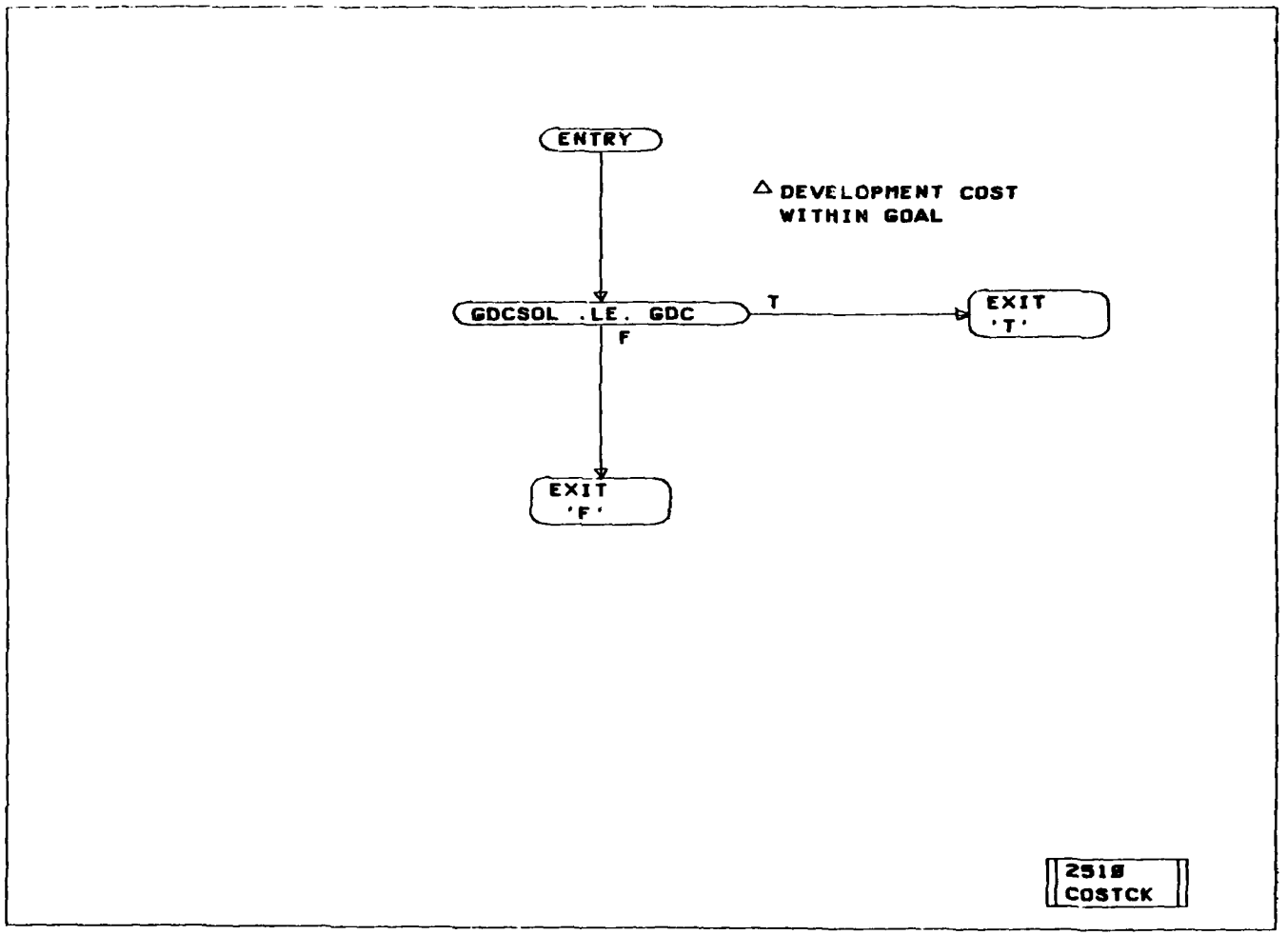
△ RANK INDICES OF LOCAL,SCRATCH, INSTRUCTION BLOCKS FROM HIGHEST TO LOWEST MEMORY ALLOCATION

△ RANK INDICES OF GLOBAL AND SYSTEM BLOCKS FROM HIGHEST TO LOWEST MEMORY ALLOCATION

DEALS


ENTRY
2417
PA2427
△ SET OFFLOAD
GOAL TOLERANCE
2428
PA2428
△ PROCESS CANDIDATE SCRATCH,
LOCAL, AND INSTRUCTION
BLOCKS FOR POTENTIAL TRADE(s)
ALLOCATION
POSSIBLE
T
2329
PA2329
△ MAKE
ALLOCATION(s)
F
IMTOL.LE.GTOLMU
F
2438
PA2438
△ PROCESS CANDIDATE
GLOBAL AND SYSTEM
BLOCKS FOR
POTENTIAL TRADES
T
F
ALLOCATION
POSSIBLE
T
RETURN
2329
PA2329
△ MAKE
ALLOCATIONS
2422
PAMJ2K
(J,K,ILEV)

DEALS



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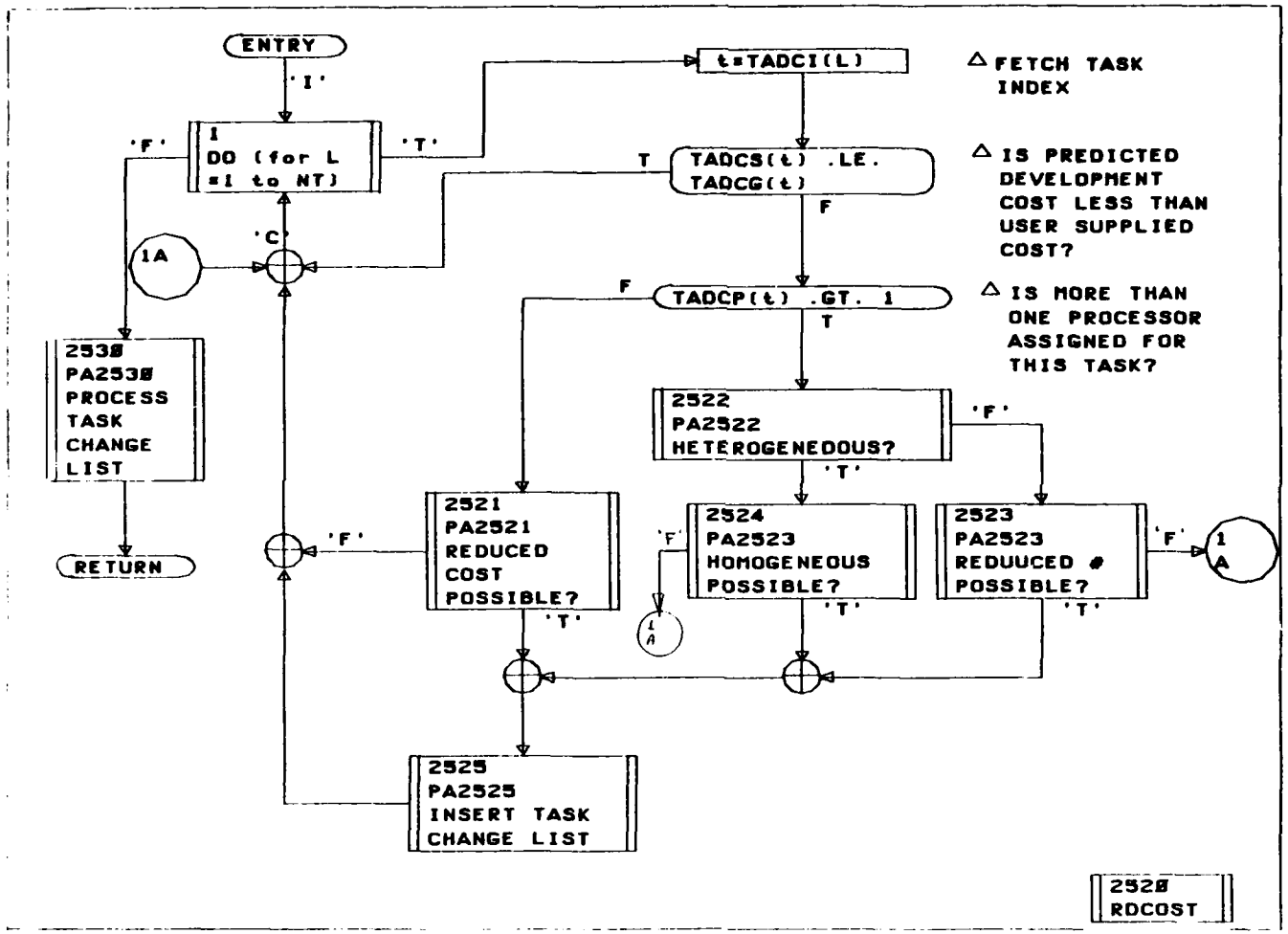
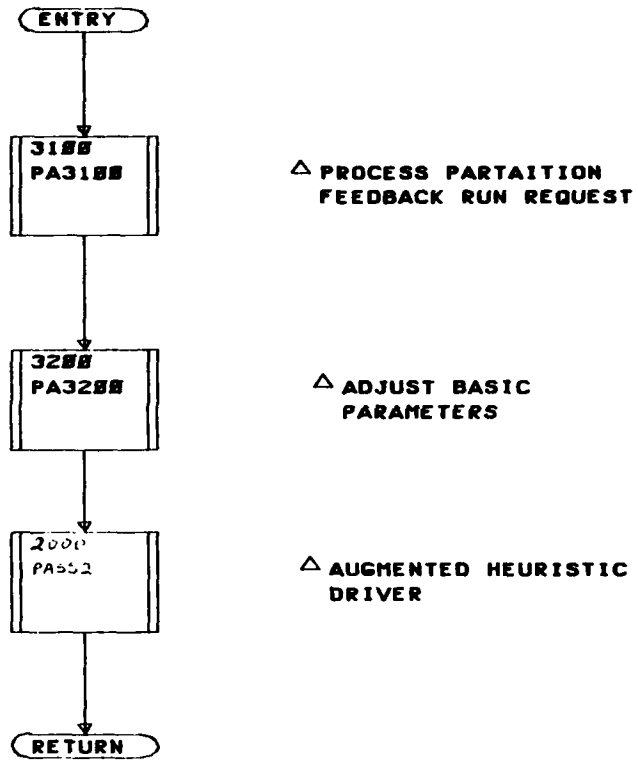
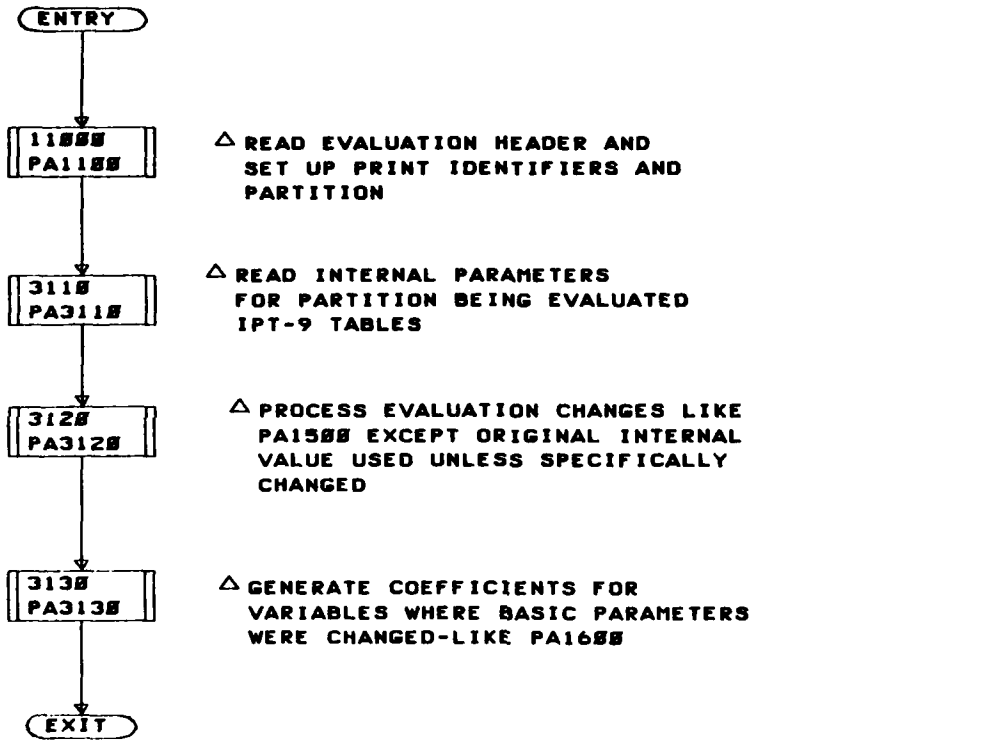

ENTRY
'I'
I
DO (for L
=1 to NT)
'F'
'T'
'C'
1A
2530
PA2530
PROCESS
TASK
CHANGE
LIST
RETURN
t=TADCI(L)
△ FETCH TASK INDEX
TADCS(t) .LE.
TADCG(t)
T
F
△ IS PREDICTED DEVELOPMENT COST LESS THAN USER SUPPLIED COST?
TADCP(t) .GT. 1
F
T
△ IS MORE THAN ONE PROCESSOR ASSIGNED FOR THIS TASK?
2522
PA2522
HETEROGENEDOUS?
'F'
'T'
2521
PA2521
REDUCED
COST
POSSIBLE?
'F'
'T'
2524
PA2523
HOMOGENEOUS
POSSIBLE?
'F'
'T'
2523
PA2523
REDUUCED #
POSSIBLE?
'F'
'T'
1
A
2525
PA2525
INSERT TASK
CHANGE LIST
2520
RDCOST

DEALS



3000
PASS3

DEALS



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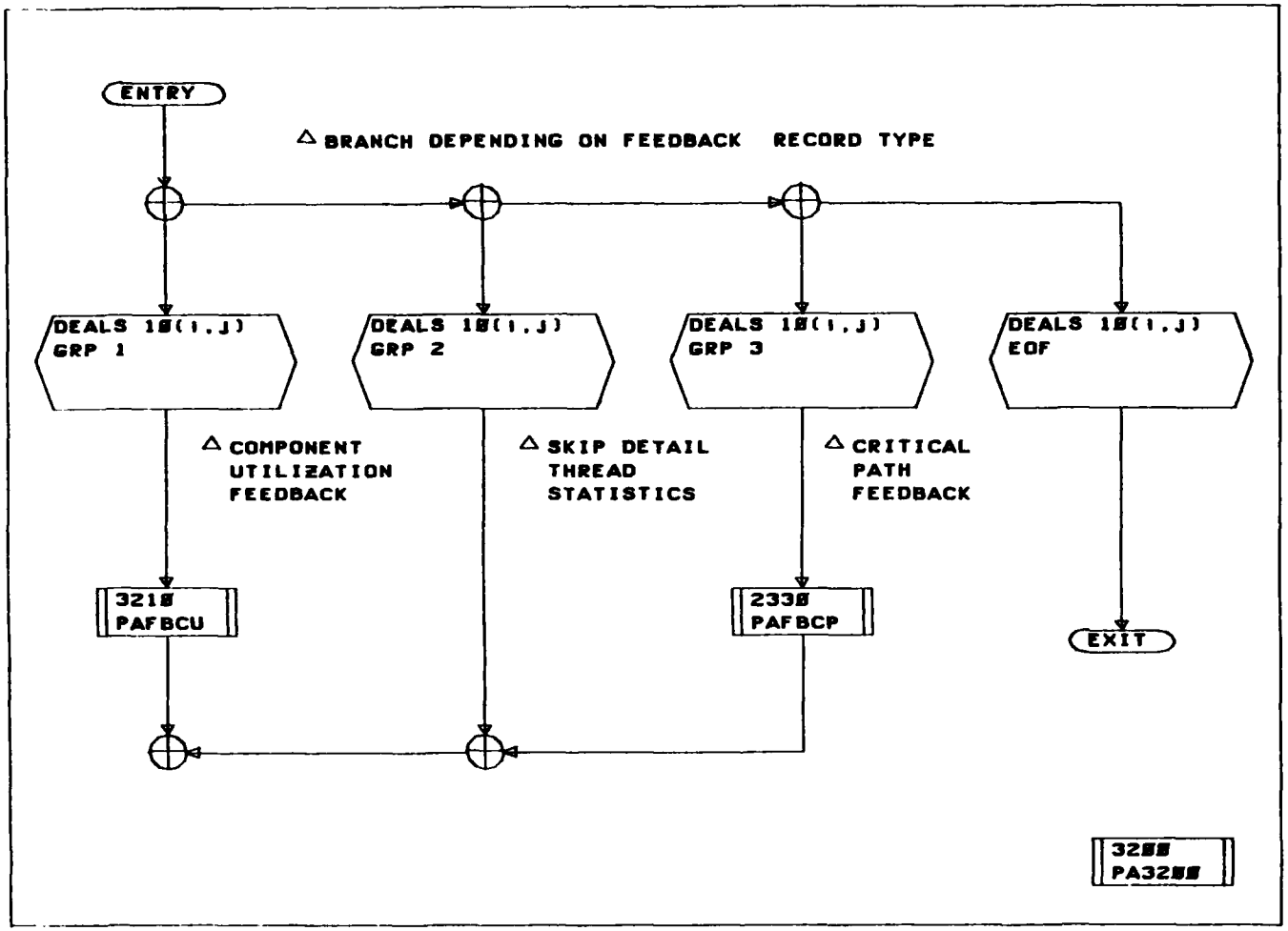
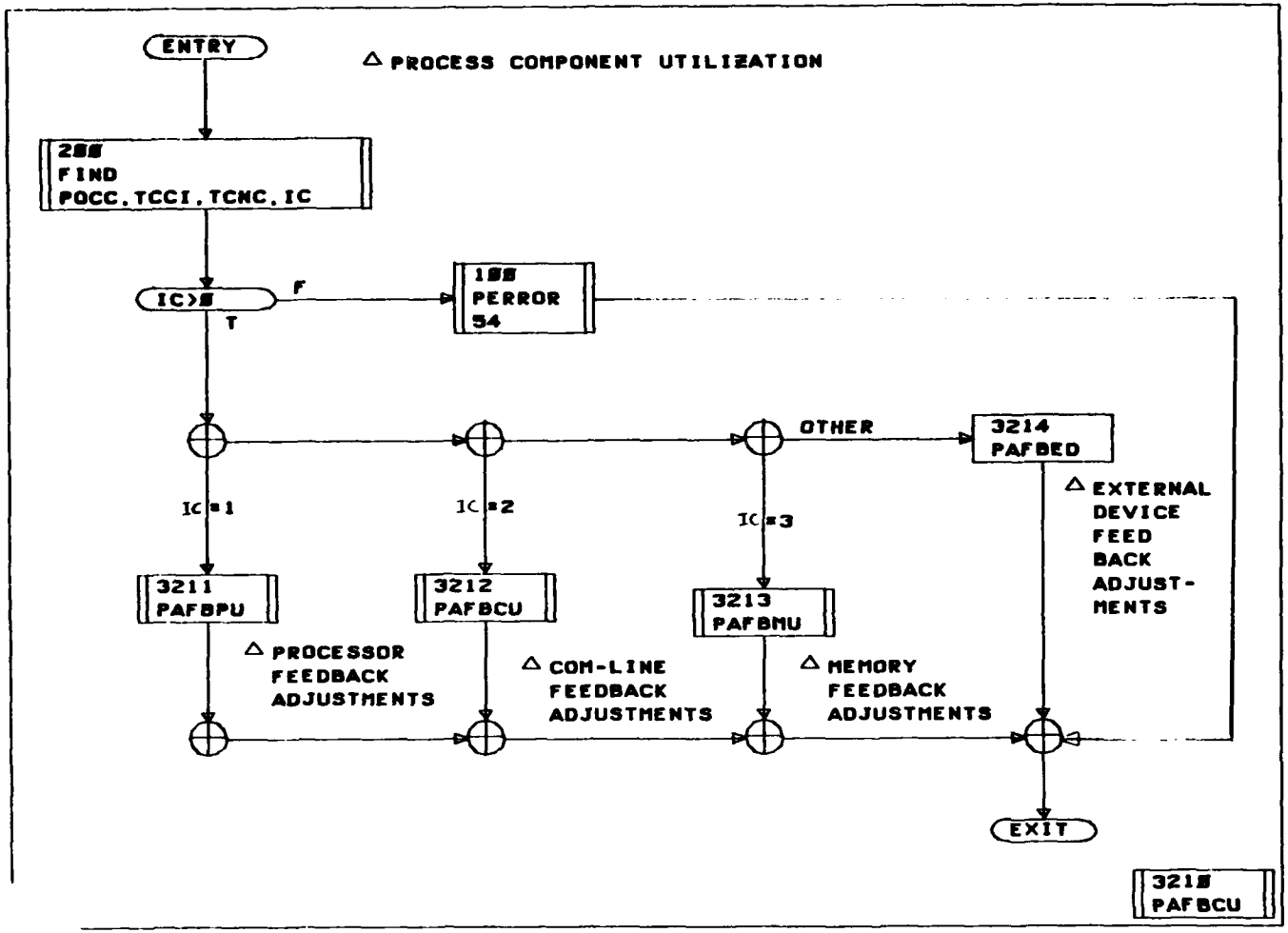
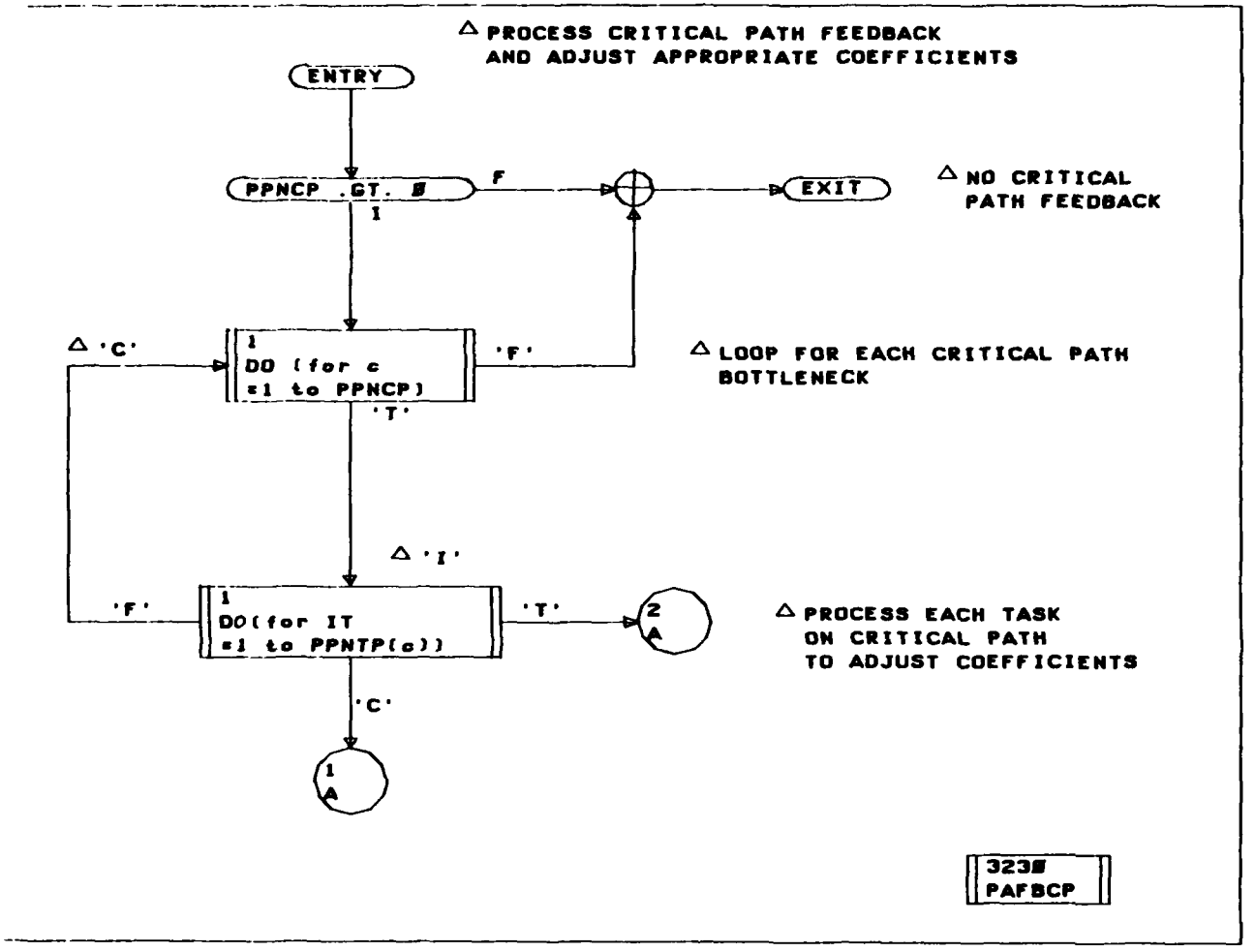
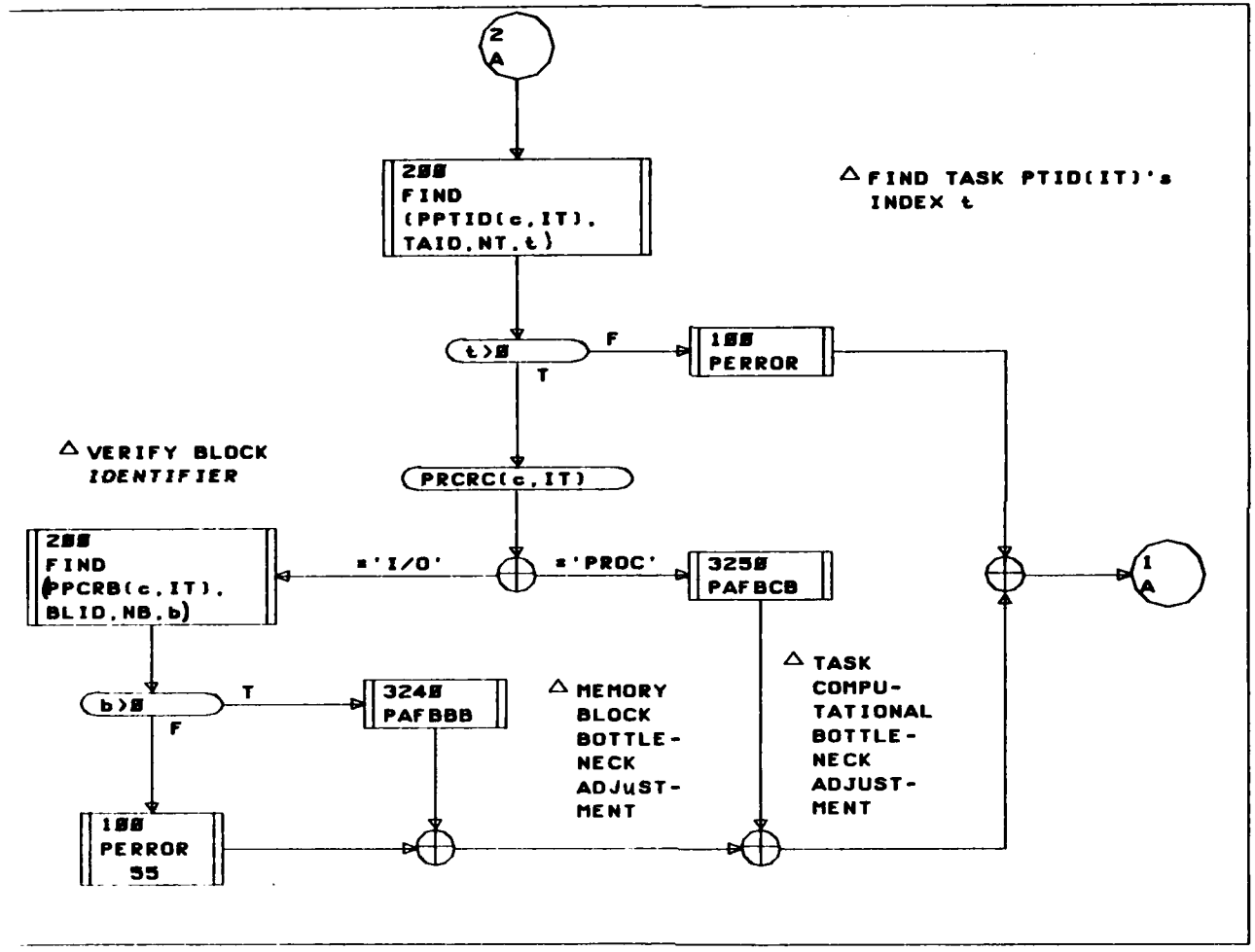
DEALS


ENTRY
△ BRANCH DEPENDING ON FEEDBACK RECORD TYPE
DEALS 1Ø(I,J)
GRP 1
DEALS 1Ø(I,J)
GRP 2
DEALS 1Ø(I,J)
GRP 3
DEALS 1Ø(I,J)
EOF
△ COMPONENT UTILIZATION FEEDBACK
△ SKIP DETAIL THREAD STATISTICS
△ CRITICAL PATH FEEDBACK
321Ø
PAFBCU
233Ø
PAFBCP
EXIT
32ØØ
PA32ØØ

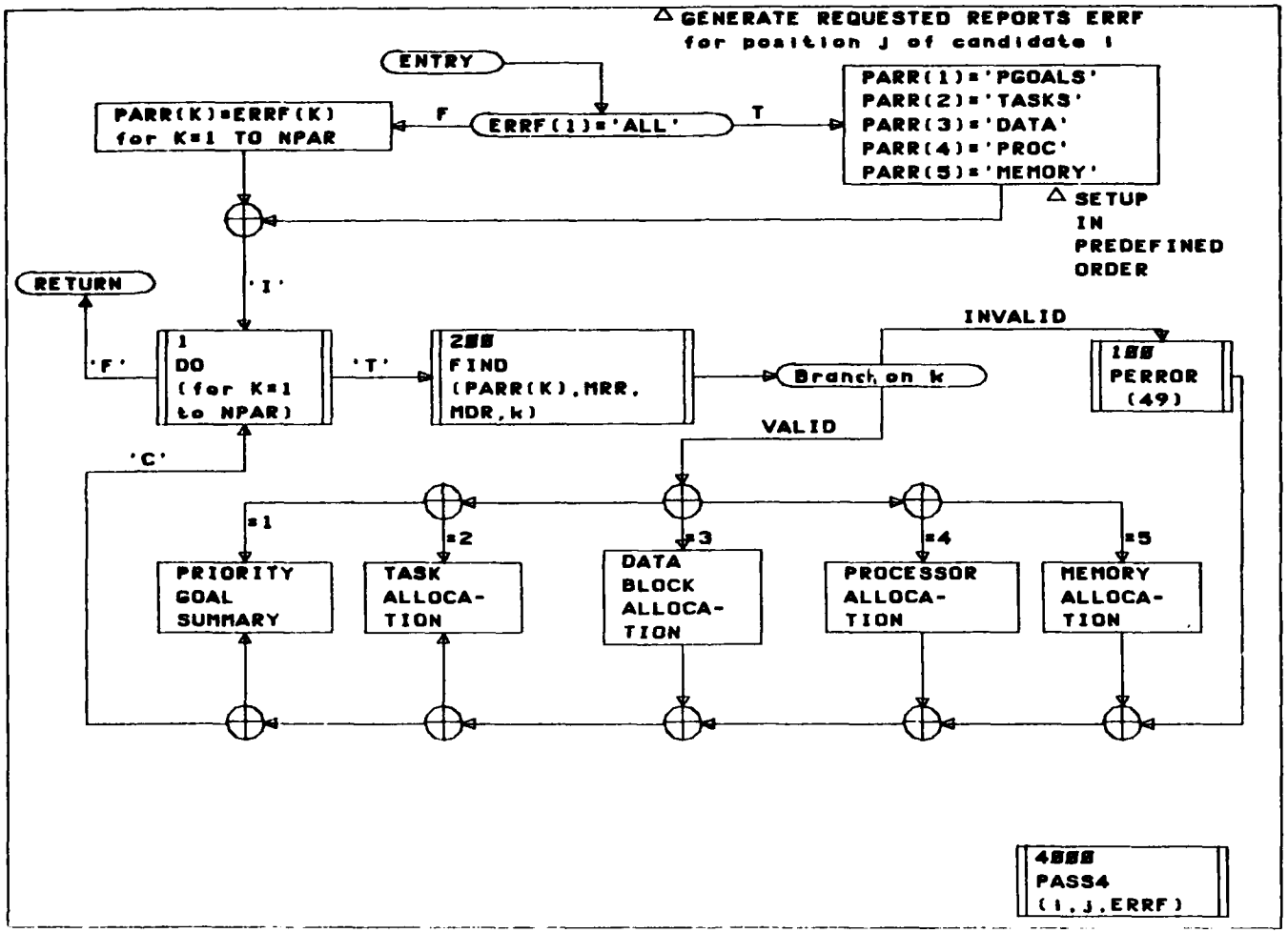
DEALS


ENTRY
△ PROCESS COMPONENT UTILIZATION
200
FIND
POCC,TCCI,TCNC,IC
IC>0
F
T
100
PERROR
54
OTHER
3214
PAFBED
△ EXTERNAL DEVICE FEED BACK ADJUST-MENTS
IC=1
IC=2
IC=3
3211
PAFBPU
3212
PAFBCU
3213
PAFBMU
△ PROCESSOR FEEDBACK ADJUSTMENTS
△ COM-LINE FEEDBACK ADJUSTMENTS
△ MEMORY FEEDBACK ADJUSTMENTS
EXIT
3210
PAFBCU


△ PROCESS CRITICAL PATH FEEDBACK
AND ADJUST APPROPRIATE COEFFICIENTS
ENTRY
PPNCP .GT. 0
F
T
EXIT
△ NO CRITICAL
PATH FEEDBACK
△ 'C'
1
DO (for c
=1 to PPNCP)
'F'
'T'
△ LOOP FOR EACH CRITICAL PATH
BOTTLENECK
△ 'I'
'F'
1
DO(for IT
=1 to PPNTP(c))
'T'
2
A
△ PROCESS EACH TASK
ON CRITICAL PATH
TO ADJUST COEFFICIENTS
'C'
1
A
3230
PAFBCP


2
A
200
FIND
(PPTID(c,IT),
TAID,NT,t)
△ FIND TASK PTID(IT)'s
INDEX t
t>0
F
T
100
PERROR
PRCRC(c,IT)
△ VERIFY BLOCK
IDENTIFIER
200
FIND
(PPCRB(c,IT),
BLID,NB,b)
≠'I/O'
≠'PROC'
3250
PAFBCB
1
A
b>0
T
F
3240
PAFBBB
△ MEMORY
BLOCK
BOTTLE-
NECK
ADJUST-
MENT
△ TASK
COMPU-
TATIONAL
BOTTLE-
NECK
ADJUST-
MENT
100
PERROR
55

DEALS



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D.4 ERROR MESSAGES

MASTER ERROR CODES

ERROR	PPD	BRIEF DEFINITION
1	1100	Invalid technology data base identifier
2	1200	Invalid required interface file identifier
3	1210	Invalid technology type
4	1210	Invalid technology device
5	1211	Duplicate system or candidate processor device identifier
6	1211	Maximum processors exceeded
7	1213	Duplicate system or candidate memory device identifier
8	1212	Duplicate system or candidate device identifier
9	1212	Maximum communication devices exceeded
10	1213	Maximum memory devices exceeded
11	1300	Invalid baseline application file identifier
12	1310	Duplicate system block identifier
13	1310	Maximum blocks exceeded
14	1320	Maximum task identifier
15	1320	Maximum tasks exceeded
16	1400	Invalid candidate file identifier
17	1510	Undefined goal priority index
18	1510	Two goal priorities at same level
19	1510	Processor utilization goal is greater than absolute limit

MASTER ERROR CODES (CON'T)

ERROR	PPD	BRIEF DEFINITION
20	1510	Memory utilization goal is greater than absolute limit
21	1510	Development cost goal is greater than absolute limit
22	1510	Invalid default coefficient code
23	1520	Invalid goal index
24	1521	Invalid processor identifier
25	1521	User supplied processor goal greater than user supplied absolute limit
26	1521	Invalid processor coefficient level code
27	1522	Invalid memory identifier
28	1522	User specified memory goal greater than user specified absolute memory
29	1522	Invalid memory coefficient level code
30	1523	Invalid task identifier
31	1523	User supplied task cost goal is greater than user supplied absolute limit
32	1523	Invalid task coefficient level code
33	1540	Invalid constraint type
34	1541	Invalid task or processor identifier in constraint definition
35	1541	Duplicate task to processor constraint encountered
36	1541	Invalid task to processor constraint
37	1542	Invalid block or memory identifier in constraint definition

MASTER ERROR CODES (CON'T)

ERROR	PPD	BRIEF DEFINITION
38	1542	Duplicate block to memory constraint encountered
39	1542	Invalid block to memory constraint
40	2200	Saturated processor bottleneck detected
41	2200	Saturated memory bottleneck detected
42*	2300	Invalid goal index
43	2320	Fixed allocation has overloaded processor j
44	2320	Unable to offload processor j to be within absolute limit level
45	2320	Maximum processor balance iterations encountered
46	2320	Offloading has converged to single processor
47	2320	Least loaded processor unable to take on additional tasks
48*	2322	Invalid processor reallocate code
49	4000	Invalid report request
50	2420	Fixed allocation has overallocated memory j
51	2420	Unable to offload memory j to absolute limit level
52	2420	Maximum memory iterations
53	2420	Least loaded memory j unable to take additional blocks

*Fatal Algorithm Error

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
1	LIMITS, CONSTANTS, AND CODES			
	Maximum blocks	MB	Integer=400	
	Maximum columns of current optimization matrix	MC	Integer=10000	
	Maximum external devices	MED	Integer=20	
	Maximum replicates of any block	MH	Integer=4	
	Maximum number of distinct input and/ or output blocks per task	MIO	Integer=6	
	Maximum memories	MM	Integer=20	
	Maximum processors	MP	Integer=20	
	Maximum partitions saved	MPS	Integer=3	
	Maximum communication devices	MQ	Integer=100	
	Maximum rows of current optimization matrix	MR	Integer=10000	

AD-A096 456 TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/G 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
FEB 81 S J CLYMER F33615-78-C-0013
UNCLASSIFIED AFHRL-TR-80-42-PT-2 NL

4 OF 4
AD A
096456

END
DATE
FILMED
4-81
DTIC

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Maximum tasks	MT	Integer=100	
	Preemptive priority code i=1 to 3	MPC (i)	2 characters	
		MPC (1)	='PB'	Processor utilization balance
		MPC (2)	='MB'	Memory utilization balance
		MPC (3)	='TC'	Task development cost
	Coefficient selection level codes i=1 to 3	MCL (i)	1 character	
		MCL (1)	='A'	Average
		MCL (2)	='W'	Worst case
		MCL (3)	='	Use default
	Master Restriction Codes	MRC (i)	1 character	
		MRC (1)	='F'	Fixed allocation
		MRC (2)	='I'	Initial allocation
		MRC (3)	='P'	Prohibited allocation

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
2	CURRENT PROBLEM SIZING CONTROLS			
	Number of blocks	NB	Postive Integer 1.LE.NB.LE.MB	
	Number of columns in current optimizer matrix	NC	Positive Integer .LE.MC	
	Number of external devices	NED	Positive Integer .LE.MED	
	Number of memory devices	NM	Positive Integer .LE. MM	
	Number of processor devices	NP	Positive Integer .LE. MP	
	Number of communication devices	NQ	Positive Integer .LE. MQ	
	Number of rows in current optimizer matrix	NR	Positive Integer .LE. MR	
	Number of tasks	NT	Positive Integer .LE. MT	
	Number of variables	NV	Positive Integer .LE.(MC-2NR)	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
3	PRIORITY CONTROLS			
	Number of goals	NG	Integer 1.LE.NG.LE.3	
	Priority selected as goal L	GOAL (L)	Integer Code	
	L=1 to NG		=1	Processor Utilization Load Balance Heuristic
			=2	Memory Utilization Allocation Balance Heuristic
			=3	Minimize Development Cost Heuristic
	Priority default coefficient selection level	GDCS(L)	Integer Code =1 =2	 Average Worst Case
	-Processor Coefficients	GDCS (1)		
	-Memory Coefficients	GDCS (2)		
	-Task Coefficients	GDCS (3)		

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Processor utilization goal	GPU	real	
	Processor utilization limit	GPUU	real	
	Processor utilization tolerance	GTOLPU	real	=GPUU-GPU
	Processor utilization solution measure	GPUSOL	real	
	Maximum processor balance iterations	MPITER	integer	
	Processor utilization penalty	GPNLT	real	
	Memory utilization goal	GMU	real	
	Memory utilization upper limit	GMUU	real	
	Memory utilization tolerance	GTOLMU	real	=GMUU-GMU
	Memory utilization solution	GMUSOL	real	
	Maximum memory blance iterations	MMITER	integer	

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Memory utilization penalty	GMPNLT	real	
	Development cost goal	GDC	real	
	Development cost upper limit	GDCU	real	
	Development cost tolerance	GTOLDC	real	=GDCU-GDC
	Development cost solution	GDCSOL	real	
	Maximum Development Cost Iterations	MCITER	integer	
	Number of processors for which the utilization is greater than supplied goal	NPGTG	non-negative integer 0.LE.NPGTG .LE. NP	
	Number of processors for which the utilization is greater than the upper limit	NPGTL	non negative integer 0.LE.NPGTL .LE.NPGTG	
	Number of memories for which the allocation is greater than supplied goal	NMGTG	non-negative integer 0.LE.NMGTG .LE.NM	

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Number of memroies for which the allocation is greater than supplied upper limit	NMGTL	non-negative integer 0.LE.NMGTL .LE. NMGTG	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
4	CURRENT PROCESSOR LIST			
	Number of distinct processor devices	CDPNT		
	For each distinct processor device d			
	.Benchmark instruction flag i	CDPIF (d,i)	=0	Currently not in active solution
			=1	Currently in active solution

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	For processor p=1 to NP			
	-Identifier	CDPID (p)	10 characters	
	-Technology device index	CDPTI (p)	Integer > 0	
	-Operating system	CDPOS (p)	10 char code	
	-Active task levels	CDPTL (p)	Integer > 0	
	-Language l=1 to 3	CDPL (p,l)	10 Char code	
	-Goal utilization	CDPGU (p)	real	
	-Maximum acceptable utilization	CDPMU (p)	real	
	-Current solution utilization	CDPCU (p)	real	
	-Current utilization deviation for goal	CDPCD (p)	real	
	-Coefficient selection level	CDPCD (p)	integer code =1 =2	 Average Worst Case
	-Current solution SW development cost	CDPDC (p)		

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
5	CURRENT MEMORY LIST			
	For memory m=1 to NM			
	-Identifier	CDMID (m)	10 characters	
	-Technology device index	CDMTI (m)	Integer > 0	
	-Sizing			
	.Unit Index	CDMSU (m)	Integer	
	.Amount	CDMSA (m)	Integer > 0	
	.Total bits	CDMSZ (m)	real >0	
	-Goal utilization	CDMGU (m)	real	
	-Maximum acceptable utilization	CDMMU (m)	real	
	-Current solution utilization	CDMCU (m)	real	
	-Current utilization deviation from goal	CDMCD (m)	real	
	-Coefficient selection level	CDMCL (m)	integer code =1 =2	 Average Worst Case
	-Current solution total memroy access time	CDMTA (m)		

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
6	CURRENT COMMUNICATION LINK LIST			
	For communication device q=1 to NQ			
	-Identifier	CDQID (q)	10 characters	
	-Technology device index	CDQTI (q)	positive integer	
	-Number of interfacing devices	CDQND (q)	positive integer	
	-Interfacing device i =1 to CDQNI (q)			
	.Type	CDLIT(q,i)	Integer Code	
			=1	for processor
			=2	illegal for current algorithms
			=3	memory
			=4,5,...14	for external devices
	.Candidate index	CDLII(q,i)	Integer > 0	
	.Priority level	CDLIP(q,i)	Integer > 0	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
7	CURRENT EXTERNAL DEVICE LIST			
	For device d=1 to NED			
	-Identifier	CDEID (d)		
	-Type index	CDETY (d)		
	-Technology device index	CDETI (d)		
	-Number of system data blocks	CDENB (d)		
	-For each data block b=1 to CDEDB(d)			
	.Block Index	CDEBI(d,b)		

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
8	TASK/PROCESSOR ALLOCATION AND RESTRICTIONS			
	Task t processor p map	TPMAP (t,p,1)		
		TPMAP (t,p,1)	Ø,1,...,Nt	current task t executions allocated to processor p
		TPMAP (t,p,2)	Ø,1,...,Nt	lower bound on task t executions on processor p
		TPMAP (t,p,3)	Ø,1,...,Nt	upper bound on task t executions on processor p
		TPMAP (t,p,4)	Integer Code	
			=Ø	No user allocation input (default value)
			=1	User allocation processed

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Task t processor p coefficient values			
	Time for task t execution on processor p	TPVAL (t,p,1)	real > 0	milliseconds
	Resource task management coefficient for task t on processor p if time or data enabled	TPVAL (t,p,2)	real > 0	microseconds
	Resource task managent per task t execution on processor p for slaved enabled task	TPVAL (t,p,3)	real > 0	microseconds
	The cost coefficient for developing	TPVAL (t,p,4)	real > 0	manyears
	The cost coefficient for resource management of task t development on processor p	TPVAL (t,p,5)	real > 0	manyears

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
9	MEMORY/PROCESSOR COMMUNICATION ALLOCATIONS, RESTRICTIONS			
	Basic communication between memory m and processor p			
	-Read access	MPMAP (m,p,1)	Real .LE. Ø otherwise	no access read rate bits/ second
	-Write access	MPMAP (m,p,2)	Real .LE. Ø otherwise	no write access write rate bits/ second
	-Number of current solution entries	MPMAP (m,p,3)	Non-negative integer	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	For each current solution entry e	MPSOL		
	.Task index t	MPSOL (m,p,e,1)		
	.Block index b	MPSOL (m,p,e,2)		
	.Type of access	MPSOL (m,p,e,3)	Integer code	
			=1	read only
			=2	write only
			=3	read and write
	.Number of task executions on p making access to memory m	MPSOL (m,p,3,4)	Integer	
			.GE. 1	Must be at least one for entry
			.LE. NT Where t= MPSOL(m,p,e,1)	At most all task t executions are on processor p and utilize block b from memory m

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
10	MEMORY/BLOCK ALLOCATION RESTRICTIONS, AND COEFFICIENTS			
	Memory m block b map	MBMAP (m,b,1)		
		MBMAP (m,b,1)	0,1	current allocations 0-not allocated 1-allocated
		MBMAP (m,b,2)	0,1	lower bound for 0-does not have to be allocated 1-must be allocated
		MBMAP (m,b,3)	0,1	upper bound for 0-cannot be allocated 1-may be allocated
		MBMAP (m,b,4)	0,1	user option processed 0-not processed (default) 1-processed
		MBVAL(m,b)	real	length of block b if stored on memory m

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
11	MASTER BLOCK LIST			
	For each block b=1 to NB			
	-Identifier	BLID (b)		
	-Level	BLLEV (b)	Integer code =1 =2 =3 =4 =5	 System level block Global block Local block Scratch block Instruction block
	-Discipline	BLDSP (b)	Integer code	Must match technology data base blode discipline codes in IOPT-5
	-Number of suitable memories	BLNSM (b)	Integer .GE. 0	
	-Suitable Memory list i=1 to BLNSM(b)	BLSMM (b,i)	Positive integers	Indices to candidate memory devices
	-Maximum Records	BLMXR (b)	Positive integers	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	-Record length			
	.Bits/Byte	BLRBI (b)	positive integer	bits
	.Bytes/word	BLRBY (b)	positive integer	bytes
	.Minimum Words	BLRW(b,1)	positive integer	words
	.Average Words	BLRW(b,2)	positive integer	words
	.Maximum Words	BLRW(b,3)	positive integer	words
	-Number of tasks referencing block b	BLNTR (b)		
	-List of tasks *referencing block b* for e=1 to BLNTR(b)			
	.Task index	BLTID (b,e)		
	.Reference index	BLTRF (b,e)	=1	as input
			=2	as output
			=3	as update

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
12	MASTER TASK LIST			
	For each task t=1 to NT			
	-Identifier	TAID (t)	6 characters	
	-Source code index	TASC (t)	positive integer	
	-Number of benchmark instruction references in task instruction mix list	TANIM(t)	Positive Integer .GE. 1	
	-Instruction mix list for each benchmark reference i=1 to TANIM(t)	TAIMX (t,i,j)		
	.Benchmark instruction index	TAIMX (t,i,1)		
	.Count for sizing			
	Average	TAiMX (t,i,2)	Positive Integer	
	Worst Case	TAIMX (t,i,3)	Positive Integer	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	.Execution counts for timing			
	Average	TAIMX (t,1,4)	Positive integer	
	Worst Case	TAIMX (t,1,5)	Positive Integer	
	-Overlay flag	TAOLF (t)	=0	not an overlay
			=1	overlay
	-Number of task I/O blocks	TANIO (t)	positive integer	
	-For each block i=1 to TAIO(t)			
	.Block index	TAIOB(t,i)	positive integer	
	.How referenced index	TAHBR(t,i)	positive integer	
			=1	Input
			=2	Output
			=3	Update

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	.When referenced index	TANBR(t,i)	positive integer	
			=1	START
			=2	ALONG
			=3	END
	.Records read per task t execution	TARR (t,i,k)	positive integer	k=1 minimum k=2 average k=3 maximum
	.Fraction of records read from block i task t based upon current coefficient selection level	TARRF (t,i)	Positive real F10.5	
	.Records output per task t execution	TARW (t,i,k)	Positive Integer	k=1 minimum k=2 average k=3 maximum
	.Fraction of records written to block i by task t based upon current coefficient selection level	TARWF (t,i)	positive real F10.5	

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	-Task enablement index	TAEN (t)	positive integer code =1 =2 =3	
	-Master Task	TAMT (t)	6 characters	
	-Maximum execute time	TAMET (t)	real	
	-Frequency	TAFRQ (t)	real	iterations per second

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	-Task development cost			
	.Goal	TADCG (t)	real	manyears
	.Upper limit	TADCU (t)	real	manyears
	.Current solution	TADCS (t)	real	manyears
	.Current deviation from goal	TADCD (t)	real	manyears
	.Current task cost index	TADCI (t)	integer	
	.Number of processor currently allocated to task t	TADCP (t)	integer .GE. 1	
	.List of processors for e=1 to TADCP (t)	TADCL(t,e)	integer	candidate processor index
	-Coefficient generation level	TACLS (t)	integer code	
			=1	Average
			=2	Worst Case

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
13	BASELINE STATIC LOAD			
	Evaulation interval	BLPER	Positive Real	Seconds
	Number of threads active	BLPAT	Non-negative Integer	
	For each active thread k			
	.Number of tasks [BLPAT]	BLTNT(k)	Positive Integer .LE.NT	
	.Task Indices [BLPAT,BLTNT]	BLTIN(k,g)	Positive Integer .LE.NT	
	Number of distinct parallel task groups	BLPAG	Non-negative Integer	
	For each active parallel group g			
	.Number of tasks [BLPAP]	BLGNT(g)	Positive Integer .LE. NT	
	.Task Indices [BLPAP,BLGNT]	BLGIN(g,i)	Positive Integer .LE. NT	

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