FABRICATION AND DESIGN ISSUES OF BULK PHOTOCONDUCTIVE SWITCHES USED FOR ULTRA-WIDEBAND, HIGH-POWER MICROWAVE GENERATION

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Abstract—**The Army Research Laboratory (ARL), in collaboration with the Air Force Phillips Laboratory, has been developing the fabrication process for lateral topology, high-power photoconductive semiconductor switches (PCSS) used in phased-array, ultra-wideband (UWB) sources. This work presents issues associated with the development of these switches. First-generation devices (1.0 cm gap spacing) have been shown to achieve sub-nanosecond risetimes, working hold-off voltages of 50 kV, switched currents of 333 A into a 75 Ω load, and lifetimes in excess of 2 x 10^6 shots at 10 Hz. Later-generation devices (0.25 gap spacing) operate at 20 kV and 1 kHz, with improved risetimes, jitter characteristics, and trigger requirements.**

I. Introduction

There is considerable interest within the technical community in pulse power sources capable of producing high-power, UWB microwave radiation. Typical applications require a high voltage (> 10 kV) to be switched with sub-nanosecond risetime into an impulse radiating antenna. A phased-array antenna system is often employed to achieve steering of the generated microwave pulse. This configuration requires a switch which exhibits trigger jitter that is much less than the switching risetime. Furthermore, in most applications, high repetition rates (> 1 kHz) and long device lifetimes (> 10^6) are necessary.

A typical approach to obtaining the above device requirements is the utilization of commercially available semiconducting materials such as gallium arsenide (GaAs), indium phosphide (InP), and silicon (Si). Both laser light and electron beams have been employed to trigger the device into a conducting state. In the work presented here, optically triggered GaAs is used.

Two modes of operation are observed when considering the optical trigger aspects of both GaAs and InP. In the case of "linear" switching, each incident photon generates, at most, one electron-hole pair and the resistivity of the on-state material is linearly related to the incident optical power[1,2]. In this case the risetime of the current is determined primarily by the risetime of the optical trigger. Upon removal of the incident optical energy, the photo-generated carriers recombine with the lattice in approximately one nanosecond, allowing short fast-risetime pulses to be generated. Although this mode of device operation has demonstrated virtually jitter-free response, the power requirements of the laser trigger system are excessive, limiting the practical usage of this mode of operation.

A second mode of operation, termed "lock-on", "avalanche," or "high-gain", relies on an optically induced carrier multiplication process within the bulk of the semiconducting material[3]. In this mode of operation, a single incident

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14. ABSTRACT
The Army Research Laboratory (ARL), in collaboration with the Air Force Phillips Laboratory, has been developing the fabrication process for lateral topology, highpower photoconductive semiconductor switches (PCSS) used in phased-array, ultrawideband (UWB) sources. This work presents issues associated with the development of these switches. First-generation devices (1.0 cm gap spacing) have been shown to achieve sub-nanosecond risetimes, working hold-off voltages of 50 kV, switched currents of 333 A into a 75 !2 loa~ and lifetimes in excess of 2 x ld shots at 10 HZ Later-generation devices (0.25 gap spacing) operate at 20 kV and 1 kHz, with improved risetimes, jitter characteristics, and trigger requirements.

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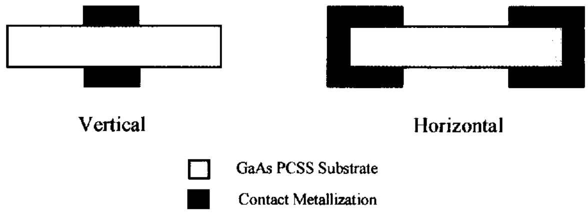

Figure 1. Generic vertical and lateral PCSS topologies.

photon will ultimately induce the formation of many electron-hole pairs. In general, the switched risetime of the current is much faster than the risetime of the optical trigger pulse. The avalanche process acts as an internal gain mechanism, drastically reducing the optical trigger system requirements. Typical applications utilize an inexpensive, small laser diode array as a trigger source.

The vertical and/or lateral switch topologies are typically employed for photoconductive switch development[3,4]. In the case of vertical switches, the anode and cathode are placed on the top and bottom of the semiconducting material while lateral switches have the anode and cathode on both sides of the material in a planer fashion as shown in Fig. 1. Vertical switches are attractive because the hold-off voltage is primarily determined by the bulk properties of the material in contrast to the lateral topology where surface flashover effects can severely limit the working voltage of the device. However, in the case of vertical devices, a higher hold-off potential requires increased wafer thickness which may be prohibitive with respect to device fabrication. Furthermore, since the depth of optical trigger penetration is critical to device performance, vertical devices typically utilize a longer wavelength optical pulse. Longer wavelengths produce photons of energy less than the band gap of the semiconducting material allowing optical energy to penetrate the entire depth of the device. In this mode of operation, device conductivity is altered through deep defect related transitions. Although electron-hole pair generation occurs relatively uniformly throughout even the thickest devices, it is inefficient when compared to the direct band-to-band transitions that occur when photons with energies closer to the band gap are utilized. Lateral devices, however, can sustain an increase in the hold-off voltage simply by spacing and shaping the contacts appropriately. The lateral topology allows illumination of the entire switch gap, resulting in a high trigger efficiency.

The geometry of the anode and cathode contact has been shown to be important. High-gain photoconductive switching is accompanied by current filamentation[5]. If the current filaments are allowed to occur repeatedly in specific locations, severe device damage will result. A Rogowski[6] profile has been shown to produce uniform fields across the device, allowing current filamentation to occur at random locations on a shot to shot basis. This has been shown to greatly increase switch lifetime[7].

This work presents data concerning the development of high-gain, hybrid, lateral switches, with Rogowski-pattered anode and cathode contacts[8]. Both a high energy laser system and a low-energy laser diode system have been used for device triggering. These devices, which make use of both the vertical and lateral topologies, are shown to satisfy the voltage, current, jitter and lifetime requirements, and are promising candidates for the UWB systems suggested above.

II. PCSS Device Fabrication

The devices are fabricated from (100) semi-insulating GaAs substrate material. Each substrate is 25 mil thick, 50 mm in diameter, and is determined by the manufacturer to have a resistivity of 2 - 5 x $10^7\,\Omega$-cm. The VGF material is supplied by the manufacturer with both sides polished and is considered to be MBE growth-ready. The LEC material used had only one side polished (as supplied by the manufacturer) and an outside vendor was employed to polish the remaining side. In both cases no further cleaning is performed prior to the deposition of 1,000A of stoichiometric Si_3N_4.

Following the nitride deposition, one of two procedures is followed, depending on whether the 1.0 cm switch (one device per wafer) or the 0.25 cm switch (four devices per wafer) is being fabricated. The contact geometries are shown in Fig. 2. In the case of the single 1.0 cm device, both sides of the substrate are coated with photoresist and the Rogowski contact pattern is photolithographically defined and developed on one side. The sample is then placed in a reactive ion etcher and the nitride coating removed in the patterned area. Following the removal of the nitride coating, the sample is immersed for 10 seconds in a solution of $NH_4OH:H_2O$ to remove any native oxide. The sample is then placed in an e-beam evaporator and the appropriate metallization scheme is deposited (see Table 1). Upon removal from the evaporator, the sample is soaked in a warm acetone bath to facilitate metal liftoff. Once liftoff is complete, both sides of the sample are then re-coated with resist and the remaining side contact is

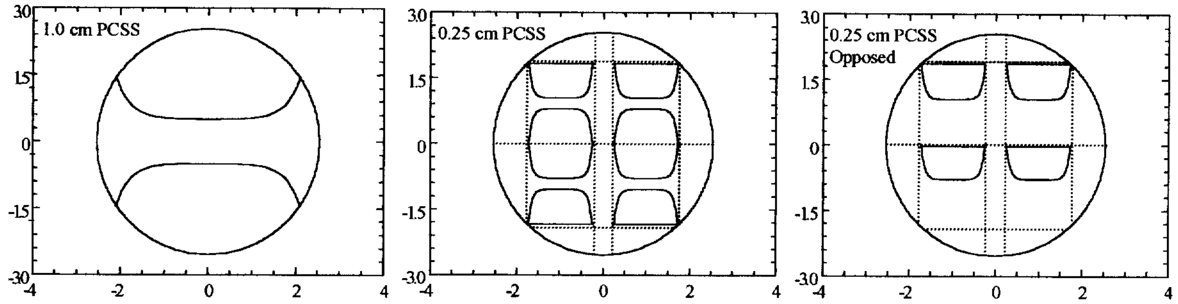

Figure 2. The three lateral PCSS geometries as fabricated on 50 mm wafers. All axes are in cm.

Standard Ohmic Contact		Refractory Ohmic Contact	
Metal	(Å)	Metal	(Å)
Ni Ge Au Pd Au	50 750 750 750 2,000	Pd Ge Ti Pt	200 400 400 300
RTA 10 sec. @ 480°C		RTA 30 sec. @ 480°C	

Table 1. Metallization schemes used in PCSS fabrication.

photolithographically defined. The procedure for nitride removal and metal deposition is then repeated. For the case of the 1.0 cm device, front-to-back alignment of the contacts is achieved using a mark on the mask plates that aligns the entire pattern to the primary flat of the wafer.

When patterning the 0.25 cm device substrate, the sample is sandwiched between the appropriate mask plates and each side is exposed and developed. Although reasonable success was achieved with this method, it is not the optimum procedure. If a problem were to arise during the processing of one side of the wafer, it was found to be difficult to strip the pattern and repeat the photolithography for a single side. For this reason, procedures for front-to-back side alignment are currently being investigated that employ either an infrared imaging camera or a new set of mask plates that have alignment marks associated with the primary and secondary flats of the wafer, as well as the wafer edge.

In both cases, following metal deposition and pattern liftoff, the samples were alloyed in a rapid thermal annealer for the times shown in Table 1. The 0.25 cm devices were then cleaved using a scribe-and-break technique

III. Experimental Hardware

For testing, the PCSS devices are series-connected between a 75 Ω, 1 ns source transmission line and a 75 Ω, 4 ns load-transmission line that is contained within a 40 psi SF_6 environment. The source line is pulse charged to a voltage adjustable between 0 and 50 kV, as required by switch experiments. A high-current, FET-based pulse modulator (developed by Phillips Laboratory) is used to drive a 100:1 pulse transformer which charges the source line to a predetermined voltage. The FET circuit is configured to shunt the primary of the pulse transformer 1 μs before the switch is triggered. This timing delay eliminates the possibility of direct late time current injection from the pulse transformer. This technique is found to greatly improve the device lifetime. The load transmission line incorporates a high bandwidth capacitive voltage sensor (calibrated to 6 GHz) to monitor the switched voltage. Output of the sensor is recorded using Tektronix SCD-5000 transient digitizers.

Optical trigger energy is provided by a tunable, high energy Nd:YAG pumped Ti:Sapphire, 10 Hz laser system or a low energy 904 nm, 10 kHz laser diode array module. The high-power laser system is tuned from 880 nm to 910 nm and can produce a 1 mJ, 5 ns optical pulse. The laser diode module produces a 650 Watt peak, 20 ns, 904 nm pulse with a 175 ps risetime.

IV. Experimental Results

The Ti:Sapphire laser system is tuned to 885 nm used to trigger the 1 cm gap PCSS. Test results indicate that the LEC-based switches have a risetime of approximately 420 ps and the VGF-based switches have a risetime of

1.0 cm gap	Parameter	0.25 cm
50 kV	Working Potential	20 kV
5 kV	On-state Potential	1 kV
50 kV/cm	Working Field	80 kV/cm
333 A	Switched Current	133 A
430 ps	Risetime	350 ps
500 ps rms	Jitter	65 ps rms
10 Hz	PRR	1 kHz
2.0×10^6	Lifetime	5.0×10^4

Table 2. 1.0 cm and 0.25 cm opposed-contact PCSS operating parameters.

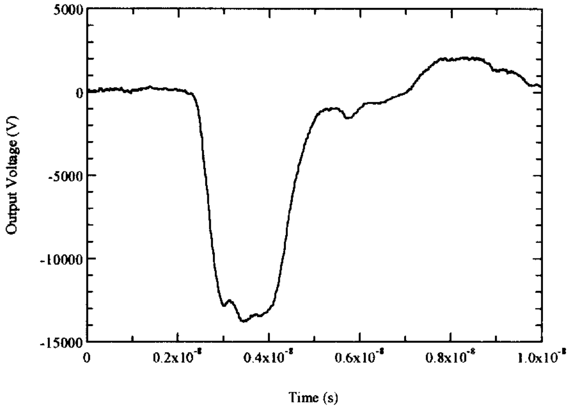

Figure 3. Typical switched waveform.

approximately 900 ps The reason for the increased turn-on time is not immediately known but prompted the discontinuation of the VGF material for device fabrication. It was found that the deposition of a layer of Si_3N_4 prior to device fabrication resulted in an improved switch lifetime. It is believed that the silicon nitride serves to protect the active switching region of the PCSS during device processing.

The 0.25 cm switches were investigated to facilitate a reduction in the overall size of a UWB system. The devices are reliably triggered with the laser diode module. Although the switch performed well, the switch reliability was significantly reduced. To increase the operating voltage and reliability, while still maintaining a small physical size, the 0.25 cm device was fabricated with contacts on opposing sides of the wafer. These vertical/lateral hybrid switches have been operated at 24 kV as compared 18 kV for the standard 0.25 cm PCSS. A summary of the simultaneous test results for the 1.0 cm and 0.25 cm device is shown in Table 2. A typical PCSS switched waveform is shown in Fig. 3.

Switch lifetimes as high as 2×10^6 switching events have been demonstrated with the 1.0 cm switch while operating at 50 kV charge voltage. Severe erosion of the Ni-Ge-Au-Pd-Au contacts is observed after 10^5 events. To mitigate contact erosion, the refractory contact was tested. The refractory contact was found to be much less susceptible to contact erosion and is therefore currently being tested for lifetime considerations.

V. Conclusions

Use of LEC GaAs, in an opposed contact, hybrid topology, with Rogowski contacts formed from refractory metals appears to be the best configuration for UWB source applications. Laser diode triggering of relatively small geometry switches suggests that a compact, low cost, UWB source can be realized. The low jitter exhibited by these switches also suggests the possibility of utilizing the phased-array technology for increased power delivery. Next generation switches will be of the opposed-contact topology with thicker substrate materials in anticipation of increasing the PCSS working voltage. Investigations of methods for optimum device packaging and thermal management for improved reliability and system maintenance are currently underway.

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