Micro-Electro-Mechanical Systems (MEMS) Fabrication Course Projects Review for FY15

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Approved for public release.

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ADMINISTRATIVE INFORMATION

This work was prepared by the Advanced Circuit Technology Branch (Code 55250) of the Networks Division (Code 55190), Space and Naval Warfare Systems Center Pacific (SSC Pacific), San Diego, CA. SSC Pacific’s Naval Innovative Science and Engineering (NISE) Program provided funding for this Workforce Development project.

Released by
M. Wood, Head
Advanced Integrated Circuit Technology Branch

Under authority of
P. Juarez, Head
Networks Division

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SSC Pacific S&T Workforce Development
MEMS Fabrication Course
Projects Review for FY15

Presented to:
San Diego State University (SDSU) Students and Staff
June 18, 2015

Paul D. Swanson et. al.
7.1
Code 55250
**Pl: Dr. Paul D. Swanson, Engineer**

Paul Swanson received a Ph.D. in electrical engineering from the University of Illinois at Urbana Champaign. As a post-doc he fabricated devices at the Cornell NanoScale Science & Technology Facility (CNF). He was an industrial user at Stanford Nanofabrication Facility (SNF) and in charge of Nanogen’s internal semiconductor fabrication clean-room. He has 33 issued patents, 17 refereed publications, and is a listed author on six conference proceedings. At SSC Pacific, he invented Time Domain Switched Inertial Sensors (TDSIS). (Not a SMART scholarship recipient.)

**Co-Pl: Bruce W. Offord, Engineer**

Bruce Offord received his B.S. in Engineering Physics from the University of California, San Diego. Bruce has more than 13 patents, has authored more than 20 publications, received a Navy Meritorious Civilian Service award, an Exemplary Achievement award, Distinguished Publication and Excellence in Publications awards, and Navy Award of Merit for Group Achievement. Mr. Offord has more than 25 years of experience in integrated circuit design, fabrication, and testing. He has worked on R&D projects for the Navy, DARPA, ARDA, and commercial entities in radiation hardened silicon fabrication processes, radio frequency switches, displays, sensors, and carbon-nanotube switches. (Not a SMART scholarship recipient.)
Class of FY15

SSC PACIFIC MEMS Course Student/Project List

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<td>Jonathon Oiler:</td>
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Instructors:

- Paul D. Swanson
- Bruce W. Offord
- Prof. Samuel K. Kassegne (SDSU)
Wayne McGinnis:

Backside Alignment without a Backside Mask Aligner

Presenter:
Wayne McGinnis
SSC Pacific, Code 81320

Presented to:
SDSU MEMS Course Participants
June 2015
Method 1: Use etched through-holes as alignment marks.

- Through-holes
- Wafer placement holes
- Bottom pattern (looking “through” wafer from the top)
- Top pattern
Method 2: Use wafer piece corners as alignment marks

Bottom pattern
(looking “through” wafer from the top)

Top pattern

1"-square wafer outline

alignment corners

wafer placement bars
Process Steps and Results for Method 1

- Clean wafer with solvents (acetone, isopropanol, water)
- Clean wafer with O\textsubscript{2} plasma etch
- Coat/cure Durimide 7510 (photo-definable polyimide) on frontside
- Coat/pattern/cure Durimide on backside
- Etch through backside openings (circles) with KOH etchant
- Remove Durimide from both sides with O\textsubscript{2} and then O\textsubscript{2}/CF\textsubscript{4} plasma etches
- Pattern frontside with photoresist using etched through-holes as alignment marks

![Image 1](image1.jpg)
![Image 2](image2.jpg)
![Image 3](image3.jpg)

06/18/2015
Next Steps

- Find different KOH etch mask material (Apiezon W wax, ProTEK, ?)
- Test etch mask viability on small Si piece(s)
- Demonstrate backside alignment methods 1 and 2
Jonathan Oiler: Enhanced Pathogen Detection with Microfluidics

Presenter: Jonathan Oiler
SSC Pacific, Code 71750

Presented to: SDSU MEMS Course Participants
June 2015
Pathogen Detection

Need: The Navy has a need for a reagent-less, portable, rapid pathogen detection system in order to detect pathogens in aquatic environments for the safety of Navy divers and forward deployed soldiers requiring safe water resources.
Pathogen Detection – Current

▼ How are water-based pathogens detected?

▼ Current State of Sampling Technology

AWT Lab
Pathogen Detection – Near Future

▼ Portable system developed by commercial company:

▼ Current Technology Development

06/18/2015
Pathogen Detection - Future

▼ Include flow cytometry and cell sorting/concentrating
Microfluidic Front End

▼ Flow Cytometer
- Companies like CytoChip are developing tiny microfluidic flow cytometry systems
Microfluidic Front End

▼ Filtering

- Due to high particle (organic/non-organic) concentration in seawater – pre-filtering is required
- Secondary micro-fluidic filtering necessary for dealing with small sample size for micro-cytometer systems
Microfluidic Front End

Microfluidic Filter

- Eliminate large cells/particles

Peh et al., IEEE Transducers, 2007
Microfluidic Front End

▼ Cell separation/collection/concentration
  ▪ Mechanical means:

Hasegawa et al., Micro/Nano Mechatronics Hum Sci., 2013

Karunanidhi et al., IEEE Nano/Mol. Med and Eng., 2013
Howard Dyckman:
Suspended Infrared Waveguides

Presenter:
Howard Dyckman
SSC Pacific, Code 71730

Presented to:
SDSU MEMS Course Participants
June 2015
Objective & References

- Objective: Develop fabrication procedures to make suspended waveguides for infrared in wavelength range 1-5 um.


▼ S. Zlatanovic et al. (2013). Silicon-on-Sapphire Waveguides for Widely Tunable Coherent Mid-IR Sources, SSC Pacific TD 3275

▼ S. Zlatanovic et al. (2014). Silicon-on-Sapphire Waveguides: Mode-converting Couplers and Four-Wave Mixing, SSC Pacific TD 3283
Suspended Waveguide for Infrared
**Pattern for Suspended Waveguides**

Suspended waveguide with horizontal supports

- A: 5 um; B: 5–10 um; C: 10–50 um; D: 15–20 um; E: 2–4 mm

**Goal:** develop fabrication methods; 5-um lithography limit prevents making single-mode waveguides for 1- to 5-um IR
Many waveguides, each 5 um wide
Positive mask for positive photoresist is shown
Negative mask for negative photoresist is inverse
Wafers

▼ Silicon wafers
- SiO₂ layer 3659 Angstrom
- Si top layer 2165 Angstrom

▼ Photolithography done on four wafers
- 1. Shipley S1813 (positive photoresist)
- 2. Shipley S1813 (positive photoresist)
- 3. SU-8-10 (negative photoresist)
- 4. PMGI + Shipley S1813 (positive photoresist with PMGI underlayer)
Overall Procedure

▼ Protect waveguides and supports
  ▪ Positive mask for positive photoresist (Shipley S1813; Shipley S1813 with PMGI underlayer)
  ▪ Negative mask for negative photoresist (SU-8-10)

▼ Etch around waveguide and supports, through top Silicon layer, using CF$_4$ plasma; may etch partway through lower SiO$_2$ layer

▼ Etch SiO$_2$ around and under waveguides and supports

▼ Examine in Scanning Electron Microscope (SEM) for degree of etch
Waveguide After Exposing Shipley S-1813 Photoresist

▼ Spin 2000 rpm Shipley S-1813 for 45 sec to produce 2-um coating
▼ Prebake 115 °C for 60 sec
▼ Shipley MF-319 Developer
▼ Shown is one of the cleaner looking photoresists before etching
▼ Limited optical resolution of lithography (approx. 5 um) causes rounded corners
▼ Horizontal center-to-center of ovals measures 24 mm; Waveguide width measures 5.1 mm (viewed in optical microscope)
Pre-Baking SU-8: Slow Is Better

▼ SU-8 shrunk (many holes) due to fast pre-baking, approximately as follows:
  - 65 °C for 2 to 3 min
  - 95 °C for 5 to 6 min

▼ SU-8 shrunk very little (few holes) due to slower pre-baking
  - 45 °C for 8 min
  - 65 °C for 2 min
  - 95 °C for 3.5 min
  - 105 °C for 8 min
CF4 Etch of Top Silicon Layer

- Technics Series 85-RIE plasma etcher
- CF$_4$ plasma etch: about 470-490 mTorr, 50 W, 16 minutes
- CF$_4$ etch "burnt" some wafers
- Proposed Solution: Etch for less time, add O$_2$ to plasma
Mounting Wafers in SEM
Shipley S-1813 positive photoresist with CF$_4$ etch and HF vapor etch, not tilted in SEM

Most likely shows top Si layer, ring from SiO$_2$ layer, and Si wafer exposed inside ring
SEM Photo: Shipley

▼ Shipley S-1813 positive photoresist with CF$_4$ etch and HF vapor etch, tilted 45 deg in SEM

▼ May be showing slight undercut
PMGI + Shipley
S1813 positive photoresist with CF$_4$ etch and HF vapor etch, not tilted in SEM
Perhaps has etched Si and SiO$_2$ layers
SU-8-10 negative photoresist with CF$_4$ etch and HF vapor etch, tilted 45 deg, with measurements
SU-8-10 negative photoresist with CF$_4$ etch and HF vapor etch, tilted 45 deg

Shows 3-D structure of SU-8 layer but unclear what was etched and probably no undercut
Lessons Learned

▼ Add O₂ to CF₄ plasma etch of Si to moderate it – avoid burnt effect.

▼ HF vapor etch for SiO₂ can roughen silicon surface; find a liquid etch for SiO₂ that does not attack silicon. (Or, can leave photoresist on during HF vapor etch to prevent roughened waveguide surfaces, but hard to remove it from suspended structures afterwards.)

▼ Etch SiO₂ for longer time to get good undercut.

▼ SU-8 negative photoresist needs slow pre-bake with gradual raising of temperature to prevent shrinking. Bake "well done" to prevent sticking to mask. But exposed SU-8 is difficult or impossible to remove and would alter waveguide properties; use a different photoresist.
Why wasn’t there more undercut?
Lessons Learned, cont’d

▼ Higher resolution photolithography needed to make good IR waveguides - avoid rounded corners, make narrow waveguides for single-mode.

▼ Make waveguides longer to enable dicing and testing with infrared.

▼ Cut across waveguides and mount samples at 90 deg in SEM to see cross section better.

▼ Consider cleaning blank wafers with O₂ etch after Acetone/Isopropyl/DI H₂O.
Possible Follow-On Work

▼ Procure wafers with SiO$_2$ and Si layers with thicknesses more appropriate for IR waveguides (1 to 2 um).
▼ Use glass or quartz mask for 1 um lithography.
▼ Find better etch for SiO$_2$ and proper duration.
Acknowledgments

▼ Professor Sam Kassegne of SDSU and students
▼ Paul Swanson, Bruce Offord, and colleagues
▼ SSC Pacific Workforce Development program
Technical Execution

Teresa Emery:

Safe Cantilever Release Using KOH

Presenter:
Teresa Emery
SSC Pacific, Code 71730

Presented to:
SDSU MEMS Course Participants
June 2015
Bistable MEMS systems for Energy Harvesting

Non-linear devices are showing promise for responding to low frequency vibrations for energy harvesting applications. Most MEMS scale energy harvesters take the form of cantilevers operating in their resonant frequency, but such operation is usually confined to the higher frequencies due to their small size. Non-linear energy harvesters do not operate at their resonant frequency and can harvest lower frequency vibration while still being MEMS scale. One way to introduce non-linearity into a MEMS scale device is to make it bistable. This bi-stability can be created in several ways including shape, magnet repulsion and attraction, and material stress. Each methods benefits and drawbacks will be discussed as it applies to energy harvesting and ease of fabrication.
**Why use KOH Release the Cantilever?**

- KOH creates a very selective etch between silicon and silicon nitride.
- Low stress nitride is good insulating material used as a structural component of MEMS devices.
- KOH bath can release several wafers at a time with very repeatable results.
- The last step in all MEMS fabrication procedures is the release. Devices are too fragile to process after release.
Protecting Devices from KOH

- KOH is a common wet silicon etch, very corrosive. Top side electronic must be covered to prevent damage
- Two different spinable polymers are possible solutions: Durimide and ProTEK
- Sample piece will be covered and put in the KOH bath to test durability of the polymer
- The sample must also survive the removal of the polymer by solvent bath or oxygen plasma.
Technical Execution

Sam Chieh:

mm-Wave Antennas on Quartz Substrate

Presenter:
Sam Chieh
SSC Pacific, Code 55250

Presented to:
SDSU MEMS Course Participants
June 2015
mm-Wave Antennas on Quartz Substrate

Future innovative Navy systems will need to operate at high millimeter wave frequencies due to recent advancement and adoption of millimeter-wave and sub-millimeter wave communication systems, radars, and imaging systems.

We propose the design and development of monolithic wideband antennas for mm-Wave operation, and more specifically in the W-band (75–110 GHz). Shown is a conceptual diagram of how the sinuous antenna may look.
MEMS Fabrication – Sinuous Antenna

▼ Lift-Off process
- Plasma Etch Wafer
- PMGI Photoresist (150 °C for 5 min)
- Shipley 1813 Photoresist (115 °C for 90s)
- Expose and develop
- Chromium Sputtering (10 u, 20 u)
- Aluminum Evaporation
- Acetone Wash

▼ Observations
- Plasma etching critical for clean wafer
- Sensitive photoresist baking times
- Chromium sputtering necessary for aluminum to adhere
- Chromium sputtering 30 u caused burning. Needed 2 instances (10 u and 20 u)
Everly Yeo: mm-Wave Antenna Arrays for Millimeter Wave Camera

Presenter: Everly Yeo
SSC Pacific, Code 55250

Presented to: SDSU MEMS Course Participants
June 2015
Antenna Array for Use with Pin-Hole Camera
Ben McCoy: MEMS for Antenna
Summary

The objective of this work force development project was to further develop and offer a course for SSC Pacific S&T professionals to broaden their skills, experience, and understanding of Micro-Electro-Mechanical Systems (MEMS) through instruction and hands on experience in MEMS and semiconductor fabrication. It also had the objective of providing a means to access local university fabrication capabilities that will continue after this workforce development project is completed. By making the students familiar with the capabilities of accessible semiconductor fabrication labs, less money in the future will be needed to outsource MEMS fabrication, and more creative solutions and technology will be developed by SSC Pacific S&T scientists and engineers.
Micro-Electro-Mechanical Systems (MEMS) Fabrication Course Projects Review FY15

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Bruce W. Offord                      San Diego State University
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In Fiscal Year (FY) 2015, the third year of a three-year Naval Innovative Science and Engineering (NISE) Program Workforce Development project, Space and Naval Warfare Systems Center Pacific (SSC Pacific) held a course on micro-electro-mechanical (MEMS) and semiconductor device and fabrication techniques to assist its Science and Technology (S&T) scientists and engineers to develop technologies that increase the capabilities of the U.S. Navy warfighters. The objective of this workforce development project is to further develop and offer a course for SSC Pacific S&T professionals to broaden their skills, experience, and understanding of MEMS and lithography-based device fabrication through instruction and hands-on experience. The course was 14 weeks, consisted of 16 hours of lectures at SSC Pacific, and 32 hours at a local semiconductor fabrication facility with an external user program (in this case, at the San Diego State University [SDSU] MEMS lab). The SSC Pacific and SDSU instructors were experienced in semiconductor processing and MEMS design. The students became familiar with the capabilities of semiconductor fabrication, allowing device development using less money (compared to outsourcing) and more hands-on interaction and process ownership. The course was not for the students to complete their projects in the initial 14 weeks, but to act as a launching pad for new innovations that will assist funded projects and stimulate the creation of new funded projects.

Mission area: Micro-electronics
wafer etching               mm-wave antenna arrays
Infrared waveguides            MEMS for antennas
miniaturized flow cytometer     bistable MEMS systems
energy harvesting               mm-wave antennas
quartz substrate

In Fiscal Year (FY) 2015, the third year of a three-year Naval Innovative Science and Engineering (NISE) Program Workforce Development project, Space and Naval Warfare Systems Center Pacific (SSC Pacific) held a course on micro-electro-mechanical (MEMS) and semiconductor device and fabrication techniques to assist its Science and Techno (S&T) scientists and engineers to develop technologies that increase the capabilities of the U.S. Navy warfighters. The objective of this workforce development project is to further develop and offer a course for SSC Pacific S&T professionals to broaden their skills, experience, and understanding of MEMS and lithography-based device fabrication through instruction and hands-on experience. The course was 14 weeks, consisted of 16 hours of lectures at SSC Pacific, and 32 hours at a local semiconductor fabrication facility with an external user program (in this case, at the San Diego State University [SDSU] MEMS lab). The SSC Pacific and SDSU instructors were experienced in semiconductor processing and MEMS design. The students became familiar with the capabilities of semiconductor fabrication, allowing device development using less money (compared to outsourcing) and more hands-on interaction and process ownership. The course was not for the students to complete their projects in the initial 14 weeks, but to act as a launching pad for new innovations that will assist funded projects and stimulate the creation of new funded projects.

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