Final Report: Low Power Monolayer MoS2 Transistors for RF Applications

High quality MoS2 monolayers have been formed by CVD and DC and RF transistors were fabricated using e-beam lithography and a gate last process. Initial DC characterizations of fabricated MoS2 FETs yielded current densities exceeding $I_{ds} = 200 \, \mu A/\mu m$ at $V_{gs} = 5 \, V$ and $V_{ds} = 3.5 \, V$, and a transconductance $g_{m} = 38 \, \mu S/\mu m$ at $V_{gs} = -4.5 \, V$ and $V_{ds} = 3.5 \, V$. Operating at a low-field $V_{ds}$ of 0.01 V, we extract a contact resistance corrected mobility of 55 cm$^2$/Vs. To our knowledge these are the highest reported transconductance and mobility values for CVD MoS2. Radio frequency FETs were fabricated in the ground-signal-ground (GSG) layout and standard de...
High quality MoS2 monolayers have been formed by CVD and DC and RF transistors were fabricated using e-beam lithography and a gate last process. Initial DC characterizations of fabricated MoS2 FETs yielded current densities exceeding $I_{DS} = 200 \, \mu A/\mu m$ at $V_{GS} = 5 \, V$ and $V_{DS} = 3.5 \, V$, and a transconductance $g_{m} = 38 \, \mu S/\mu m$ at $V_{GS} = -4.5 \, V$ and $V_{DS} = 3.5 \, V$. Operating at a low-field $V_{DS}$ of 0.01 $V$, we extract a contact resistance corrected mobility of 55 cm$^2$/Vs. To our knowledge these are the highest reported transconductance and mobility values for CVD MoS2. Radio frequency FETs were fabricated in the ground-signal-ground (GSG) layout and standard de-embedding structures were applied. Operating at the peak $g_{m}$ conditions, we measured short-circuit current-gain cutoff frequency, $f_{T}$, of 6.7 GHz and a maximum oscillation frequency, $f_{MAX}$, of 5.3 GHz in 250 nm gate length $L_{G}$ devices. A new process has been developed for wafer scale MoS2 fabrication using sulfurization of ultra thin deposited Mo films.

(a) Papers published in peer-reviewed journals (N/A for none)


TOTAL: 1

(b) Papers published in non-peer-reviewed journals (N/A for none)

TOTAL:

(c) Presentations
Number of Presentations: 0.00

<table>
<thead>
<tr>
<th>Received</th>
<th>Paper</th>
</tr>
</thead>
</table>

**TOTAL:**

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

<table>
<thead>
<tr>
<th>Received</th>
<th>Paper</th>
</tr>
</thead>
</table>

**TOTAL:**

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

**Peer-Reviewed Conference Proceeding publications (other than abstracts):**

<table>
<thead>
<tr>
<th>Received</th>
<th>Paper</th>
</tr>
</thead>
</table>

**TOTAL:**

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

**(d) Manuscripts**

<table>
<thead>
<tr>
<th>Received</th>
<th>Paper</th>
</tr>
</thead>
</table>


**TOTAL:**  2
### Books

<table>
<thead>
<tr>
<th>Received</th>
<th>Book</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TOTAL:**

<table>
<thead>
<tr>
<th>Received</th>
<th>Book Chapter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TOTAL:**

### Patents Submitted

### Patents Awarded

### Awards

N/A

### Graduate Students

<table>
<thead>
<tr>
<th>NAME</th>
<th>PERCENT SUPPORTED</th>
<th>Discipline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atresh Sanne</td>
<td>1.00</td>
<td></td>
</tr>
<tr>
<td>Chris Corbet</td>
<td>1.00</td>
<td></td>
</tr>
<tr>
<td><strong>FTE Equivalent:</strong></td>
<td>2.00</td>
<td></td>
</tr>
<tr>
<td><strong>Total Number:</strong></td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

### Names of Post Doctorates

<table>
<thead>
<tr>
<th>NAME</th>
<th>PERCENT SUPPORTED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FTE Equivalent:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Total Number:</strong></td>
<td></td>
</tr>
</tbody>
</table>
### Names of Faculty Supported

<table>
<thead>
<tr>
<th>NAME</th>
<th>PERCENT_SUPPORTED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FTE Equivalent:**

**Total Number:**

### Names of Under Graduate students supported

<table>
<thead>
<tr>
<th>NAME</th>
<th>PERCENT_SUPPORTED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FTE Equivalent:**

**Total Number:**

### Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

- The number of undergraduates funded by this agreement who graduated during this period: ...... 0.00
- The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields: ...... 0.00
- The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields: ...... 0.00
- Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale): ...... 0.00
- Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering: ...... 0.00
- The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense: ...... 0.00
- The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields: ...... 0.00

### Names of Personnel receiving masters degrees

<table>
<thead>
<tr>
<th>NAME</th>
<th>Total Number:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Names of personnel receiving PHDs

<table>
<thead>
<tr>
<th>NAME</th>
<th>Total Number:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Names of other research staff

<table>
<thead>
<tr>
<th>NAME</th>
<th>PERCENT_SUPPORTED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FTE Equivalent:**

**Total Number:**
Scientific Progress

UT-Austin and AND have together demonstrated the following: (a) feasibility of wafer scale MoS2 fabrication (b) Transistors fabricated on CVD MoS2 monolayers that show highest reported mobility and DC performance along with highest reported $f_T$ and $f_{max}$ values and (c) working with Army Research, we have demonstrated complete physical characterization of the MoS2 monolayers by temperature dependent Raman and Photoluminescence spectroscopy, TEM, SEM and STM.

Technology Transfer

Initial stage of large area MoS2 growth feasibility and RF characterization methodology transferred from University to Company
Contract and Proposal Number: W911NF-14-P-0030

Contractor's name and address: Applied Novel Devices, Inc.
15844 Garrison Circle, Austin, TX 78717, USA

Title of the project: Low Power Monolayer MoS\textsubscript{2} Transistors for RF Applications

Contract performance period: Sep 1, 2014 to Feb 28, 2015

Period covered by this report: Sep 1, 2014 to Feb 28, 2015

Total contract amount: $149,999.67

Amount of funds paid by DFAS to date: $124,999.73

Total amount expended/invoiced to date: $149,999.67

Number of employees working on the project: 3

Number of new employees placed on contract this month: 0

Report Prepared by

Name: Rajesh Rao
Telephone Number: 512-287-9732
Email Address: rajesh.rao@appliednoveldevices.com
1. Project Objectives:

Atomically layered transition metal dichalcogenides The objective of this proposal is to demonstrate the feasibility of producing large area, single crystal monolayer Molybdenum disulfide (MoS$_2$) for high frequency applications. In order to be able to achieve this aim, this project is focused on three main components: (a) large area growth of high quality MoS$_2$ material, (b) the transistor fabrication on the MoS$_2$ monolayers and (c) DC and RF characterization of the transistors.

2. Project Approach:

We followed a two-pronged approach for fabrication of MoS$_2$ monolayers as needed for this project. While device quality films were fabricated with an established CVD MoS$_2$ process using solid source MoO$_3$ and S precursors for quick learning and device development, a novel wafer scale process was developed in parallel using large area Mo deposition followed by sulfurization at high temperatures.

Figure 1: (a) Schematic of the MoS$_2$ growth system using solid precursors, (b) top view of the crucible/substrate arrangement before growth, (c) top view of the crucible/substrate arrangement after growth showing regions of bulk and monolayer MoS$_2$ growth.

The MoS$_2$ atomic films on SiO$_2$/Si and Si$_3$N$_4$/Si substrates were prepared by the sulfurization of MoO$_3$ in alumina crucibles placed inside a quartz tube. The temperature of the furnace was
raised to 850 °C with temperature of sulphur end of the furnace at roughly 350 °C. The growth continues for 5 minutes at 850°C, after which the heater in the furnace was turned off and the N₂ flow rate was set to 200 sccm for cooling down. The schematic of the deposition system used for MoS₂ growth is shown in figure 1(a). The modularity of the system allows us to easily control the growth environment as well as provides ease of scaling up. Using this system, large single monolayer domains up to 100 micron edge lengths as well as pseudo-continuous single layer films a few hundred microns wide and few mm long have been synthesized. In figures 1(b, c) we schematically show the different regions of the substrate and there relation with respect to the position of the MoO₃ precursor before and after the growth process.

The transistor fabrication and device characterization leverages heavily from previous work on graphene devices. Using e-beam lithography, the active device region is defined and source and drain contacts are formed. Subsequently, a high-k dielectric is deposited as the gate dielectric and a gate metal is patterned and defined with e-beam lithography. Low temperature and RF characterization methodologies that were previously developed for graphene FETs were modified for MoS₂ FETs and used in this project with additional de-embedding structures.

Table I below shows the work plan for the various technical tasks in order to meet the project objectives. To align with the project objectives, the tasks have been split up into three major categories - (1) Material synthesis and characterization (2) Device fabrication and (3) Transistor Characterization.

<table>
<thead>
<tr>
<th>Task #</th>
<th>Technical Tasks</th>
<th>Phase 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Material synthesis and characterization</strong></td>
<td>1 2 3 4 5 6</td>
</tr>
<tr>
<td></td>
<td>CVD growth of large area single domain monolayer MoS₂ on Si-SiO₂</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Complete material characterization including defects</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Controlling size of dendritic region on monolayer MoS2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Controlling domain size of monolayer MoS2 films in CVD growth</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td><strong>Device fabrication and analysis</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Back gated devices to identify optimum source, drain contacts</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Top gated devices to identify optimum gate dielectric</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Device characterization on CVD grown MoS₂ with dendritic regions as intermediate contacts</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td><strong>Transistor Characterization for RF application</strong></td>
<td></td>
</tr>
</tbody>
</table>

Table I: Work Plan with tasks versus timeline

As shown in Table I, the first few runs of MoS₂ growth and device fabrication were preliminary runs to develop the process and the later runs were for device optimization.

3. Work Completed:

In this Phase 1 proposal, we had proposed five different goals focusing on fabrication of MoS₂ monolayers, device fabrication and transistor characterization. Table II below highlights the main goals and the work completed for each of the goals.
Task # | Goal Description | Work Completed
--- | --- | ---
1. | Growth of CVD Monolayer MoS\(_2\) domains | We have demonstrated both high quality and large area MoS\(_2\) monolayer depositions. Conventional CVD process has been developed to demonstrate a few mm scale large pseudo-continuous monolayer regions for transistor and RF device development. A novel process with sulfurization of deposited Mo has also been developed for large area wafer scale MoS\(_2\) fabrication.
2. | MoS\(_2\) Transistor Fabrication. | We have fabricated MoS\(_2\) monolayer FETs using e-beam lithography with a gate last process. High mobility (72 cm\(^2\)/V·sec) and good device characteristics have been demonstrated on both SiO\(_2\)/Si and Si\(_3\)N\(_4\)/Si substrates.
3. | Transistor characterization for RF performance | We have demonstrated intrinsic short-circuit current-gain cutoff frequency, \(f_T\), of 6.7 GHz and a maximum oscillation frequency, \(f_{\text{max}}\), of 5.3 GHz in 250 nm gate length \(L_g\) devices. For the first time, we have also demonstrated a common-source amplifier and an active frequency mixer using CVD monolayer MoS\(_2\).

**Table II:** Work completed for each of the goals outlined in the proposal.

4. **Results of research tasks carried out and milestones achieved:**

This section discusses the work performed on each of the individual tasks towards the project goals:

4.1 CVD of monolayer MoS\(_2\) with MoO\(_3\) and S precursors

High quality CVD MoS\(_2\) films were deposited on SiO\(_2\)/Si and Si\(_3\)N\(_4\)/Si substrates using the system described in Fig. 1. The growth rate of MoS\(_2\) film is a function of the local concentration of the precursors. By selectively masking the flux of the precursors, we were able to control the flow rate of the starting material to the target substrate resulting in pseudo-continuous monolayer regions in some areas of the substrate. Initial growth (at the beginning of the project) showed large areas of bulk MoS\(_2\) growth with relatively smaller areas of monolayer regions as shown in figure 2. Systematically studying the effects of various growth parameters (mentioned in earlier reports) allowed us to increase the ratio of area of monolayer region to bulk growth region on the target substrate. We have been able to show that large (> 100 microns edge length) individual domains as well as continuous monolayer regions in the mm x mm with high...
material and device quality can be achieved using this setup. Similar growth and material quality was obtained on different substrates including bare Si, Si-SiO$_2$ (285 nm) and Si-Si$_3$N$_4$ (90 nm).

Figure 2 shows SEM images of the deposited MoS$_2$ at different regions of the substrate as a function of distance from the source. It is clear that the location of the substrate has an influence on the MoS$_2$ deposition. Monolayers regions are seen on the substrate regions that are partially masked by the edge of the crucible. Figure 3 shows further characterization of an individual monolayer domain. High magnification SEM imaging is shown in Fig. 3(b). Atomic force microscopy (AFM), and Microwave Impedance Microscopy (MIM) and Raman spectroscopy as well as Photoluminescence (PL, 3e) mapping are also used for physical characterization of the domains. AFM shows the thickness of the films to be a single layer. However, it does appear that dendrite like structures that appear randomly distributed on the surface are roughly two-layers thick. MIM is a unique technique that allows us to map the dielectric response of the domains without any post-processing steps as well as in a non-destructive fashion. The bright spots on the MIM map which corresponds to the dendritic regions, tells us that the conductivity of those regions are much higher than the monolayer region. The quality of the film is ascertained using Raman and Photoluminescence mapping. The dendritic regions show a larger separation between the E peaks on the Raman maps while a quenched PL signal. These results are consistent with the optical properties of the dendritic regions being similar to bilayers.

![Figure 2: SEM images of MoS2 growth as a function of distance from the precursor. The right corner in the top panel (blue scale bar = 1mm) is a low magnification image with the region (D) being bare Si-SiO$_2$, and (A) being bulk growth. Somewhere between these two regions is the pseudo-continuous monolayer growth (C) while (B) indicates a region with the onset of ad-layer on top of the monolayer region (yellow scale bar = 100 μm).](image-url)
In order to increase the overall area of the monolayer region and minimize bulk MoS$_2$ growth, the direct vapor flux reaching the target substrate was blocked out with masking wafers. The masking wafer pieces were arranged to leave small openings that restricts the vapor flux reaching the growth substrate. Thus, the substrate regions exposed by the narrow openings received the direct vapor flux, while the rest of the substrate regions were blocked out. Figure 4 shows optical microscopy images of the target substrate after the growth. The regions exposed by the Si masks exhibit bulk growth, while regions at the edge of the openings exhibit large pseudo-continuous mono-layer growth, where different mono-layer domains are merged. Regions far away from the openings do not see any significant vapor flux and show no deposition. Figures 4(b) and (c) shows a region on the substrate where the monolayer growth region extends up to 1mm$^2$ in area. An isolated monolayer domain of approx. 100µm in linear dimension is shown in figure 4(d).

4.2 Physical Characterization of deposited MoS$_2$:

The quality of the material grown was characterized using multiple techniques. Some of this was done in-house, while others were done in collaboration with Dr. Madan Dubey’s team at the Army Research Laboratories.
Raman and Photoluminescence spectroscopy: The variation of optoelectronic properties of MoS$_2$ as a function of number of layers allows Raman and Photoluminescence spectroscopy to be used as standard tools to characterize the material quality. In our work we have used a combination of room temperature and low temperature Raman and PL mapping (collaboration with Dr Madan Dubey’s lab at ARL) to get an understanding of not only the monolayer regions but the different defect states as well.

It is well known that the peak separation between the in-plane ($E_{2g}^1$) and out-of-plane ($A_{1g}$) vibrations is a function of the number of layers. In figure 5(a), we note that the $E_{2g}^1$ peak is at 383.5 cm$^{-1}$ with the $A_{1g}$ at 403.1 cm$^{-1}$. This corresponds to a delta ($\Delta$) of 19.6 cm$^{-1}$, which is characteristic of CVD grown monolayer MoS$_2$. The full width at half maximum (FWHM) of the $E_{2g}^1$ and $A_{1g}$ peaks is an indicator of the material quality of the films, and for our samples they were 4.6 cm$^{-1}$ for the $E_{2g}^1$ peak and 5.9 cm$^{-1}$ for the $A_{1g}$ peak. $A_{1g}$ peak respectively, which is similar to that reported for other CVD grown MoS$_2$. The strong signal obtained from the PL spectroscopy [Fig. 5(b)] further confirms the existence of a direct band gap that is expected of monolayer MoS$_2$. The strong peak at around 669 nm (1.85 eV) and a much smaller peak at around 623 nm (1.99 eV) corresponds to the A and B excitons and is similar to those observed for exfoliated monolayer MoS$_2$.

![Figure 5: Room temperature (a) Raman and (b) Photoluminescence spectra of CVD grown MoS$_2$. The Raman peak separation of around 19 cm$^{-1}$ and the strong PL signal with a peak around 669 nm is characteristic of monolayer MoS$_2$.](image)

The low temperature Raman studies shown in figure 6(a), shows slight shifting of the peaks and only very little changes in the separation of the peaks. However, the PL spectra at low temperatures (figure 6b) shows significant differences as compared to room temperature. Besides the B excitonic peak becoming much stronger there seems to be a new peak arising at around 1.7 eV that has not been reported before. We are currently working on understanding this phenomenon.

Although most of the work on this project has focused on the growth and characterization of monolayer MoS$_2$, we have been able to obtain multilayer stacked MoS$_2$ by controlling the heating and cooling rate during the growth process. One such domain is shown in figure 7 (a).
As is expected, the separation between the Raman peaks decrease and the intensity of the PL signal increases with lesser number of layers as shown in figure 7 (b, c). However, one of the possible applications for layered MoS$_2$ is in the field of flexible electronics and it is therefore important to understand how strain affects its material properties.

Figure 6: Low temperature vs room temperature (a) Raman and (b) PL spectra of monolayer MoS$_2$. The Raman peaks do not show much change with lower temperature except a slight red shifting. However, for the PL spectra the B excitonic peak round 2 eV is shifted and stronger. And a strong peak also appears at around 1.7 eV.

Figure 7: (a) A stacked multilayer CVD MoS$_2$ domain. (b) Raman spectra obtained from different layers showing the dependence of the spectra on the film layer thickness (c) PL spectra showing the same variations as in (b).

In figure 8(a) we show the same domain shown in figure 7(a) after being transferred on to a flexible substrate. Figure 8(b) shows the experimental setup used for learning about the effects of strain on the MoS$_2$ transferred on to the flexible substrate. Figure 8 (c, d) show the effect of strain on the Raman and PL spectra on a single point of this domains (pt 3 as shown in figure 7a). Figure 8 (e, f) shows the same effects for different layer thicknesses. These results that are shown here for the first time on CVD grown MoS$_2$ are in contrast to what is seen for exfoliated MoS$_2$ and might point to significant material property differences between the two. The change
in the PL peak points to a small change in bandgap with increasing strain. This effect is more pronounced in multi-layer MoS$_2$. This suggests that the changing strain in flexible multi-layer devices can influence the device characteristics by modulating the band gap.

**Figure 8:** Strain study on vertically grown MoS$_2$ layers. The triangle shown in Figure 7 (a) was transferred onto flexible PET shown in (a). The yellow arrow shows the approximate direction of applied strain. (b) The strain is applied by bending the PET by pressing two plates together using micrometers. (c) and (e) show changes in Raman and PL for pt 3 as a function of stress. The position of the E' or E$_{2g}^\prime$ Raman peak is shown in (d) and the A exciton energy of the PL is shown in (f), respectively. It can be seen that while the E' Raman peak for monolayer only changes by about 1-2 wavenumbers, the change is much more drastic for multi-layers.

**Figure 9:** HR-TEM image of mono-layer MoS$_2$. Inset shows Selected Area Diffraction from the same region.

Transmission Electron Microscopy: TEM was used in order to visualize the crystallinity of the CVD-MoS$_2$. Figure 9 (a) shows the FFT filtered TEM image of mono-layer MoS$_2$, while the inset shows the selected area diffraction (SAD) of the same region. The hexagonal lattice structure and the lattice spacing of 0.27 nm is as expected from crystalline MoS$_2$. 
4.3 Wafer Scale Growth of MoS$_2$

A route to obtain electronic device quality monolayer MoS$_2$ in the wafer scale is being pursued. This two step process involves the deposition of a thin Mo film on a suitable substrate using electron beam evaporation followed by annealing the film in a sulfur rich atmosphere. Four inch diameter Si wafers were cleaned and a 3500Å thick SiO$_2$ layer was formed over some of the wafers. Mo films of different thicknesses were then evaporated onto these wafers. The wafers were then cleaved into smaller pieces and heated in a sulfur ambient at 850°C. Initial material characterization of the films has been done using Raman spectroscopy and TOF-SIMS. The Raman spectra of the films after sulfurizing is shown in figure 10 as a function of initial Mo thickness. Two peaks are observed for both samples corresponding to MoS$_2$. The peak shift with Mo thickness indicates the trend towards monolayer MoS$_2$ with decreasing Mo thickness. For comparison, the raman spectra from a conventional CVD monolayer MoS$_2$ is overlaid in the same plot.

![Raman Spectra](image)

Figure 10: (a) Comparison of Raman signals obtained from CVD monolayer MoS$_2$ (dashed line) versus MoS$_2$ obtained by sulfurization (solid line) of different thicknesses of evaporated Mo films on SiO$_2$/Si substrates. The thickness of the deposited Mo is shown in the legend. (b) TOF-SIMS analysis after direct sulfurization of evaporated 10nm Mo film on bare Si substrate.

In order to understand the thickness of the different layers and depth penetration of S in the films, we analyzed the samples with Time Of Flight- Secondary Ion Mass Spectroscopy (TOF-SIMS). Direct sulfurization of as deposited Mo film results in bulk MoS$_2$ on top of a MoO$_x$-SiO$_x$ layer on Si. Thickness control of the starting Mo film is crucial to form only a few layers of MoS$_2$.

4.4 CVD of monolayer MoS$_2$ on Si$_3$N$_4$/Si substrates

Most of the mono-layer MoS$_2$ growth reported so far has been obtained on 285nm SiO$_2$/Si substrates. As part of this project we are also exploring the suitability of other substrates. During this month, the work was focussed on Si$_3$N$_4$ substrates as it offers superior insulating
qualities over thermal oxide, such as reduced leakage and higher breakdown voltages. Furthermore, for the gate first integration, the nitride substrate would act as a good etch stop layer for the gate stack etch. Additionally, it serves as a better diffusion barrier against moisture and metal ions. Preliminary growth on Si$_3$N$_4$ is very similar to that achieved on thermal oxide with comparable domain sizes and material quality. Figure 11 shows the optical micrographs of monolayer MoS$_2$ domains on Si$_3$N$_4$ substrate. The figure also compares the Raman and PL spectra on SiO$_2$ and Si$_3$N$_4$ substrates. As seen in the figure while the film growth is very similar on both substrates, the narrower peaks in the Raman spectra for the film grown on nitride indicates slightly better crystallinity compared to the film grown on oxide substrate [Fig 11(b)]. The PL spectra shown in Fig 11 (c) indicates a shift to slightly higher wavelengths on the nitride substrate, suggesting a slightly lower bandgap for the film on nitride. Further characterization is underway to better understand the growth on both substrates.

![Figure 11. Growth of monolayer MoS$_2$ on Si$_3$N$_4$/Si substrate (a) optical micrographs showing individual domains (top) and pseudo-continuous regions (bottom). Material characterization using (b) Raman and (c) PL spectra.](image)

4.5 MoS$_2$ transistors RF performance characterization:

Top-gated CVD MoS$_2$ FETs in the ground-signal-ground (GSG) layout for high-frequency characterization were fabricated as follows. Monolayer MoS$_2$ domains grown on highly resistive Si/SiO$_2$ substrates were identified using a combination of optical contrast, Raman spectroscopy, and atomic force microscopy (AFM) images. Device active regions were defined using e-beam lithography (EBL). Excess MoS$_2$ was etched using Cl$_2$ plasma. Next, source/drain metal electrodes were defined with EBL. A stack of Ag/Au (20 nm/30 nm) was deposited as low-work function (4.26 eV) source/drain metal electrodes to enhance n-type conduction of the MoS$_2$ FET. Atomic layer deposition (ALD) was used to deposit a 30 nm thick layer of HfO$_x$ as the top gate dielectric. The top gate electrode was then defined using a final EBL step. The top gate metal fingers were deposited as 50 nm of Ni. Figure 12(a) shows an optical image of the final device structure in the GSG configuration used in high frequency measurements. Figure 12(b) shows a cross-sectional schematic of the GSG MoS$_2$ FET. The gate length ($L_g$) of all our
devices was 250 nm, and was verified using AFM after device fabrication. Underlap regions of 100 nm were left on either side of the gate to prevent parasitic source/drain capacitances. Measurements presented in this paper were taken in ambient.

Figure 12. RF MoS\textsubscript{2} FET layout and structure. (a) Optical image of a CVD MoS\textsubscript{2} FET in the ground-signal-ground structure (GSG) required for high frequency measurements. The inset shows a zoomed in layout of a device with \( W = 20 \mu m \) and \( L_g = 250 \text{ nm} \). (b) Cross-sectional view of the MoS\textsubscript{2} transistor highlighting the underlap regions to eliminate parasitic capacitances.

Figure 13(a,b) shows the \( I_{ds}-V_{gs} \) transfer characteristics and \( I_{ds}-V_{ds} \) output characteristics of a monolayer MoS\textsubscript{2} FET with a width, \( W \), of 20 \( \mu m \). The device achieves current densities of 200 \( \mu A/\mu m \) at \( V_{gs} = 5 \) V and \( V_{ds} = 3.5 \) V. The threshold voltage (\( V_{th} \)) is around -9 V, indicating unintentional n-type doping of the MoS\textsubscript{2} during growth or fabrication. This is common for both CVD and exfoliated MoS\textsubscript{2} devices, intrinsically caused by sulfur vacancies in the MoS\textsubscript{2} and extrinsically by doping sources such as uncompensated interfacial Hf atoms at the MoS\textsubscript{2}–HfO\textsubscript{x} interface. These uncompensated Hf atoms lead to the creation of donor states near the conduction band of monolayer MoS\textsubscript{2} resulting in n-type charge transfer doping [23]. The Hf:O ratio in our ALD HfO\textsubscript{x} film was determined to be \(~ 1:1.75\) from x-ray photoelectron spectroscopy (XPS), thereby confirming the oxygen deficiency. Furthermore, the doping of the MoS\textsubscript{2} channel upon ALD HfO\textsubscript{x} encapsulation was confirmed by the red shift and peak broadening of the out-of-plane A\textsubscript{1g} Raman mode of MoS\textsubscript{2}. It can be surmised that this doping caused by the overlying HfO\textsubscript{x} film is primarily responsible for the enhanced performance of our CVD MoS\textsubscript{2} FETs. The inset of Figure 3(a) shows the \( g_{m}-V_{gs} \) transconductance curves for our CVD MoS\textsubscript{2} FET. The device achieves a maximum \( g_m \) of 38 \( \mu S/\mu m \) at \( V_{gs} = -4.5 \) V and \( V_{ds} = 3.5 \) V. Using the \( I_{ds}-V_{gs} \) transfer curves at a low-field \( V_{ds} \) of 0.01 V and a TMD FET model, we extract estimates for mobility and contact resistance to be \( \mu_{FE} = 55 \text{ cm}^2/\text{Vs} \) and \( R_c = 2.5 \text{ k}\Omega \cdot \mu m \), respectively. To investigate further, a four point (4pt.) CVD MoS\textsubscript{2} FET (\( L = 4 \mu m \), \( W = 5 \mu m \)) was fabricated in parallel. From this 4pt. device a \( \mu \) of 72 cm\textsuperscript{2}/Vs and an \( R_c \) of 2 k\( \Omega \cdot \mu m \) were extracted. These values are better than those extracted from the RF device due to accurate removal of parasitic contact and access resistances.
Figure 13. CVD MoS$_2$ DC characterization. (a) $I_{ds}$-$V_{tg}$ transfer curves of a CVD MoS$_2$ RF FET. The current density exceeds 200 $\mu$A/$\mu$m at $V_{gs} = 5$ V and $V_{ds} = 3.5$ V. The inset is the $g_m$-$V_{tg}$ transconductance curves. The peak $g_m$ is 38 $\mu$S/$\mu$m biased at $V_{gs} = 5$ V and $V_{ds} = 3.5$ V. (b) $I_{ds}$-$V_{ds}$ output curves of a CVD MoS$_2$ RF FET. The $V_{ds}$ is swept from 0 V to 4 V with different $V_{tg}$. The $V_{tg}$ is swept from -5 V to 5 V in steps of 1 V. These curves are used to find the minimum drain conductance $g_{ds}$ from which the voltage gain $A_v = g_m/g_{ds}$ is determined.

The radio frequency performance of CVD MoS$_2$ can be evaluated from the transit frequency $f_T$. The frequency at which the $|h_{21}|$ current gain reaches 0 dB is the $f_T$ of the device. In order to measure this value, an Agilent Microwave Network Analyzer (VNA-E8361C) was used for RF characterization in the range of 100 MHz to 10 GHz. To determine the intrinsic frequency performance of CVD MoS$_2$ FETs, standard OPEN and SHORT structures were used to de-embed parasitic capacitances and resistances. These structures were fabricated in close vicinity to the device-under-test (DUT) on the same substrate with identical layouts. The as-measured S-parameters were extracted from a monolayer CVD MoS$_2$ device with $L_g = 250$ nm and $W = 20$ $\mu$m (Figure 14(d)). The short circuit current gain $|h_{21}|$ vs. frequency plot is shown in Figure 14(a). Operating at $V_{gs} = -4.5$ V and $V_{ds} = 3.5$ V corresponding to the maximum $g_m$ point, the device extrinsic $f_T$ is measured to be 2.8 GHz. After applying de-embedding parameters, the intrinsic $f_T$ reaches 6.7 GHz. The devices show good linearity with the expected -20 dB/dec slope. To our knowledge, this is the largest reported $f_T$ for CVD MoS$_2$. A higher $f_T$ can be achieved by improving the $g_m$ (by shortening the $L_g$), optimizing the layout to reduce parasitic capacitances, and by reducing the contact resistance. From the maximum $f_T$ obtained, the carrier saturation velocity $v_{sat}$ is estimated to be $\sim 1.1 \times 10^6$ cm/s. This result is consistent with a theoretical estimates of monolayer MoS$_2$ saturation velocities.

Another figure of merit for high-frequency transistors is the maximum frequency of oscillation, $f_{max}$. This is the frequency limit at which there is voltage gain given perfect input and output matching. The $f_{max}$ of a FET depends on the drain conductance $g_{ds}$, which in turn depends on the saturation characteristics at the device operating point. The unity maximum available gain was obtained from the measured S-parameters and is shown in Figure 14(b). Operating at the same DC bias point, we measure an extrinsic $f_{max} = 3.6$ GHz. Using the same de-embedding procedure, the intrinsic maximum oscillation frequency is extracted to be $f_{max} =$
5.3 GHz. To our knowledge, this is the highest reported \( f_{\text{max}} \) for CVD MoS\(_2\). The \( f_{\text{max}} \) can be further improved by operating the device in deeper saturation to reduce \( g_{\text{ds}} \), and by using a thicker gate metal to reduce gate resistance.

**Figure 14.** CVD MoS\(_2\) frequency performance of a device with \( L_g = 250 \) nm operating at the peak \( g_m \) point. (a) Short circuit current gain \(|h_{21}|\) vs. frequency showing an extrinsic \( f_T \) of 2.8 GHz and an intrinsic \( f_T \) of 6.7 GHz. The device shows good linearity with the expected -20 dB/dec slope. (b) Maximum frequency of oscillation \( f_{\text{max}} \) vs. frequency showing an extrinsic \( f_{\text{max}} \) of 3.6 GHz and an intrinsic \( f_{\text{max}} \) of 5.3 GHz. (c) Voltage gain \( A_v \) expressed in \( Z \)-parameters as \( A_v = Z_{21}/Z_{11} \) vs. frequency. The \( A_v \) is 6 dB at the minimum frequency 100 MHz and voltage gain is realized until 3 GHz. (d) S-parameters extracted from a CVD MoS2 FET with 250 nm channel length.

In amplifier design, it is important to know the intrinsic voltage gain \( A_v \). The intrinsic voltage gain can be extracted from DC measurements as \( A_v = g_m/g_{\text{ds}} \). The voltage gain can also be measured as a function of frequency by converting the S-parameters to impedance \( Z \)-parameters. Figure 14(c) shows the measured extrinsic and intrinsic voltage gain \( A_v = Z_{21}/Z_{11} \). At 100 MHz, the extrinsic voltage gain is equal to 6 dB and voltage gain is realized until a
frequency of 3 GHz. This voltage gain exceeds those of graphene RF devices due to the inherent bandgap present in MoS$_2$.

A preliminary common source (CS) amplifier was implemented using our monolayer CVD MoS$_2$ FETs. The schematic of the CS amplifier is shown in Figure 15(a). A RF input ($V_{in}$) is applied to the gate terminal of the FET and the drain output ($V_{out}$) is connected to an oscilloscope (1M$\Omega$ load). Bias tees were used for feeding the DC bias and AC signals. The MoS$_2$ FET is biased at the same maximum transconductance point ($V_{gs} = -4.5$, $V_{ds} = 3.5$). Applying an input sine wave at 135 kHz we measure a voltage gain ($A_v = V_{out}/V_{in}$) of 10.5 dB. These measurements were carried out using DC probes for demonstration of analog circuits. With proper RF impedance tuners and noise matching circuits we expect operation of low noise amplifiers (LNAs) in the GHz range. The gain of amplifier is slightly lower than expected due to the large contact resistance and Miller capacitance. A cascode topology and an optimized layout would mitigate these effects, giving improved performance.

![Figure 15. Implementation of common-source amplifier using CVD MoS$_2$. (a) Implementation of a common-source (CS) amplifier using CVD MoS$_2$. (a) Schematic for a CS amplifier showing the input applied to the gate and the output at the drain using bias tees to set the DC operating point. (b) Applying an input sine signal at 135 kHz with a peak-to-peak voltage $V_{pp} = 0.2$ V, we measure an output signal of $V_{pp} = 2.3$ V. This corresponds to a voltage gain $A_v = 10.6$ dB.](image)

5. Conclusions:

During this phase of the project, we have demonstrated the following:

- Highest $f_T$ (6.7 GHz) and $f_{max}$ (5.3 GHz) reported for CVD MoS$_2$ FETs
- High quality monolayer MoS2 by conventional CVD extending to mm scale pseudo-continuous monolayer regions
- A high mobility of 72 cm$^2$/Vs and an $R_c$ of 2 k$\Omega$·$\mu$m for CVD MoS$_2$ monolayer FETs.
- A scalable process for fabricating MoS$_2$ using sulfurization of deposited ultra thin Mo films.
- Complete physical analysis of CVD MoS$_2$
6. Recommendations

CVD MoS$_2$ has shown the potential to meet the RF performance requirements of this project. Based on our learning from this phase of the project we have the following recommendations to accelerate the RF performance improvement efforts:

(1) MoS$_2$ Deposition: The novel wafer scale deposition process should be optimized for high quality uniform MoS$_2$ deposition. The MoS$_2$ fabrication process should be developed for uniform deposition of multilayer MoS$_2$ films.

(2) Transistor Fabrication: The MoS$_2$ FET fabrication process should be developed to use a gate first approach to protect the gate stack interfaces and should also include doping of MoS$_2$ using TiO$_x$ or other charge transfer mechanisms to minimize parasitic access resistance and improve performance.

(3) RF Performance: RF transistors should be fabricated on multi-layer MoS$_2$ with optimal doping to obtain higher mobility and better device performance.

(4) Defect Characterization: Characterization of defects and dendritic structures on MoS$_2$ should be carried out to improve device performance and understand the difference in quality of CVD MoS$_2$ vs exfoliated MoS$_2$.

7. Short Abstract of Proposed Follow On Research and Development

In Phase II we propose to optimize wafer scale MoS$_2$ deposition process to fabricate uniform large area monolayer and multi-layer MoS$_2$ films and analyze the defects on these films. Monolayer regions that can result in device periphery larger than 50µm will be targeted. Further, the charge transfer doping process using TiO$_x$ will be optimized for MoS$_2$ multi-layer and RF transistors will be fabrication on these multilayers. The device structure (geometry, length of underlap region, choice of gate dielectric, gate and contact materials) will be optimized to meet DC and RF performance targets of this solicitation. The transistors will be targeted to show an RF performance of $f_{\text{max}} > 20$GHz.