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14. ABSTRACT

The purpose of this Internal Rapid Experimentation (IRE) is to develop a Gallium Nitride (GaN) replacement for 10kW Traveling Wave Tube (TWT). A phased approach will be used to develop a solid state replacement for the TWT. Phase I covered by this IRE, was to do market research on commercially available GaN transistors as a substitute for traveling wave tubes in high power radar and Electronic Warfare (EW) applications. GaN transistors, using evaluation boards, were tested and analyzed, supplementing and compared against the data found on the vendor's data sheet. Using vendor models of selected transistors, an initial design approach and architecture was developed using Keysight ADS software. Simulations were run for comparison against vendor data sheets and the test data collected.

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10kW TWT Transition to GaN IRE

Prepared for: S&T Working Group Chairs

Prepared by:
Naval Surface Warfare Center, Crane Division
Global Deterrence & Defense Department
Radar Technologies Division
Systems Engineering Branch
Crane, IN 47522-5010

Points of Contact:
Mark Schaefer, 812-854-3566
Jeremiah J. Robbennolt, 812-854-1204
Rob Bechtel, 812-854-6437
GXR, Bldg 3168

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RADAR TECHNOLOGIES DIVISION

INTERNAL REVIEW SHEET

Document Title	10kW TWT Transition to GaN IRE
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	Person	**Date**
Technical Points of Contact	Rob Bechtel Jeremiah J. Robbennolt Mark E. Schaefer	
Branch Manager	Tony Peters Dedric Dennist	
Division Chief Engineer	John P. Schofield	
Division Quality Focal Point	Daniel Hunter	
Division Manager	Roger A. Becker	

Executive Summary

The purpose of this Internal Rapid Experimentation (IRE) is to develop a Gallium Nitride (GaN) replacement for 10kW Traveling Wave Tube (TWT). A phased approach will be used to develop a solid state replacement for the TWT. Phase I covered by this IRE, was to do market research on commercially available GaN transistors as a substitute for traveling wave tubes in high power radar and Electronic Warfare (EW) applications. GaN transistors, using evaluation boards, were tested and analyzed, supplementing and compared against the data found on the vendor's data sheet. Using vendor models of selected transistors, an initial design approach and architecture was developed using Keysight ADS software. Simulations were run for comparison against vendor data sheets and the test data collected.

The team was successful in all facets of Phase I of this IRE. The initial design approach and architecture was developed using Keysight ADS and are provided in sections 3.1.2 & 3.1.3. Simulations were run to verify the test data taken from the CREE transistors with results can be reviewed in sections 3.1.4 and 3.1.5. Testing and evaluation of the selected transistors from CREE was performed and data captured. The data captured, analyzed and compared favorably with both the vendor data sheet and model. The results of the test analysis are provided in sections 4.1.3 and 4.1.4. The primary objective of this data collection and analysis was to determine the feasibility of using COTS transistors to develop a solid state replacement for a TWT. The results of this IRE provide proof that, not only is it a very feasible option, but it would be tragic not to investigate and develop further with follow-on efforts.

Our technical team recommends proceeding with a Phase II Internal Rapid Experimentation for this effort. The recommended tasking included in Phase II is to design, develop and simulate a model using Keysight ADS. The model developed would be for a sub-module capable of achieving greater than 1kW of output power. Using the model, a prototype of the sub-module and bias board shall then be fabricated and tested using bench-top test equipment very similar to those used in Phase I. The test data taken will then be compared to the simulation data to validate the model. Following the successful completion of Phase II, there is further effort that could be done to prepare the 10kW TWT transition to GaN for sponsorship by a Program Office. Phase III of this effort would align to a NISE 219 project due to the amount of funding required for thermal modeling and analysis, FEA, modeling & simulation of prototype 10kW GaN amplifier, acquisition cycle for components, prototype assembly and final test.

Table of Contents

List of Tables

List of Figures

1. **Overview**

Supportability of microwave tubes is a challenging issue because of reliability, maintenance burden, and diminishing manufacturing sources. A few Program Offices have already begun investigating replacement of TWTs with solid state technology. For example, PEO-IWS researched replacing the Klystron on the SPS-49 radar with GaN technology. Recent design contracts have been completed on a solid-state amplifier replacement for the Band 4 & 5 tubes in ALQ-99. GaN technology offers several benefits over traveling wave tubes including; improved reliability, reduced maintenance burden, and smaller mechanical footprint. Traveling wave tube replacement with solid state technology has the potential to have game changing impact for the warfighter. Specifically for airborne applications, the reduced footprint and lower voltage requirements would certainly benefit high power requirements on air platforms. The surface and shore applications are already moving toward solid state solutions as can be seen with programs such as AMDR, SEWIP Block 3, Space Fence, AN/TPY-2 and G/ATOR. The medium to long term warfighter impact is improved reliability and reduced maintenance burden. The predicted reliability of GaN based high-power amplifiers have the potential to improve on TWTs by an order of magnitude. Developing and maintaining Government Subject Matter Expert understanding will break the continued reliance on defense contractors for expertise and design knowledge.

1.1. **Scope**

This document provides a phased approach used to develop a solid state replacement for a traveling wave tube. Phase 1 covered by this IRE is to do market research on commercially available GaN transistors as a substitute for traveling wave tubes in high power radar and EW applications. GaN transistors and evaluation boards were tested and analyzed, supplementing and compared against the developed model and the vendor's data sheet. A preliminary architecture model was developed to notionally depict the design approach. Simulations were run on the model to validate against the test data and vendor data sheets. The remaining phases will include detailed amplifier and high power combining design, thermal management design, finite element analysis, waveform test and analysis, and modeling and simulation.

1.2. **Purpose**

The purpose of this document is to detail the research, analysis, and testing performed during Phase I of the 10kW TWT Transition to GaN Internal Rapid Experimentation.

1.3. **References**

a. 89 ADM 10 1111   Workflow Operational Procedure

b. NSWCCRANEINST 5100.1   Occupational Health and Safety Program

c. 12255-8843-940026   Training Plan

d.	Microwave Engineering 2nd, Pozar, David M., Copyright © 1998, by John Wiley & Sons, Inc.	Design of Microwave Amplifiers and Oscillators, Ch 11
e.	Microwave Technology & Computational Electromagnetics (ICMTCE), 2011 IEEE International Conference, May 2011	An X-band high power pulsed amplifier with high efficiency based on radial waveguide spatial combining technique, Chen, H.
f.	Power Modulator Symposium, 1990, IEEE Conference, June 1990	Power Supply Considerations for Pulsed Solid-State Radar, Gardenghi, R.A.
g.	Microwave Journal, May 2014	GaN-on-Diamond: The Next GaN, F. Ejeckam, D. Francis, F. Faili, F. Lowe, J. Wilman, T. Mollart, J. Dodson, D. Twitchen and B. Bolliger, Element Six Technologies and D. Babic, University of Zagreb
h.	CREE Transistor Data Sheet	CGHV35400F: 400 W, 2900 - 3500 MHz, 50-Ohm Input/Output Matched, GaN HEMT for S-Band Radar Systems

1.4. Background

The transition to solid state technology away from traveling wave tubes is already happening. Many emerging systems are using GaN technology for the high power RF applications. For example, Air and Missile Defense Radar (AMDR), Surface Electronic Warfare Improvement Program (SEWIP) Block 3, Space Fence and Ground/Air Task Oriented Radar (G/ATOR) are just a few examples of radar and electronic warfare moving away from tube based systems. NSWC Crane is already the center of excellence for vacuum electron device test and repair. If the workforce is going to continue to grow, maintaining expertise in these aging systems, technology insertion needs to be addressed sooner rather than later. If we wait until the replacement devices are being designed by defense contractors the expertise will always reside with the OEM and vendor lock will be unavoidable. Keeping the expertise and knowledge base within the government will support a competitive environment amongst contractors. Moreover, maintaining organic expertise will allow for supportability options within the government driving down future O&S costs.

2. Safety Concerns

There are no exclusive safety concerns with this test set-up and execution

3. **Modeling and Simulation**

The majority of GaN transistor manufacturers provide device models for their products and were made available from CREE for all the transistors researched for this effort. Modeling and simulation will facilitate in verifying product performance and potential use in more complex amplifier architectures to obtain the power level of a TWT. Electronic Design Automation (EDA) tools such as Keysight's Advanced Design System (ADS) will be used to validate simulation performance versus measurement and will aid in the design and analysis.

3.1. **Initial Design Concept and Architecture**

3.1.1. **Market Research Findings**

Criteria used for market research was limited to GaN transistor technologies, frequency range, power out capability, and device packaging. Majority of commercially available GaN transistors utilized GaN on SiC (Silicon Carbide). SiC is the host substrate for the GaN and has a thermal conductivity range of 390-450 W/m-K. Previous generation GaN transistor used Si (Silicon) as the host substrate which has a smaller thermal conductivity in the range of 135-150 W/m-K. This translates to allowing better thermal management in the transistor device. Current research is looking at GaN on diamond to decrease the thermal limitations of current generation devices and increase power out capability. Diamond's thermal conductivity ranges in the low 1000s W/m-K.

S-band TWT replacement was the focus of this research and therefore the market research limited the frequency range to cover at least 3.0 to 3.5 GHz.

Power out capability and device packaging were criteria used to decrease the design risk associated with building up amplifier stages to meet the high power capability of TWTs. Using transistors with the highest power out capability decreases component count and inherently increases reliability. This also decreases total system footprint. In addition, using packaged transistor devices minimizes the extra design step in having to integrate the GaN transistor die into a package. If not done right this could lead to yield issues. Table 1 provides the manufacturer and device information researched based on the above criteria.

Table 1. Market Research Results as of Jan. 24th, 2015

Vendor/OEM	Device Part Number	Frequency Range (GHz)	Drain Voltage (V)	Power Out Capability (Watts)
NXP Semiconductor	CLFG0035-100	0 – 3.5	50	100
M/A-COM	MAMG-002735-085L0L	2.7 – 3.5	50	85

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Vendor/OEM	Device Part Number	Frequency Range (GHz)	Drain Voltage (V)	Power Out Capability (Watts)
M/A-COM	MAGX-003135-120L00	3.1 – 3.5	50	120
Qorvo (Triquint & RFMD)	T1G4020036-FL	0 – 3.5	36	260
Qorvo (Triquint & RFMD)	TGF2819-FL	0 – 3.5	32	126
Qorvo (Triquint & RFMD)	RF3934	0 - 3.5	48	120
Microsemi	3135GN-170M	3.1 – 3.5	60	170
CREE	CGHV35150	2.9 – 3.5	50	150
CREE	CGHV35400F	2.9 – 3.5	45	400

Cree's CGHV35400F device was selected due to it having the highest power out capability at 400 W. In addition, the size of the device is approximately 0.945 inches by 0.685 inches and is fully matched to 50 Ohms. Having a small footprint and being fully matched to 50 Ohms at our frequency of interest reduces the Non-Recurring Engineering (NRE) costs associated with designing board level matching networks for system impedance matching and it allows for tighter integration with system footprint constraints.

3.1.2. Design Approach

RF models of the CGHV35400F device are available for Keysight's Advanced Design System (ADS) software which will be used to design the prototype TWT replacement. ADS is a circuit & Electromagnetic (EM) simulator used to design complex RF & Microwave printed circuit boards (PCB). Cree's CGHV35400F model is based on a 6-port large signal capable model. These ports include access to gate, source, drain, temperature, intrinsic drain voltage, and intrinsic drain current information of the device. The intrinsic voltage and current information allows for waveform engineering in designing highly efficient power amplifier architectures. Figure 1 illustrates the large signal model.
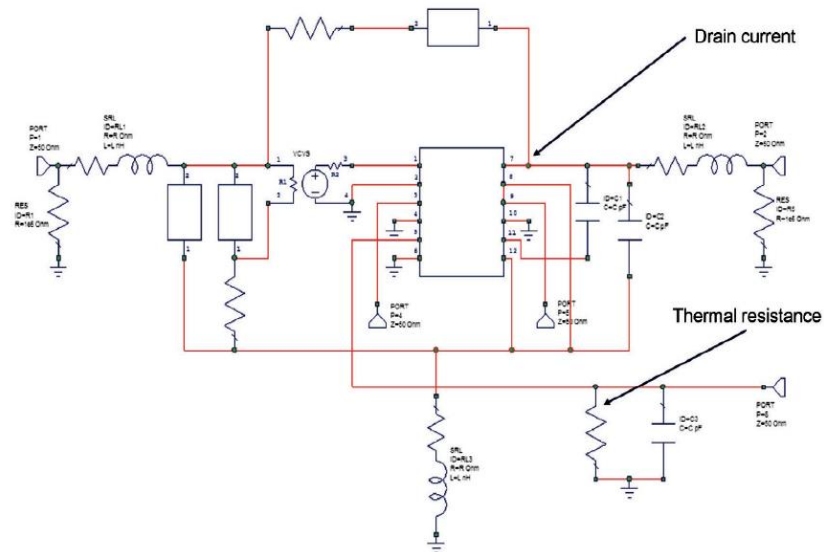
Figure 1. Large-signal model schematic

In addition to RF models, an evaluation circuit board and fixture were available to facilitate the development of a prototype amplifier. This test fixture also provides the basis for validation of the RF circuit model versus actual performance measurements using network and real time spectrum analyzers.

The CGHV35400F device will be simulated and characterized. Data will be used to determine power out capability and help determine the quantity of GaN devices needed to develop a 10kW TWT replacement. Figure 2 shows the schematic generated in ADS for simulation.
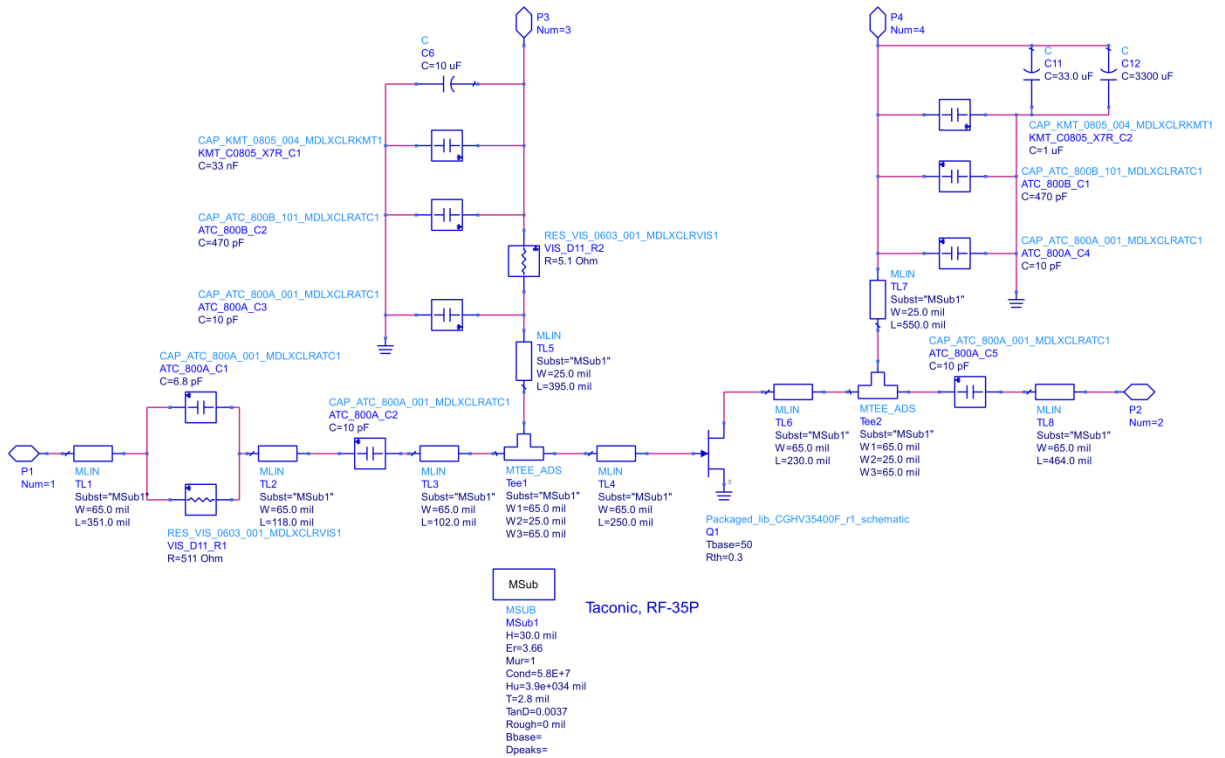
Figure 2. ADS schematic of evaluation fixture

Two simulations were run on the above schematic. The first simulation used ideal passive components whereas the second simulation used component models from Modelithics, Inc. Modelithics provides accurate, scalable measurement-based models for RF, microwave and millimeter-wave components from various manufacturers. A bill of materials was provided with the Cree test fixture but component values and manufacturers could not be verified. Components chosen for the second simulation were based on familiarity with certain manufacturers and past performance. Figure 3 shows the simulation setup in ADS.

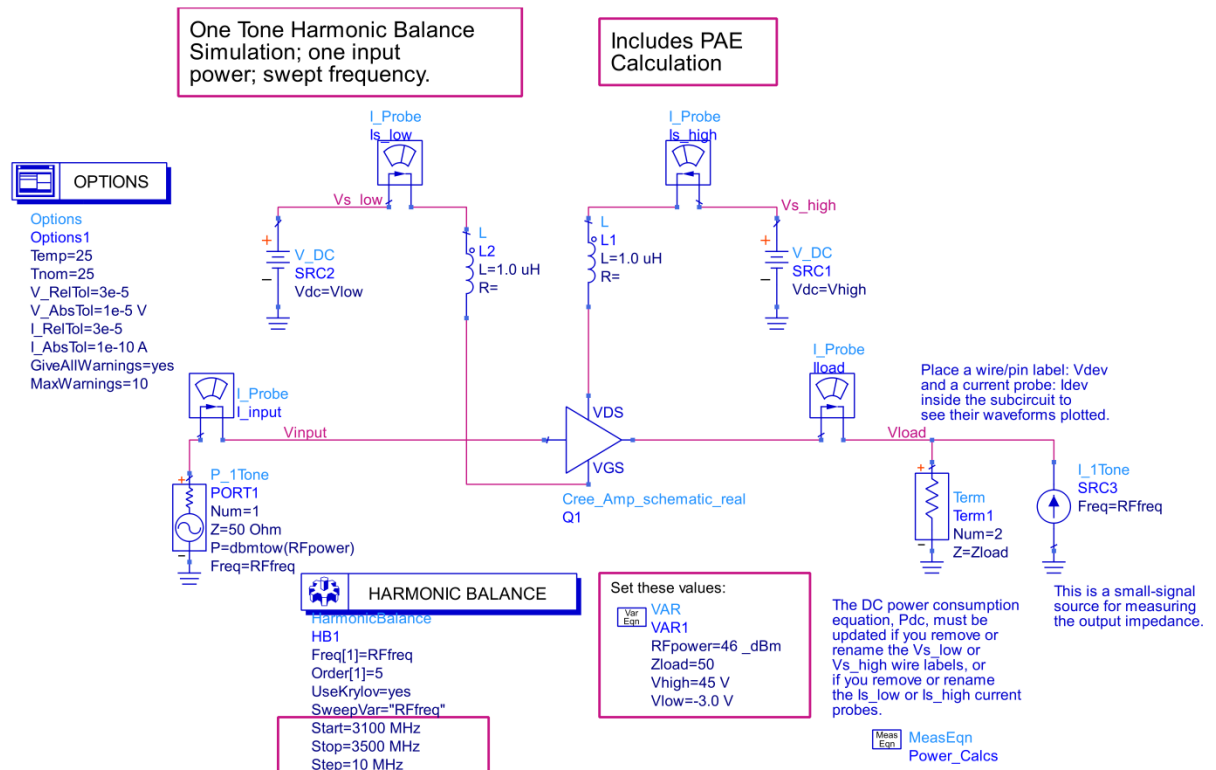*Harnessing the Power of Technology for the Warfighter*

Figure 3. ADS CREE evaluation board simulation

The ADS simulation uses Harmonic Balance which is a frequency-domain analysis technique for simulating nonlinear circuits and systems. The simulation calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit.

3.1.3. Design Architecture

To achieve 10 kW output power, amplifier stages utilizing Cree's CGHV35400F device would need to be combined in parallel. Theoretically, it would take twenty-five CGHV35400F devices combined coherently to obtain 10 kW. In reality, there are losses associated with various combining architectures, protection and monitoring circuits. There are three combining schemes typically employed; corporate, radial, and spatial. Corporate combining will typically be done with hybrid couplers and/or Wilkerson's combiner circuits. In terms of design risk, the impact is low due to the availability of COTS solutions but this technique will suffer the most loss and thus increase the amplifier component count. Radial combiner uses waveguide structures to efficiently combine up any number of ports needed. The ports are equally spaced around the output of the combiner. This structure incurs minimal loss. The design risk is medium due to complexity of the design of the waveguide structures and the machining needed to manufacturer. In addition, the footprint can be large depending on the number of amplifiers needed to combine. Spatial combining is similar to radial but the combining is done in free space within a machined cavity. Each amplifier module would need an antenna to radiate in the cavity and a probe feed would be placed such that the radiated

power would combine coherently at the probe. The design of the spatial combiner is more challenging compared to the radial combiner due to necessity of incorporating antenna elements and designing the spatial output feed but this design can be more compact versus the radial design.

The architecture chosen was a combination of the corporate and radial combiner techniques. A submodule consisting of the parallel combining of the CREE devices using corporate COTS hybrid circuits will provide enough power to decrease the size constraints of the radial combiner for the final combining. Figure 4 illustrates the combining of two amplifier circuits whereas figure 5 shows the combining of four amplifier circuits.
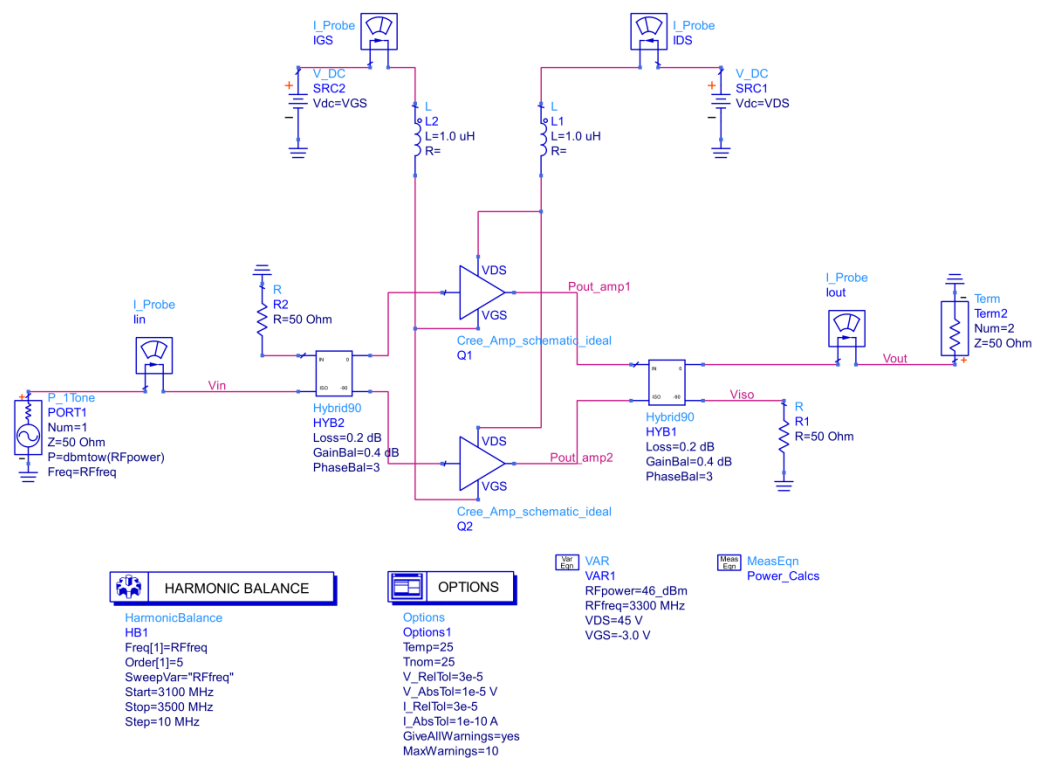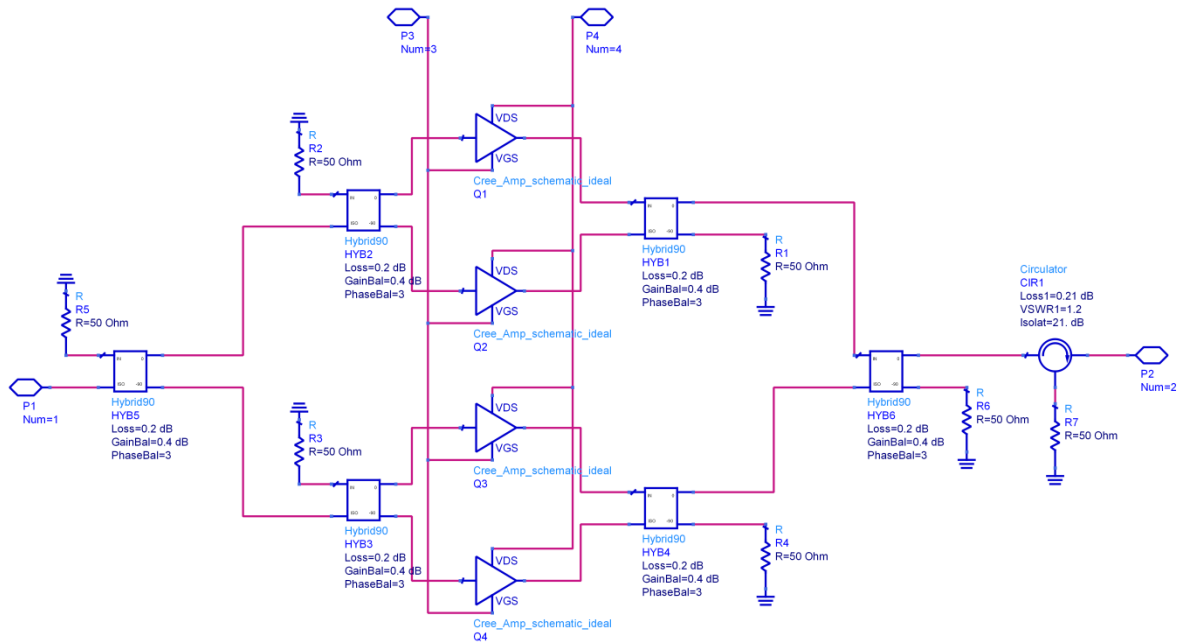

Figure 4. Balanced Amplifier

Figure 5. HPA Module

Using four CREE CGHV35400F devices at 400W each, would theoretically produce an RF output of 1.6kW. However, due to circuit board, hybrid coupler, and circulator losses, estimated between 0.75 to 1 dB, the final RF power should be in the range of 1,270W to 1,346W. The corporate combining of four amplifiers will be the basis of the high power amplifier (HPA) module. Multiple HPA modules will be used in the final radial combining design to achieve a minimum of 10 kW of output power. Figure 6 illustrates the HPA conceptual design. The circuit board is approximately 3.15 inches wide and 6.00 inches long.

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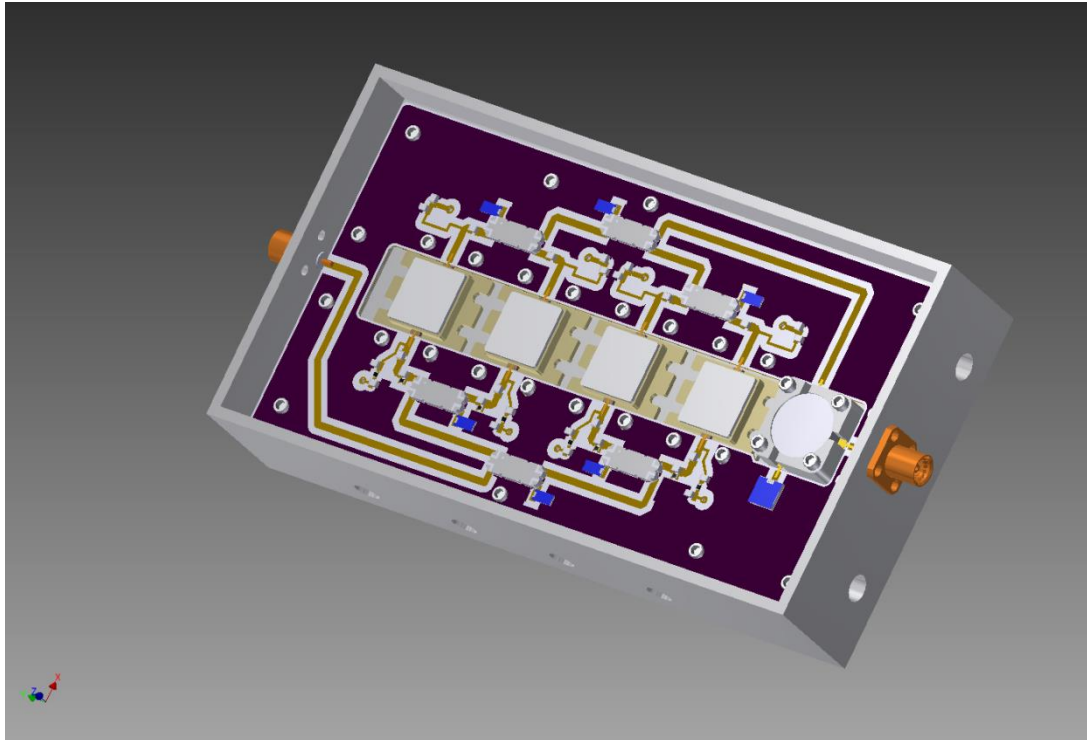
Figure 6. HPA Concept

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3.1.4.   Simulation Data
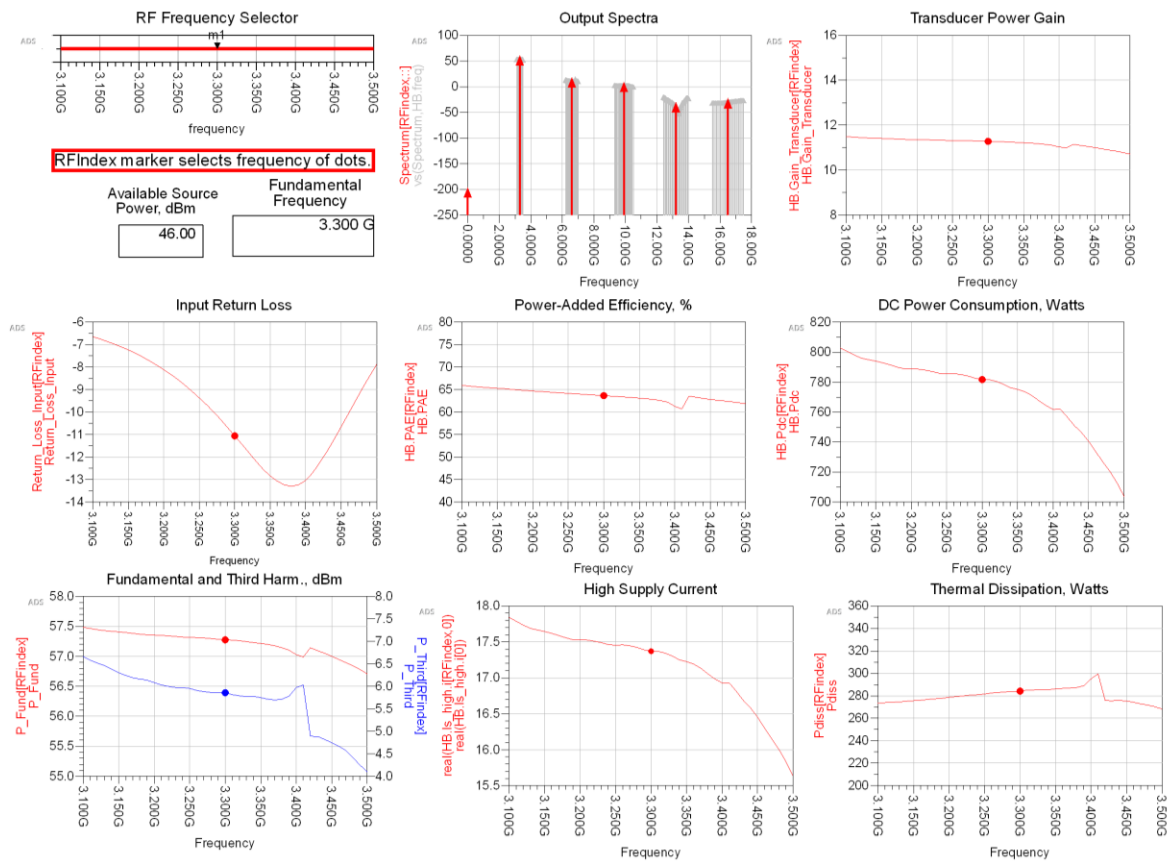
Figure 7. ADS Simulation of Cree Test Board using Ideal Components
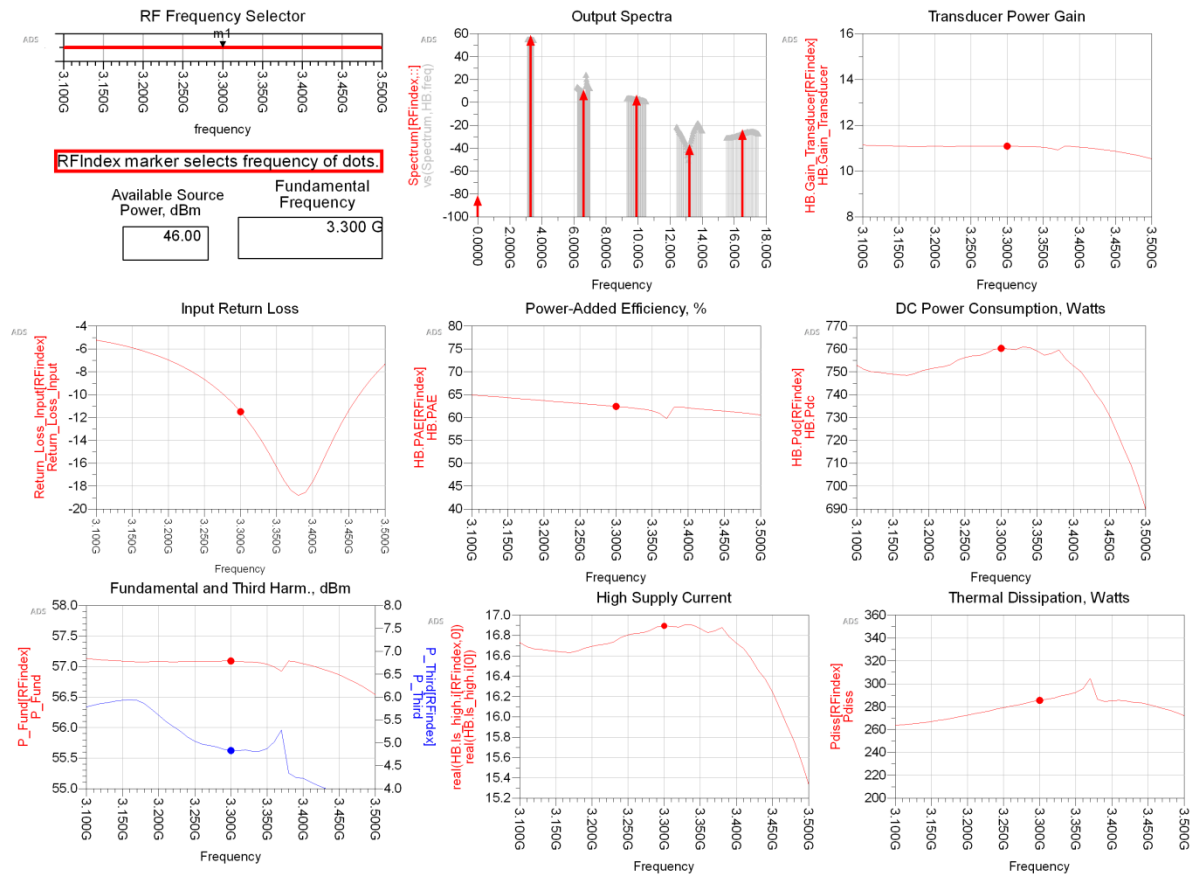
Figure 8. ADS Simulation of Cree Test Board using Modelithic Component Models
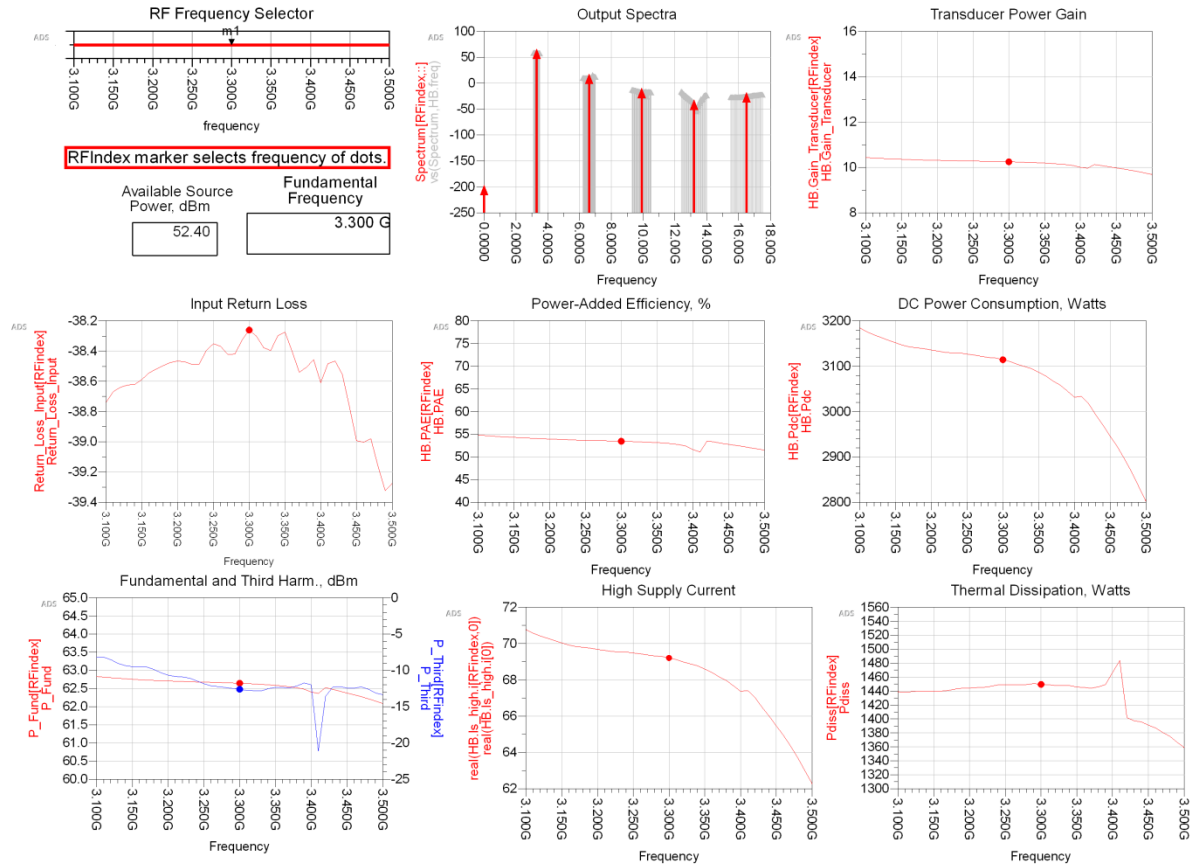
Figure 9. ADS Simulation of HPA Concept using Ideal Components

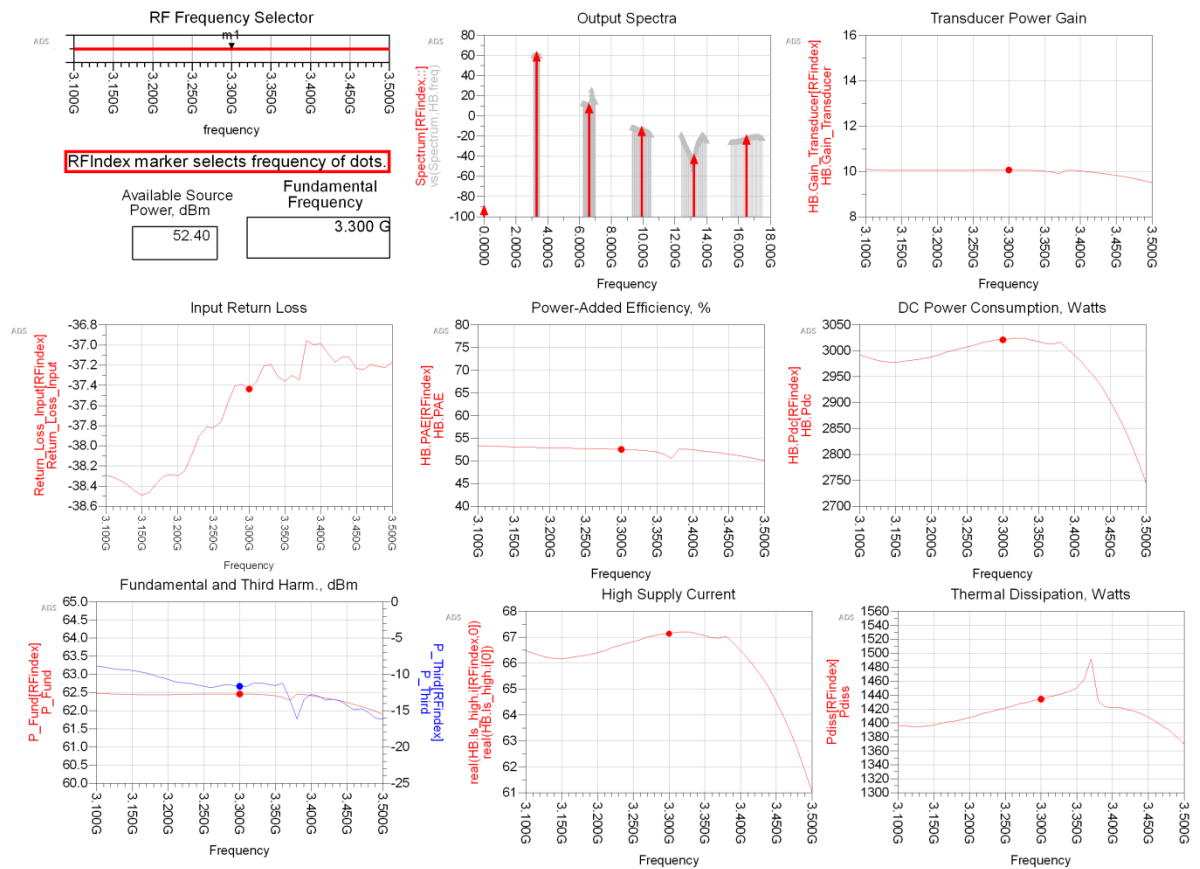**Harnessing the Power of Technology for the Warfighter**

Figure 10. ADS Simulation of HPA Concept using Modelithic Component Models

3.1.5. Simulation Data Analysis

Figures 7 through 10 above presented the progression of simulations directed to build up an HPA module and provide validation that the CREE GaN devices could potential be used to combine enough power to replace TWTs.

The first simulation, depicted in Figure 7, is of a single CREE CGHV35400F device with idealized RF circuit board components. These passive components do not include packaging parasitics which can increase loss and affect the overall amplifier frequency response. The circuit was driven with 46dBm at the input across the frequency range of 3.1 to 3.5GHz. The fundamental output power at center frequency was approximately 57.3dBm or 537 W. It had a transducer power gain of 11.3 dB and had an estimated peak current of 17.35 Amps. At a drain voltage of 45V, the simulated drain efficiency of the CREE device was approximately 68.8%. The overall power gain is reasonably flat within a 0.75 dB range. The simulation also shows a resonance at around 3.41 to 3.42 GHz. The cause of this resonance is unknown but mostly likely adjustments in the harmonic

balance simulation controller will need to be optimized or additional harmonic data points may need to be taken.

The second simulation, depicted in Figure 8, uses Modelithic component models that include packaging parasitics in addition to the effects of mounting surface mount components to board substrates. The circuit was driven with 46dBm at the input across the frequency range of 3.1 to 3.5 GHz. The fundamental output power at center frequency was approximately 57.1dBm or 513W. It had a transducer power gain of 11.1dB and an estimated peak current of 16.9 Amps. At a drain voltage of 45V, the simulated drain efficiency was approximately 67.5%. The power gain is flat within a 0.5 dB range. The resonance is still noticeable around 3.41 to 3.42GHz. As expected, using realistic component models will show the potential losses to the circuit. The overall gain dropped a few tenths of a dB versus the ideal simulation.

The third simulation, depicted in Figure 9, is of the HPA concept consisting of four CREE devices combined using hybrid couplers. The passive components are ideal and the hybrid couplers and output protection circulator are based off of COTS components. The circuit was driven with 52.4dBm at the input across the frequency range of 3.1 to 3.5GHz to account for the 6.4dB of divider loss due to the input hybrid couplers. This would allow for a nominal 46dBm power input at each device. The fundamental output power at center frequency was approximately 62.7dBm or 1,862W. The simulation showed a transducer power gain of 10.3dB and an estimated peak current of 69.2 Amps. At a drain voltage of 45V, the simulated drain efficiency was approximately 59.8%. The power gain is reasonably flat with less than 1dB across the frequency band.

The final simulation, depicted in Figure 10, is the HPA with the Modelithic component models. The hybrid couplers and circulator models were the same as the third simulation. The circuit was driven with 52.4dBm at the input. The fundamental output power at center frequency was approximately 62.5dBm or 1,778W. The simulation showed a transducer power gain of 10.1dB and an estimated peak current of 67.1 Amps. At a drain voltage of 45V, the simulated drain efficiency was 58.9%. The power gain is flat with approximately 0.5 dB range across the frequency band. As expected, the overall gain dropped a few tenths of a dB versus the ideal HPA simulation.

Table 2 summarizes the results at 3.3 GHz

Table 2. Results @ 3.3GHz

Simulation Description	Power In (dBm)	Power Out (dBm)	Power Gain (dB)	Efficiency (%)	Drain Voltage (V)	Drain Current (A)
Single Cree simulation with ideal components	46	57.3	11.3	68.8	45	16.9
Single Cree simulation with Modelithic models	46	57.1	11.1	67.5	45	16.9
HPA concept with ideal components	52.4	62.7	10.3	59.8	45	69.2

Simulation Description	Power In (dBm)	Power Out (dBm)	Power Gain (dB)	Efficiency (%)	Drain Voltage (V)	Drain Current (A)
HPA concept with Modelithic components	52.4	62.5	10.1	58.9	45	67.1

3.1.6. Simulation Key Points of Interest

The above simulation details can be summed up with the following key points of interest

- Simulation results show sufficient RF output power in CREE GaN devices
- Accurate component models are a necessity in getting real world performance
- A more detailed investigation is required to solve simulation resonance

4. Testing

The 400W GaN device from CREE, model number CGHV35400F was used to evaluate the feasibility of COTS GaN technology as a 10kW TWT replacement. The device selected to drive this 400W GaN amplifier was CREE model number CMPA2735075F. The device is a 75W packaged-MMIC power amplifier. These two devices were combined and tested using a modified high power amplifier test station built by Radar Technologies Division engineers. The high power amplifier test station was originally built and configured to test a UHF 500W amplifier. The test station architecture was built with MOSA principles in mind. This concept allowed for test station configuration changes to accept an S-Band 400W device for evaluation testing. All of the testing during this IRE was accomplished using this modified high power amplifier test station. A photograph of the high power amplifier test station is shown in figure 11.
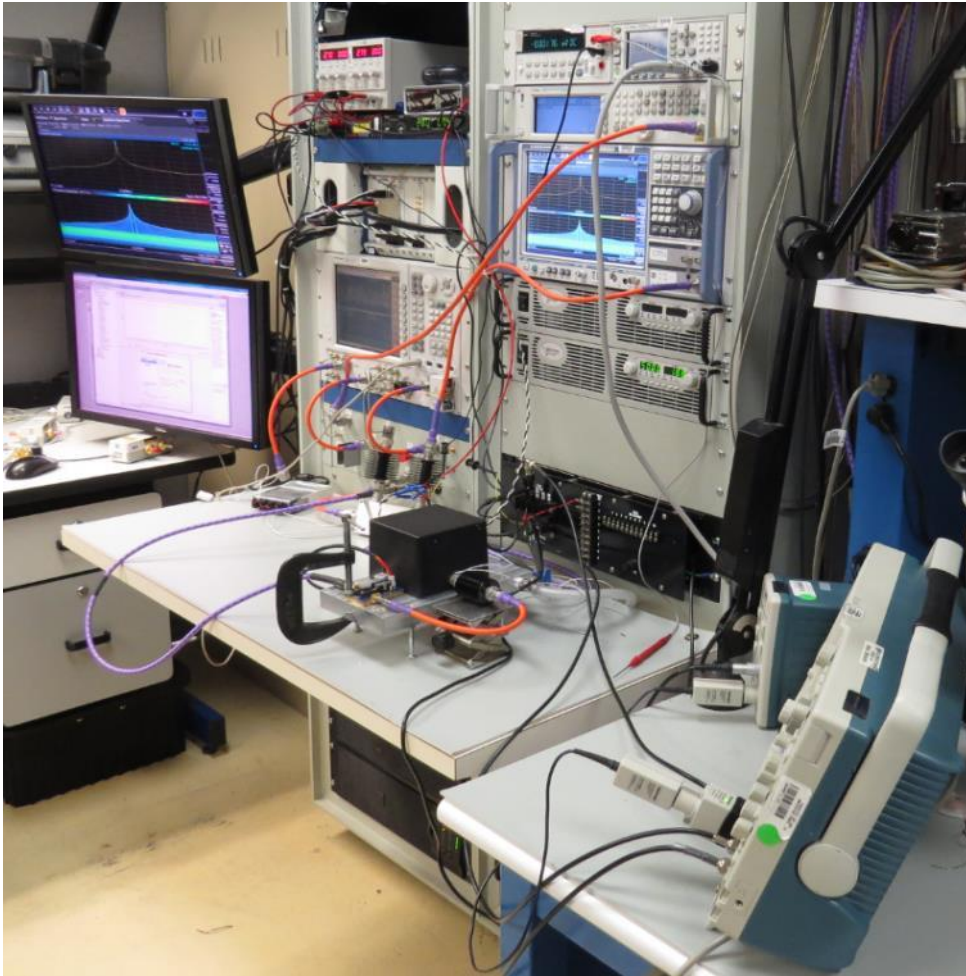
Figure 11. High Power RF Amplifier Test Set

4.1. Bench Level Testing

4.1.1. Bench Test Specifications

The specifications used to validate COTS GaN devices for use in this application are listed in the table below. The specifications were developed using considerations of the most critical parameters of amplifier design.

Table 3. Bench Testing Specifications

#	Specification	Requirement
1	RF Power Output	400W min
2	HPA Drain-Source Voltage (Vds)	45VDC min, 50VDC max

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3	Operating Frequency	3.1GHz to 3.5GHz
4	Total Gain (Driver + HPA)	34dB min
6	Pulse Width Capability	≥ 100uSec
7	Duty Cycle	10% Max
8	Input VSWR	2.5:1 max
9	Harmonics	20dBc min

The next phase of this project will combine four GaN devices to create a ~1.2kW output power HPA module. The HPA module will have different requirements/specifications than the 400W setup. The final phase of the project will be to combine ten of the 1.2kW modules to create a 10kW solid state amplifier (SSA). This SSA will, again, require new or additional requirements/specifications that will differ from the first two phases.

4.1.2. Bench Test Methods

Two main pieces of test equipment were used in characterizing the 400W device; a Performance Network Analyzer (PNA-X) and a Real Time Spectrum Analyzer (RSA). Figure 12 below shows the connections of these two devices to the DUT.
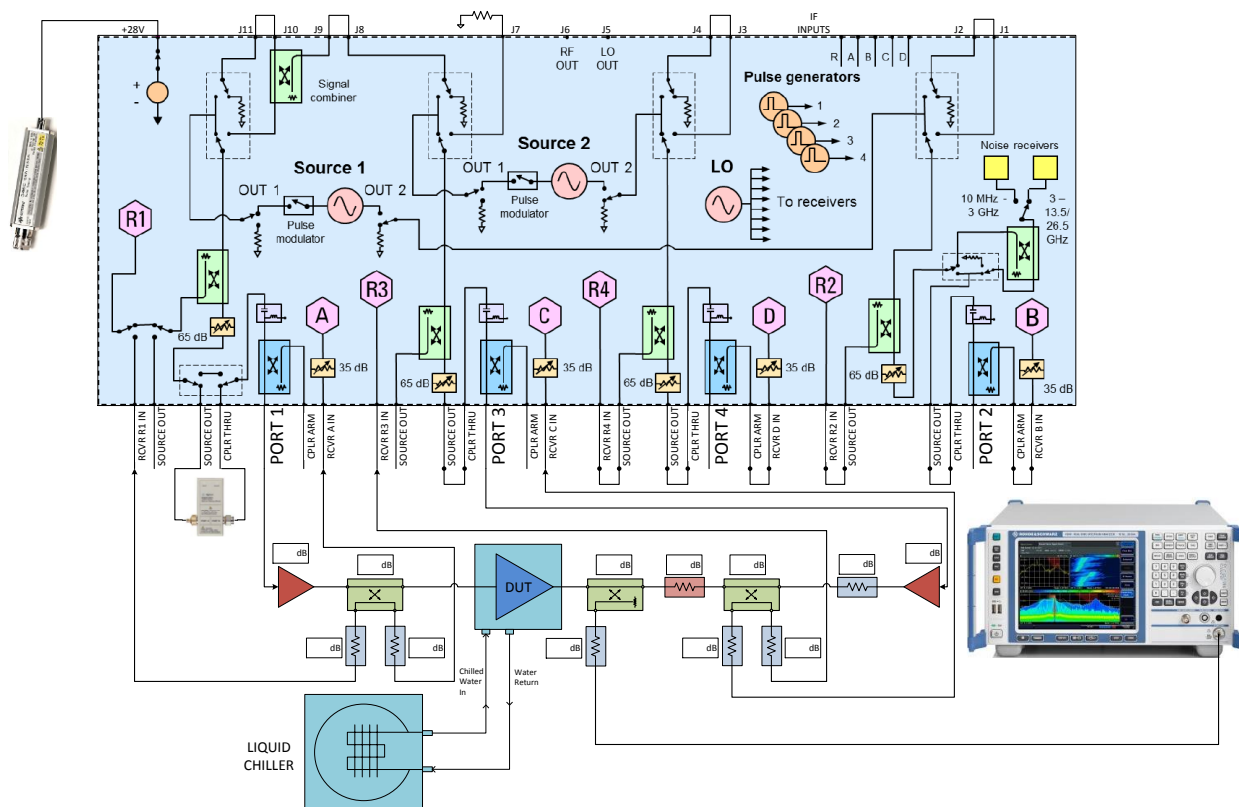

Figure 12. HPA Test Set Diagram

The equipment and quantity used in the high power amplifier test station is listed below in Table 4.

Table 4. Bench Test Equipment List

| Manufacturer	Model Number	Description	Qty Used
Keysight Technologies	N5242A	PNA-X	1
National Instruments	NI 9219	4CH USB Analog Input DAQ	1
National Instruments	PXIe-1082	PXI Chassis	1
National Instruments	PXIe-8115	Embedded Controller for PXI Systems	1
National Instruments	PXIe-6361	PXI Multifunction DAQ	1
Keysight Technologies	85052B	3.5mm Manual Calibration Kit	1
TECA		Liquid Chiller	1
Keysight Technologies	N8737A	3.3kW DC Power Supply	1
Sorensen	DCS40-30E	1.2kW DC Power Supply	1
Sorensen	XEL 30-3DP	180W DC Power Supply	1
Keysight Technologies	34401A	6 ½ Digit Benchtop Multimeter	1
Keysight Technologies	N1912A	P-series Power Meter	1
Tektronix	DPO4054	500MHz 2.5Gs/s Oscilloscope	1
Tektronix	TCP305	50ADC Current Probe	1
Tektronix	TCP A300	AC/DC Current Probe Amplifier	1
Rhode & Schwarz	FSW26	Real Time Spectrum Analyzer	1
Keysight Technologies	N5183A	MXG Series Analog Signal Generator	1
Omega	RTD-830-B	Bolt-On Flange RTD	2
Omega	RTD-809-B	Encapsulated RTD	1

4.1.3. Bench Test Data
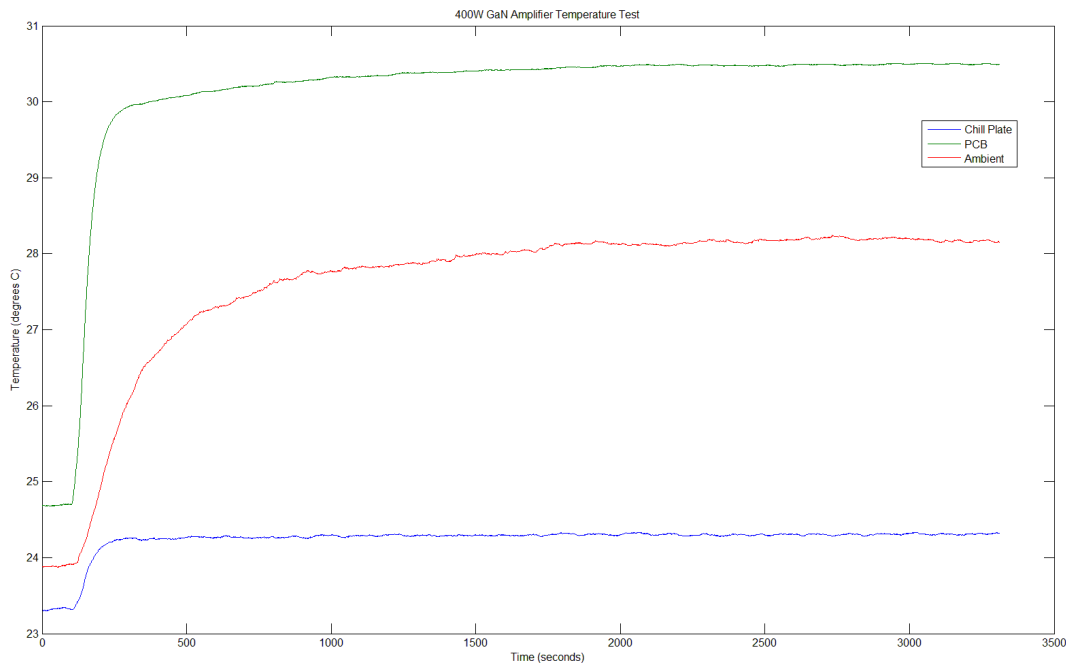
Figure 13. Temperature Test results

The temperature chart shown above is the result of 1 hour of continuous operation of the 400W device. The 400W device had an RF pulse injected into it for the duration of this test. The pulse width of the pulse was 100us and the duty cycle was 10%. The Drain-Source Voltage used was 45VDC. The device was able to maintain its 400W output power throughout the temperature test duration. The device was liquid cooled during the temperature test using a chiller water temperature held at 25°C.
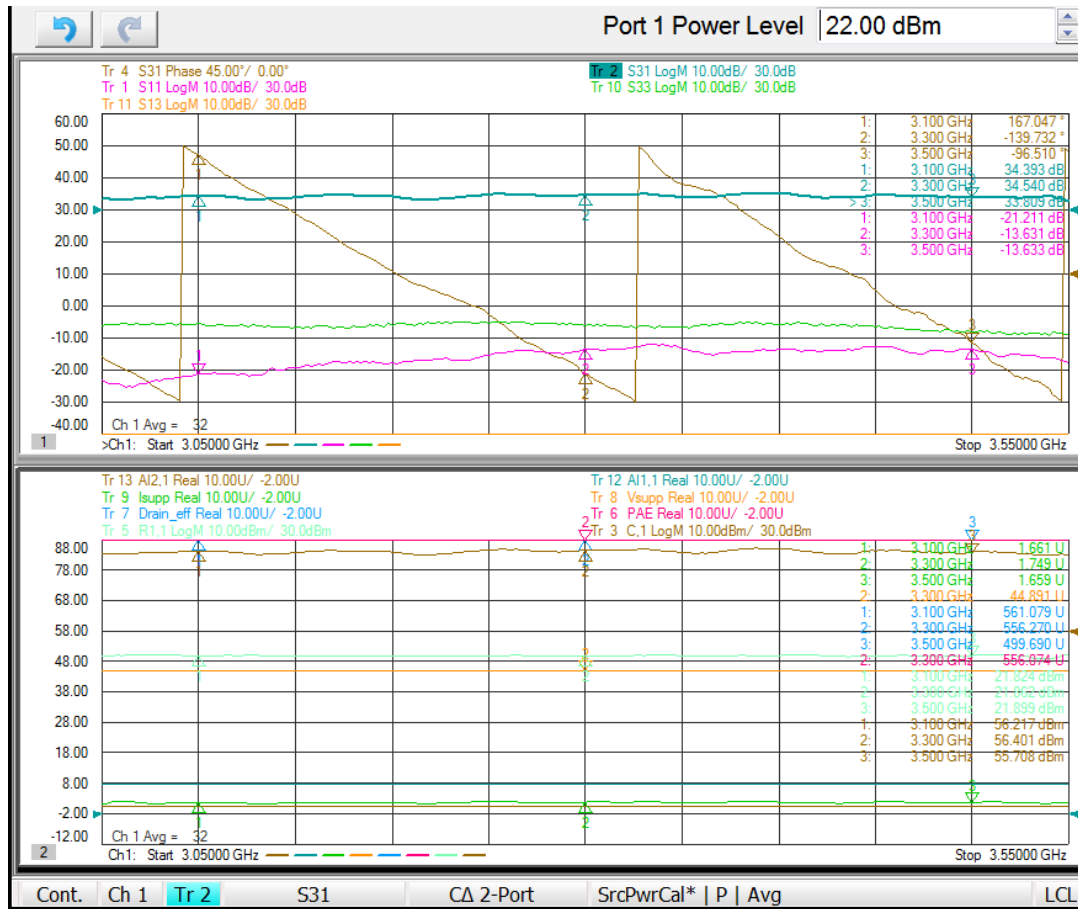
Figure 14. PNA-X Testing Results

Shown above are the results plotted on the PNA-X for the 400W device. The input given to the driver amplifier was +22dBm (noted in Port 1 Power Level above). On the top display trace S_{31} (turquoise) is the small signal gain for the combined driver amplifier, attenuator, and 400W device. Trace S_{11} is the input Return Loss into the amplifier chain. Trace S_{31} (brown) shows the Insertion Phase of the amplifier chain. On the bottom display Trace 3 C,1 (brown) is the output power of the amplifier chain in dBm. Trace 5 R1,1 (light blue) is the input power coming into the amplifier chain.

Trace 6, 7, 8, & 9 are all the traces used to calculate and develop the PAE of the amplifier. There was an issue with the Pulse I_{ds} current measurement which caused these traces to generate incorrect measurements. The pulsed I_{ds} measurement coming from the 3.3kW power supply was giving the PNA-X an average current measurement not a peak current measurement. A peak current measurement is needed to calculate the PAE correctly on the PNA-X.

4.1.4. Bench Test Data Analysis

Table 5. Overall RF Characteristics Analysis

Fc (GHz)	PW (uSec)	Duty (%)	RF P$_{IN}$ (dBm)	RF P$_{OUT}$ (dBm)	RF P$_{OUT}$ (W)	Overall Gain (dB)	Calculated CGHV35400F Gain (dB)	Overall Input VSWR
3.1	100	10	21.824	56.217	418.50	34.393	8.333	1.19:1
3.3	100	10	21.862	56.401	436.62	34.539	8.259	1.53:1
3.5	100	10	21.899	55.708	372.22	33.809	7.509	1.53:1

Table 6. CMPA2735075F RF Characteristics Analysis

Fc (GHz)	PW (uSec)	Duty (%)	RF P$_{IN}$ (dBm)	RF P$_{OUT}$ (dBm)	RF P$_{OUT}$ (W)	CMPA2735075F Gain (dB)	Input VSWR
3.1	100	10	25.92	48.98	79.07	23.06	1.13:1
3.3	100	10	26.1	49.38	86.70	23.28	1.41:1
3.5	100	10	26.07	49.37	86.50	23.3	1.31:1

Table 7. Drain-Source VI Analysis

Vds (VDC)	Ids Peak (Arms)	Vds Ripple (V)	Vds Capacitance (uF)
45	7.6	0.288	3,333
45	9.12	0.12	13,333
45	9.84	0.08	23,333
50	8.08	0.296	3,333

4.1.5. Bench Testing Key Points of Interest

- The critical specification, RF power out, was achieved with a total RF output power of 436.6W at the 3.3GHz center frequency.
- The amplifier was able to maintain its 400W output power with a pulse that had a duty cycle of 10%. This is very promising considering the average duty cycle the 10kW TWT sees is around 2%.
- No thermal issues were observed with the simulated cooling environment.

5. Bench Testing v. Simulation Comparison

- Measured data shows CREE device capable of delivering 400W
- Simulated data shows better performance but board interactions, environmental effects, coaxial RF transition to board effects are not taken into account in the model.
- Accurate component models are a necessity in getting real world performance. Actual component values on CREE's test fixture where unknown. Future testing will use known component values.

- Measured data did not show a resonance around 3.41 to 3.42 GHz. Additional investigation needed to refine simulation.

6. Conclusions

The team was successful in all facets of Phase I of this IRE. The initial design approach and architecture was developed using Keysight ADS and were provided in this report. Simulations were run to verify the test data taken from the CREE transistors. Testing and evaluation of the selected transistors from CREE was performed and data captured. The data captured, analyzed and compared favorably with both the vendor data sheets and model. The primary objective of this data collection and analysis was to determine the feasibility of using COTS transistors to develop a solid state replacement for a TWT. The results of this IRE provide proof that, not only is it a very feasible option, but it would be tragic not to investigate and develop further with follow-on efforts. The feasibility of using COTS transistors to develop a technology insertion prototype using GaN to replace a traveling wave tube

7. Recommendations

Our technical team recommends proceeding with a Phase II Internal Rapid Experimentation for this effort. The recommended tasking included in Phase II is to design, develop and simulate a model using Keysight ADS. The model developed would be for a sub-module capable of achieving greater than 1kW of output power. Using the mature model a prototype shall then be fabricated and tested using bench-top test equipment very similar to those used in Phase I. The test data taken will then be compared to the simulation data to validate the model. Following the successful completion of Phase II, there is further effort that could be done to prepare the 10kW TWT transition to GaN for sponsorship by a Program Office. Phase III of this effort would align to a NISE 219 project due to the amount of funding required for thermal modeling and analysis, FEA, modeling & simulation of prototype 10kW GaN amplifier, acquisition cycle for components, prototype assembly and final test.

Appendix A. Acronyms, Abbreviations, and Symbols

Table A-8. Acronyms, Abbreviations, and Symbols

Term	Definition
COTS	Commercial Off The Shelf
IRE	Internal Rapid Experimentation
DUT	Device Under Test
EW	Electronic Warfare
FEA	Finite Element Analysis
GaN	Gallium Nitride
HPA	High Power Amplifier
kW	Kilowatt
MMIC	Monolithic Microwave Integrated Circuit
MOSA	Modular Open Systems Architecture
NRE	Non-Recurring Engineering
PAE	Power Added Efficiency
SSA	Solid State Amplifier
TWT	Traveling Wave Tube
UHF	Ultra-High Frequency
VSWR	Voltage Standing Wave Ratio

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Appendix B**. High Power Amplifier Testing Data**
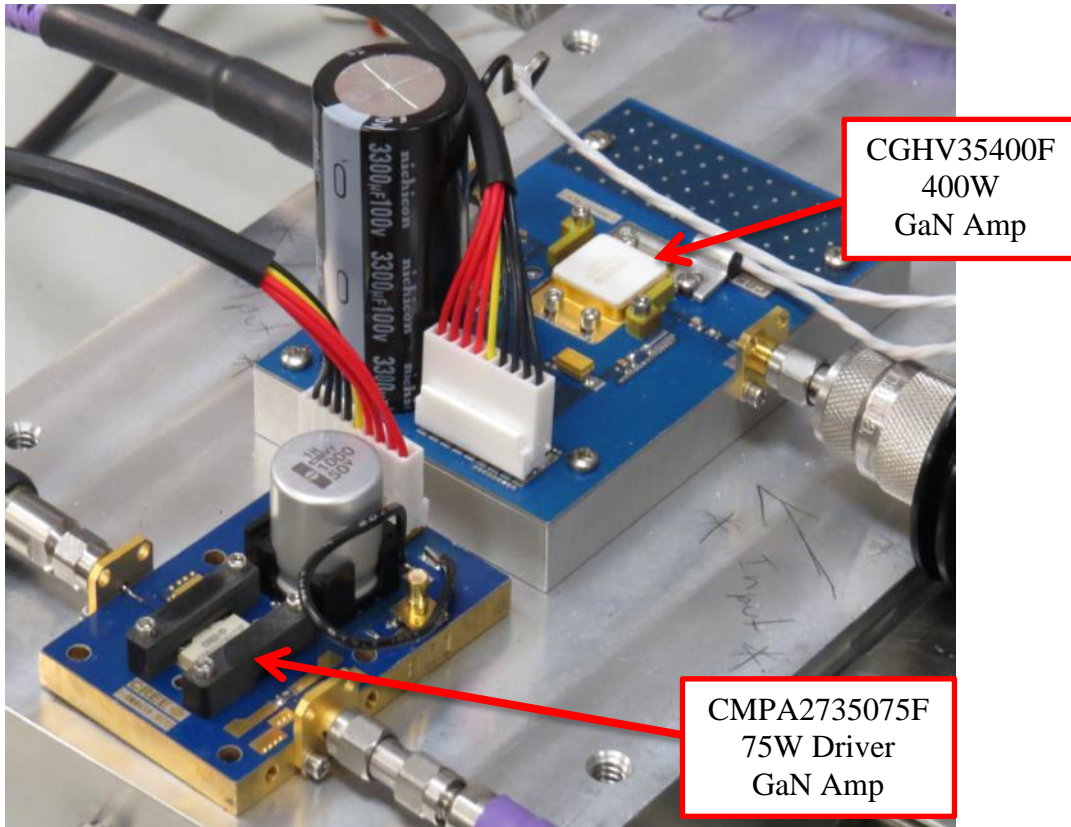
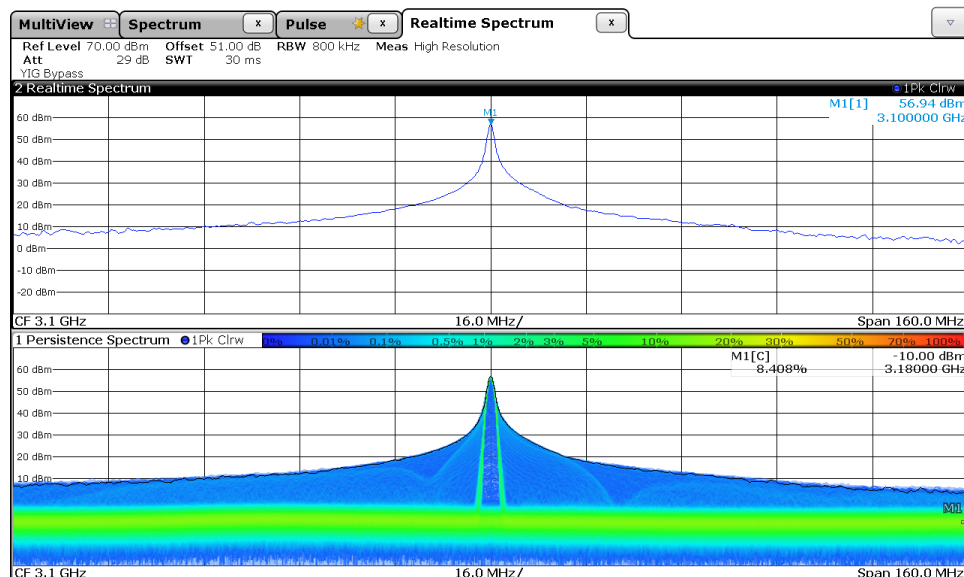**Figure 15. CREE Amplifiers Installed in the HPA Test Set**

Figure 16. Real Time Spectrum Plot of 400W Amplifier @ 3.1GHz

V_{DS} = 45VDC
Pulse Width = 100 μSec
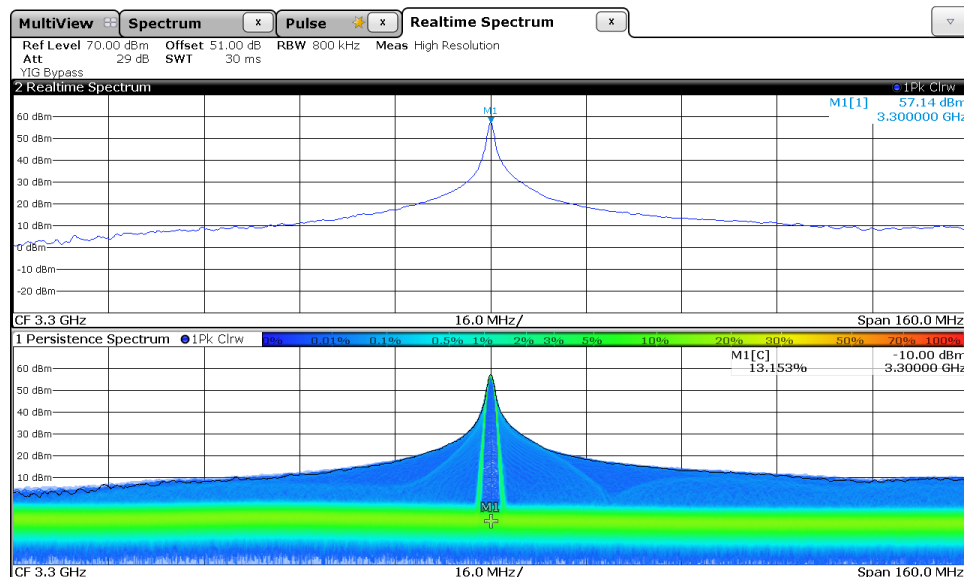Duty Cycle = 10%
Frequency = 3.1GHz
P_{OUT} = 56.94dBm

Figure 17. Real Time Spectrum Plot of 400W Amplifier @ 3.3GHz

V_{DS} = 45VDC
Pulse Width = 100 μSec
Duty Cycle = 10%
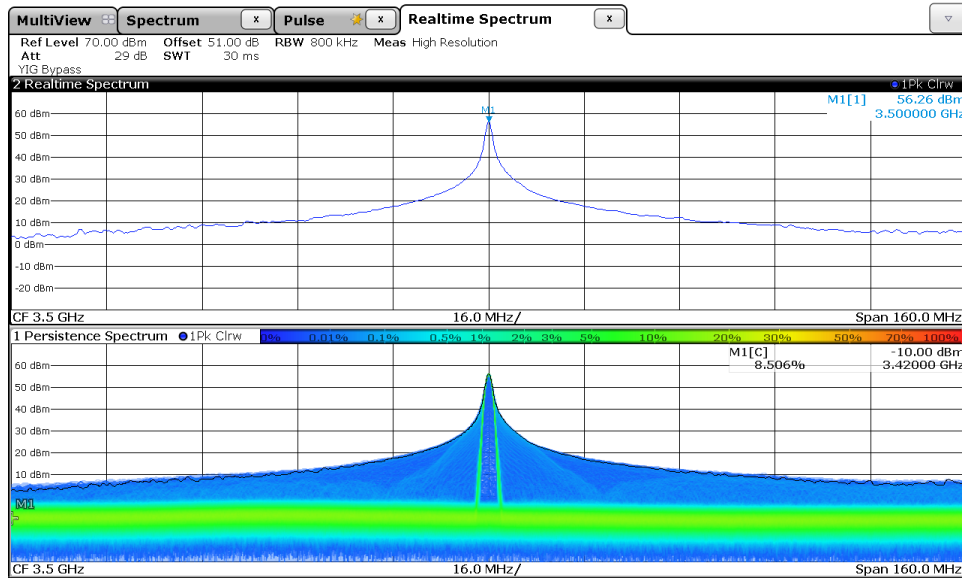Frequency = 3.3GHz
P_{OUT} = 57.14dBm

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Figure 18. Real Time Spectrum Plot of 400W Amplifier @ 3.5GHz

V_{DS} = 45VDC
Pulse Width = 100 µSec
Duty Cycle = 10%
Frequency = 3.5GHz
P_{OUT} = 56.26dBm

Figures 16 through 18 are screen shots of the real time spectrum analyzer display in the test set. The input signal used was a pulsed RF power signal with an input power of +22dBm and a pulse width of 100 mircoseconds. The duty cycle of the pulse was 10 percent. The center frequency of the signal was adjusted to the low, mid, and high frequenices of the operating bandwidth to characterize the output power of the HPA using the real time spectrum analyzer. The overall estimated flatness of the response is shown below:

$$RF_{BW} = 3.5GHz - 3.1GHz = 400MHz$$

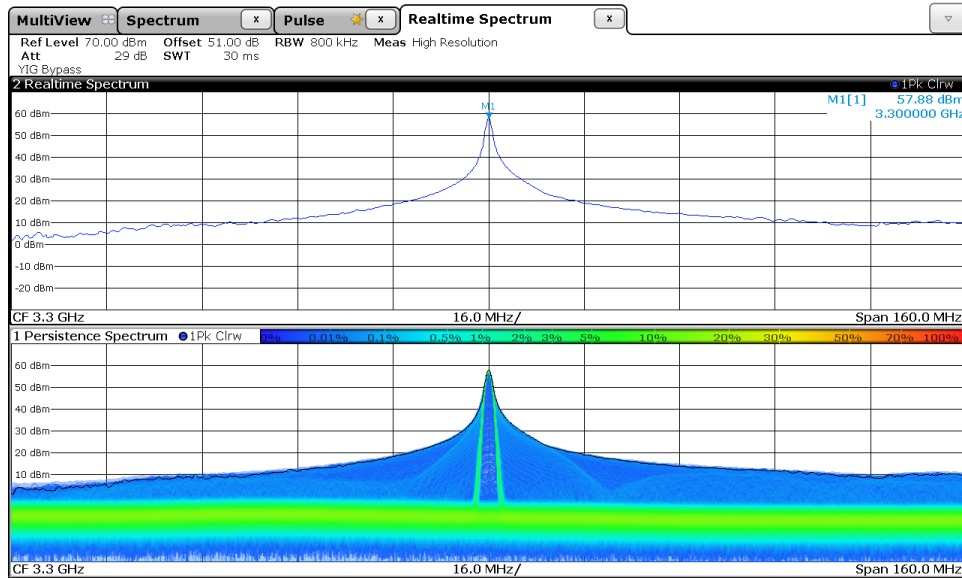$$P_{OUT} \text{ flatness} = abs[56.26dBm - 56.94dBm] = 0.68dB$$

Figure 19 Real Time Spectrum Plot of 400W Amplifier @ Vds = 50VDC

V_{DS} = 50VDC
Pulse Width = 100 µSec
Duty Cycle = 10%
Frequency = 3.3GHz
P_{OUT} = 57.88dBm

Figure 19 is a screen shot of the real time spectrum analyzer display in the test set. The input signal used was a pulsed RF power signal with an input power of +22dBm and a pulse width of 100 mircoseconds. The duty cycle of the pulse was 10 percent. The center frequency of the signal is 3.3GHz. The Drain-Source Voltage was increased to 50VDC to observe the effect it had on the RF ouput power. The increase in the RF power output from increasing the Drain voltage is seen below:

$$P_{OUT} @ (V_{DS} = 50VDC) - P_{OUT} @ (V_{DS} = 45VDC)$$

$$57.88dBm - 57.14dBm = 0.74dB \text{ power gain}$$

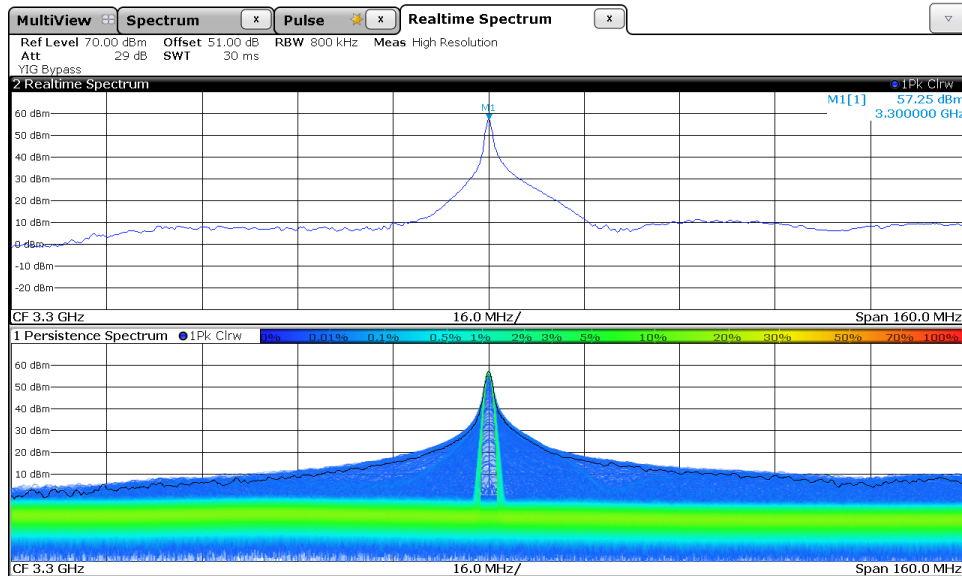$$613.762W - 517.607W = 96.155W \text{ power increase}$$

Figure 20. Real Time Spectrum Plot of 400W Amplifier @ PW = 500 μSec

V_{DS} = 45VDC
Pulse Width = 500 μSec
Duty Cycle = 10%
Frequency = 3.3GHz
P_{OUT} = 57.25dBm

Figure 20 is a screen shot of the real time spectrum analyzer display in the test set. The input signal used was a pulsed RF power signal with an input power of +22dBm. The amplifier was operated at a drain-source voltage of 45VDC. The duty cycle of the pulse was 10 percent. The center frequency of the signal3.3GHz. The pulse width of the RF pulse was increased to 500 microseconds to see the effect it had on the RF output power, as shown below:

$$P_{OUT} @ (PW = 500 \ \mu Sec) - P_{OUT} @ (PW = 100 \ \mu Sec)$$

$$57.25dBm - 57.14dBm = 0.11dB \text{ power gain}$$

$$530.884W - 517.607W = 13.277W \text{ power increase}$$

As shown by the calculation above there was very little change in RF power when the pulse width was increased to the pulse width that CREE recommends the amplifier to be operated at. This is very promising results and shows that the amplifier is stable with respect to fluctuations in pulse characteristics.

Input Capacitance Adjustments and Results

The Oscilloscope was used to capture the I_{ds} pulse current waveform as well as the RF input pulse and the V_{ds} voltage. These measurements were needed to find the drain-source DC voltage ripple and the drain-source DC peak current. The DC voltage ripple is used to figure out the effects of the input capacitance on the Drain-Source voltage going to the amplifier. The DC peak current is used to make sure we are not operating the amplifier above the recommended limits and to manually calculate the PAE of the device.

The three sections of the following screen shots are for the amount of capacitance on the drain-source voltage line coming into the 400W amplifier. We needed to see the effects on the DC input voltage line when capacitance is added to compensate for the voltage droop from the pulsed current. The first two screen shots Figures 21 & 22 are of the drain-source line with no external capacitance added to the amplifier board. The amplifier board already has soldered in a radial electrolytic 3300uF capacitor and a surface mount 33uF electrolytic capacitor in a parallel configuration on the drain source line. The next two screen shots (Figures 23 & 24) are of the drain-source line with a 10000uF electrolytic capacitor added in parallel between the power supply and the RF amplifier. The final two screen shots (Figures 25 & 26) are of the drain-source line with two 10000uF electrolytic capacitors added total of 20000uF of capacitance in parallel between the power supply and the RF amplifier.

Here are the oscilloscope channel definitions for the following screen shots:

Channel 1 Probe = DC Voltage @ Vds

Channel 2 Probe = TCP305 Current Probe @ Ids

Channel 3 Probe = Pearson Coil @ Ids

Channel 4 Probe = RF Input Pulse

3333uF Input Capacitance (No External Capacitors Added to Power Supply)

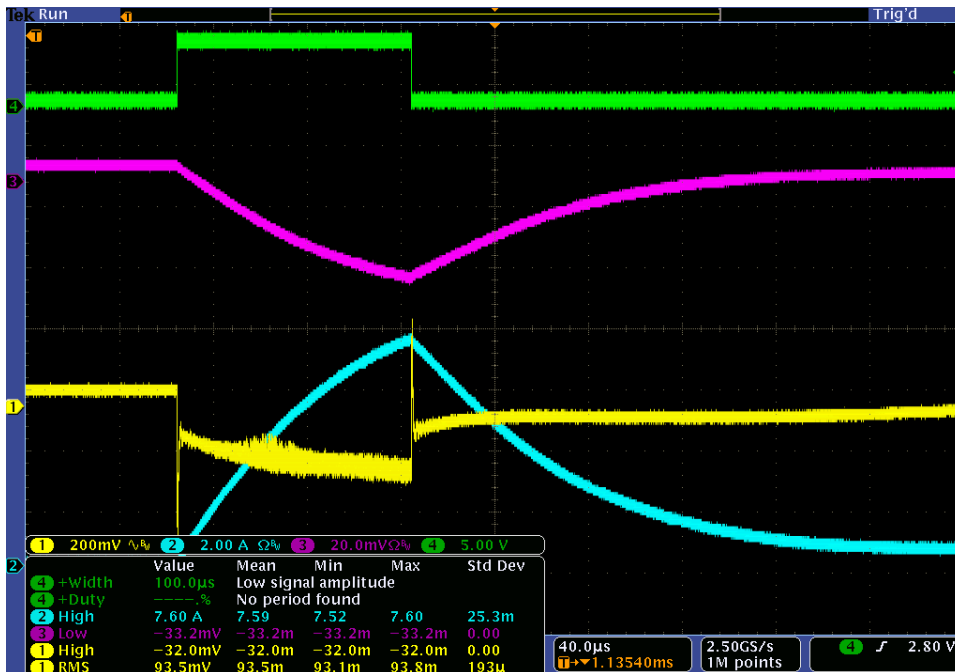**Figure 21. Vds Voltage Ripple Measurement**

Figure 22. Ids Current Pulse Measurement

Vds Ripple ~ 288mV
Peak Current ~ 7.60A

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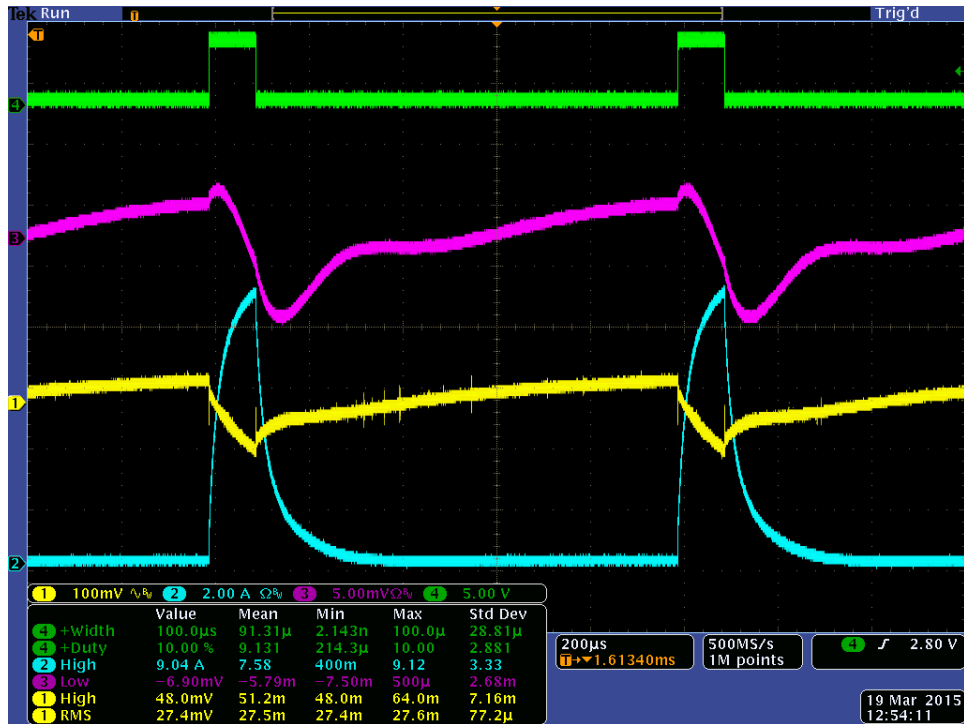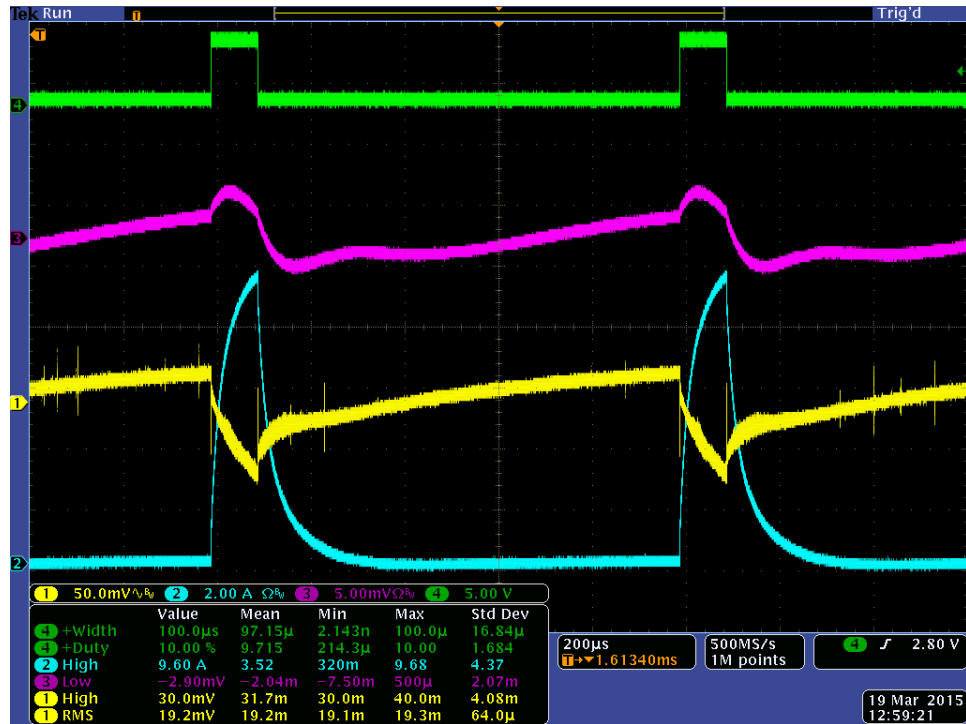13333uF Input Capacitance (10000uF Capacitor Added to Power Supply)

Figure 23. Vds Voltage Ripple Measurement

Figure 24. Ids Current Pulse Measurement

Vds Ripple ~ 120mV
Ids Peak Current ~ 9.12A

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23333uF Input Capacitance (20000uF Capacitor Added to Power Supply)

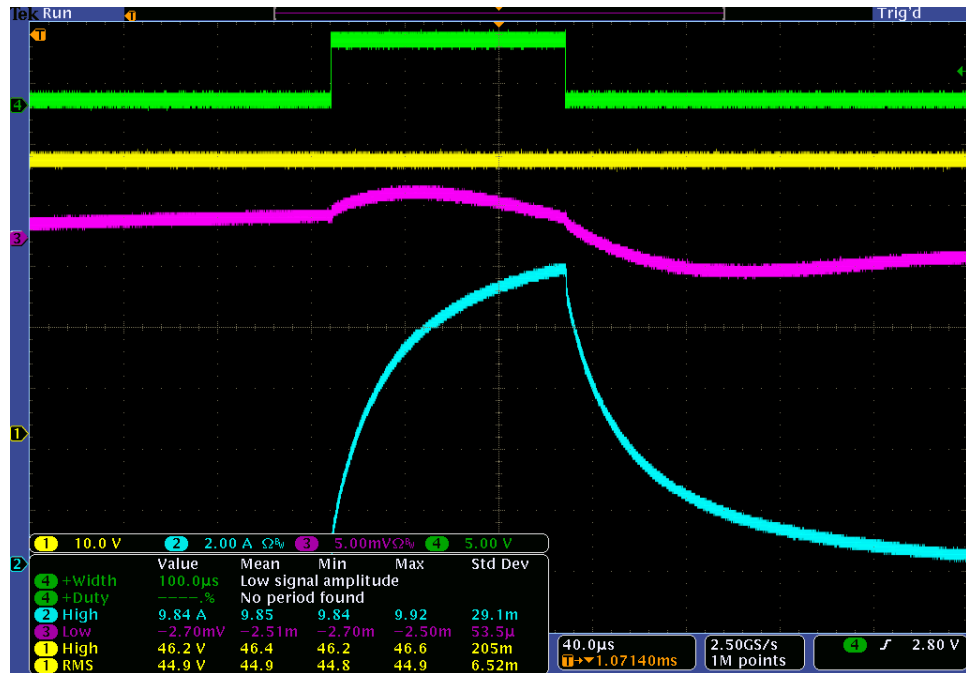**Figure 25. Vds Voltage Ripple Measurement**

Figure 26. Ids Current Pulse Measurement

Vds Ripple ~ 80mV
Ids Peak Current ~ 9.84A

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