Abstract

Inductive voltage adder topology has attracted great attentions in pulse power community for near two decades. However, there has been lack of literatures on inductive voltage adder network analysis and circuit design model. We have recently developed a simplified model and a set of simple formulas. An expanded model and more detailed analysis are presented in this paper. Our model reveals the relationship of output waveform parameters and hardware designs. Computer simulations have demonstrated that parameter estimation based on this approach is accurate. This approach can be used in early stages of project development to assist feasibility study, geometry selection in engineering design, and parameter selection of critical components. A set of fundamental estimation formulas including system impedance, rise time, and number of stages are presented. This approach is also applicable to induction LINAC design. In addition, the model presented in this paper shows a new topology of high voltage waveform generator.

I. INTRODUCTION

In our earlier papers [1] and [2], we presented an inductive voltage adder (IVA) transmission network model based on circuit element simplification approach and a set of estimation formulas derived from the model. It was the first step to reveal IVA mechanism. They are intended for industrial applications.

We introduce here an expanded model and a more formal approach of IVA analysis.

II. SIMPLIFICATION

A single cell circuit model of inductive voltage adder, shown in Figure 1., was given in [3] and [4]. Where, SW is the main switch, C_S is the capacitance of energy storage capacitor, R is the parallel resistor, L_K is core leakage inductance, L_P is primary core inductance, and L_1 and C_1 are the distributed inductance and capacitance of stalk per stack section length.

![Figure 1. A single cell model of inductive voltage adder](image)

When storage capacitors are large enough to keep constant voltage, they can be substituted by batteries in the circuit model. The switch and large capacitor, or a battery, can be represented by a “step input” source of voltage V_{in}, where V_{in} is the initial voltage of storage capacitors. Therefore, a single-stack inductive voltage adder model can be replaced by a new one as shown in Figure 2.

![Figure 2. A single stack model of inductive voltage adder with step input](image)

In each stack cell, the resistor R is in parallel with the input source of zero impedance hence it can be eliminated, as shown in Figure 3.

![Figure 3. A single stack model of inductive voltage adder with step input and R eliminated](image)
# Inductive Voltage Adder Network Analysis And Model Simplification

Inductive voltage adder topology has attracted great attentions in pulse power community for near two decades. However, there has been lack of literatures on inductive voltage adder network analysis and circuit design model. We have recently developed a simplified model and a set of simple formulas. An expanded model and more detailed analysis are presented in this paper. Our model reveals the relationship of output waveform parameters and hardware designs. Computer simulations have demonstrated that parameter estimation based on this approach is accurate. This approach can be used in early stages of project development to assist feasibility study, geometry selection in engineering design, and parameter selection of critical components. A set of fundamental estimation formulas including system impedance, rise time, and number of stages are presented. This approach is also applicable to induction LINAC design. In addition, the model presented in this paper shows a new topology of high voltage waveform generator.
Comparing impedance of two parallel branches of $L_k$ and $L_p$, the leakage inductance $L_k$ is usually much, much smaller than the primary inductance $L_p$, so is its impedance. Therefore, the circuit branch of $L_p$ can be eliminated in analysis. The single cell inductive voltage adder model is simplified as shown in Figure 4.

![Figure 4](image1.png)

**Figure 4.** A simplified single stack model of inductive voltage adder with step input

The single cell model given in Figure 1 is unsymmetrical. We change this model to a symmetrical one as in Figure 5.

![Figure 5](image2.png)

**Figure 5.** A symmetrical style single stack model

Its corresponding simplified model is given in Figure 6.

![Figure 6](image3.png)

**Figure 6.** A symmetrical style simplified single stack model of inductive voltage adder with step input

### III. NETWORK ANALYSIS AND DESIGN FORMULAS

The multi-stack inductive voltage adder is shown in Figure 7. The model is a ladder network of multiple “step input” sources.

Since the ideal step voltage source shall have zero impedance, the network transmission impedance of inductive voltage adder based on the circuit model of Figure 7 is then given by

$$ Z = \frac{L_k + L_p}{C_1} \quad (1) $$

This result shows that the circuit output impedance is larger than the stalk impedance due to the contribution of the leakage inductance. In order to minimize pulse reflections, the output cable and load shall match to the circuit output impedance $Z$ rather than the stalk impedance.

The transmission delay time per stack cell is simply the propagation time of each transmission line section. It is given by

$$ T_c = \sqrt{\frac{L_k + L_p}{C_1}} \quad (2) $$

Each stack cell has a natural resonant frequency of

$$ \omega_0 = \frac{1}{\sqrt{(L_p + L_k)C_1}} \quad (3) $$

Commonly used configuration of inductive voltage adder is shown in Figure 8.

![Figure 8](image4.png)

**Figure 8.** Common configuration of multi-stack inductive voltage adder

It is called a single-ended IVA, if one of the load, $Z_L$ or $Z_R$, is a short and the other one is matched to IVA transmission impedance $Z$. It is called a double-ended IVA, if both loads are identical and equal and matched to IVA transmission impedance $Z$.

Assuming all step input here has a voltage $V_{IN}$ as in previous section, and $Z_L$ is a short and $Z_R$ equals to $Z$. The load voltage of single-ended matched IVA can be expressed as

$$ -V_{IN} + \frac{2}{C_1S} $$

![Figure 7](image5.png)

**Figure 7.** A symmetrical style simplified multi-stack model of inductive voltage adder with step input
\[ V_{\text{load}} = N V_{IN} \]  
(4)

Where \( V_{\text{load}} \) denotes output voltage across load \( Z_R \) and \( N \) is number of stacks. The response voltage or current rise time, \( T_R \), of single-ended matched IVA can be expressed as

\[ T_R = 2N \sqrt{(L_K + L_1)C_1} \]  
(5)

Similarly, the load voltage of either end, \( V_{\text{Dload}} \), of double-ended matched IVA can be expressed as

\[ V_{\text{Dload}} = \pm \frac{N V_{IN}}{2} \]  
(6)

Where, \( V_{\text{Dload}} \) is positive for \( Z_R \) and negative for \( Z_L \). The load voltage or current rise time, \( T_{DR} \), of a double-ended matched IVA can be expressed as

\[ T_{DR} = N \sqrt{(L_K + L_1)C_1} \]  
(7)

Here \( C_1 \) and \( L_1 \) are stalk capacitance and inductance, and \( L_K \) is leakage inductance. They serve as transmission line elements during pulse propagation.

It is interesting to note distinctive differences of inductive-voltage-adder (IVA) and pulse-forming-network (PFN).

1. The output voltage of IVA is linearly dependent of number of stack cells, but output voltage of PFN is independent of number of cells.
2. The pulse rise time of IVA is linearly dependent of number of stack cells, but pulse rise time of PFN is independent of number of cells.
3. The pulse length of IVA is independent of number of stack cells, but PFN pulse length is dependent of number of cells.

IV. APPLICATION EXAMPLES

To demonstrate design application, we show a few simulation examples. Simulation parameters are from an actual circuit given in [3]. All switches are assumed to be ideal and identical.

<table>
<thead>
<tr>
<th>Symbol 1</th>
<th>Parameter</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_s )</td>
<td>storage capacitance</td>
<td>( 24 \times 10^{-9} ) F</td>
</tr>
<tr>
<td>( L_P )</td>
<td>primary inductance</td>
<td>( 20.9 \times 10^{-6} ) H</td>
</tr>
<tr>
<td>( L_K )</td>
<td>leakage inductance</td>
<td>( 6.5 \times 10^{-8} ) H</td>
</tr>
<tr>
<td>( L_1 )</td>
<td>stalk inductance per stake</td>
<td>( 20 \times 10^{-6} ) H</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>stalk capacitance</td>
<td>( 2.6 \times 10^{-12} ) F</td>
</tr>
<tr>
<td>( N )</td>
<td>number of stakes</td>
<td>30, 20, 10</td>
</tr>
<tr>
<td>( V_0 )</td>
<td>initial voltage of ( C_s )</td>
<td>( 1000 ) V</td>
</tr>
<tr>
<td>( R )</td>
<td>parallel resistance</td>
<td>50</td>
</tr>
<tr>
<td>( Z_{\text{STALK}} )</td>
<td>stalk impedance</td>
<td>50</td>
</tr>
</tbody>
</table>

From the above parameters, we can calculate the load impedance as

\[ Z = \sqrt{\frac{L_K + L_1}{C_1}} = \sqrt{\frac{(6.5 + 20) \times 10^{-9}}{2.6 \times 10^{-12}}} = 100.96 \, \Omega \]  
(8)

Here, the calculated load impedance is about twice of the stalk impedance.

Assuming a single-ended 30 stack IVA where \( Z_L \) is a short, the voltage pulse rise time across \( Z_R \) can be estimated by using equation (5).

\[ T_R = 2 \times 30 \sqrt{(20 + 6.5) \times 2.6 \times 10^{-12}} = 15.75 \, \text{ns} \]  
(9)

Using equation (6), we have the estimated output load voltage of the single-ended IVA

\[ V_{\text{load}} = 30 \times 1000 \, V = 30 \, kV \]  
(10)

The simulation result is in Figure 10. A comparison of matched and mismatched impedance cases are shown in Figure 11, which illustrate effects on pulse waveforms.

![Figure 9. The output pulse waveform of a 30-stack single-ended IVA](image1)

![Figure 10. Output pulse waveforms of a 30-stack single-ended IVA with matched or mismatched impedance](image2)

Here we shown a set of simulation examples of double-ended IVA of 10, 20, or 30 stacks with switch on at 0.1 ns and off at 40 ns. The estimated parameters shown in Table 2 are calculated using equations given in the previous section. Simulation results and estimated parameters are well agreed.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N )</td>
<td>Number of stacks</td>
<td>10, 20, 30</td>
</tr>
<tr>
<td>( T_{PR} )</td>
<td>Pulse rise time</td>
<td>2.62, 5.25, 7.87 ns</td>
</tr>
<tr>
<td>( V_{\text{load}} )</td>
<td>Pulse voltage</td>
<td>5, 10, 15 kV</td>
</tr>
</tbody>
</table>
The circuit model is given in Figure 14.

V. CONCLUSION

The method introduced in this paper can be further extended to high voltage function generator design. We have build and tested a model function generator based on inductive voltage adder.

VI. REFERENCES


