Strained InGaAs/InAlAs quantum wells for complementary III–V transistors

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**A B S T R A C T**

Quantum wells of InGaAs clad by InAlAs were grown on AlGaAsSb buffer layers by molecular beam epitaxy. The buffer layer lattice parameters were near 6.0 Å, yielding tensile strains up to 2% in the InGaAs and InAlAs. Room-temperature electron mobilities of 9000–11,000 cm²/V·s were achieved. Field-effect transistors (FETs) were fabricated and exhibited good DC and RF characteristics. Previous work demonstrated compressively-strained GaSb quantum wells on similar buffer layers with high hole mobilities and good transistor performance. Hence, a single buffer layer of AlGaAsSb should be suitable for complementary circuits comprised of n-channel FETs based on the mature InGaAs/InAlAs technology and p-channel FETs based on high-mobility antimonides.

**1. Introduction**

Recently, there has been considerable interest in the potential of III–V field-effect transistors (FETs) for advanced logic applications [1,2]. A III–V high-speed, low-power logic technology could enhance digital circuit functionality and sustain Moore’s law for additional generations. When utilized in mixed-signal circuits, a significant reduction in power consumption could also be obtained. For these applications, complementary circuits based on n- and p-channel III–V FETs would be highly desirable due to their low-power, high-speed advantages. A key issue is the composition of the channel and barrier materials for both the n-FET and the p-FET. A strong candidate for the n-FET is a high-mobility InGaAs channel clad by InAlAs barriers. This can take advantage of the mature InP high-electron-mobility transistor (HEMT) technology – so named because InP is usually used as a substrate for lattice-matched or strained InGaAs and InAlAs. Integrated circuits based on InP HEMTs are suitable for a variety of microwave applications including cell phones, cellular base stations, fiber optic systems, radar, radio astronomy, and satellite communications. Quantum wells of InGaAs/InAlAs have a sufficient valence band offset for hole confinement. Hence, one CMOS option is to combine InGaAs p-FETs and n-FETs. A few groups have investigated p-type modulation doped InGaAs/InAlAs QWs, but the hole mobilities are only 200–400 cm²/V·s at room temperature [3–6]. This will limit the performance of InGaAs p-FETs. In contrast, mobilities greater than 2000 cm²/V·s have been achieved for strained Ge/SiGe QWs [7]. Therefore, a second option is to combine InGaAs n-FETs with Ge p-FETs to take advantage of the attractive electron and hole mobilities, respectively, in these materials [2]. Integration is a challenge with this approach, however, because of the different crystalline structures and lattice parameters for the two material systems [8,9].

The use of Sb-based materials for both the n- and p-channels is also an attractive possibility since these materials have excellent electronic properties. This combination may enable the use of heterostructures which have the same buffer layer. The use of antimonide/arsenide heterostructures for n-FETs and other electronic devices was reviewed in Ref. [10]. Work on enhancing the hole mobilities for p-FET applications has been encouraging. Confinement and biaxial strain have been used to lift the heavy-hole/light-hole degeneracy, reduce the effective mass, and enhance the hole mobility [3,11]. Room-temperature hole mobilities as high as 1100–1500 cm²/V·s have been reported for InSb [12], GaSb [13–15] and InGaSb [16,17]. These antimonide quantum wells have been used in Schottky-barrier p-FETs with good DC and microwave performance [12,18]. In addition, (In)GaSb-channel MOSFETs have been fabricated; they have the attractive advantage of much lower gate leakage current which is a critical requirement in low-power logic
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Quantum wells of InGaAs cladded by InAlAs were grown on AlGaAsSb buffer layers by molecular beam epitaxy. The buffer layer lattice parameters were near 6.0?, yielding tensile strains up to 2% in the InGaAs and InAlAs. Room-temperature electron mobilities of 9000–11,000 cm²/V s were achieved. Field-effect transistors (FETs) were fabricated and exhibited good DC and RF characteristics. Previous work demonstrated compressively-strained GaSb quantum wells on similar buffer layers with high hole mobilities and good transistor performance. Hence, a single buffer layer of AlGaAsSb should be suitable for complementary circuits comprised of n-channel FETs based on the mature InGaAs/InAlAs technology and p-channel FETs based on high-mobility antimonides.
The heterostructures studied here are grown by solid-source molecular beam epitaxy (MBE) on semi-insulating (001) InP substrates using a Riber Compact 21T MBE system. A cross-section is shown in Fig. 2. As$_2$ and Sb$_2$ are provided by valved cracking cells. The first layer is 160 nm of In$_{0.52}$Ga$_{0.48}$As lattice matched to InP, followed by a 0.9–2.8 μm In$_{0.52}$Al$_{0.48}$As superlattice of different anion ratios across each wafer. The In$_{0.52}$Ga$_{0.48}$As layer was grown at 1.0 ML/s, and the InGaAs layers were grown at 0.5 ML/s, as calibrated from reflection high-energy electron diffraction oscillations. Based upon previous results on this MBE system, we expect the layer thicknesses to be uniform to within 1% across the 76-mm-diameter substrate if the wafer is rotated. Table 1 includes relevant parameters for the five MBE growths in this study. The wafers were rotated during the growth of all the layers except the Al$_{0.8}$Ga$_{0.2}$Sb$_{1–x}$ barrier layer, which was grown as a short-period superlattice of Al$_{0.8}$Ga$_{0.2}$Sb and Al$_{0.8}$Ga$_{0.2}$As by toggling the As and Sb shutters while the Al and Ga shutters remained open, allowing better control of composition compared to random alloys [13,34,35]. Short-period superlattices may also aid in the reduction of threading dislocations through the film [36]. The anion ratio was adjusted by changing the length of time the Sb shutter is open relative to the As shutter, e.g., 3.7 s Al$_{0.8}$Ga$_{0.2}$Sb/1.3 s Al$_{0.8}$Ga$_{0.2}$As. The buffer layer composition dictates the amount of biaxial strain in the thin pseudomorphic InAlAs and InGaAs layers. The MBE growth temperature is near 450 °C for the InAlAs buffer layer. The temperature is then raised to 510 °C for the Al$_{0.8}$Ga$_{0.2}$As$_{1–x}$, a 5 nm In$_{0.52}$Al$_{0.48}$As spacer, Te delta doping [32], a 4 nm In$_{0.52}$Al$_{0.48}$As barrier, and a 2 nm In$_{0.52}$Ga$_{0.48}$As cap. (We note that InGaAsSb will provide a sufficient conduction band offset for electron confinement in the InGaAs. We included the InAlAs barrier layers to make the active region of the device similar to conventional InP HEMTs. Recent reports on both electron mobilities in InGaAs quantum wells clad by AlAsSb lattice-matched to InP [31].) The Al$_{0.8}$Ga$_{0.2}$As$_{1–x}$, a 5 nm In$_{0.52}$Al$_{0.48}$As, and a 2 nm In$_{0.52}$Ga$_{0.48}$As cap. (We note that InGaAsSb will provide a sufficient conduction band offset for electron confinement in the InGaAs. We included the InAlAs barrier layers to make the active region of the device similar to conventional InP HEMTs. Recent reports on both electron mobilities in InGaAs quantum wells clad by AlAsSb lattice-matched to InP [31].) The Al$_{0.8}$Ga$_{0.2}$Sb$_{1–x}$, a 5 nm In$_{0.52}$Al$_{0.48}$As, and a 2 nm In$_{0.52}$Ga$_{0.48}$As cap. (We note that InGaAsSb will provide a sufficient conduction band offset for electron confinement in the InGaAs. We included the InAlAs barrier layers to make the active region of the device similar to conventional InP HEMTs. Recent reports on both electron mobilities in InGaAs quantum wells clad by AlAsSb lattice-matched to InP [31].)
3. Results and discussion

In Fig. 3, we show the resistivity map for growth #2, with a 15 nm In0.64Ga0.36As channel. The resistivity varied from 197 to 1100 Ω/□. A 5-mm wide strip was cleaved as indicated, yielding thirteen 5 × 5 mm² samples for characterization. The transport results will be discussed later.

The Al0.8Ga0.2As0.33Sb0.67 buffer layer for growth #2 is fully relaxed as confirmed by a reciprocal space map of the asymmetric (224) peaks on sample #3d. In Fig. 4, we show the XRD scan for two pieces (labeled f and j in Fig. 3) from growth #2. The buffer layer consisted of 1554 periods of (3.7 s Al0.8Ga0.2Sb/1.3 s Al0.8Ga0.2As). Peaks are visible for the InP substrate and the short-period superlattice (n = −1, 0, +1). Simulations were generated by adjusting the superlattice thicknesses to match the experimental peak positions. The simulation for sample 2f is shown below the experimental data in Fig. 4. The layer thicknesses were 0.43 nm Al0.8Ga0.2As and 0.86 nm Al0.8Ga0.2Sb, yielding a period of 1.29 nm. Based upon the nominal growth rates, we expect a period of 1.50 nm in the InP substrate and the short-period superlattice (n=0). One interpretation is that the Al and Ga increase, the lattice parameter increases, meaning the tensile strain is smaller, −1.00%. Samples with higher As concentrations in the buffer layer generally exhibited weaker satellite peaks. This indicates that the superlattices are not as well defined but does not necessarily imply lower crystalline quality.

X-ray measurements and simulations were performed on all 34 samples. The AlGaAsSb barrier layers for wafers #3 and #5 were grown with the same superlattice growth times (3.7 s AlGaSb and 1.3 s AlGaAs) and the same As and Sb cell temperatures and valve settings. The growths were performed only one week apart, meaning that the As and Sb fluxes should be similar for the two growths. In Fig. 5, we plot the lattice parameter of the buffer layer vs. the superlattice period for six samples from wafer #3 and seven from wafer #5. They follow the same pattern. As the fluxes of Al and Ga increase, the lattice parameter increases, meaning the fraction of Sb is increasing and the fraction of As is decreasing.\(^{1}\) One interpretation is that the As is preferentially incorporated and enough Sb is incorporated to maintain the 1:1 V:III stoichiometry [38,39]. The solid curve in Fig. 5 was generated by fixing the AlGaAs thickness at 4.2 Å and varying the Al0.8Ga0.2Sb thickness. It matches the trend of the data. The experimental data for wafer #5

1. The ten concentric cells in the MBE are evenly spaced. Ga is adjacent to Al. Our previous work showed that the Al flux varied by about a factor of two across the 76 mm substrates [33]. We expect a similar variation for Ga, and that the Al and Ga mole fractions are approximately 0.8 and 0.2, respectively. We have less knowledge about the As and Sb nonuniformities. The As and Sb cells are adjacent, so we do not expect the difference in the As and Sb gradients to be a dominant factor in the anion mole fractions of the AlGaAsSb.
ranges from (4.7 Å Al0.8Ga0.2As/5.7 Å Al0.8Ga0.2Sb, 5.916 Å) to (3.9 Å Al0.8Ga0.2As/13.8 Å Al0.8Ga0.2Sb, 6.024 Å) with very similar results for wafer #3. Hence, it is primarily the Al0.8Ga0.2Sb thickness that is varying across each wafer. We also observe a small but consistent decrease in the Al0.8Ga0.2As thickness as the superlattice period increases which is reflected in the deviations (data points above the curve for SL period of 17–18 Å and data points below the curve for SL period ~10 Å) from the calculated curve.

In Fig. 6, we plot the mobility vs. lattice parameter for samples from all five growths. Growths #1 and 2 had 15 nm In0.80Ga0.20As channels. Growth #2 had 0.2 s less Al0.8Ga0.2As and 0.2 s more Al0.8Ga0.2Sb per period compared to #1. This should result in an overall shift to larger buffer layer lattice parameters across the wafer. The data in Fig. 6a show that trend, although the range shown for each growth is also a function of which 5 × 5 mm² samples were selected for characterization. For #1, a 3 nm In0.52Al0.48As bottom barrier layer was grown, followed by 5 s under an As2 flux and then the 15 nm channel. For #2, the sequence was 2 nm In0.64Ga0.36As, 30 s As2 interrupt, 2 nm In0.52Al0.48As, 30 s As2 interrupt, 2 nm In0.52Al0.48As, 5 s As2 interrupt, InGaAs channel. The goal of the growth interrupts was to create a smoother starting surface for the channel deposition. The mobility results in Fig. 6a show that the thicker bottom barrier with growth interrupts did indeed result in higher electron mobilities, with values as high as 9900 cm²/V·s at 300 K. Growths #3–5 used the same bottom barrier layer as #2.

In Fig. 6b, we plot the mobility for growths #3 and #4 which had 15 nm In0.64Ga0.36As channels. The growths were nominally identical except that the GaTe shutter was open for 120 s for #4 compared to 60 s for #3. (The AlGaSb/AlGaAs duty cycles were also different but that only affects the range of samples.) As expected, the measured densities for #4 were higher: ~2 × 10¹²/cm² compared to ~1 × 10¹²/cm² for #3. The room-temperature mobilities peak at lattice parameters of 5.97–6.00 Å, similar to the results of growth #2. The highest values were 10,200 cm²/V·s for #3 and 11,300 cm²/V·s for #4. A pure InAs channel was used for growth #5; the mobilities are plotted in Fig. 6c. The pattern is similar to the other growths, with a peak mobility of 9300 cm²/V·s at a lattice parameter of 5.97 Å.

For all three channel compositions (growths #2–5), room-temperature mobilities of 9000–11,000 cm²/V·s were achieved; these values are comparable to the state-of-the-art for InP HEMT structures. Our samples include heterostructures with the InGaAs channel in tension, compression, and nearly lattice-matched to the buffer layer. The mobilities are consistent with the fact that strain effects on the band structure of n-channel quantum wells are expected to be less pronounced than for p-channel quantum wells where compressive strain can give a large mobility enhancement [16]. We achieved high mobilities for both the 888- and 1554-period superlattices, suggesting that the buffer layer thickness is not a critical parameter over the range investigated. The highest values of mobility are found for buffer layer lattice parameters of 5.97–6.00 Å. For smaller or larger lattice parameters, the mobility drops substantially. The decrease for larger lattice parameters was expected because of the large strains in the InAlAs layers. The In0.52Al0.48As barrier layers have a lattice parameter of 5.869 Å and are in tension. For a 6.01 Å buffer layer, the strain is ~2.41%. For buffer layers with smaller lattice parameters, the strain is lower. For the 6.01 Å buffer layer, the channel strains vary from ~1.65% for the In0.64Ga0.36As channel to ~0.55% for the In0.80Ga0.20As channel and ~0.81% for the InAs channel. Given the larger strains for the InAlAs barriers compared to the InGaAs channel and the similar results at the different channel compositions, it seems likely that the InAlAs layers exceed the critical layer thickness for the larger buffer layer lattice parameters, resulting in the formation of additional misfit dislocations and a degradation

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**Fig. 5.** Buffer layer lattice parameter vs. superlattice period for growths #3 and 5. Solid line is calculated (see text).

**Fig. 6.** Room-temperature mobility as a function of buffer layer lattice parameter for samples from all five growths. Peak mobilities are achieved for lattice parameters of 5.97–6.00 Å. Mobility decreases for smaller lattice parameters due to roughness in the buffer layers. For larger lattice parameters, mobility decreases due to high tensile strains (>2%) in the InAlAs barriers.
in mobility. As can be seen in Table 1, high mobilities can be achieved for InAlAs strains up to ~2.2%. Most previous work on strained InGaAs/InAlAs QWs for HEMTs focused on compressive strain in the InGaAs channel. A few studies included strained InAlAs barriers [40,41]. For lattice parameters of 5.92–5.96 Å, strains in the InGaAs and InAlAs layers are smaller. For example, for a 5.94 Å buffer layer an microwave integrated circuit (MMIC) processing [44,45]. These results do not imply that smooth buffer layers cannot be grown in InAlAs barriers [40,41].

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In contrast, samples with buffer layer lattice parameters greater than 5.96 Å have rms values between 0.8 and 1.1 nm. The AFM images reveal surface undulations with amplitudes less than 2 nm. These may arise from the Asaro–Tiller–Grinfeld instability as observed by Gendry et al. and Ponchet et al. [42,43]. These earlier studies examined tensile-strained InGaAs on InP. In our case, the instability probably results from the tensile-strained InAlAs layers grown on fully relaxed AlGaAsSb buffer layers. These rms roughness values of ~1 nm are as good or better than what was measured for InAs-channel HEMT structures on AlGaAsSb buffer layers and GaAs or InP substrates and are fully compatible with monolithic-microwave integrated circuit (MMIC) processing [44,45]. These results do not imply that smooth buffer layers cannot be grown in the 5.92–5.96 Å regime. The optimal growth temperatures for arsenides are generally higher than for antimonides. Higher buffer layer growth temperatures might yield smoother layers in this range with smaller lattice parameters and higher arsenide mole fractions. Our goal in this work, however, is to have buffer layers with lattice parameters near 6.0 Å. Hence, we did not attempt to optimize the growth conditions for the smaller lattice parameters.

Material from growth #2 (In0.64Ga0.36As channel) was processed into HEMTs. The room-temperature sheet density and mobility were 3.5 × 10^12/cm² and 7900 cm²/V·s, respectively. The HEMTs were fabricated using a Pd/Pt/Au alloyed source-drain metallization and a Ti/Au gate metallization using standard lithography and lift-off techniques. A typical set of drain characteristics for a HEMT with a 100 nm gate length is shown in Fig. 7. For this device, the gate width is 31 μm and the threshold voltage is 1.1 V. The low-field source-drain resistance at V_DS = 1.0 V is 1.1 Ω-mm, and the threshold voltage is 0.1 V. A maximum DC transconductance of 300 mS/mm is measured at V_DS = 0.3 V. Using S-parameter measurements at V_DS = 0.8 V and V_GS = 0.4 V, an f_T of 160 GHz and an f_MAX of 150 GHz are obtained on a HEMT with a 90 nm gate length after removal of the gate bond capacitance. This corresponds to an f_T × f_MAX product of 14 GHz·μm. At this bias condition, the gate leakage current was 1.4 μA/mm. The performance of these devices is currently limited by a relatively high contact resistance; reduction of the contact resistance should lead to higher f_T values. The key breakthrough here is that the layers are in tension and hence compatible with p-channel FETs on a common buffer layer.

Our recent work demonstrated high-mobility (1000–1500 cm²/V·s) GaSb QWs for compressive strains as high as 2.3% [14]. Hence, the 5.97–6.00 Å AlGaAsSb buffer layers demonstrated here could be used with GaSb-channel p-FETs. It may be desirable to use InGaAsSb alloys for the p-channel [23]. In that case, buffer layers with larger lattice parameters (6.0–6.1 Å) will be needed to avoid excessive lattice mismatch with the InGaSb. At these larger lattice parameters, however, the lattice mismatch in the In0.52Al0.48As barriers will be too large. An alternative is to use barriers with higher InAs mole fractions. The trade-off is that the conduction band offset will be smaller. To explore this option, we simulated a quantum well with In0.52Al0.48As barriers and an In0.60Ga0.40As well on a 6.05 Å AlGaAsSb buffer layer. The tensile strains in the barrier and channel are ~1.5% and ~1.21%, respectively. The band structure was calculated using the NextNano program [46] and is shown in Fig. 8. The conduction band offset is 316 meV. This value is smaller than the offset for an In0.52Al0.48As/In0.60Ga0.40As QW (570 meV), but may be sufficient for FET applications. It is larger than the 200 meV offset for In0.15Al0.85Sb/InSb MQWs used in high-performance FETs [47]. Higher conduction band offsets could be achieved with InGaAs/AlGaAsSb quantum wells, but this would not take full advantage of the maturity of the InGaAs/InAlAs HEMT technology.

**4. Summary**

We have demonstrated that InGaAs/InAlAs QWs with InAlAs barriers in ~2% tension and InGaAs wells in ~1.5% tension to ~1.5% compression can be successfully grown on AlGaAsSb buffer layers with smooth surfaces, high mobilities, and good FET performance. Using epitaxial regrowth [48], it should be possible to integrate InGaAs n-FETs with compressively-strained (In)GaSb p-FETs on a common AlGaAsSb buffer layer. This combination would have much higher hole mobility compared to the n-InGaAs/ p-InGaAs CMOS option, and higher Ion/Ioff ratios than are likely with an n-InSb/p-InSb system. It could potentially be grown on a Si substrate and incorporate oxides from atomic layer deposition to form n-InGaAs MOSFETs [49] and p-(In)GaSb MOSFETs [20,50,51]. The implementation of epitaxial regrowth on a common lattice-constant buffer layer may ease the integration complexity of
n- and p-channel FETs and represents a viable path towards high performance III–V CMOS logic.

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