

# High-Density 3-D IC Integration Technology for Mixed-Signal Microsystems

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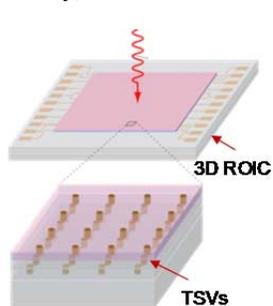
**Abstract:** We present results of the development of high-density 3-D interconnect technology that is applicable to the integration of heterogeneous integrated circuits. The technology relies on through-silicon vias, advanced thinning of silicon wafers and copper/tin-copper solid-liquid diffusion bonding to produce vertical interconnects at a density of  $1 \times 10^6/\text{cm}^2$ . The processing approach allows for the integration of known-good-die in either die-to-die or die-to-wafer bonding configurations, providing the flexibility desirable for the implementation in mixed-signal microsystems.

**Keywords:** 3-D integration; through-silicon vias; 3-D packaging; 3-D IC

## Introduction

High-density 3-D integration technology enables order-of-magnitude reductions in size, weight, and power consumption of mixed-signal microsystems. One example of a microsystem that can benefit from high-density 3-D integration is an infrared focal plane array (FPA) supported by analog and digital readout integrated circuits (ICs) [1].

**Figure 1** illustrates the integration concept. The readout IC (ROIC) is composed of multiple layers of silicon (Si) circuitry, which are integrated by means of vertical interconnects at the individual pixel level. The FPA, which may be fabricated in a compound semiconductor material (e.g., mercury-cadmium-telluride [HgCdTe]), is hybridized with the ROIC in a face-up configuration. Electrical signals created in individual photodiodes are transferred to the ROIC, where they undergo

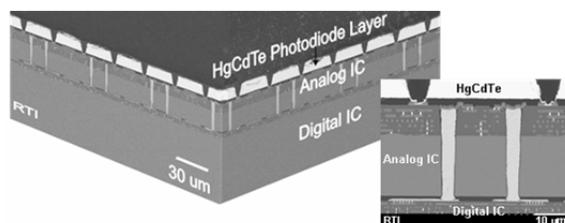


**Figure 1.** 3-D integration applied to FPA devices.

amplification, further processing, analog-to-digital conversion, and are directed through a multiplexer to the output.

**Figure 2** shows a two-plane cross-section scanning electron micrograph (SEM) of a previously reported 3-D integrated heterogeneous circuit which combines full-thickness digital IC die, 30  $\mu\text{m}$ -thick analog IC and 10  $\mu\text{m}$ -thick HgCdTe FPA [2–5]. The pixel size is 30  $\mu\text{m}$  by 30  $\mu\text{m}$ . The layers were integrated using vertical interconnects 4  $\mu\text{m}$  in diameter. These high-aspect-ratio through-silicon

vias (TSVs) were insulated using a polymer dielectric and were filled with copper (Cu) by metal-organic chemical vapor deposition (MOCVD).



**Figure 2.** Cross-section SEM of a heterogeneous 3-D IC comprising a 3-D ROIC and an FPA.

The FPA device shown in **Figure 2** implemented advanced signal processing that was enabled by (1) the increased real estate for pixel electronics gained by using two 3-D integrated layers of ICs instead of one IC layer as in 2-D ROICs and (2) the ability to separate analog from digital functions, instead of combining them in a 2-D mixed-signal system-on-chip. These attributes resulted in an approximately 3X decrease in the size of the FPA and about a 3X decrease in the power required to operate the device, as compared with an FPA based on a 2-D ROIC with comparable functionality [6].

In this paper, we describe a scaled-down, second-generation 3-D integration process that can support a vertical interconnect density of  $1 \times 10^6/\text{cm}^2$ , such as would be required for FPAs with 10  $\mu\text{m}$  pixel sizes. This small pixel pitch requires a significant reduction in the TSV diameter, as 4  $\mu\text{m}$  diameter vias would occupy too large a portion of the pixel to provide a design advantage. The first-generation process (**Figure 2**) uses a vias-last approach which is not easily scalable to smaller via diameters due to difficulties in creating small-diameter high-aspect-ratio vias in the approximately 10  $\mu\text{m}$ -thick silicon dioxide ( $\text{SiO}_2$ ) of the multilevel metal structure of a modern IC. The second-generation process is therefore designed to use a vias-middle approach in which the TSV fabrication is performed by a foundry as part of the bulk complementary metal-oxide semiconductor (CMOS) IC manufacture. **Figure 3** is a schematic representation of the 3-D integration flow. The TSVs are inserted between front-end-of-line and back-end-of-line (BEOL) portions of the bulk CMOS process, avoiding the need for etching of high-aspect-ratio vias in BEOL  $\text{SiO}_2$ . Finished analog IC wafers then undergo thinning and backside processing in preparation for the stacking operation. In parallel, digital

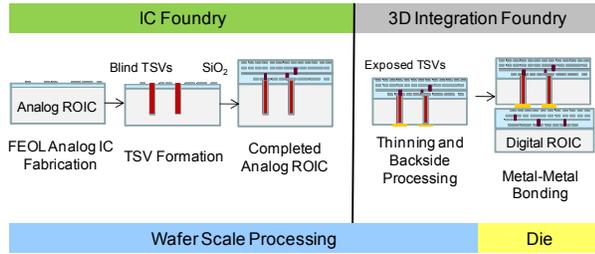
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14. ABSTRACT <b>We present results of the development of highdensity 3-D interconnect technology that is applicable to the integration of heterogeneous integrated circuits. The technology relies on through-silicon vias, advanced thinning of silicon wafers and copper/tin-copper solidliquid diffusion bonding to produce vertical interconnects at a density of 1×106/cm2. The processing approach allows for the integration of known-good-die in either die-to-die or die-to-wafer bonding configurations, providing the flexibility desirable for the implementation in mixed-signal microsystems.</b>			
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IC wafers are processed to prepare them for the stacking operation. Both wafers are diced, and known-good-die (KGD) from analog IC wafers are bonded to KGD from digital IC wafers using metal-metal bonds.

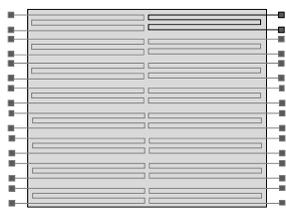


**Figure 4.** High-level schematic of the vias-middle 3-D integration process flow.

One of the enabling technologies for the vias-middle approach is a temporary wafer bonding system that provides support for thin wafers through thinning and backside processing. Unlike the vias-last process where interconnects are implemented after chip stacking, in the vias-middle approach, fabrication processes such as SiO<sub>2</sub> deposition, chemical-mechanical polishing (CMP), photolithography, electroplating, and solvent cleans must be carried out on the thinned analog wafer. This sequence requires a temporary wafer bond that can support very thin wafers through mechanical polishing, a combination of temperature and vacuum steps, and a variety of wet processes. As part of this demonstration lot, two different temporary wafer bonding systems were evaluated for their compatibility with the 3-D integration process.

The proof-of-concept of the 3-D integration process described in this paper employed area arrays of TSVs with a nominal diameter of 2 μm, positioned on a 10 μm pitch. The TSV array was used, in conjunction with area array Cu/Sn-Cu bonds, to interconnect two passive Si die serving as surrogates for digital (full-thickness) bottom die and thin (approximately 20 μm thickness) analog IC top dies.

### Test Vehicle Design and Fabrication

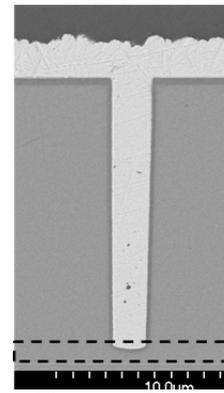


**Figure 5.** Configuration of daisy chains of vertical interconnects.

The two-die stack test vehicle incorporates area arrays of TSVs and Cu/Sn-Cu bonds connected into daisy chains. The vertical interconnects are arrayed in a 640×512 format with a 10 μm pitch. **Figure 4** shows the configuration of the daisy chains. Each test channel contains 1,272 interconnects from four neighboring rows. There are 256 test channels.

For the fabrication of the test vehicle, we used 150 mm diameter Si wafers. Surrogate analog IC wafers were of the silicon-on-insulator (SOI) type to emulate a specific CMOS process from a specific foundry. The thickness of the top

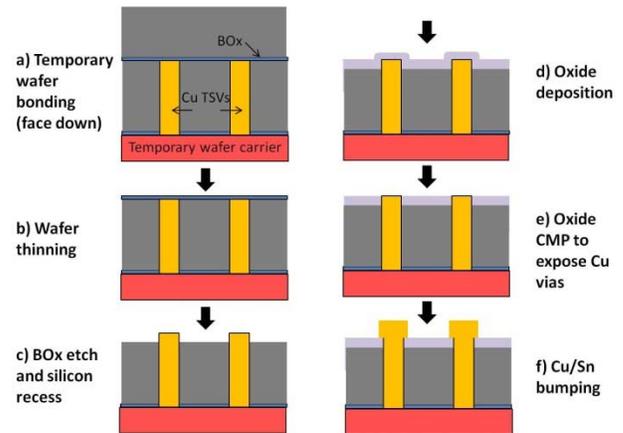
Si layer was 15 μm, and the thickness of the buried oxide (BOX) was 2 μm. For the purpose of the proof-of-concept demonstration of the full 3-D integration process, TSVs were fabricated in-house, whereas in the ultimate implementation, the TSV module will be executed by a CMOS foundry. The proxy fabrication process employed a conformal SiO<sub>2</sub> layer to serve as the TSV insulator and MOCVD Cu as the TSV metallization. **Figure 5** shows a cross-section of a monitor wafer following the deposition of Cu. The dashed lines indicate the position of the BOX layer in SOI device wafers.



**Figure 3.** Cross-section SEM of a TSV in a monitor wafer.

Following the TSV metallization, the Cu overburden on the top surface of the wafer was removed using CMP, leaving Cu in only the blind via. Thin tungsten layers were subsequently deposited on the top surface and patterned using reactive ion etching (RIE) to form the top links of the daisy chain connections.

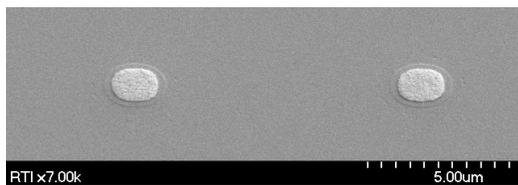
**Figure 6** shows the details of the processing that the wafer with TSVs undergoes in preparation for stacking.



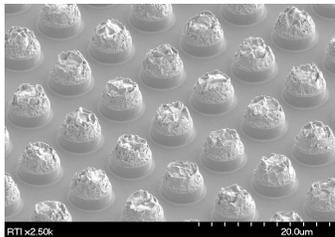
**Figure 6.** Schematic of the process for the top wafer.

The process begins by mounting the top wafer face down on a temporary carrier, using a layer of adhesive that is applied onto the carrier as shown in **Figure 6a**. We used Si wafers as carriers, and one of two temporary adhesive materials: TMAT™ (Thin Materials AG) and WaferBond™ (Brewer Scientific). The top wafer was then thinned from the back by backgrinding followed by high-rate wet spin etching (**Figure 6b**). The BOX layer provides an effective etch stop for the thinning. At the end of the thinning process, the device wafers were 17 μm thick, 15 μm of which was Si and 2 μm was the buried SiO<sub>2</sub> layer. In the next step (**Figure 6c**), the BOX layer was removed

using a selective RIE process. The wafers were then exposed to SF<sub>6</sub> plasma to recess the Si surrounding the insulated Cu TSV. Next, a conformal SiO<sub>2</sub> layer was deposited using a plasma-enhanced chemical vapor deposition (PECVD) technique to passivate the surface and the exposed portion of the TSVs. Then, as shown in **Figure 6d**, CMP was used to re-planarize the top surface. These steps produced a planar surface with TSVs embedded in a 1 μm-thick layer of SiO<sub>2</sub>. The fabrication of Cu/Sn bond pads, described in detail elsewhere [7], completes the backside processing of the analog surrogate wafer (**Figure 6e**). The Cu/Sn bond pads were 5 μm thick and 6 μm wide. **Figure 7** shows an SEM micrograph of the backside of the analog surrogate wafer following the CMP step that exposes TSVs, and **Figure 8** shows a micrograph of electroplated Cu/Sn bond pads.



**Figure 7.** SEM micrograph of the back surface of thin wafers following CMP of PECVD SiO<sub>2</sub>.



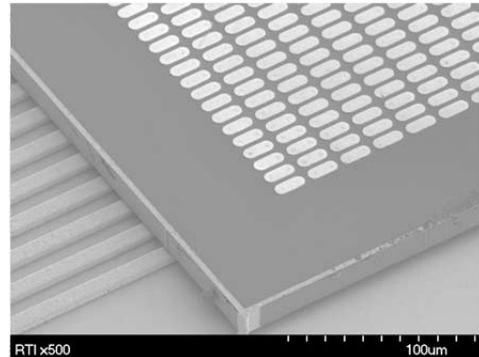
**Figure 8.** SEM micrograph of Cu/Sn pads electroplated over the TSVs visible in Figure 7.

Surrogate digital wafers that provide bottom die for the stack underwent processing to form routing lines for daisy chains and probe pads. The process includes the deposition of a titanium (Ti)/Cu seed layer on wafers with a 0.3 μm-thick thermal SiO<sub>2</sub> layer. Cu bond pads were fabricated by electroplating Cu into a photoresist template. The resulting bond pads were 4 μm thick and 6 μm wide.

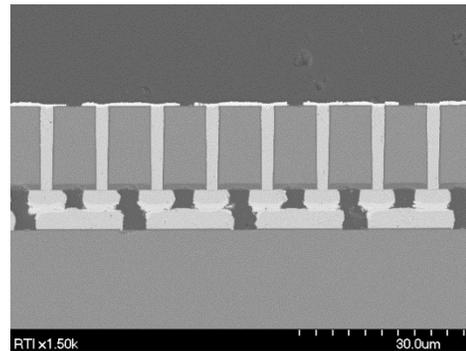
Completed analog and digital surrogate wafers were diced. During the dicing operation, the analog surrogate remained on the carrier wafer. To maximize the die yield, we applied a dice-by-etch technique to singulate the wafers bonded with TMAT™. This approach involves the creation of trenches in the dicing streets of the thinned wafers using RIE. The second step employs standard dicing, in which the blade cuts through the adhesive and the thick carrier, but does not come into contact with the thin Si layer.

Analog surrogate and digital surrogate die were integrated using solid-liquid Cu/Sn-Cu diffusion bonding at a temperature of 250°C in a nitrogen gas (N<sub>2</sub>) ambient atmosphere [8]. We noted that the WaferBOND adhesive flowed during bonding and squeezed out onto the bottom

chip. However, it provided adequate support during the bonding process to form bonds across all parts of the array. With both TMAT™ and WaferBOND™, the carrier die could be easily removed from the thinned die after bonding. **Figure 9** presents an SEM micrograph of the top surface of a die stack. **Figure 10** shows a cross-section of an integrated die pair.



**Figure 9.** SEM of a bonded die pair after the carrier release.



**Figure 10.** Cross-section view of a bonded die pair.

The mechanical strength of integrated die pairs was estimated through the measurement of the shear force required to separate analogous but full-thickness monitor die pairs, using a Nordson DAGE die-shear apparatus. The value of the die shear force was greater than 10 kG, translating into a die shear strength of greater than 11 MPa, supporting previously published data [8].

### Electrical Test Results

**Table 1** shows the summary of electrical tests of daisy chains connecting the bonded die pair. As indicated earlier, the test vehicle contains 256 test channels, each comprising 1,272 vertical interconnects. The results are grouped in two columns, corresponding to the two different temporary adhesive materials that were used to mount the analog surrogate wafer to the carrier. For each of the materials, the table lists values of channel resistance measured in a two-probe configuration, the number of open (non-functional) channels, the channel operability, defined as the ratio of non-functional channels to the total number of tested channels, and the calculated operability in the 640×512 array of interconnects. The measured channel resistance contains contributions from the routing lines, TSVs, Cu/Sn-

Cu bonds and probe-to-pad contacts. As expected, the routing line contribution dominates the channel resistance.

	WaferBond 9001	TMAT
CuSn/Cu Bond Conditions	250°C for 180sec	250°C for 180sec
No. of Bonded Die Tested	8	9
Channel Resistance ( $\Omega$ )	596 - 721 mean=660	603 - 652 mean= 640
No. of Open Channels	0 - 5 avg. = 2	1 - 23 avg. = 8
Channel Electrical Yield (%)	98.0 - 100 avg. = 99.2	91.0-99.6 avg. = 96.9
Extrapolated Interconnect Electrical Bond Yield (%)	99.99	99.99

**Table 1.** Results of electrical tests of daisy chains connecting bonded die pairs. The results are shown for two adhesives that were used to mount analog surrogate wafers to carriers.

As seen in **Table 1**, both of the process splits resulted in interconnect operabilities greater than 99.99%, satisfying operability requirements of the intended application.

We used four-probe measurement to obtain values of resistance ( $R_i$ ) of interconnect links consisting of a TSV and a metal routing layer. The fit of an electrical model to the experimental data gave  $R_i$  values ranging from 0.3–0.4  $\Omega$ . By using leakage current measurements taken at 5 V between adjacent channels of TSV chains, the insulation resistance per TSV was estimated to be greater than 100 G $\Omega$ .

## Conclusions

We successfully integrated two Si die with high-density area array vertical interconnects consisting of TSVs and Cu/Sn-Cu bonds. The passive test vehicle emulates a 3-D IC composed of digital and analog ICs for use as an advanced readout circuit for high-performance infrared imaging devices. The vertical interconnects were arrayed in a 640×512 format, with a pixel size of 10  $\mu\text{m}$  on a side. We have demonstrated the full integrated process, the key parts of which involve Si wafer thinning to 20  $\mu\text{m}$ , film deposition and patterning on the back surface of the thinned wafers while they are still mounted on carriers, Cu/Sn-Cu bonding, and the carrier release. We have demonstrated operabilities exceeding 99.99% for both types of temporary adhesives that were used for mounting wafers on the carriers. The vertical interconnect resistance was found to be in the tens of m $\Omega$  range, well within typical specifications of an imaging array. Similar architecture and integration processes can be applied to other advanced mixed-signal microsystems.

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