

# Reverse gate bias-induced degradation of AlGaN/GaN high electron mobility transistors

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A threshold reverse bias of  $\sim 21$  V was observed leading to a sharp increase in the gate current of AlGaN/GaN high electron mobility transistors biased at low source-drain voltage (5 V). The gate current increases by one to two orders of magnitude at this bias, corresponding to an electric field strength around  $1.8$  MV cm<sup>-1</sup>. The gate current increased by roughly five orders of magnitude after step-stressing the gate bias from 10 to 42 V in 1 V increments for 1 min at each bias. The drain current was also decreased by  $\sim 20\%$  after this step-stress cycle. The photoluminescence and electroluminescence intensity from the semiconductor is decreased along the periphery of the gate region after stressing and transmission electron microscopy shows a thin native oxide layer under the gate and this disappears as the gate metal reacts with the underlying AlGaN. © 2010 American Vacuum Society. [DOI: 10.1116/1.3491038]

## I. INTRODUCTION

The promising performance of AlGaN/GaN high electron mobility transistors (HEMTs) under high frequency and high output power density has intensified efforts to understand the reliability and degradation mechanisms under different operating conditions.<sup>1–18</sup> At high source-drain biases, crystallographic defects and even cracking occur as a result of the inverse piezoelectric effect.<sup>2,3,7,12,13</sup> Under these conditions, the presence of a strong electric field in the piezoelectric GaN and AlGaN leads to additional mechanical stress that is concentrated in the AlGaN barrier layer. At a high enough field, the change in AlGaN elastic energy can produce extended and point defects. During on-state stressing, other degradation mechanisms observed include thermally induced gate contact degradation and creation of traps under the gate

and in the gate-drain access region.<sup>1,4–6,8–10</sup> The degradation under off-state conditions is clearly electric field driven, with devices of different gate lengths failing at different drain-source biases but similar electric field thresholds. It is likely that different bias stressing conditions exacerbate different failure mechanisms because of the presence or absence of high fields, hot electron populations, or temperature increases due to self-heating. For example, in the on-state stress condition, there may be strong self-heating of the HEMT and a high density of hot electrons in the channel, but accompanied by smaller vertical electrical field and low leakage through the gate. By sharp contrast, operating in the so-called off-state with the channel pinched off increases the vertical electric field component and gate leakage, but should reduce contributions from hot electrons and self-heating.<sup>13,19,20</sup>

In this article, we report on the degradation of AlGaN/GaN HEMTs under step-stressing of the gate reverse bias.

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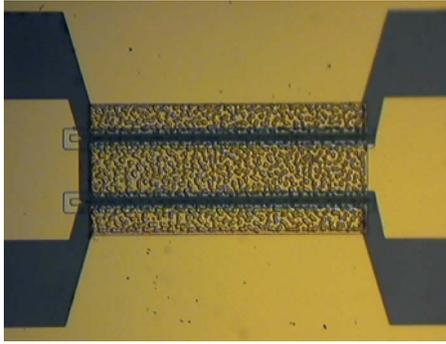


FIG. 1. (Color online) Optical micrograph of typical HEMT device with dual gate. In terms of scale, the gate widths are  $150 \mu\text{m}$ .

The devices exhibit a threshold gate bias for the onset of increased gate leakage. The degradation of gate current is irreversible and is accompanied by a small decrease in drain-source current. Electroluminescence (EL) imaging shows the creation of dark regions along the gate periphery and a reduction in photoluminescence (PL) intensity from the degraded region. These results are consistent with the formation of nonradiative traps in the gate region. Transmission electron microscopy (TEM) shows a degree of gate sinking into the underlying AlGaN.

## II. EXPERIMENT

The HEMT device structures were grown on semi-insulating 6H SiC substrates and consisted of a thin AlN nucleation layer,  $2.25 \mu\text{m}$  of Fe-doped GaN buffer,  $15 \text{ nm}$  of  $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ , and a  $3 \text{ nm}$  undoped GaN cap. On-wafer Hall measurements showed sheet carrier concentrations of  $1.06 \times 10^{13} \text{ cm}^{-2}$ , mobility of  $1907 \text{ cm}^2/\text{V s}$ , and sheet resistivity of  $310 \Omega/\text{sq}$ . The HEMTs employed dry etched mesa isolation, Ti/Al/Ni/Au Ohmic contacts alloyed at  $850^\circ\text{C}$  (contact resistance of  $0.3 \Omega \text{ mm}$ ), and dual-finger Ni/Au gates patterned by lift-off. The gate lengths ranged from  $0.1\text{--}0.17 \mu\text{m}$ , but in these experiments we fixed the gate length at  $0.14 \mu\text{m}$ . Both source-to-gate gap and gate-to-drain distances were  $2 \mu\text{m}$ . These  $0.14 \mu\text{m}$  gate length devices with  $2 \times 150 \mu\text{m}^2$  gate width exhibited typical maximum drain currents of  $1.1 \text{ A/mm}$ , extrinsic transconductance of  $250 \text{ mS/mm}$  at  $V_{DS}$  of  $10 \text{ V}$ , threshold voltage of  $-3.9 \text{ V}$ ,  $f_T$  of  $60 \text{ GHz}$ , and  $f_{\text{max}}$  of  $90 \text{ GHz}$ . With the devices biased at  $28 \text{ V}$ , the output power is about  $5 \text{ W/mm}$  and the power added efficiency was  $30\%$  at  $10 \text{ GHz}$ . Figure 1 shows an optical micrograph of a typical HEMT used in these experiments.

Five devices were step-stressed biased at each voltage in the dark at room temperature with  $-10$  to  $-42 \text{ V}$  reverse gate voltage at a fixed source-drain bias of  $5 \text{ V}$ . The devices were stressed for  $60 \text{ s}$  at each voltage step. Self-heating effects were negligible based on the low drain-source currents under our test conditions,<sup>1</sup> a fact supported by thermal simulations. All the electrical data were measured by an HP 4156C semiconductor parameter analyzer. The devices were also examined by cross-sectional TEM, and high spatial res-

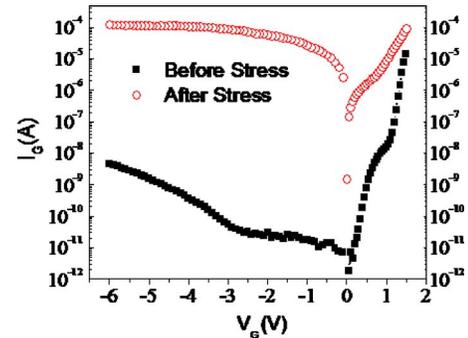


FIG. 2. (Color online) Gate  $I$ - $V$  curves before and after stress.

olution EL and PL before and after stressing. EL imaging using a liquid nitrogen-cooled charge-coupled device (CCD) camera with a  $50\times$  magnification and  $10 \text{ s}$  integration time was used to examine the devices before and after stressing.<sup>21</sup> No optical filters were used, so the images depict the entire spectral range of the CCD camera ( $200\text{--}1100 \text{ nm}$ ). Photoluminescence spectroscopy was performed at room temperature using an Ar-ion laser (excitation power of  $40 \text{ mW}$ , spot size  $<1 \mu\text{m}$ ), operated in single line mode, emitting the  $351 \text{ nm}$  line. Photoluminescence was collected through an optical fiber and was detected via an Ocean Optics HR-4000 spectrometer using a  $10 \text{ ms}$  integration time. For the EL experiments, the stressed and unstressed devices were biased at  $V_{ds}=5 \text{ V}$  and  $V_g=-2 \text{ V}$ . Finally, we also used automatically tuned linear algebra software<sup>22</sup> (ATLAS/BLAZE) to simulate the electric field at different gate biases.

## III. RESULTS AND DISCUSSION

Figure 2 shows the gate current-voltage ( $I$ - $V$ ) characteristics before and after the step-stress cycle. The reverse leakage current is increased almost five orders of magnitude and the degradation was irreversible, as judged by testing the same device on subsequent days. Both before and after stress, the forward  $I$ - $V$ 's exhibited plateaus typical of the presence of both thermionic field emission and thermionic emission mechanisms of current transport.<sup>23</sup> The changes in barrier height and diode ideality factor were small ( $\sim 5\%$

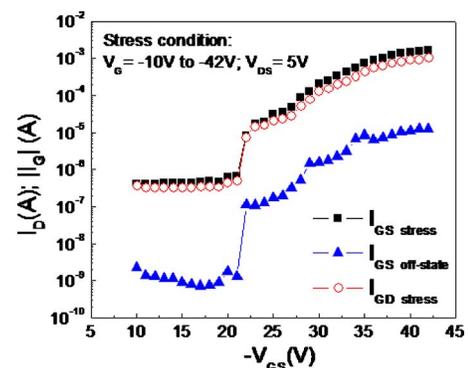


FIG. 3. (Color online) Off-state gate current, stress gate current, and stress drain current as a function of stress gate voltage.

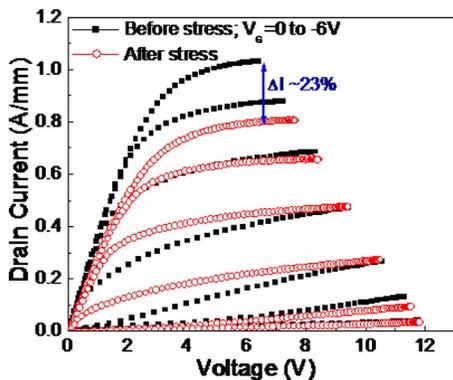


FIG. 4. (Color online) Drain *I*-*V* curves before and after stress.

reduction in barrier height and similar increase in ideality factor). Our results are consistent with past reports which show only a small change in these parameters but a large increase in gate leakage during reverse bias stressing.<sup>2,13,18</sup>

Figure 3 shows a threshold gate bias around 21+/-1 V for the onset of a sharp increase in gate and drain currents. This is similar to the value reported by Joh and del Alamo<sup>13</sup> and the degradation in their work was ascribed to crystallographic defects caused by the inverse piezoelectric effect.<sup>2,7</sup> The electric field strength at this gate bias is around 1.8 MV cm<sup>-1</sup> based on ATLAS simulations. Note that the increase in gate current is accompanied by a small decrease (~23%) in the drain current, as shown in the output characteristics in Fig. 4 due to an increase in on-state resistance. Similarly, the transfer characteristics in Fig. 5 show a reduction in maximum transconductance from 250 to 210 mS/mm as a result of the gate bias stress cycle and a shift in threshold voltage of ~0.6 V. In terms of increasing the bias at which degradation commences, a change in the Al composition and use of field plates are two features that could be adjusted to achieve this increase.

The degraded devices were examined by PL, EL, and TEM.<sup>21,24,25</sup> Representative PL spectra are shown in Fig. 6 (top) for an open area on an unstressed HEMT (labeled as “bulk”) and also for the gate periphery regions before and after the stress cycle. Note the two peaks due to the GaN centered around 366 nm and the AlGaIn at 352 nm. The bottom of Fig. 6 shows spectra taken before and after stress-

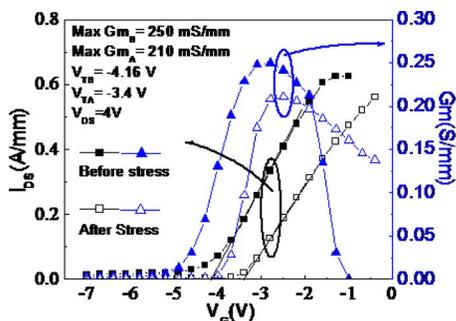


FIG. 5. (Color online) Transconductance characteristic of the AlGaIn/GaN HEMTs before and after stress.

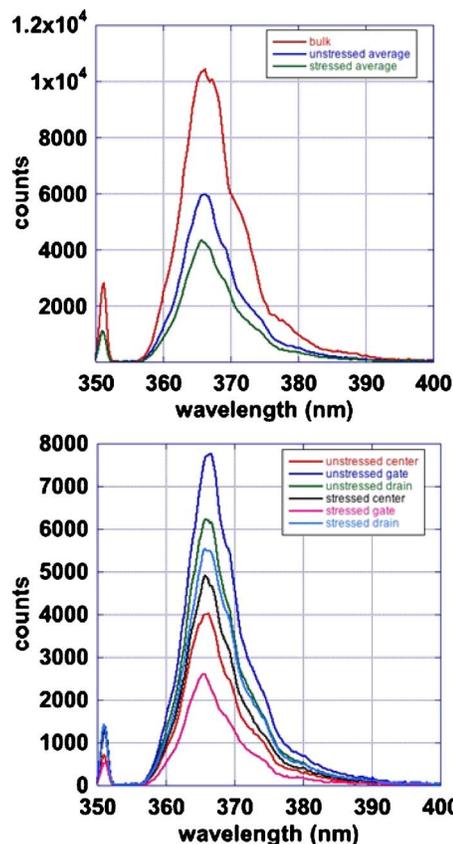


FIG. 6. (Color online) PL spectra of stressed and unstressed devices.

ing near the center and gate and drain ends of the gate. In all cases, the PL intensity is degraded after stressing, indicative of the introduction of nonradiative centers in the GaN and AlGaIn.

Electroluminescence images from both the stressed and unstressed devices are shown in Fig. 7. The EL is very uniform along the unstressed gate finger, but there is a dark spot along the stressed finger. Furthermore, EL intensity on both fingers decreased as  $V_{ds}$  was decreased to 1 V at constant  $V_g$ , and was eliminated when  $V_g$  was changed to  $-5$  V at constant  $V_{ds}$ . Such images have been attributed to hot electron effects due to the high field at the gate edge.<sup>2,3</sup> The dark spot is likely where the degradation begins and would become a failure point if one continued to stress the device. Due to the

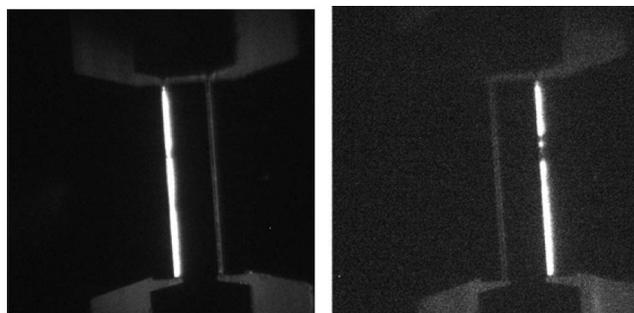


FIG. 7. EL images of stressed (right) and unstressed (left) gate fingers.

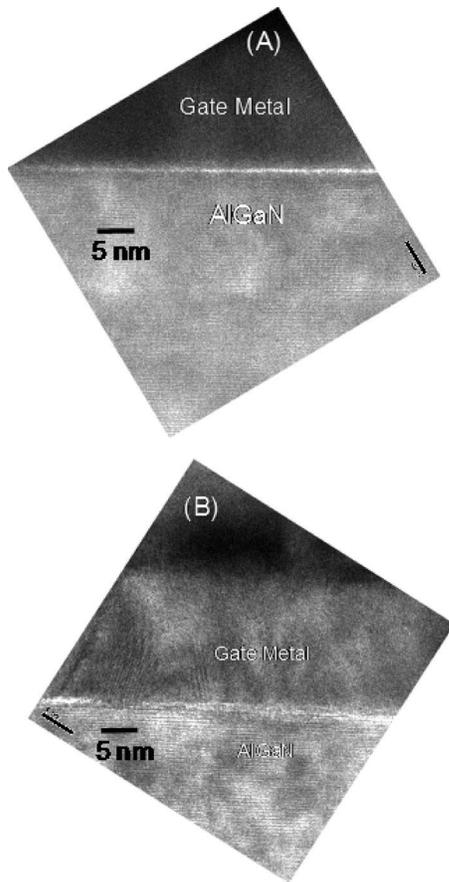


FIG. 8. Cross section TEM images of gate finger before (a) and after (b) stress.

small source-drain gap, it was not possible to resolve if the emission was uniform across the gate-drain region, or stronger at either the gate or drain edge.

TEM images of the gate stack before (a) and after (b) step-stressing are shown in Fig. 8. The native oxide present under the gate is after stressing and the gate is still stable but shows evidence of moving into the underlying AlGaIn. This is consistent with the fact that the Schottky properties of the gate contact were not severely changed as a result of the stressing and there was no intermixing of the gate metals. Note that we did not observe crack formation on the drain side of the gate edge, which is an extreme manifestation of the inverse piezoelectric mechanism when the devices are stressed for extended periods.<sup>2,3</sup> However, changes in device performance are consistent with the creation of traps in the AlGaIn barrier layer, which is the initial signature of the mechanical stress induced by the inverse piezoelectric effect.<sup>2,3,7</sup>

#### IV. SUMMARY AND CONCLUSIONS

At the high electric fields present under reverse bias stressing of AlGaIn/GaN HEMTs, the devices exhibit a five order of magnitude increase in gate current and a much smaller ( $\sim 20\%$ ) decrease in drain-source current. There is a threshold bias of  $\sim 21$  V at which a sharp increase in gate leakage current is observed and this is accompanied by a decrease in both PL and EL intensity from around the gate region. The results are consistent with nonradiative trap formation under and around the gate, which does not show much change in barrier height as a result of the step-stressing.

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