

# 11.72 cm<sup>2</sup> SiC Wafer-scale Interconnected 64 kA PiN Diode

M. Snook<sup>1,a</sup>, H. Hearne<sup>1</sup>, T. McNutt<sup>2</sup>, N. El-Hinnawy<sup>1</sup>, V. Veliadis<sup>1</sup>, B. Nechay<sup>1</sup>, S. Woodruff<sup>1</sup>,  
R. S. Howell<sup>1</sup>, D. Giorgi<sup>3</sup>, J. White<sup>4,b</sup>, S. Davis<sup>4</sup>

<sup>1</sup>Northrop Grumman Electronic Systems, 1212 Winterson Rd., Linthicum, MD 21090, USA

<sup>2</sup>Now with APEI Inc., 535 W Research Center Blvd. Suite 209, Fayetteville, AR 72701, USA

<sup>3</sup>Omnipulse Inc., 6355 Nancy Ridge Drive, San Diego, CA 92121, USA

<sup>4</sup>US Army TARDEC, 6501 E. 11 Mile Road, Warren, MI 48397-5000, USA

<sup>a</sup>megan.snook@ngc.com, <sup>a</sup>ph. 410-765-4743 (corresponding author), <sup>b</sup>joseph.d.white74.civ@mail.mil

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## Abstract

**To meet the large current handling requirements of modern power conditioning systems, paralleling of a large number of devices is required. This increases cost and complexity through dicing, soldering, and forming multiple wire bonds. Furthermore, paralleling discrete devices increases package volume/weight and reduces power density. To overcome these complexities, PiN diodes were designed, fabricated at high yields, tested, and interconnected on a three-inch 4H-SiC wafer to form an 11.72 cm<sup>2</sup> active area wafer-scale diode. The wafer-scale diode exhibited a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>. Under pulsed conditions, the peak current through the wafer-scale diode was 64.3 kA with a forward voltage drop of 10.3 V. The dissipated energy was 382 J and the calculated action exceeded 1.7 MA<sup>2</sup>-s. Preliminary development of high voltage interconnection has produced quarter wafer interconnected PiN diodes with active areas of 2.2 cm<sup>2</sup> and 3.1 cm<sup>2</sup>, exhibiting breakdown voltages of 4.5 kV and 4.0 kV, respectively.**

## INTRODUCTION

Silicon carbide (SiC) is ideally suited for power conditioning applications due to its high temperature capability, high thermal conductivity, and high electric field strength. Although significant progress has been made in optimizing SiC material quality and fabrication, material and processing defects presently set an upper limit on SiC device area that can be fabricated at good yields. While a gate-turn-off (GTO) thyristor of 1 cm<sup>2</sup> has recently been reported [1], high yielding SiC chip sizes are still limited to 0.1 - 0.5 cm<sup>2</sup> and high power applications necessitate a large number of discrete devices operated in parallel [2]. This increases cost and complexity through wafer dicing, device soldering, and forming multiple wire bonds. The latter introduce stray inductance, while high voltage operation dictates large "keep-out" distances between devices that increase package

volume/weight and reduce power density. In addition, discrete device current sharing typically necessitates ballast resistors which further increase package volume/weight and overall complexity.

The high power potential of SiC wafers can be realized with the wafer-scale interconnection methodologies, where discrete devices are fabricated on a SiC wafer each with a termination region for high breakdown voltage performance. Discrete devices are then tested and screened for predetermined electrical specifications and those that meet these criteria are interconnected with metallization to form a large area, wafer-scale device [3]. To overcome the drawbacks of device paralleling, discrete PiN diodes were fabricated at high yields, and diodes that passed electrical screening were successfully interconnected on wafer to form a wafer-scale PiN diode with an active area of 11.72 cm<sup>2</sup>.

## DISCRETE PiN DIODE DESIGN AND FABRICATION

Design of the discrete diodes is critical to maximizing yield and active area of the final interconnected wafer-scale diode. A discrete diode size that is smaller than optimal ensures excellent wafer yields, however, much of the total area is wasted with inactive regions such as edge termination. Low yields are expected from the design of a very large discrete diode size due to the detrimental effects of material and processing defects. Based on defect distribution calculations [4], a diode active area of 0.09 cm<sup>2</sup> (0.17 cm<sup>2</sup> total area) was chosen as the optimal size for maximizing area and yield. This size allows for fabrication of 207 PiN diodes on a three-inch 4H-SiC n+ substrate. For high voltage operation, n- drift epitaxial layers of 20 μm thickness are utilized with doping of 5 x 10<sup>14</sup> cm<sup>-3</sup>. A beveled edge mesa was etched into the SiC and defined the anode region of the diode. A single aluminum implant done at 1000 °C formed a junction termination extension (JTE), which allows for blocking voltage close to the theoretical value (determined by the drift epitaxial layer characteristics) by minimizing field crowding at the device periphery. Subsequently, the wafer

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was annealed at >1600 °C for activation of dopants and recrystallization of ion-bombarded SiC. The diode anode and cathode regions were metallized with Ni, which was sintered at 900-1000 °C for ohmic contact formation. A detailed cross-sectional schematic of the PiN diode device can be seen in Figure 1.

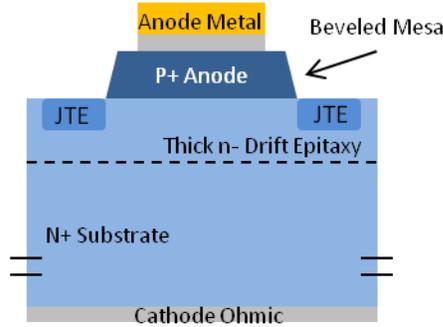


Figure 1: Schematic cross-section of a discrete PiN diode prior to wafer-scale interconnection.

An initial breakdown voltage test was performed following anode metallization. Discrete diodes were selected for interconnection based on limits set for threshold voltage at a leakage current density of 0.2 mA/cm<sup>2</sup>, and are shown in green on the breakdown voltage wafer map depicted in Fig. 2. An overall breakdown voltage yield of 83% was achieved. The diodes selected demonstrate sharp onsets of breakdown voltage as illustrated in Fig. 3. Diodes with higher pre-breakdown leakage currents and softer breakdown knees were excluded due to defect related long term reliability concerns [5]. Also excluded were diodes located at the wafer edges due to the higher defect densities in these areas.

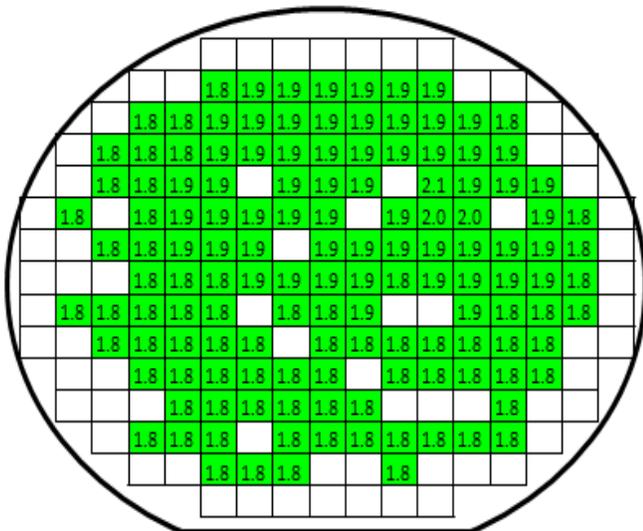


Figure 2: Wafer map of PiN diode breakdown voltage (values shown are in kV). The yield is 83% (diodes in green pass) at a leakage current density of 0.2 mA/cm<sup>2</sup>.

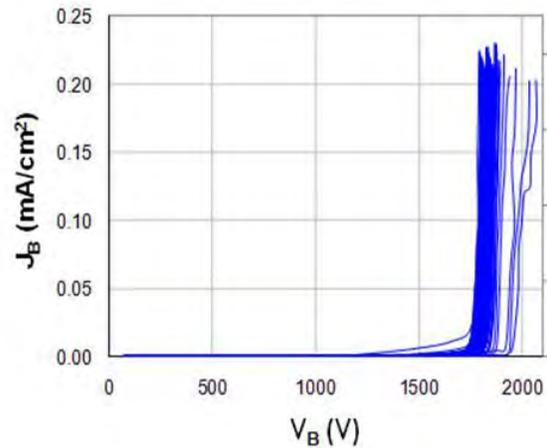


Figure 3: PiN diodes selected for wafer-scale interconnection demonstrate low leakage currents and sharp onsets of voltage breakdown.

#### WAFER-SCALE INTERCONNECTION

A thick dielectric film, designed to withstand high voltage operation, was uniformly deposited on the wafer following selection of good discrete diodes (diodes that passed electrical testing). A lithographic process patterned vias over the good discrete diodes in photoresist, which was used as an etch mask. Subsequently, reactive ion etching (RIE) opened vias in the dielectric to contact the anodes of the good discrete diodes, Fig 4. Each wafer has a unique via interconnection pattern due to variations in good discrete diode locations. In a highly manufacturable process, the lithographic stepper is programmed to expose the different via pattern of each wafer. Programming of the lithographic stepper allows for exposure of a unique via interconnection pattern, without additional processing cycle-time.

Diodes that failed breakdown voltage testing remained inactive under the dielectric, as shown in Fig 4. A final metallization step interconnected the anodes of the qualified discrete diodes to form a large area wafer-scale diode, as shown in Figure 5 (a).

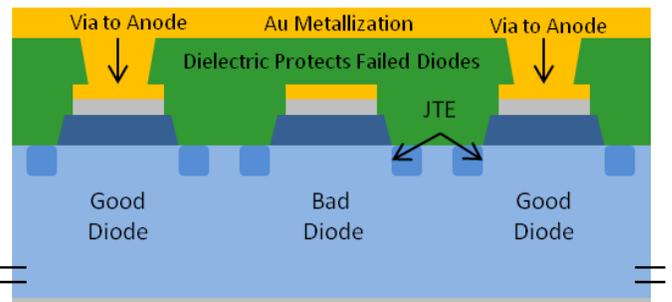


Figure 4: Anodes of PiN diodes passing breakdown voltage testing are interconnected across the wafer. Diodes that fail breakdown voltage testing are not interconnected and remain inactive under dielectric.

## RESULTS AND DISCUSSION

Interconnection of 135 discrete diodes gives an active area of 11.72 cm<sup>2</sup> for the wafer-scale diode shown in Fig. 5 (a). Wafer-scale reverse voltage measurements demonstrated a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>, Fig. 6. This confirmed that wafer-scale interconnection of discrete diodes does not compromise the breakdown characteristic of the wafer-scale diode. A schematic of a “hockey puck” package used in pulsed wafer-scale testing is shown in Fig. 5 (b). Once assembled, the package was potted and pressurized with SF<sub>6</sub> to 30 psi for high voltage insulation. Centering rings were used to ensure even pressure. Voltage probe contacts extending radially through the package were used to measure voltage drops. This minimized the package inductance contribution to the voltage measurements. The center of mass of the wafer was on the package axis to minimize stress due to off center forces when clamping the assembly.

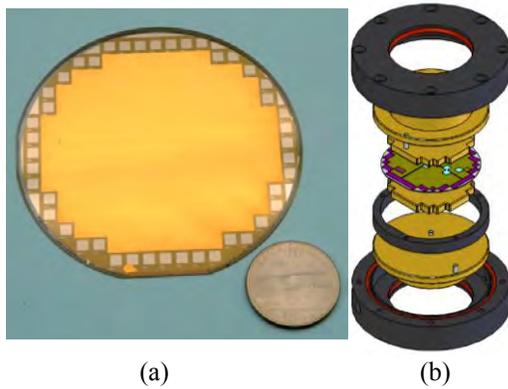


Figure 5: Photograph of the wafer-scale interconnected diode. The active area is 11.72 cm<sup>2</sup> (a). Schematic of a “hockey puck” package for on-state pulsed testing (b).

The packaged wafer-scale diode was subjected to high power pulsed testing. The reverse leakage current was measured before and after each high current shot. A 3.1 mF capacitor bank Pulsed-Forming-Network (PFN) was used for pulsing. The PFN is capable of producing a peak current of approximately 96 kA (~6 kA/kV of charge voltage) with a current rise time of 33 μs for a 470 μsec FWHM pulse width. The PFN is switched by a spark gap. When the PFN is switched, initial energy stored in the capacitor bank discharges through the wafer-scale diode into a resistive load. Under these pulsed conditions, the wafer-scale diode conducted a peak current of 64.3 kA with an on-state voltage drop of 10.3 V (at di/dt = 0) as shown in Fig. 7. This corresponds to a peak current density of 5.5 kA/cm<sup>2</sup> and a diode on-state resistance of 0.13 mΩ. The energy dissipated by the wafer-scale diode during this switching transient was 382 J. The calculated wafer-scale diode action (surge current integral), a key reliability parameter, exceeded 1.7 MA<sup>2</sup>-s.

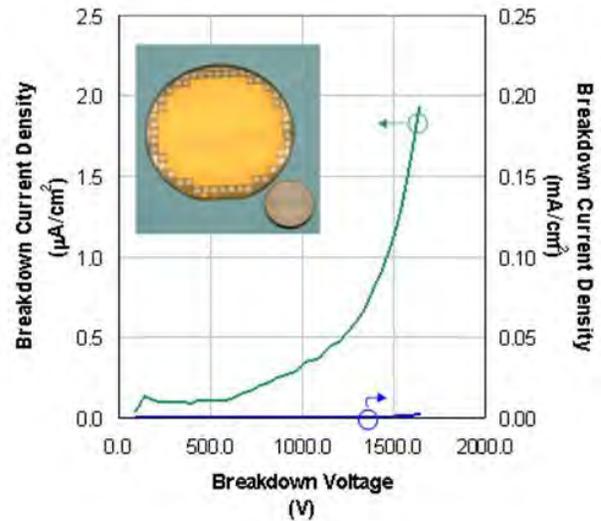


Figure 6: The wafer-scale interconnected diode exhibited a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>.

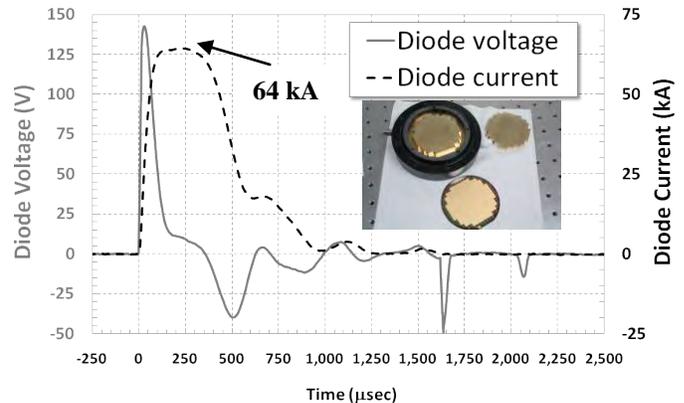


Figure 7: The 1790 V wafer-scale interconnected diode was pulsed at a peak current of 64.3 kA (5.5 kA/cm<sup>2</sup>) with an on-state voltage drop of 10.3 V. The energy dissipated by the wafer-scale diode was 382 J and the calculated action exceeded 1.7 MA<sup>2</sup>-sec.

High voltage operation of PiN diodes, thyristors, and other semiconductor devices is required for applications such as solar inverters and low-loss solid state transformers. Successful demonstration of a 1.8 kV wafer-scale diode has led to development work on interconnection of higher voltage PiN diodes. Discrete high voltage diodes were fabricated on three-inch n+ 4H-SiC substrates with n- drift epitaxial layers of 50 μm thickness doped at 5 x 10<sup>14</sup> cm<sup>-3</sup>. The theoretical breakdown voltage value increases with the thickness of the drift epilayer. A 50 μm drift epilayer enables breakdown voltages greater than 2 kV. A triple zone JTE was used to maximize high voltage performance. Twenty four PiN diodes were interconnected to form a 2.2 cm<sup>2</sup> active area quarter wafer diode, which exhibited a breakdown voltage of 4.5 kV at a leakage current density of 0.03 mA/cm<sup>2</sup>, Fig. 8. In

addition, thirty six PiN diodes were interconnected to form a 3.1 cm<sup>2</sup> active area quarter wafer diode with a breakdown voltage of 4.5 kV at an extremely low leakage current density of 0.03 mA/cm<sup>2</sup>.

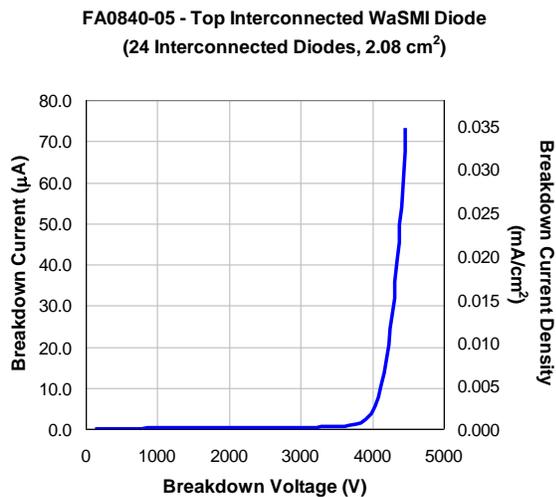


Figure 8: A quarter wafer diode with an active area of 2.2 cm<sup>2</sup>, exhibited a breakdown voltage of 4.5 kV at an extremely low leakage current density of 0.03 mA/cm<sup>2</sup>.

## CONCLUSIONS

Wafer-scale interconnection of discrete PiN diodes was developed to meet the large current handling requirements of modern power conditioning systems. Discrete PiN diodes were designed with an active area of 0.09 cm<sup>2</sup>, and fabricated at a yield of 83%. They were subsequently tested and interconnected on a three-inch 4H-SiC wafer, to form a wafer-scale diode of 11.72 cm<sup>2</sup> active-area. This interconnected area is more than an order of magnitude larger than that of state of the art discrete SiC diodes, and provides significant packaging volume/weight reductions. Under reverse voltage testing, the wafer-scale interconnected diode demonstrated a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>. This confirmed that wafer-scale interconnection of discrete diodes does not compromise the breakdown characteristic of the wafer-scale diode. The wafer-scale diode was mounted in a "key puck" package and subjected to high power pulsed testing. The diode conducted a peak current of 64.3 kA, which corresponds to a peak current density of 5.5 kA/cm<sup>2</sup>. The energy dissipated was 382 J and the calculated action exceeded 1.7 MA<sup>2</sup>-s. Overall, wafer-scale interconnection techniques allow for manufacture of large device areas presently unattainable by discrete parts.

Further development of the high voltage interconnection process has produced quarter wafer PiN diodes of 2.2 cm<sup>2</sup> and 3.1 cm<sup>2</sup> active areas, which exhibited breakdown voltages 4.5 kV and 4.0 kV, respectively. On-state current characterization as well as high voltage wafer-scale interconnection will be the focus of future work.

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## ACRONYMS

SiC: Silicon Carbide  
 PiN: p-doped, intrinsic, and n-doped semiconductor layers  
 GTO Thyristor: Gate-Turn-Off thyristor  
 JTE: Junction Termination Extension  
 PFN: Pulsed Forming Network  
 FWHM: Full Width Half Maximum