THESIS

DEVELOPMENT OF THREE-PHASE SOURCE INVERTER FOR RESEARCH AND LABORATORIES

by

Henry O. Amadasu

March 2011

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The small-scale implementation of a power system that explores a three-phase voltage source inverter (VSI) controlled by a Field Programmable Gate Array (FPGA) is investigated in this thesis. The Naval Postgraduate School (NPS) continuously develops new power systems that explore FPGA control of power electronics. The development, testing and documentation of a three-phase voltage source inverter interfacing with an FPGA and hardware is focused on in this thesis. The development of a three-phase VSI, the thermal and power loss analysis of a three-phase VSI and the hardware interface between the FPGA and the three-phase VSI used for research and laboratory procedures at NPS are particularly concentrated on.
DEVELOPMENT OF THREE-PHASE SOURCE INVERTER FOR RESEARCH AND LABORATORIES

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<td>A</td>
<td>Amps</td>
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<tr>
<td>A/D</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>ac</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>C/W</td>
<td>Degree per Watt</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial off the Self</td>
</tr>
<tr>
<td>D/A</td>
<td>Digital to Analog Converter</td>
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<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>dc</td>
<td>Direct Current</td>
</tr>
<tr>
<td>dc-ac</td>
<td>Direct Current to Alternating Current</td>
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<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESO</td>
<td>Electric Ships Office</td>
</tr>
<tr>
<td>FPD</td>
<td>Field Programmable Device</td>
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<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
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<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
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<tr>
<td>IPM</td>
<td>Intelligent Power Module</td>
</tr>
<tr>
<td>IPS</td>
<td>Integrated Power Systems</td>
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<tr>
<td>LC</td>
<td>Inductance Capacitive</td>
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<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Silicon Field Effect Transistor</td>
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<td>NAVSEA</td>
<td>Naval Sea Systems Command</td>
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<td>NGIPS</td>
<td>Next Generation Integrated Power Systems</td>
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<td>NPS</td>
<td>Naval Post Graduate School</td>
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<td>ns</td>
<td>Nanosecond</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PETS</td>
<td>Power Electronics Teaching System</td>
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<td>PWM</td>
<td>Pulse Width Modulation</td>
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<tr>
<td>R</td>
<td>Resistance</td>
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<tr>
<td>R&amp;D</td>
<td>Research and Development</td>
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<td>RMS</td>
<td>Root Mean Square</td>
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<tr>
<td>Abbreviation</td>
<td>Definition</td>
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<tr>
<td>SDC</td>
<td>Student Design Center</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
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<tr>
<td>V</td>
<td>Volts</td>
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<td>VSI</td>
<td>Voltage Source Inverter</td>
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<td>W</td>
<td>WATTS</td>
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<td>Z</td>
<td>Impedance</td>
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<td>ZEDS</td>
<td>Zonal Electrical Distribution System</td>
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EXECUTIVE SUMMARY

Future Navy ships will benefit from more compact, integrated, lighter and more versatile power electronics. The existing direct current (dc) Zonal Electrical Distribution System (ZEDS) requires a more innovative approach to the conversion of dc power to alternating current (ac) for motor drives. These innovations could save cost, improve efficiency and enhance the overall war fighting capability of future ships.

Today, COTS (Commercial off the Self) technology is of great interest for military applications. The Secretary of the Navy has stated that the electric drive would be used to propel all future Navy Ships. As a result, the Navy has initiated the Next Generation Integrated Power Systems (NGIPS) effort with centralized leadership by the Electric Ships Office (ESO). The mission of the ESO (PMS 320, organizationally a part of the Program Executive Office—Ships) is to develop and provide smaller, simpler, more affordable, and more capable ship power systems for all Navy platforms by defining open architectures, developing common components, and focusing Navy and industry investments.

The newly developed voltage source inverter (VSI) encompasses this vision by selecting the insulated gate bipolar transistor (IGBT) Intelligent Power Module (IPM) as its choice for a high performance, optimum cost, optimum volume and increased system reliability device. The IGBT IPM key features include a 17A, 600V, three-phase IGBT inverter bridge including gate driving control integrated
circuit (IC) and freewheeling diodes, short circuit protected IGBT’s, a thermal monitoring surface mount, smart shutdown and a comparator fault detection function. This thesis focused on the interface between a Field Programmable Gate Array (FPGA) and the VSI. Emphasis was placed on the design, layout, and testing of the interface, as well as techniques used to minimize or eliminate adverse performance due to electromagnetic interference (EMI).

The development of the three-phase VSI on a printed circuit board for research at NPS was proposed to downscale the current Semikron-Semiteach Power Electronics Teaching System (PETS) module to an integrated, cost optimized, size optimized, and readily available solution. The Student Design Center (SDC) at NPS was created to expose students to the process of transforming performance requirements into power electronics design. The three-phase VSI was incorporated into the design center exercises and student design concepts using software simulation and actual hardware to verify laboratory results.

This thesis begins with a brief introduction to the new VSI, the theory of operation of the IGBT IPM, its purpose, motivation, and research goals. Similarly, the design, layout, thermal analysis, and hardware interfaces, such as the FPGA and Chipscope, are discussed to provide the reader with a better understanding of the software associated with the simulation and testing process. Overall, the new Laboratory VSI achieves a small-scale, less costly implementation of a power system, as well as providing an avenue for establishing a more flexible
research and testing capability here at NPS. The hardware interfaces of the proposed VSI configuration are depicted in the following figure.
I. INTRODUCTION

A. PURPOSE

The development of the three-phase voltage source inverter (VSI) on a printed circuit board for research at NPS was proposed to downscale the current Semikron Semiteach power electronics teaching system (PETS) to a more integrated, cost optimized, and size optimized solution. The insulated gate bipolar transistor (IGBT) based pulse width modulated (PWM) VSI was selected as the inverter of choice for ac-fed motor drives. The power stage, which mainly consists of the rectifier, bridge inverter IGBT, thermal management system, inductive-capacitive (LC) filter load and a resistive load, is the major contributor to VSI overall cost and size. The work in this thesis was developed to expose students to the process of transforming performance requirements into a power electronics design. The three-phase VSI incorporated into the Student Design Center (SDC) exercises the student’s design concepts using a newly released three-phase IGBT inverter bridge, software simulation, and hardware to verify results. Laboratory sessions using the SDC provide students with flexible procedures and testing capability to conduct research in a real-world environment while preparing them for future study in power electronics design and control [1].

B. MOTIVATION

Future Navy ships will require a more compact, integrated, lighter and more versatile power electronics system. The Naval Sea Systems Command (NAVSEA) is
interested in white papers for long and short-term research and development (R&D) projects that offer potential for advancement and improvements in the implementation of shipboard Integrated Power Systems (IPS) at the major component, subsystem and system level [2]. As a result, the current dc Zonal Electrical Distribution System (ZEDS) requires a more innovative approach to the conversion of dc power to ac power for motor drives. These innovations could save cost, improve the efficiency and enhance the overall war fighting capability of future ships. The newly developed VSI encompasses this vision by using the IGBT IPM as its main part. The IGBT IPM provides a compact, high performance ac motor drive for a simple and optimum layout for reduced component and cost savings [3]. A field programmable gate array (FPGA) controls an IGBT IPM easily with high reliability and frequency.

The IGBT IPM key features comprise a 17A, 600V, three-phase IGBT inverter bridge including gate driving control integrated circuit (IC) and freewheeling diodes, short circuit protected IGBT’s, a thermal monitoring surface mount, smart shutdown and a comparator fault detection function [3]. The exploration of the interface between an FPGA and voltage source inverter (VSI) were focused on in this thesis. Emphasis is placed on the design, layout, and testing of the interface, as well as thermal performance.

A secondary objective is to present the reader with an experimental result based on thermal analysis of the IGBT IPM device and an overview of the VSI hardware and software used in the student design center (SDC) and current FPGA technology.
C. APPROACH

The three-phase VSI printed circuit board (PCB) consists of an IGBT IPM employing three parallel-connected half-bridges, three gate signals and an optional temperature monitoring surface mount. The three-phase inverter is connected to an LC filter in a delta configuration to run a load of three variable resistors in delta configuration. The PCB consists of two current sensors, three voltage sensors, and multiple optocouplers for ground isolation. The PCB's were designed and constructed to interface the FPGA with a Virtex-4 development board, the inverter, and a stand-alone computer. The analog signal interface PCB includes an output control for the inverter and two analog-to-digital (A/D) converters for converting load currents and voltages. The FPGA was programmed with XILINX® software (embedded in the Simulink® model) and used to drive the inverter.

D. THESIS ORGANIZATION

The purpose, research goals and the organization of the thesis were given in this chapter. The voltage source inverter major components, design, hardware, software and background information on VSI conversion principles are given in Chapter II. Construction, testing and interfacing the three-phase source inverter circuit board are explored in Chapter III. The results, conclusions and future research opportunities are presented in Chapter IV. The PCB Schematics are in Appendix A. The MATLAB code for simulation data are presented in Appendix B. Information on the SEMITEACH® voltage inverter is provided Appendix C.
E. CHAPTER SUMMARY

A brief introduction of the three-phase voltage source inverter objectives, research goals, and the approach taken to meet those goals were given in this chapter. The theory of operation, the hardware and software interfaces used with the source inverter are introduced Chapter II.
II. BACKGROUND INFORMATION

A. INTRODUCTION

The theory of operation of the three-phase source inverter is covered in this chapter. The theory of operation, the major parts of the three-phase voltage source inverter, their interaction with other components and its interface with the FPGA are discussed.

B. THEORY OF OPERATION

1. Overview

An inverter, a critical component of most large motor drive systems, converts a dc power source into a controlled sinusoidal input current for an ac motor at a desired operating frequency. The dc power can be produced by rectifying an ac source. The inverter uses a network of solid-state switches to alternate between the positive and negative input dc source to produce the ac voltage across the load [4]. A simple half bridge inverter is depicted in Figure 1.

Figure 1. Simple half-bridge inverter.
The inverter’s sinusoidal amplitude and frequency output can be directly controlled by timing the opening and closing of switches S1 and S2.

The IGBT is an example of a type of solid-state switch commonly used for inverters. The quality of the output waveform is dependent on a number of variables that include the relative switching frequency speed and is generally specified in number of pulses (or switchings) per half-cycle of the output fundamental voltage or current [4]. For most loads, the ideal voltage and current waveforms are sinusoidal at the desired operating frequency. For nonlinear loads, it is common to force the voltage to be sinusoidal while letting the load characteristics define the output waveform.

Given a fixed amount of filtering and sufficient control bandwidth, the switching sequence, including the relative rate at which the switches operate, determines the inverter’s output accuracy when following a reference sinusoid. As a result, the output of an inverter at a lower relative switching frequency does not match the desired sinusoidal pattern as closely as an inverter switching at a higher frequency. Non-sinusoidal waveforms are rich in harmonic content not directly usable by a machine load. The total harmonic content that is not directly usable by a machine load is known as the total harmonic distortion (THD) of the current. The THD should be minimized to alleviate unwanted noise from torque pulsations and excess heating from eddy current losses.
The load current waveform $I_{L(t)}$ can be represented by a composite series of the fundamental component and the sum of the higher harmonic components and is given by [4]

$$ I_L(t) = I_{L1}(t) + \sum_{h=1}^{\infty} I_{Lh}(t). \quad (2.1) $$

The first term ($I_{L1}$) is the desired fundamental frequency component, while the summation of the $I_{Lh}$ terms represents harmonic content. Ideally, the harmonic terms are zero for a perfectly sinusoidal waveform at the fundamental frequency. The root-mean-squared (RMS) value of the current waveform is given by [4]

$$ I_L = \sqrt{I_{L1}^2 + \sum_{h=1}^{\infty} I_{Lh}^2}. \quad (2.2) $$

The actual distortion present in the current waveform due to its harmonics can be derived from the above relations. The THD as a percentage of the total current waveform is given by [4]

$$ \%THD = 100 \sqrt{\sum_{h=1}^{\infty} \left( \frac{I_{Lh}}{I_{L1}} \right)^2}. \quad (2.3) $$

The objective of the inverter system is to minimize the THD to match a sinusoidal reference signal as closely as possible.
Various methods can be employed to control the switches within the inverter to produce an ac output current. The objective of any switching control scheme is to sequence the switches to match the desired reference signal. Some switching schemes are very simple, while others are quite complex and require the use of microprocessors and FPGAs.

The simplest of switching methods for inverters is square-wave switching. With this method, the inverter cycles the voltage across the load by alternating the positive dc voltage and then the negative dc voltage at the desired output frequency. This method closes the top switch (S1 in Figure 1) when the reference signal is positive and closes the bottom switch (S2 in Figure 1) when the reference signal is negative. Although easy to implement, the square-wave switching method produces an output waveform that falls short of matching the sinusoidal reference signal. Consequently, the THD of the voltage is 47.8% and 30.5% for single-phase and three-phase, respectively [4]. The distortion in the current is based on the significant amount of harmonic current in the output.

A more complex but commonly used switching scheme is called pulse-width modulation (PWM). PWM techniques are capable of producing a good representation of the desired waveform with only the inclusion of higher, easily filterable, harmonics at the switching frequency. With PWM, the positive or negative dc input source voltage is applied to the load in pulses of varying length at a frequency much higher than the fundamental frequency. While the amplitude and frequency of the pulses is fixed, the width of the
individual pulses is weighted by multiplying a reference waveform by a higher frequency triangular-carrier to produce a digitized representation of the reference.

A more complex and widespread technique for inverter control is sine-PWM. In a sine-PWM inverter, a sinusoidal reference signal of the desired output frequency is compared to a triangular modulation signal at a much higher frequency.

The resultant applied voltage levels for a typical cycle in a sine-PWM inverter is depicted in Figure 2.

![Figure 2. Typical sine-PWM applied load voltage (From: [5]).](image)

The controller, typically an FPGA or microprocessor, uses a constant frequency to switch the inverter IGBT. This process, as stated earlier, is known as PWM, as shown in Figure 2. It uses a reference signal, shown in Figure 2, to compare to a constant frequency saw-tooth waveform. When the reference signal is of a higher value than the saw-tooth waveform, the FPGA controller sends out a “high” or “on” signal to the inverter top IGBT switch. When the reference signal is of lower value than the saw-tooth waveform, the FPGA controller sends out a “low” or “off” signal to the upper inverter IGBT switch and turns on the
bottom switch. In Figure 2, the resulting signal from the constant comparison of the reference signal to the saw tooth waveform is shown as red. As can be seen, the PWM signal is a square-wave signal of varying duty cycle that operates at the same frequency as that of the saw tooth waveform. This type of inverter can produce a very high fidelity current waveform and its use is widespread. The two control signals (pulse-width modulation reference and carrier signals) and the switching scheme are illustrated in Figure 2.

A brief description of the algorithm to control the applied voltage to the load is as follows.

If \( V_{\text{ref}} > V_{\text{tri}} \):

Close S1 (top switch), open S2 (bottom switch)

Set \( V_{\text{LOAD}} \) to \( +V_{\text{dc}} \).

If \( V_{\text{ref}} < V_{\text{tri}} \):

Open S1 (top switch), close S2 (bottom switch)

Set \( V_{\text{LOAD}} \) to \( -V_{\text{dc}} \).

For this thesis, a three-phase VSI was designed [6]. The VSI was developed to generate a three-phase ac power supply from a single-phase ac supply. An FPGA controller is used to control the voltage source inverter to generate a third voltage, which along with the single voltage from the supply, creates a balanced three-phase ac to drive the motor. The newly developed three-phase VSI was designed as a compact, cost optimized, and readily available
alternative to the current system at NPS using IPM IGBTs as identified in Chapter I. A simple block diagram of a basic inverter using the new ST IPM IGBT device is shown in Figure 3.

![VSI IPM module diagram](image)

Figure 3. VSI IPM module diagram.

2. Voltage Source Inverter

The VSI printed circuit board discussed in this thesis operates by converting single-phase ac power from the wall outlet to dc and then back to three-phase ac using an IGBT inverter. In the three-phase voltage source inverter, the rectified dc power from a wall outlet is fed into the three half bridges in series with an LC filter with a delta configured capacitor bank to run a three variable resistors
load in delta configuration. The IGBTs are controlled by the FPGA through the gate drivers. The inverter consists of six IGBTs, which creates an ac voltage by drawing on the power of the dc bus. The amplitude and frequency of the sinusoidal waveform can be controlled directly by properly timing the opening and closing of the IGBT switches. The quality of the output waveform is dependent on a number of variables including the relative switching frequency, the filtering, and the bandwidth of the FPGA controller. Voltages created by the IGBT power switching are not sinusoidal but are pulse width modulated waveforms with high harmonic distortion. The PWM voltages are then passed through a LC filter network to produce a sine wave with less distortion. The FPGA monitors and adjusts the generated voltage to produce a constant, balanced three-phase voltage. The IPM is also embedded with a protective smart shut down function in case of over-voltage, under-voltage, or fault. With the ability to adjust to changing conditions, the three-phase voltage source inverter can operate safely and effectively on three-phase systems. A pictorial view of the new VSI is shown in Figure 4.
C. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

A field programmable gate array is a semiconductor device containing programmable logic components and programmable interconnects. The programmable logic components, such as AND, NOR, OR and XOR gates and other complex logic, can be programmed to duplicate the functionality of basic logic gates or more complex combinational functions [7]. In this case, the FPGA function is used to readily and effectively control the switching of the IGBTs and also provide the required signals to drive the voltage and current sensors. A major advantage of this technology is that FPGAs can execute code in parallel. FPGAs can be thought of as a Table-of-Equations executed simultaneously (when feasible) during a given clock cycle and they have traditionally been used in high-speed custom digital applications where designs tend to be more constrained by performance. Their widespread use and reduction in price makes them the controller of choice in embedded applications, such as the VSI. The number of parallel calculations is limited by the size of the FPGA.
Current technology produces speeds up to 600 MHz in certain designs; however, the SDC operates at 25 MHz using only a fraction of this speed [7],[8].

XILINX®, a leading manufacturer of FPGAs, primarily builds array-based circuits. These circuits incorporate chips comprised of two-dimensional arrays of logic blocks that can be interconnected via horizontal and vertical routing channels [7]. The XILINX® Virtex-4™ development board is shown in Figure 5.

Figure 5. XILINX® Virtex-4™ development board (From: [7]).
The Virtex-4™ was designed as a user-friendly platform for prototyping, simulating, testing and verifying designs. A high-level block diagram of the Virtex-4™ is shown in Figure 6.

Figure 6. High-Level block diagram of the Virtex-4™ (From: [7]).

D. HARDWARE INTERFACE USING CHIPSOCPE™ PRO

Chipscope interface software is a computer-based interface that communicates with the FPGA through the JTAG ports. The Xilinx Chipscope block can be accessed at run-
time using the Chipscope pro analyzer software. The analyzer configures the FPGA, sets up trigger conditions and views data run-time. Chipscope is a PC accessible software able to program, interact with, export data from the FPGA and read back into the MATLAB workspace, making it particularly useful throughout the design, simulation and testing of the voltage source inverter. The user can remotely control the inverter through the computer using ChipScope™ Pro software. ChipScope™ Pro inserts a logic analyzer, bus analyzer, and virtual I/O low-profile software core directly into the design. This allows the user to view any internal signal or node, including embedded hard or soft processors. Signals are captured at or near operating system speed, and the process is limited only by the speed of the acquisition of analog signals in digital form [7],[8]. The data is then viewed through the programming interface and analyzed with the ChipScope™ Pro Logic Analyzer [7].

The virtual input-output (VIO) console in the software allows the user to control the hardware. For example, one bit can be toggled to turn the converter on and off.

In this manner, the user can remotely control the FPGA, and thus, the voltage conversion process, using ChipScope™ Pro. Detailed analyses of input and output signals can be accomplished digitally; hence, an oscilloscope is no longer necessary for laboratory measurements. The user can evaluate a signal bit-by-bit if necessary. Furthermore, calibration of the sampled signal
can be accomplished by adjusting gain blocks in the Simulink® model. The next chapter explains this feature in more detail.

E. CHAPTER SUMMARY

An overview of the VSI board was presented with a brief background of the voltage conversion process, the new IGBT IPM, FPGA and software utilization process. The development, construction, and testing of the printed circuit board and experimental thermal analysis conducted using the Celsius temperature sensor are covered in the next chapter.
III. PRINTED CIRCUIT BOARD DESIGN AND TESTING

A. SCHEMATIC DESIGN

PCB123 software was used to create and prepare the board schematics and layout [6]. Individual components were manually placed on the board, and prior to energizing, a system check was done to verify continuity.

The circuit diagram in Figure 7 depicts the major components of the system.

![Hardware Architecture Diagram](image)

Figure 7. Schematic diagram of the VSI laboratory hardware architecture.
The VSI design is given in [6]. It consists of the new intelligent IPM module as the main part of the system. The main components are the following: six pack IPM module, voltage rectifier, optocouplers, FPGA interface jacks, and voltage and current sensors.

The IPM IGBT is a three-phase inverter with the output connected in series with an inductor and then connected to a delta configuration of capacitors to produce an LC filter load. The value of the LC filter and the load resistor is adjusted to be equal to the computer-simulated values. The LC filter limits the current and the voltage in the time domain to produce a low pass filter.

B. THERMAL ANALYSIS

To utilize the newly developed VSI IGBT IPM module fully, sufficient attention must be paid to proper heat removal of the IGBT. The IGBT IPM will have conduction and switching power losses. The heat generated as a result of these losses must be conducted away from the power chip and into the environment using a heatsink. For efficient thermal management, the user must rely on important parameters supplied by the manufacturer, such as junction-to-case and junction-to-ambient thermal resistances and maximum operating junction temperature. The device temperature depends on the power dissipation level, the means for removing the heat generated by this power dissipation and the temperature of the body (heat sink) to which this heat is removed.
A simplified equivalent circuit for a typical semiconductor device in equilibrium is shown in Figure 8.

![Simplified thermal circuit](image)

Figure 8. Simplified thermal circuit.

The power dissipation, which is analogous to current flow in electrical terms, represents the heat source. Temperature is equivalent to voltage potential and thermal resistance to ohmic resistance. If $\theta_{JA}$ is the junction to ambient thermal resistance, $\theta_{JC}$ is the junction-to-case thermal resistance, $\theta_{CS}$ is the case-to-sink thermal resistance and $\theta_{SA}$ is the sink-to-ambient thermal resistance, then the total required thermal resistance is given by
\[ \theta_{JA(total)} = \theta_{JC} + \theta_{CS} + \theta_{Xa} = \frac{T_j - T_a}{P_D}. \] (3.1)

The rise in the temperature of a package above some reference level per unit of power dissipation is expressed in degrees Celsius per watt. Several factors affect thermal resistance including die size, the size of the heat source on the die (series-pass transistor in an IC regulator), die-attach material and thickness, lead frame material, and construction and thickness.

To measure thermal resistance, the difference between the junction temperature and the chosen reference temperature, case, sink or ambient, must be determined. An ambient or sink temperature measurement is straightforward. For a case-temperature measurement, the device should have a sufficiently large heat sink. Measurement of the junction temperature, unfortunately, is not as simple and involves some approximation as practical as possible [9].

The thermal behavior analysis of a three-phase VSI developed at NPS is covered in this section. The thermal analysis is an ongoing research effort; its benefits include increasing reliability by estimating the thermal impedance of the IGBT module. Estimation of thermal impedance quantifies the characteristics of the heat sink needed to dissipate the heat under worst-case conditions. The IPM IGBT is embedded with a temperature-monitoring surface. The setup of the LM 35 temperature sensor consists of a 5V power supply, a ground connection and a multimeter readout on the output. An LM35 chip is mounted on the heat sink and a typical application connection shown in Figure 9.
Figure 9. LM 35 basic Celsius temperature sensor (From: [10]).

Based on the setup shown in Figure 9, the following measurements in Table 1 were obtained and plotted by MATLAB. The experimental data measurement shown in Table 1 provides the relationship between measured temperature and voltage values, which are 10mV/C.

Table 1. Thermal behavior analysis data.

<table>
<thead>
<tr>
<th>Thermal Behavior analysis Data (LM35 on IGBT IPM Heat sink)</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{LOAD} (\Omega)$</td>
<td>voltages (mV)</td>
<td>Time (Seconds)</td>
<td>Temperature (Celsius) = mV/10</td>
<td>Remarks</td>
</tr>
<tr>
<td>240</td>
<td>230mV</td>
<td>0</td>
<td>23</td>
<td>LM 35 Precision Centigrade Temperature Sensor Gain: OUTPUT up to 10mV per Celsius 10mV/C</td>
</tr>
<tr>
<td>240</td>
<td>304mV</td>
<td>60</td>
<td>30.4</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>370mV</td>
<td>120</td>
<td>37</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>399mV</td>
<td>180</td>
<td>39.9</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>434mV</td>
<td>240</td>
<td>43.4</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>460mV</td>
<td>300</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>490mV</td>
<td>360</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>508mV</td>
<td>420</td>
<td>50.8</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>524mV</td>
<td>480</td>
<td>52.4</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>529mV</td>
<td>540</td>
<td>52.9</td>
<td></td>
</tr>
</tbody>
</table>
A plot of temperature versus time showing an exponentially rising temperature that reaches equilibrium after 500 seconds is shown in Figure 10.

Figure 10. Temperature vs. time for the IGBT IPM heat sink.

Due to various implementations of new design features on newer ships and electric load distributors, thermal issues are increasingly becoming a problem. The shrinking component sizes result in greater surface in many devices as material advances and switching speed of smaller electronics components reach new heights. Thus, these new devices require a significant innovation in cooling capacity.
The new VSI Intelligent IGBT semiconductor device was tested under various lab conditions. The experiment utilized the LM35 precision centigrade temperature sensor. Its low cost, low self-heating, low output impedance, linear output and precise inherent calibration make interfacing to the LM35 readout or control circuit especially easy [10].

Other experimental assumptions made due to their negligible effect are as follows:

- Each half-bridge inverter, including its free wheeling diode temperature drop from IGBT case to the heat sink, is neglected
- Thermal coupling between the IGBT and free wheeling diode is also neglected
- The thermal boundary, which represents the IGBT case to its package, is neglected due to the amount of surface area for heat to dissipate and thermal paste applied

The thermal and switching loss data used in this thesis are shown in Table 2.

Table 2. Thermal data from the manufacturer.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thJC}$</td>
<td>Thermal resistance junction-case single IGBT</td>
<td>2.4</td>
<td>C/W</td>
</tr>
<tr>
<td>$R_{thJC}$</td>
<td>Thermal resistance junction-case single diode</td>
<td>5.0</td>
<td>C/W</td>
</tr>
<tr>
<td>$R_{thJC}$</td>
<td>Thermal resistance case-sink</td>
<td>4.6</td>
<td>C/W</td>
</tr>
<tr>
<td>$E_{on}$</td>
<td>Turn-on switching losses</td>
<td>290</td>
<td>μJ</td>
</tr>
<tr>
<td>$E_{off}$</td>
<td>Turn-off switching losses</td>
<td>250</td>
<td>μJ</td>
</tr>
</tbody>
</table>

The thermal equivalent circuit for the VSI is shown in Figure 11. In the thermal modeling diagram, $T_s$ is the heat
sink temperature measured with the probe and $P_{\text{Loss}}$ symbolizes the current source representing the injected power. The objective is to estimate the semiconductor junction temperature based on the estimated thermal impedance for the mechanical system. This analysis is simplified by making the diode junction and the IGBT junction the same temperature, which is represented by a short circuit in Figure 11 from $T_{\text{IGBT}}$ to $T_{\text{diode}}$. The thermal model in Figure 11 relates to Figure 9 if assuming $\theta_{CS}$ is zero and two semiconductors are in parallel ($\theta_{JC}$ for the diode and transistor).

![Thermal model of the IGBT IPM heat sink.](image)

Figure 11. Thermal model of the IGBT IPM heat sink.

The IGBT inverter module was operated under the following conditions: $V_{dc}=155\, \text{V}$, $F_{\text{switching}}=10\, \text{KHz}$, and $I_{\text{RMS}}=0.8990\, \text{A}$. 

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The temperature measured on the heat sink was 50°C. The estimated losses for this operating condition are shown in Table 3.

1. **RMS in Frequency Domain**

The RMS was computed using Parseval’s theorem for the sampled signal in Figure 12.

![Sample current waveform from Chipscope.](image)

Figure 12. Sample current waveform from Chipscope.

The $I_{\text{RMS}}$ was calculated given

$$I_{\text{RMS}} = \sqrt{\frac{1}{\text{length}(\text{timedata})} \sum (\text{ch6}\text{final}^2)}.$$  \hspace{1cm} (3.2)

The $I_{\text{RMS}} = 0.899\text{A}$ was calculated using Equation (3.2) and the MATLAB data provided in Appendix C.
The power losses \( P_{\text{total}} \) are the sum of the conduction losses and the on/off or switching losses as given by

\[
P_{\text{total}} = P_{\text{cond}} + P_{\text{switch}}
\]

(3.3)

where \( P_{\text{cond}} \) represents conduction losses while the IGBT is on and conducting current and \( P_{\text{switch}} \) is the power dissipated during the turn-on and turn-off switching transition.

The switching losses \( P_{\text{switch}} \) are the product of the turn on/off energy dissipated in the IGBT and the switching frequency, which is multiplied by six to account for six IGBTs. For an IGBT, the switching losses are

\[
P_{\text{switch}} = (E_{\text{on}} + E_{\text{off}}) f_{\text{sw}}
\]

(3.4)

where \( E_{\text{on}} \) is the turn-on switching energy, \( E_{\text{off}} \) is the turn-off switching energy and \( f_{\text{sw}} \) is the switching frequency (see Table 2).

The conduction losses \( P_{\text{cond}} \) are estimated by multiplying the average forward voltage drop of the semiconductors times the RMS current. This quantity is multiplied by three since there are three half bridge legs in the VSI. For each IGBT/diode pair, the losses are

\[
P_{\text{cond}} = \left( \frac{V_{\text{ce}} + V_{\text{d}}}{2} \right) I_{\text{RMS}} \frac{1}{2}
\]

(3.5)

where \( V_{\text{ce}} = 2.2 \text{V} \) and \( V_{\text{d}} = 3.8 \text{V} \). The calculated power dissipation values are shown in Table 3.
Table 3. The power dissipation table for each IGBT.

<table>
<thead>
<tr>
<th>$I_{RMS}$ (A)</th>
<th>$P_{Total}$ (C/W)</th>
<th>$P_{switch}$ (W)</th>
<th>$P_{cond}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8990</td>
<td>6.75</td>
<td>5.40</td>
<td>1.35</td>
</tr>
</tbody>
</table>

The average device voltage is used as an approximation of the semiconductor voltage drop.

The estimated temperature from the junction to the heat sink is 42.5°C. A measurement of 50°C at the heat sink predicts that the junction temperature is 92.5°C in this operating mode. The thermal impedance is computed from Figure 11. The thermal impedance is multiplied by the power dissipated by one diode/IGBT pair to find the junction temperature above the heatsink temperature. Evaluating Equation (3.1) for the temperature rise obtains

$$
\left(\frac{2.4 \times 5.0}{7.4} + 4.6\right) \times 6.75 = 42.5°C = T_J - T_S.
$$

The allowable IGBT junction temperature is 125°C; enhance, the thermal analysis predicts that the device is not overheating.

C. VOLTAGE SENSOR ANALYSIS

The voltage sensor's circuit diagram is shown in Figure 13. The power dissipation in each resistor of the dc voltage sensor is computed in Table 4. The calculated power for each resistor in the ac voltage sensors is summarized in Table 5. The resistors and capacitor shown in Figure 13 form a lowpass filter. The filter gain and phase shift are plotted in Figures 14 and 15, respectively.
Figure 13. DC bus sensor.

The dc bus sensor with three resistors: $120\,\text{k}\Omega$, $120\,\text{k}\Omega$, and $6.8\,\text{k}\Omega$ is shown in Figure 13. The dc bus voltage is designed to be as high as $350\,V_{dc}$. The dc current is given by

$$I_{dc} = \frac{V_{max}}{R_{total}}.$$  \hspace{1cm} (3.7)

For dc, $I_{dc} = \frac{350}{(120+120+6.8)\,\text{k}\Omega} = 1.42\,\text{mA}$ and the dissipated power per resistor is given by

$$P_{dc} = (I_{dc}^2\,R).$$  \hspace{1cm} (3.8)

Table 4. Calculated dc bus sensor tables.

<table>
<thead>
<tr>
<th>Resistor Values (ohms)</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{dc} = (I_{dc}^2,R)$</td>
<td>242mW</td>
<td>242mW</td>
<td>14mW</td>
</tr>
</tbody>
</table>
The ac output voltage is designed to be as high as 220 Vac. AC sensor resistances are 56kΩ, 56kΩ, and 3kΩ and the $R_{total}$ is the sum of the three sensor resistors. The power dissipated on each ac sensor resistor shown in Table 5 is given by

$$P = (I_{RMS}^2 R_{total}) .$$

A 2mA $I_{RMS}$ current is given by

$$I_{RMS} = (V_{RMS} / R_{total}) .$$

Table 5. Calculated ac sensor tables.

<table>
<thead>
<tr>
<th>Resistor</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor Values (ohms)</td>
<td>56</td>
<td>56</td>
<td>3</td>
</tr>
<tr>
<td>Power</td>
<td>224mW</td>
<td>224mW</td>
<td>17mW</td>
</tr>
</tbody>
</table>

1. Low Pass Filter MATLAB Code

The filter corner frequency is shown to be about 10 KHz in Figure 14. The filter gain and phase shift plotted for the ac voltage sensor using MATLAB are depicted in Figures 14 and 15. The power dissipated in each resistor is shown in Table 5.
Figure 14. Lowpass filter amplitude response.

Figure 15. Lowpass filter phase shift.

The lowpass filter passes low-frequency signals but attenuates or reduces the amplitude of the signals above the cutoff frequency. A lowpass filter consists of a resistor in series with a load, and a capacitor in parallel with the load. The capacitor exhibits reactance, and blocks low-frequency signals, causing them to go through the load
instead. At higher frequencies, the reactance drops, and the capacitor effectively functions as a short circuit. The combination of resistance and capacitance provides the time constant of the filter \( \tau = RC \). The cutoff frequency (in hertz), is given by

\[
f_c = \frac{1}{2\pi RC}.
\] (3.11)

The transfer function for the lowpass filter is

\[
H(j\omega) = \frac{R_3 \parallel \frac{1}{j\omega C}}{R_1 + R_2 + R_3 \parallel \frac{1}{j\omega C}}
\] (3.12)

where \( R_1, R_2 \) and \( R_3 \) represent the impedance of the resistors and \( \frac{1}{j\omega C} \) represents the impedance of the parallel capacitor.

At 4700 pF, the cutoff frequency is approximately 10 kHz.

2. Current Sensor

The current sensor gain is 1/333 and the burden resistor is 330 \( \Omega \) ohms. Thus, the current sensor output signal is 330V/333A. The connection option used in this thesis is shown in Table 6.
Table 6. 25_NP transducer datasheet connection option.

<table>
<thead>
<tr>
<th>Number of primary Turns</th>
<th>Primary Current Nominal [A]</th>
<th>Primary Current maximum [A]</th>
<th>Nominal Output current [mA]</th>
<th>Turns Ratio $K_n$</th>
<th>Primary Resistance $R_p$ [mΩ]</th>
<th>Primary insertion Inductance $L_i$ [μH]</th>
<th>Recommended PCB connections</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>8</td>
<td>18</td>
<td>24</td>
<td>3 : 1000</td>
<td>1.62</td>
<td>0.110</td>
<td>3 2 1 IN OUT 4 5 6</td>
</tr>
</tbody>
</table>

The internal connections of the LAH 25_NP current transducer are shown in Figure 16. A current of 10A yields a 10V signal with a 3:1000 turns ratio ($K_n$) and a $333\,\Omega$ burden resistor ($R_m$ in Figure 16). Connection of the current sensor so that a turns ratio of 3/1000 is achieved is explained in Appendix B.

![Internal schematic of the current transducer](From: [11]).

Figure 16.

3. Optocouplers

Optocouplers are used for electrical isolation. It generally consists of a light emitting diode (LED) and a photodiode in one opaque package. The functional block
A diagram and schematic of the FOD2220 optocoupler is shown in Figure 17. The FOD2220 is an optically coupled logic gate that combines an aluminum gallium arsenide (ALGaAS) LED and an integrated high gain photo detector for electrical isolation [12].

![Functional Block Diagram and Schematic](image)

*Figure 17. Schematic diagram of optocoupler (From: [12]).*

The gate drive signals coming from the FGPA are isolated from the VSI and are sent to the VSI through optocouplers. This is necessary because the ground references for the gate drive control signals in the VSI are the negative DC bus, which can be as much as 350 volts away from earth ground or logic ground from the FPGA.

### D. CHAPTER SUMMARY

An overview of the IGBT thermal behavior analysis, printed circuit board construction and testing, and experimental results based on the thermal behavior analysis of the IGBT IPM were presented in this chapter. The summary of this thesis and topics for future research are presented in the next chapter.
IV. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY

This thesis began with an overview of the voltage source inverter. The purpose and function of each major component and interfaces was explained to develop a working knowledge of the inverter. The design and testing of a VSI and its interface circuit boards was discussed, and system performance testing was done to ensure EMI from the switching inverter did not inhibit signal sampling. Finally, a thermal experiment was performed on the IGBT heat sink to ensure reliable performance such that the heat sink was able to maintain the device temperature below the maximum allowable temperature specified by the manufacturer.

B. CONCLUSIONS

The development of the three-phase voltage source inverter is an excellent resource for establishing flexible research capability at NPS. Students gain a fundamental understanding of schematics, circuit design, the advantages of using an FPGA for the control of power systems and digital signal analysis using ChipScope™ Pro. Students are enabled to make accurate predictions of component behavior using software simulation, testing and verifying results. New programs and ideas can be implemented without changing hardware and increasing costs. Students in other curricula can also experiment with other power electronics design for control of electrical systems.
C. RECOMMENDATIONS FOR FURTHER RESEARCH

There are many ongoing research opportunities in the area of Intelligent Power IGBT Module for power systems. Ideas for further research include thermal management solutions for three-phase VSI switching method with high quality power and least heat dissipation, the development of VSI laboratories for other electrical engineering curriculum tracks using FPGA technology, and cost optimized research for intelligent power electronics and electrical systems to improve efficiency, reliability and reduced cost.

The reprogrammable nature of the FPGA hardware enables a large number of programs and systems to be explored without the cost of purchasing and installing new hardware. For this reason, electrical engineering students at NPS can gain significantly from the use of FPGA technology as a valuable tool for flexible research capability at NPS.
APPENDIX A. PCB SCHEMATICS

Figure 18. VSI schematic (From: [6]).
Figure 19. VSI printed circuit board.
SECTION 2
HEAT DISSIPATORS FOR PLASTIC CASE, CASE-MOUNTED SEMICONDUCTORS

Vertically mounted heat dissipators with board mounting tabs

- Designed for high power levels in order to accommodate operating temperatures while occupying a minimum of available space.
- Allows back-to-back dual mounting for enhanced thermal matching applications.
- Mechanical tabs simplify installation to the circuit board — no mounting hardware or special tools required.
- Dissipators are available with brass or tin finishes — allows heat sink mounting tabs to be flow-soldered onto board along with other components.
- Each dissipator is optimally designed for maximum effective surface area in a minimum working envelope.

PB2-35 Series

PSB2-1 Series

Figure 20. Heat sink datasheet.
Figure 21. Typical application of STGIPS20K60.
5.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The SD/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see Section 4: Smart shutdown function for detailed info).

Table 13. Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_PN</td>
<td>Supply Voltage</td>
<td>Applied between P-Hu_1, Ux_Nx</td>
<td>300</td>
<td>400</td>
</tr>
<tr>
<td>V_CC</td>
<td>Control supply voltage</td>
<td>Applied between V_CC-GND</td>
<td>12.5</td>
<td>15</td>
</tr>
<tr>
<td>V_BS</td>
<td>High side bias voltage</td>
<td>Applied between V_CC_OUTj for HUj, VW</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>t_bl</td>
<td>Blanking time to prevent arm-short</td>
<td>For each input signal</td>
<td>1</td>
<td>µs</td>
</tr>
<tr>
<td>f_PWM</td>
<td>PWM input signal</td>
<td>-40°C ≤ T_J ≤ 100°C</td>
<td>20</td>
<td>kHz</td>
</tr>
</tbody>
</table>

Figure 22. STGIPS20K60 recommendations (From: [3]).
Figure 23. Test circuit switching time.
Figure 24. Switching time definition.
Figure 25. LM35/LM35A/LM35C/LM35CA/LM35D precision centigrade temperature sensors (From: [10]).
Figure 26. Current transducer LAH 25-NP data (From: [11]).
Figure 27. Current transducer LAH 25-NP characteristics (From: [11]).
Figure 28. Dimensions of LAH 25-NP (From: [11]).
FOD2200
Low Input Current Logic Gate Optocouplers

Features
- 1kV/us minimum common mode rejection
- Compatible with LSTTL, TTL, and CMOS logic
- Wide VCC range (6.3V to 18V)
- 2.5MHz guaranteed over temperature
- Low input current (1.9mA)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to 85°C
- Hysteresis
- Safety approvals – UL, CSA, VDE (pending)
- VDD = 8V/16V

Applications
- Isolation of high speed logic systems
- Computer peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated bus driver
- High speed line receiver

Description
The FOD2200 is an optically coupled logic gate that combines an AlGaAs LED and an integrated high gain photodetector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data buses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a VCC range of 4.5V to 18V. Low VCC and wide VCC range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a maximum propagation delay of 30ns. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Truth Table (Positive Logic)

<table>
<thead>
<tr>
<th>LED</th>
<th>Enable</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>On</td>
<td>H</td>
<td>Z</td>
</tr>
<tr>
<td>Off</td>
<td>H</td>
<td>Z</td>
</tr>
<tr>
<td>On</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Off</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Figure 29. FOD2200 low input current logic gate optocouplers (From: [12]).
% Alex Julian, Giovanna Oriti, 13 Nov 2009
% acquiring 32 channels of data "totalpoints" times
buff_size=2^5*4;
if not(libisloaded('ftd2xx')) %if the library is NOT loaded
execute the following code
    loadlibrary('ftd2xx.dll', 'ftd2xxM.h');
end
h=libpointer('uint32Ptr', uint32(0));
disp('opening');
s=calllib('ftd2xx', 'FT_Open', 0, h);
if (s ~= 0)
    disp('open error');
    return;
end

% writing one word
dwBytesWritten=0;
pdwBytesWritten=libpointer('uint32Ptr', dwBytesWritten);
dwWxSize=1;
pdwWxSize=libpointer('uint32Ptr', dwWxSize);
tempy=uint8(0);        %sends zero,zero to input bits
ppcBufWrite=libpointer('uint32Ptr', tempy);
tempy=0;
ppcBufWrite.Value=tempy;
s=calllib('ftd2xx', 'FT_Write', h, ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
tempy=2^7;    % sends 10 to input bits, loads data in RAM
ppcBufWrite.Value=tempy;
s=calllib('ftd2xx', 'FT_Write', h, ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
pause(.1);
run_it=0;
tic;
flagit=0;
tempx=0;
dwBytesRead=0;    pdwBytesRead=libpointer('uint32Ptr',
dwBytesRead);
dwRxSize=0;        pdwRxSize=libpointer('uint32Ptr',
dwRxSize);
ok_flag=1;
totalpoints=2^11/4;
nopoints=0;
while (nopoints<totalpoints) & (ok_flag==1)
    nopoints=nopoints+1
    tempy=0;
    ppcBufWrite.Value=tempy;
    s=calllib('ftd2xx', 'FT_Write', h, ppcBufWrite, pdwWxSize.Value, pdwBytesWritten);
    tempy=2^7+2^6; % sends 11 to input bits
    ppcBufWrite.Value=tempy;
    s=callib('ftd2xx', 'FT_Write', h, ppcBufWrite, pdwWxSize.Value, pdwBytesWritten);
    flag=1;
    prev=0;
    pause(.04);
    s=callib('ftd2xx', 'FT_GetQueueStatus', h, pdwRxSize);
    if (pdwRxSize.Value == 0)
        pause(.1);
        flagit=flagit+1;
        disp('closing');
        s=callib('ftd2xx', 'FT_Close', h);
        libisloaded('ftd2xx');
        pause(.1);
        if not(libisloaded('ftd2xx')) %if the library is NOT loaded execute the following code
            loadlibrary('ftd2xx.dll', 'ftd2xxM.h');
        end
        disp('opening');
        s=callib('ftd2xx', 'FT_Open', 0, h);
        if (s ~= 0)
            disp('open error');
            return;
        end
        tempy=0;
        ppcBufWrite.Value=tempy;
        s=callib('ftd2xx', 'FT_Write', h, ppcBufWrite, pdwWxSize.Value, pdwBytesWritten);
        tempy=192;
        ppcBufWrite.Value=tempy;
        s=callib('ftd2xx', 'FT_Write', h, ppcBufWrite, pdwWxSize.Value, pdwBytesWritten);
    end
    while ((pdwRxSize.Value < buff_size) && s == 0)
        tempx=tempx+1
    end

end

while ((pdwRxSize.Value < buff_size) & & s == 0)
s=calllib('ftd2xx', 'FT_GetQueueStatus', h, pdwRxSize);
if ((pdwRxSize.Value ~= prev) && flag)
    flag=0;
end
prev=pdwRxSize.Value
end

dpwRxSize.Value=buf_size;
pcBufRead=uint8(75*ones(1, pdwRxSize.Value/4));
ppcBufRead=libpointer('uint32Ptr', pcBufRead);
[u, pr, data, pt]=calllib('ftd2xx', 'FT_Read', h, ppcBufRead, pdwRxSize.Value, pdwBytesRead);
if (s~=0)
    disp('read error');
    ok_flag=0;
    return;
end
datamod=typecast(uint32(data), 'uint8');
z(nopoints,:)=datamod; %storing 32 channels twice in the z matrix [totalpoints x 64]
end
toc
disp('closing');
s=calllib('ftd2xx', 'FT_Close', h);
libisloaded('ftd2xx');

%post-processing and plotting data
%processing channel 1 data
z_LSB1=z(:,1);
z_MSB1=z(:,2);
ch1_data= shiftb2 (z_LSB1, z_MSB1, totalpoints);
%processing channel 2 data
z_LSB2=z(:,3);
z_MSB2=z(:,4);
ch2_data= shiftb2alj (z_LSB2, z_MSB2, totalpoints);
I_1=(((ch2_data/2^8)-1))/1.6985-2.5)*20/.625;
%processing channel 3 data
z_LSB3=z(:,5);
z_MSB3=z(:,6);
ch3_data= shiftb2alj (z_LSB3, z_MSB3, totalpoints);
dc_voltage1=ch3_data*2*0.0011308;

%processing channel 4 data
gain1=1/(1/3000+1/2000000)/(1/(1/3000+1/2000000)+56000*2)*1.05;
z_LSB4a = z(:,7);
z_MSB4a = z(:,8);
z_LSB4b = z(:,7+32);
z_MSB4b = z(:,8+32);
z_LSB4c = z(:,7+32+32);
z_MSB4c = z(:,8+32+32);
z_LSB4d = z(:,7+32+32+32);
z_MSB4d = z(:,8+32+32+32);
z_LSB4e = z(:,7+16);
z_MSB4e = z(:,8+16);
z_LSB4f = z(:,7+32+16);
z_MSB4f = z(:,8+32+16);
z_LSB4g = z(:,7+32+32+16);
z_MSB4g = z(:,8+32+32+16);
z_LSB4h = z(:,7+32+32+32+16);
z_MSB4h = z(:,8+32+32+32+16);

for ii=1:totalpoints/2
    z_LSB4(8*ii-7) = z_LSB4a(ii);
    z_LSB4(8*ii-6) = z_LSB4e(ii);
    z_LSB4(8*ii-5) = z_LSB4b(ii);
    z_LSB4(8*ii-4) = z_LSB4f(ii);
    z_LSB4(8*ii-3) = z_LSB4c(ii);
    z_LSB4(8*ii-2) = z_LSB4g(ii);
    z_LSB4(8*ii-1) = z_LSB4d(ii);
    z_LSB4(8*ii)  = z_LSB4h(ii);
    z_MSB4(8*ii-7) = z_MSB4a(ii);
    z_MSB4(8*ii-6) = z_MSB4e(ii);
    z_MSB4(8*ii-5) = z_MSB4b(ii);
    z_MSB4(8*ii-4) = z_MSB4f(ii);
    z_MSB4(8*ii-3) = z_MSB4c(ii);
    z_MSB4(8*ii-2) = z_MSB4g(ii);
    z_MSB4(8*ii-1) = z_MSB4d(ii);
    z_MSB4(8*ii)  = z_MSB4h(ii);
end

ch4_data = shiftb2alj (z_LSB4, z_MSB4, totalpoints*4);
ch4_final = ch4_data/2^7/gain1;

% processing channel 5 data
z_LSB5a = z(:,9);
z_MSB5a = z(:,10);
z_LSB5b = z(:,9+32);
z_MSB5b = z(:,10+32);
z_LSB5c = z(:,9+32+32);
z_MSB5c = z(:,10+32+32);
z_LSB5d = z(:,9+32+32+32);
for ii=1:totalpoints/2
    z_LSB5(8*ii-7) = z_LSB5a(ii);
    z_LSB5(8*ii-6) = z_LSB5e(ii);
    z_LSB5(8*ii-5) = z_LSB5b(ii);
    z_LSB5(8*ii-4) = z_LSB5f(ii);
    z_LSB5(8*ii-3) = z_LSB5c(ii);
    z_LSB5(8*ii-2) = z_LSB5g(ii);
    z_LSB5(8*ii-1) = z_LSB5d(ii);
    z_LSB5(8*ii)  = z_LSB5h(ii);
end
ch5_data= shiftb2alj (z_LSB5, z_MSB5, totalpoints*4);
ch5_final=ch5_data/2^7/gain1;

%processing channel 6 data

%dc sensor gain

%current sensor gain
for ii=1:totalpoints/2
    z_LSB6(8*ii-7) =z_LSB6a(ii);
    z_LSB6(8*ii-6) =z_LSB6e(ii);
    z_LSB6(8*ii-5) =z_LSB6b(ii);
    z_LSB6(8*ii-4) =z_LSB6f(ii);
    z_LSB6(8*ii-3) =z_LSB6c(ii);
    z_LSB6(8*ii-2) =z_LSB6g(ii);
    z_LSB6(8*ii-1) =z_LSB6d(ii);
    z_LSB6(8*ii)  =z_LSB6h(ii);
    z_MSB6(8*ii-7) =z_MSB6a(ii);
    z_MSB6(8*ii-6) =z_MSB6e(ii);
    z_MSB6(8*ii-5) =z_MSB6b(ii);
    z_MSB6(8*ii-4) =z_MSB6f(ii);
    z_MSB6(8*ii-3) =z_MSB6c(ii);
    z_MSB6(8*ii-2) =z_MSB6g(ii);
    z_MSB6(8*ii-1) =z_MSB6d(ii);
    z_MSB6(8*ii)  =z_MSB6h(ii);
end
ch6_data= shiftb2alj (z_LSB6, z_MSB6, totalpoints*4);
ch6_final=ch6_data/2^8/gainI;
%processing channel 7 data
z_LSB7a=z(:,13);
z_MSB7a=z(:,14);
z_LSB7b=z(:,13+32);
z_MSB7b=z(:,14+32);
z_LSB7c=z(:,13+32+32);
z_MSB7c=z(:,14+32+32);
z_LSB7d=z(:,13+32+32+32);
z_MSB7d=z(:,14+32+32+32);
z_LSB7e=z(:,13+16);
z_MSB7e=z(:,14+16);
z_LSB7f=z(:,13+32+16);
z_MSB7f=z(:,14+32+16);
z_LSB7g=z(:,13+32+32+16);
z_MSB7g=z(:,14+32+32+16);
z_LSB7h=z(:,13+32+32+32+16);
z_MSB7h=z(:,14+32+32+32+16);
for ii=1:totalpoints/2
    z_LSB7(8*ii-7) =z_LSB7a(ii);
    z_LSB7(8*ii-6) =z_LSB7e(ii);
\[ \text{z_LSB7}(8*\text{ii}-5) = \text{z_LSB7b}(\text{ii}); \]
\[ \text{z_LSB7}(8*\text{ii}-4) = \text{z_LSB7f}(\text{ii}); \]
\[ \text{z_LSB7}(8*\text{ii}-3) = \text{z_LSB7c}(\text{ii}); \]
\[ \text{z_LSB7}(8*\text{ii}-2) = \text{z_LSB7g}(\text{ii}); \]
\[ \text{z_LSB7}(8*\text{ii}-1) = \text{z_LSB7d}(\text{ii}); \]
\[ \text{z_LSB7}(8*\text{ii}) = \text{z_LSB7h}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-7) = \text{z_MSB7a}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-6) = \text{z_MSB7e}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-5) = \text{z_MSB7b}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-4) = \text{z_MSB7f}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-3) = \text{z_MSB7c}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-2) = \text{z_MSB7g}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}-1) = \text{z_MSB7d}(\text{ii}); \]
\[ \text{z_MSB7}(8*\text{ii}) = \text{z_MSB7h}(\text{ii}); \]
\]
\text{end}

\text{ch7\_data} = \text{shiftb2alj (z_LSB7, z_MSB7, totalpoints*4)};
\text{ch7\_final} = \text{ch7\_data}/2^8/\text{gainI};

%processing channel 15 and 16 data to create time vector
\text{z_LSB15} = \text{z(:,29)};
\text{z_MSB15} = \text{z(:,30)};
\text{z_LSB16} = \text{z(:,31)};
\text{z_MSB16} = \text{z(:,32)};
\text{timedataold} = \text{shift\_time2 (z_LSB15, z_MSB15, z_LSB16, z_MSB16, totalpoints)};
\text{timedata} = [0:(2^{11}-1)]/25e6*2^9;

\text{Figure(1)};
\text{plot(timedata, ch4\_final, 'b', 'linewidth', 2);} \\
\text{hold on;}
\text{plot(timedata, ch5\_final, 'g', 'linewidth', 2);} \\
\text{hold off;}
\text{title('channel 4 and 5 data')}
\text{grid;}
\text{Figure(2)};
\text{plot(timedata, ch7\_final, 'g', 'linewidth', 2);} \\
\text{hold on;}
\text{plot(timedata, ch7\_final, 'go', 'linewidth', 2);} \\
\text{hold off;}
\text{title('channel 7 data')}
\text{grid;
MATLAB CODE FOR TEMPERATURE VS TIME SIMULATION

%%Temp Vs Time MEASUREMENTS

Time=[0,60,120,180,240,300,360,420,480,540,600,660,720,780,840 ];
Temp=[23,30.4,37,39.9,43.4,46,49,50.8,52.4,52.9,53,53,53,53,53];

plot(Time,Temp,'x')
hold on;
plot(Time,Temp,'r')
grid on;
title('Thermal Behavior analysis Data for LM35 on IPM IGBT Heat sink'),
xlabel('Time[s]'), ylabel('Temperature[C]');

MATLAB Code for Low Pass Filter Simulation

LowPASS Filter
R1=2*56e3;
R2=3e3;
C=4700e-12;

freq=[1:10000]*5;
jw=j*2*pi*freq;
Zp=R2.*(1./jw./C)./(R2+(1./jw./C));
gain=Zp./(R1+Zp);

Figure(1);
semilogx(freq,20*log10(abs(gain)));
grid;
title('Lowpass filter Amplitude Response'), xlabel ('Frequency(Hz)'),
ylabel('Decibel')
Figure(2);
semilogx(freq,angle(gain)*180/pi);
grid;
title('Lowpass filter Phase shift'), xlabel ('Frequency(Hz)'),
ylabel('Phase(degrees)')
APPENDIX C. SEMITEACH® POWER INVERTER

Figure 30. SEMITEACH® power inverter (From: [13])
LIST OF REFERENCES


1. Defense Technical Information Center  
   Ft. Belvoir, Virginia

2. Dudley Knox Library  
   Naval Postgraduate School  
   Monterey, California

3. Dr. R. Clark Robertson  
   Electrical Engineering and Computer Department  
   Code EC  
   Naval Postgraduate School  
   Monterey, California

4. Dr. Alexander Julian  
   Electrical Engineering and Computer Department  
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