Research Title: High κ dielectrics on InGaAs and GaN

- **Growth, interfacial structural studies, and surface Fermi level unpinning**

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Our research activities during the last five years from 2006 to 2010 have been on the science and technology of III-V InGaAs and GaN metal-oxide-semiconductor (MOS) systems using high κ dielectrics. The new technology of high-κ plus metal gate on the high carrier mobility semiconductors hybrid with Si will lead to faster devices and closing the so-called performance gap, where the expected increase in switching speed of the devices no longer keeps up with the scaling trend. This has set unprecedented challenges for material physicists and device engineers.

We have successfully continuously kept our world-leading expertise of high-κ dielectric growth on InGaAs and GaN, including high-κ enhancement, surface Fermi level unpinning, the oxide scaling (EOT) to < 1 nm, and the high temperature thermal stability. Our hetero-structures of high-κ's/InGaAs and GaN are of excellent quality such that low D_{it}'s have been obtained with meaningful, well-behaved CV, QSCV, conductance, and charge pumping characteristics. Furthermore, we have demonstrated world-record device performance in inversion-channel InGaAs MOSFET, superior to Si in the same gate length, and GaN MOSFET.

We have achieved many firsts in the nano-electronics research, critical for the technologies beyond Si CMOS:

(1) Have achieved and continued to hold **world record high** dc and rf device performances, including the drain current, transconductance, and current gain cutoff frequency **for the first time** in the self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs based on both *ex-situ* ALD-Al_2O_3 and *in-situ* MBE-Al_2O_3/$Ga_2O_3(Gd_2O_3)$ [GGO] as the gate dielectrics. The advances of the InGaAs MOSFETs achieved will enable future CMOS technology in a vital way.

(2) First to fabricate depletion-mode GaN MOSFET with very high drain currents and negligible current collapse), (via inversion/accumulation due to a very low D_{it}), and to achieve inversion-channel GaN *n*MOSFET with ALD Al_2O_3 as a gate dielectric.

(3) First to demonstrate oxide scaling of MBE-grown HfAlO/HfO_2 and GGO on $In_{0.2}Ga_{0.8}As$ to a CET of 1 and <0.8 nm, respectively, and high-temperature thermal stability withstanding 850-900°C RTA, critical for inversion-channel III-V MOSFETs.

(4) First to achieve a very low interfacial trap density in atomic layer deposited Al_2O_3 on $In_{0.53}Ga_{0.47}As$, thus setting up a standard for academics and industry in the field, and first to achieve surface Fermi level unpinning and oxide scaling of ALD-HfO_2 on $In_{0.53}Ga_{0.47}As$ to a CET of <1.0 nm.   ALD has been widely used in the Si industry for high-κ gate dielectrics deposition.

(5) First to grow high-κ hcp Gd_2O_3 on GaN with a CET of 0.5 nm.

(6) Overgrowth of single crystal GaN on Si (111) with the nm-thick single crystal oxide as a template.

(7) First to perform *in-situ* XPS analysis to determine the energy-band parameters at interfaces of high-κ oxides on GaAs and InGaAs, and showed that absence of arsenic oxide and elemental arsenic was a

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14. ABSTRACT
This is the report of a project to maintain world-leading expertise of high-κ dielectric growth on InGaAs and GaN, including high-κ enhancement, surface Fermi level unpinning, oxide scaling to < 1 nm, and high temperature thermal stability.

15. SUBJECT TERMS
CMOS, Gallium Nitride , Nanotechnology

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principal mechanism responsible for Fermi level unpinning at the dielectric oxide/GaAs interface, thereby leading to effective passivation of the GaAs and InGaAs surfaces.

(8) Have established the in-house capabilities of MOSFET photolithographic processing on both Si and GaAs semiconductor of at least 2 inch substrates with the incorporation of high-κ gate oxides and metal gates at a typical gate length of $< 1.0 \ \mu m$.

Here in this report, we present three of our major accomplishments in InGaAs and GaN MOSFETs:

✓ High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ and $In_{0.75}Ga_{0.25}As$ MOSFET's with $Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectrics

✓ High performance self-aligned inversion-channel MOSFETs with $In_{0.53}Ga_{0.47}As$ channel and ALD-Al_2O_3 gate dielectric

✓ GaN accumulation-type (depletion-mode) metal-oxide-semiconductor field-effect-transistor with atomic-layer-deposited HfO_2 as a gate dielectric

High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ and $In_{0.75}Ga_{0.25}As$ MOSFET's with $Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectrics

Key accomplishments in devices of 1μm gate length:
High drain current of 1.23 mA/μm
High transcoductance of 714 μS/μm
High electron mobility of 1600 cm^2/V·s

Introduction

The quest for technologies beyond the 16 nm node complementary metal-oxide-semiconductor (CMOS) devices has now called for research on high-κ gate dielectrics on channel materials with high carrier mobility.[1] $In_{0.53}Ga_{0.47}As$ has long been used as a backbone for virtually all high-speed electronic devices. Among several reports on the passivation of the InGaAs surface, there are two approaches that have achieved a low interfacial density of states (D_{it}) and a low electrical leakage current density without invoking interfacial layers; namely, ultra high vacuum (UHV) deposited $Ga_2O_3(Gd_2O_3)$ [GGO] [2] and Gd_2O_3, [3] and atomic layer deposited (ALD) Al_2O_3 and HfO_2. In these studies, MOS diodes and MOS field-effect-transistors (MOSFET's) with the high-κ dielectrics directly deposited on InGaAs showed inversion-channel characteristics, similar to those exhibited in the traditional SiO_2/Si.

In 1990s, employment of GGO enabled the demonstration of the first non-self-aligned inversion-channel GaAs and $In_{0.53}Ga_{0.47}As$ MOSFETs. $In_{0.53}Ga_{0.47}As$ MOSFETs with GGO 40 nm thick as the gate dielectric exhibited a maximum drain current of 375 μA/μm (1-μm gate length) and a transconductance (G_m) of 190 μS/μm (0.75-μm gate-length), respectively.[4] Recently, other non-self- aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD-Al_2O_3 as a gate dielectric were also demonstrated, in that an 0.5-μm gate-length $In_{0.53}Ga_{0.47}As$ MOSFET with an ALD-Al_2O_3 gate oxide 8 nm thick gave a maximum drain current of 367 μA/μm, and a G_m of 130 μS/μm.[5] More recently, a 0.4-μm gate-length inversion-channel $In_{0.65}Ga_{0.35}As$ MOSFET with an even higher In content and an ALD-Al_2O_3 gate oxide 10 nm thick showed a drain current of 1.05 mA/μm, and a G_m of 350 μS/μm.[6] The improved device performance was attributed to a shorter gate length, and a higher In content in the channel, which gives rise to enhancements in electron mobility, saturation velocity, intrinsic carrier concentrations, along with a smaller charge neutrality level below the conduction band minimum. Nonetheless, the non-self-aligned process is impractical for device integration, due to the complexity of mask alignment as well as the unavoidable parasitic resistance

Experimental

The experimental details in film growth, device processing, and measurements were given in References 7 and 8.

Results and Discussion

In this work, self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs, using UHV deposited Al_2O_3/GGO and a TiN metal gate, were fabricated. For a $In_{0.53}Ga_{0.47}As$ MOSFET using a gate dielectric of Al_2O_3(2nm-thick)/GGO (5nm-thick), a maximum drain current of 1.05 mA/μm, a G_m of 714 μS/μm (as shown in Fig. 1 (a) and (b)), and a peak mobility of 1300 cm^2/V·s (Fig. 3 (a)) have been achieved, the highest ever reported for III-V inversion-channel devices of 1-μm gate-length.
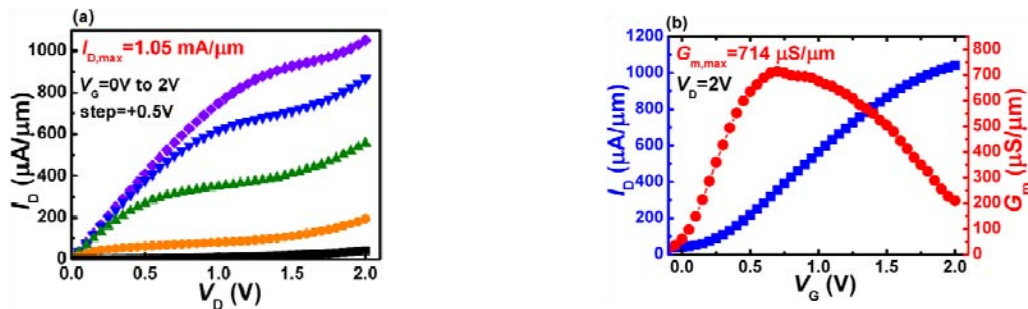
Fig. 1 (a) Drain current (I_D) vs. drain bias (V_D) of a 1μm (length)×10μm (width) inversion-channel Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$ MOSFET. A maximum I_D of 1.05 mA/μm is measured at gate bias (V_G) = 2V and V_D= 2V; (b) The transfer characteristics and transconductance (G_m) curve of the same device showing a maximum G_m of 714 μS/μm, measured at V_G= 0.7V and V_D= 2V

More recently, a 1μm-gate-length self-aligned inversion-channel $In_{0.75}Ga_{0.25}As$ MOSFET using Al_2O_3(3nm-thick)/GGO(12nm) gate dielectrics demonstrated an $I_{D\text{-}max}$ of 1.23 mA/μm, a $G_{m\text{-}max}$ of 464 μS/μm, and a peak mobility of 1600 cm^2/V·s (Fig. 3 (b)), setting a new record of maximum drain current for enhancement-mode III-V MOSFETs.
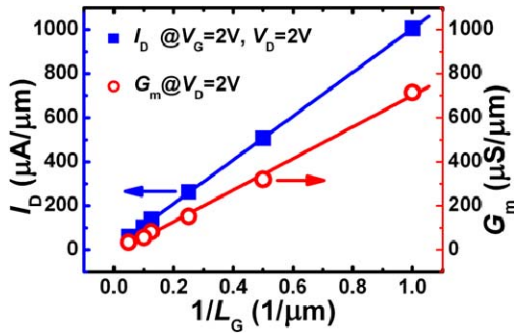

Fig. 2 I_D at V_D=2V, V_G=2V and peak G_m at V_D=2V versus inverse gate-length (1/L_G). Since Both properties are proportional to the inverse gate length, 1/L_G, a maximum drain current of approximately 2 mA/μm and a peak transconductance of about 1.4 mS/μm are expected for a device with 0.5μm gate-length, assuming that all the other parameters remain unchanged.

Fig. 3 Plot of field effective electron mobility (μ_{FE}) as a function of gate bias for (a) a 1 μm×10 μm inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFET and (b) a 4 μm×10 μm inversion-channel $In_{0.75}Ga_{0.25}As$ MOSFET. The mobility was derived using the formula shown in the inset, in which C_{ox} is the dielectric capacitance, and V_D the drain voltage.
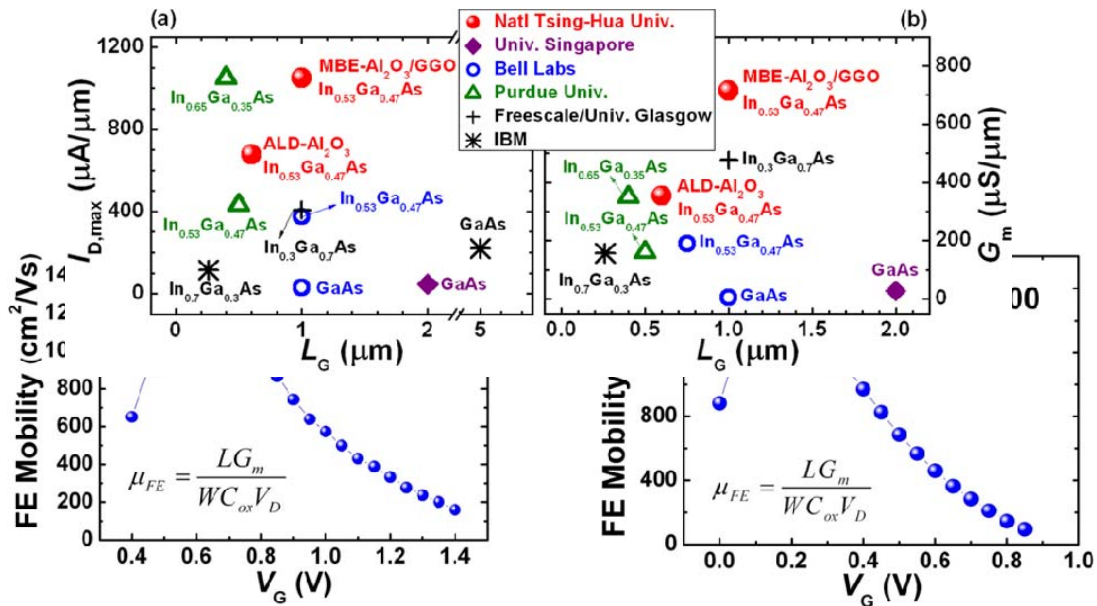
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High performance self-aligned inversion-channel MOSFETs with $In_{0.53}Ga_{0.47}As$ channel and ALD-Al_2O_3 gate dielectric

Key accomplishments:
Highest drain current and transcoductance for all the inversion-channel MOSFETs based on ALD-

Fig. 4 Summary of (a) the maximum drain current I_D and (b) peak transconductance G_m of representative work on E-mode III-V *n*-MOSFETs reported in the last decade.

Al_2O_3 gate dielectric and $In_{0.53}Ga_{0.47}As$ channel based on the gate length of $1\mu m$

Introduction

For future practical device integration, a self-aligned $In_{0.53}Ga_{0.47}As$ MOSFET was successfully implemented, using molecular beam epitaxy (MBE) grown $In_{0.53}Ga_{0.47}As$ as the channel, ALD-Al_2O_3 as the gate dielectric, and sputtered TiN as the gate metal. The key of the self-aligned process in fabricating inversion-channel III-V MOSFETs is to ensure good interface property after high-temperature thermal process to achieve optimal dopant activation with low S/D resistance.

Experimental

The transfer time from the MBE chamber to the *ex-situ* ALD reactor was less than 10 min, resulting in a high-quality Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface, which has sustained rapid-thermal-annealed (RTA) at 650^oC; Nevertheless, a very thin interfacial layer (~1-2 atomic layers), composed of In_2O_3, Ga_2O_3, $In(OH)_x$, and $Ga(OH)_x$, was inevitably formed. Near the mid-gap, a low mean interfacial density of states is ~2.5×10^{11} $cm^{-2}eV^{-1}$ and a high Fermi-level movement efficiency is ~63% determined by the charge pumping method and quasi-static CV measurement, respectively.[1] Sub-micron gates were formed by E-beam lithography and dry etching of TiN.

Results and Discussion

The $100\mu m\times0.6\mu m$ (width (W)×length (L)) device with output characteristics and G_m shows a maximum I_D of 678 µA/µm, and a peak G_m of 354 µS/µm (Fig. 1 and Fig. 2); the device performance is higher than those obtained with ALD-Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFET using a non-self-aligned process (using ammonia sulfide treatment for InGaAs surface), which showed a maximum I_D of 400 µA/µm and a peak G_m of 180 µS/µm for a 0.5-µm gate length device.[2] For devices with gate length from 20µm to 0.6 µm, both the drain current and G_m are inversely proportional to the gate length in logarithm scale (shown in Fig. 3). The threshold voltage (V_{th}) and sub-threshold swing (S.S.) showed slight variations with gate lengths from 20µm to 0.6µm (shown in Fig. 4).

In this work, a self-aligned process has been employed in device integration. For the self-aligned inversion-channel III-V MOSFETs using *ex-situ* ALD-Al_2O_3 as a gate dielectric, an optimization has been taken by using short air exposure between the oxide and semiconductor deposition, dopant activation at 650^oC, and higher implanted-ion concentration. The device with 0.6-µm gate length showed very high maximum I_D and peak G_m compared to all the other inversion-channel MOSFETs with $In_{0.53}Ga_{0.47}As$ channel and *ex-situ* deposited dielectrics. The benchmarking is shown in Fig. 5.
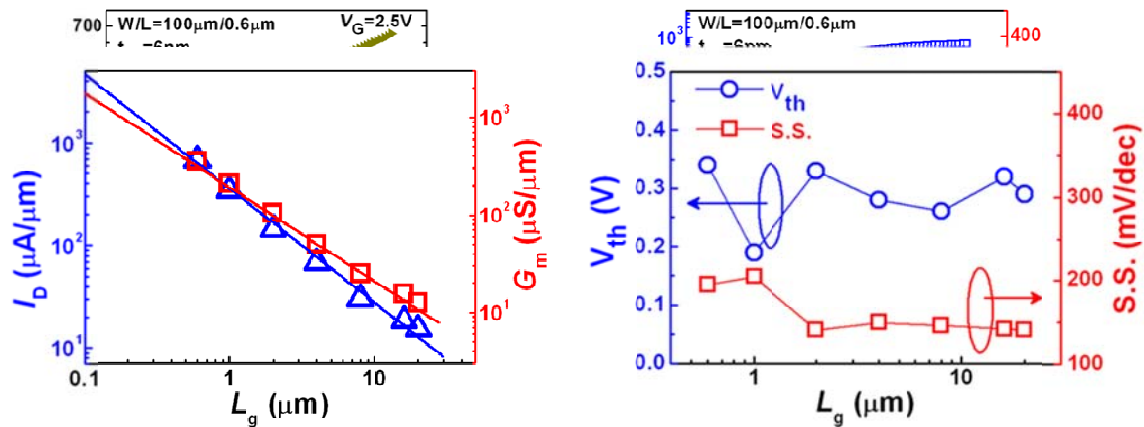
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GaN accumulation-type (depletion-mode) metal-oxide-semiconductor field-effect-transistor with atomic-layer-deposited HfO_2 as a gate dielectric

Abstract

Accumulation-type GaN metal-oxide-semiconductor field-effect-transistors (MOSFET's) with atomic-layer-deposited HfO_2 gate dielectrics have been fabricated; a 4µm gate-length device with a gate dielectric of 14.8 nm in thickness (an equivalent SiO_2 thickness of 3.8 nm) gave a drain current of 230 mA/mm and a broad maximum transconductance of 31 mS/mm. Owing to a low interfacial density of states (D_{it}) at the HfO_2/GaN interface, more than two third of the drain currents come from accumulation, in contrast to those of Schottky-gate GaN devices.
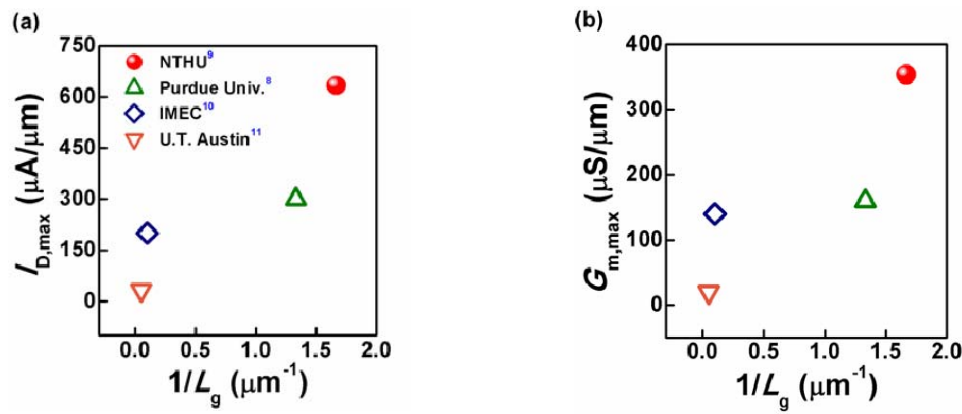
Fig. 5 Summary of (a) the maximum drain current and (b) peak transconductance of published work[2-5] on E-mode III-V n-MOSFETs using ALD-Al_2O_3 as gate dielectrics.

The device also showed negligible current collapse in a wide range of bias voltages, again due to the low D_{it}, which effectively passivate the surface states located in the gate-drain access region. Moreover, the device demonstrated a larger forward gate bias of +6 V with a much lower gate leakage current.

Introduction

GaN, with a high saturation velocity at high electrical fields ($\upsilon_{sat} \sim 3 \times 10^7$ cm/s at 150 kV/cm), a high critical electrical field (up to 3 MV/cm), good thermal conductivity, and high-quality epi-layers grown on Si, has been studied for applications in high-power and high-temperature devices, e.g. hetero-junction field-effect transistors (HFETs) and bipolar junction transistors (BJTs). Compared to conventional high power RF AlGaN/GaN HFETs, GaN metal-oxide-semiconductor field-effect-transistors (MOSFETs) feature lower gate leakage currents, a larger gate voltage sweep range, a simpler device and circuit structure, which have drawn great interest.[1-7] The gate dielectrics used in passivating GaN surface could also minimize/eliminate the current collapse that occurs in unpassivated GaN electronics, due to the traps existed in the regions between the gate and drain electrodes, and significantly reduces RF output power and degrades the device performance.

In this work, we report a high-performance depletion-mode GaN MOSFET based on ALD-HfO_2 as a gate dielectric. Compared to the previously reported depletion-mode GaN-based MOSFET's and HEMT's, the device demonstrates excellent dc output as well as transfer characteristics, such as a high drain current (I_D) with negligible current collapse, a high transconductance (G_m), low gate leakage currents, and a large gate voltage sweep range.

Experimental

The growth of HfO_2/GaN was described earlier, with GaN grown by metal organic chemical vapor deposition and HfO_2 by ALD with tetrakis-(ethyl-methyl-amino)-hafnium (TEMAH) and H_2O as the precursors. A post-deposition anneal at 600°C was carried out under nitrogen ambiance for 10 minutes to optimize oxide and interface

quality. X-ray reflectivity measurements for the annealed sample have revealed that the oxide consists of two layers with an overall thickness of 14.8 nm, bulk HfO_2 (13.2 nm) and an interfacial layer GaON 1.6 nm thick. The interfacial roughness was small of 0.41 nm, critical to make a high-performance device. The determination of oxide film thickness was needed for fabricating the device.

Results and Discussion

X-ray reflectivity (XRR) was carried out to study the oxide film thickness and roughness of HfO_2 surface and of the oxide/GaN interface for the annealed HfO_2/GaN heterostructure: the analysis of the measured fringe pattern (Fig. 1(a)) has revealed that the oxide consists of two layers with an overall thickness of 14.8 nm. The thickness of bulk HfO_2 was determined to be 13.2 nm, with an interfacial layer GaON 1.6 nm thick at the HfO_2/GaN interface. The existence of interfacial layer indicates chemical reactions among TEMAH, H_2O, and GaN during the ALD process. The determination of oxide film thickness was needed for fabricating the depletion-mode GaN MOSFET. The roughness of the HfO_2 surface and the HfO_2/GaON, GaON/GaN interfaces were determined to be 0.38 nm, 0.44 nm, and 0.41 nm, respectively.

Capacitance-voltage (C-V) characteristics of Al/HfO_2/GaN MOS capacitor exhibited accumulation, depletion, and deep depletion behavior, as shown in Fig. 1 (b). A dielectric constant of 15.1 at 100 kHz and a hysteresis of 160 mV at flatband voltage were obtained. Note that both the HfO_2 film and the interfacial GaON with a lower dielectric constant contribute to the measured dielectric constant. An equivalent SiO_2 thickness of the HfO_2 bi-layer is 3.8 nm. The D_{it} was calculated to be around $8 \times 10^{11} cm^{-2} eV^{-1}$ near conduction-band minimum of GaN using the conductance method. The C-V characteristics with small hysteresis and a low D_{it} indicate the effective passivation of ALD-HfO_2/GaN interface. The smooth interface and surface, even after a high temperature annealing, have attributed to the excellent electrical properties, critical to make a high-performance field-effect transistor. Ring-gate depletion-mode GaN MOSFET's were fabricated with a two-step process: S/D contact metal and gate metal formation. The schematic cross-sectional view and the planar view of the fabricated ring-gate GaN MOSFET are shown in Fig. 1 (c) and 1 (d), respectively.

Figure 2 shows the drain I–V characteristics of a 4 m gate-length MOSFET with the gate voltage (V_G) varying from -8 V to +6 V with a step of 2 V. The pinch-off voltage of the fabricated device is -8 V. The maximum I_D is 230 mA mm at V_G of +6 V and a drain voltage (V_D) of 20 V. Compared to Schottky-gated GaN devices with a barrier built-in voltage < 1 eV, our device demonstrated a larger positive gate voltage (+6V) with a low gate leakage current, thus leading to higher accumulated currents and better reliability. The larger positive gate voltage and gate voltage sweep range are resulted from the high conduction-band offset > 2 eV of HfO_2/GaN.[19] A low specific on-resistance (R_{on}) ~ 4.5 mΩ·cm^2 was achieved even though the gate-to-source spacing was large of 3 m and the doping concentration of channel layer was as low as 2×10^{17} cm^{-3}.

The transfer characteristics (L/W=4 μm/200 μm), with V_G sweeping from -8 V to +4 V, and for V_D of 15 V, are shown in Fig. 3. The device exhibits a broad extrinsic G_m curve, with the peak G_m being ~31 mS/mm with V_D of 15 V. The calculated channel mobility (μ_n) of ~400 cm^2/Vs was derived using the following equation: $\mu_n = G_m \cdot (L/W)/N_d T_{ch}$, where N_d and T_{ch} are the doping concentration and the thickness of the channel layer.[2] An I_{on}/I_{off} ratio was extracted to be ~10^2 with a high off-state drain current (I_{off}) of 10^{-6}A/μm at a V_D of 15 V. The channel leakage currents, resulted from the undoped GaN layer with unintentional donor doping concentration of ~10^{16} cm^{-3}, may have caused high I_{off}, which can be improved by inserting a p-type GaN layer under the n-channel layer as a junction barrier to reduce the additional channel leakage currents.

The gate-to-drain, gate leakage current density (J_g) as a function of gate voltage of the device was measured by grounding the drain, and sweeping V_G from -10 V to +8 V. The very low J_g of 10^{-8} A/cm^2 at V_G varying from -10V to +2 V was achieved (Fig. 4(a)) and is significantly lower than that of the Schottky-gate GaN devices by at least five orders of magnitude at V_G > +1 V. Even at the gate voltage of +6 V, the device also provides the gate leakage current density as low as 10^{-2} A/cm^2. The low gate leakage current reveals the high quality and robustness of the HfO_2/GaN heterostructure after 600°C annealing. The oxide breakdown voltage is 6.5 V, corresponding to an electrical breakdown field of 4.4 MV/cm. In addition, the measured I_G-V_D characteristics of the GaN MOSFET's under the off-state gate bias condition (V_G = -8 V) is also shown in the inset of Fig. 4(a). The extremely low I_G ~10^{-8} mA/mm was observed even at V_D over 30V. The three-terminal breakdown voltage (BV_{DS}) of the GaN MOSFET is more than 60V even with the gate-to-drain spacing of only 3 μm.

The pulsed I-V measurements with different pulse widths of 80 μs and 300 μs were performed to analyze the current collapse on the device, and are shown in Fig. 4(b) along with that of DC condition. No significant current collapse was observed in both pulse I-V curves, indicating the good surface passivation of using ALD-HfO_2 in the regions between gate and drain electrodes: the evidences are the negligible dispersion between DC and pulsed I-V curves in the knee region, and no I_D reduction of both pulsed I-V curves in the saturation region. Oppositely, an increased I_D of pulsed I-V curves was observed which is due to the relieving of self-heating effect occurring under high drain bias. In addition, the pulsed I-V curve with a shorter pulse width of 80 μs shows a higher I_D in the

saturation region which also manifests the existence of self-heating effect in the device. The ALD-HfO$_2$ used as an insulated gate and a surface passivation layer is very effective in decreasing the gate leakage currents and suppressing the current collapse, thereby leading to the reliability improvement of GaN-based MOS devices.

In summary, we have demonstrated a depletion-mode GaN MOSFET using ALD-HfO$_2$ as a gate dielectric; the device has achieved the highest I_D of 230 mA/mm and G_m of 31 mS/mm, compared to those of previously reported GaN MOSFET's.[1-7] The large dielectric constant of HfO$_2$ and high-quality
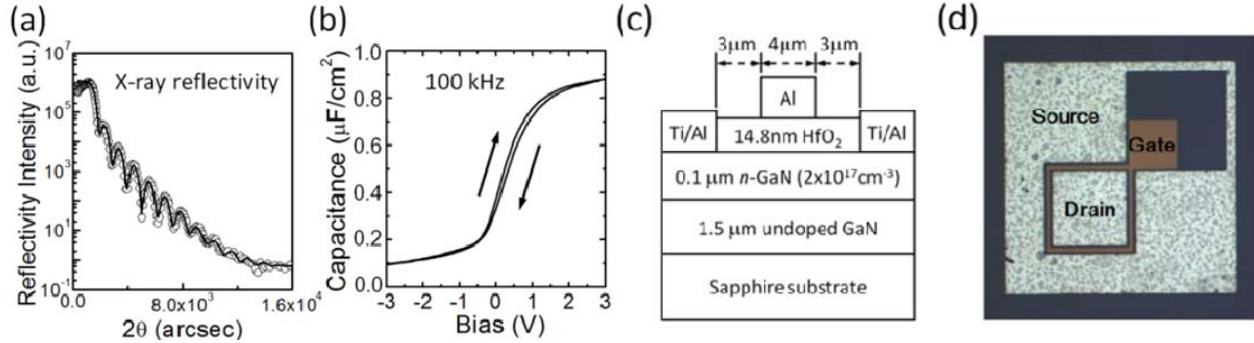

Fig. 1 (a) X-ray reflectivity of ALD-HfO$_2$ on GaN, with experimental data (dots) and a theoretical fit (line); (b) C-V hysteresis measured at 100 kHz for the Al/HfO$_2$/GaN MOS capacitor; (c) schematic device structure of the fabricated depletion-mode GaN MOSFET; (d) planar view of the ring-gate MOSFET structure
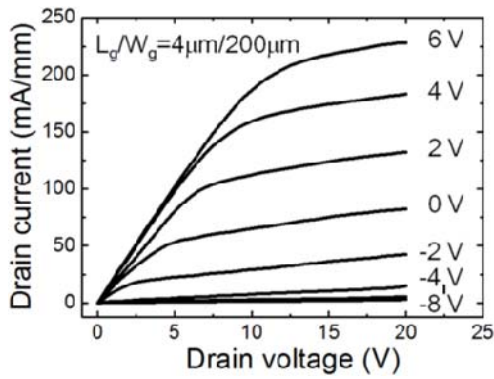

Fig. 2 Drain I_D-V_D characteristic for a 4 μm gate length GaN MOSFET with a 14.8 nm ALD-HfO$_2$ as a gate dielectric
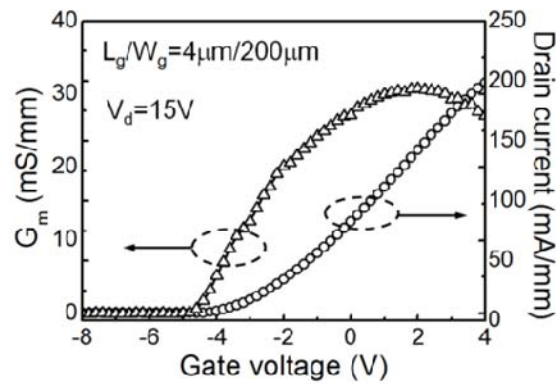
Fig. 3 Transconductance (G_m) and drain current as a function of gate bias at a drain voltage of 15 V.

HfO$_2$/GaN interface have attributed to the high device performance. In addition, compared to the state-of-the-art GaN HEMT devices, the HfO$_2$/GaN MOSFET provides not only lower gate leakage currents, negligible current collapse, and a simple design but also comparable drain currents, with the devices being normalized to the same gate length.
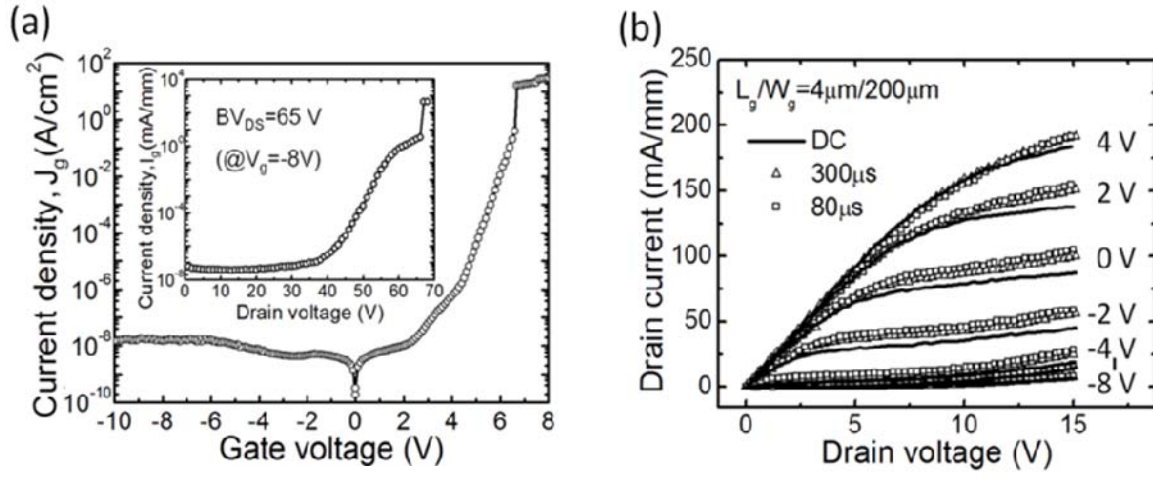
Fig. 4 (a) Gate leakage current density (J_g) vs gate voltage for GaN MOSFET, with the I_G-V_D characteristics under the off-state gate bias condition plotted in the inset; (b) pulsed I–V characteristics with pulse widths of 300 μs and 80 μs.

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List of Publications: Please list any publications, conference presentations, or patents that resulted from this work.

1. "Drain current enhancement and negligible current collapse in GaN MOSFETs with atomic-layer-deposited HfO_2 as a gate dielectric", Y. C. Chang, W. H. Chang, Y. H. Chang, J. Kwo, Y. S. Lin, S. H. Hsu, J. M. Hong, C. C. Tsai, and M. Hong, Microelectronic Engineering **87(11)** 2042 (2010).
2. "Passivation of InGaAs using *in situ* molecular beam epitaxy Al_2O_3/HfO_2 and $HfAlO/HfO_2$", P. Chang, W. C. Lee, M. L. Huang, Y. J. Lee, M. Hong, and J. Kwo, J. Vac. Sci. Technol. B 28(3), C3A9 (2010).
3. "Engineering of threshold voltages in molecular beam epitaxy-grown $Al_2O_3/Ga_2O_3(Gd_2O_3)/In_{0.2}Ga_{0.8}As$", Y. D. Wu, T. D. Lin, T. H. Chiang, Y. C. Chang, H. C. Chiu, Y. J. Lee, M. Hong, C. A. Lin and J. Kwo,   J. Vac. Sci. Technol. B 28(3), C3H10 (2010).
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