0.18 μm CMOS Fully Differential CTIA for a 32x16 ROIC for 3D Ladar Imaging Systems

Jirar Helou
Jorge Garcia
Fouad Kiamilev
University of Delaware
Newark, DE

William Lawler
Army Research Laboratory
Adelphi, MD

SPIE 2006, San Diego
0.18 μm CMOS Fully Differential CTIA for a 32x16 ROIC for 3D Ladar Imaging Systems

University of Delaware, Department of Electrical and Computer Engineering, Newark, DE, 19716

Approved for public release; distribution unlimited

Proceedings SPIE Vol. 6294, 629409, Infrared and Photoelectronic Imagers and Detector Devices II; Sep 2006, San Diego, CA
Presentation Outline

• Introduction
  – Photo-detection for AM/CW LADAR using MSM detectors
  – CDMA ROIC architecture

• Fully Differential Channel
  – Differential MSM photo-detector
  – Differential CDS CTIA
  – Mitigation of RF leakage current

• Design Implementation
  – Floor plan and Layout
  – Post-layout Simulation

• Future work
  – Testing methodology
AM/CW Ladar Photo-detection

- RF modulation and demodulation
- Parasitic leakage current
  - Four to five orders of magnitude > signal of interest
• Orthogonal sets of codes
• Column-wise encoding
Presentation Outline

• Introduction
  – Photo-detection for AM/CW LADAR using MSM detectors
  – CDMA ROIC architecture

• Fully Differential Channel
  – Differential MSM photo-detector
  – Differential CDS CTIA
  – Mitigation of RF leakage current

• Design Implementation
  – Floor plan and Layout
  – Post-layout Simulation

• Future work
  – Testing methodology
• Disadvantages
  – Not fully Differential architecture
  – Non balanced charged injection in the encoding cell
• Advantages
  – Cancel charge injection imbalance
  – Obtain true and complementary output signals at once
Fully Differential Readout Channel
Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (1)

- Things to worry about
  - Thermal noise (RTIA)
  - Sampling noise (CTIA)
- Solution
  - Correlated double sampling (CDS) capacitive trans-impedance amplifier
Fully Differential Readout Channel
Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (2)

• Single-ended CDS CTIA
  – Charge injection causing pedestal errors
Fully Differential Readout Channel
Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (2)

- **Differential CDS CTIA**
  - Charge injection cancellation
  - True and complementary signal integration
Fully Differential Readout Channel

Mitigation of radio frequency leakage current

- Filter RF before the Encoding cell
  - LC-ladder filters
  - RC-ladder filters
  - Shunt Capacitor

Moreover, Differential Shunt Capacitor

- Shunt Capacitor
Presentation Outline

• Introduction
  – Photo-detection for AM/CW LADAR using MSM detectors
  – CDMA ROIC architecture

• Fully Differential Channel
  – Differential MSM photo-detector
  – Differential CDS CTIA
  – Mitigation of RF leakage current

• Design Implementation
  – Floor plan and Layout
  – Post-layout Simulation

• Future work
  – Testing methodology
Design Implementation

- 0.18 μm CMOS 32x16 Fully Differential ROIC
  - 32x16 MSM Differential detector
  - 32 CDS CTIA’s
  - Highly Scalable
    - Special Layout of Components
      - Detector Elements
      - CTIA’s
Design Implementation
Differential Input Element

- Four transistor encoding cell
- Differential detector bond pad
- Parasitic shunt capacitor

Size
100 µm height
200 µm width
Design Implementation
Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier

Size

1500 μm length

400 μm height

*Four times the height of the detector element*

*Increases scalability*
Design Implementation
Full IC Layout

Fabricated Test ROIC

- 8.4 x 8.4 mm²
- Symmetric
- Scalable
  - A 64x32 System
Design Implementation
Post-layout Simulations

DC INPUT CURRENT
NON ENCODED
i_{in} = 5nA, i_{ip} = -5nA

Sinusoidal Characteristic
Presentation Outline

• Introduction
  – Photo-detection for AM/CW LADAR using MSM detectors
  – CDMA ROIC architecture

• Fully Differential Channel
  – Differential MSM photo-detector
  – Differential CDS CTIA
  – Mitigation of RF leakage current

• Design Implementation
  – Floor plan and Layout
  – Post-layout Simulation

• Future work
  – Testing methodology
Future Work

Testing Methodology