Sensing and Control Electronics for
Low-Mass Low-Capacitance MEMS Accelerometers

by

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Sensing and Control Electronics for

Low-Mass Low-Capacitance MEMS Accelerometers

To my parents

To Tailin

Abstract

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Jiangfeng Wu

Doctor of Philosophy in Electrical and Computer Engineering

Carnegie Mellon University, Pittsburgh, PA

Professor L. Richard Carley, Advisor

In this work, circuit and system design techniques for sensing and controlling the motion of MEMS structures with ultra-small mass and ultra-small capacitance are investigated and are used to realize low noise integrated CMOS MEMS accelerometers. Structures fabricated by CMOS MEMS surface micromachining have total mass smaller than 10^{-9} kg and total sensing capacitance smaller than 100 fF. CMOS MEMS accelerometers typically have low sensitivity around 1 mV/g and less than 0.4 fF/g acceleration-induced capacitance change, therefore, noise and other nonidealities must be minimized. There are three sources of noise in MEMS accelerometers: electronic noise from sensor interface circuits; thermal-mechanical Brownian noise due to energy dissipation caused by damping; and quantization noise when analog-to-digital conversion is included. Other nonlinearities include sensor position offset, circuit offset and undesirable charging at the high-impedance sensing nodes.

In the area of sensing circuit design, we introduce a circuit noise model that is validated by experiments and provides insights on design trade-offs. We apply a set of circuit techniques to minimize the circuit noise and suppress other nonidealities, including: a low noise architecture based on chopper stabilized continuous-time voltage sensing; input-referred noise minimization based on capacitance matching at the sensor/circuit interface; a robust sensing node biasing scheme using periodic reset for charging suppression; and offset cancellation using differential difference amplifier. An integrated CMOS MEMS accelerometer prototype using these techniques achieves 50 µg/rtHz noise floor which is close to the Brownian noise floor, and > 40 dB of sensor offset reduction.

At the system level, force-balanced electromechanical delta-sigma modulation with high-Q micromechanical transducer is investigated to reduce Brownian noise and quantization noise altogether. A single loop architecture is introduced along with the switched-capacitor circuit implementation of the loop filter. A digital force feedback scheme called complementary pulse density modulation (CPDM) is proposed to realize highly linear offset-insensitive feedback using nonlinear actuators. Simulations show such systems realize high-resolution A/D conversion with 100 dB dynamic range and µg/rtHz quantization plus Brownian noise floor while simultaneously provide robust control to the high-Q micro structure to obtain near optimum closed-loop settling and less than 2 Angstrom proof-mass position error.

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I would like to dedicate this thesis to my parents, Dr. Shangzhou Jiang and Dr. Qidi Wu, who always encourage me to pursue high education and engineering career. This thesis is also dedicated to my fiancee, Tailin Zhang, for her constant love and support.

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Chapter 1

Introduction

Over the past twenty years, advances in micro fabrication technology have enabled the integration of multiple miniaturized sensors and actuators with analog and digital microelectronic circuits to create MicroElectroMechanical Systems (MEMS). This dissertation addresses two fundamental problems in MEMS systems: sensing and control. Low-noise capacitive sensing circuit techniques and robust feedback control system architectures are presented to show that by exploiting the integration capability of the MEMS technology to compensate for its inherent nonidealities, high-performance MEMS systems can be realized.

1.1 Motivation

The MEMS technology offers the capability to manufacture integrated systems of complex functionality on a single substrate at low cost and high volume. However, the performance of MEMS technology suffers from two inherent weaknesses: MEMS devices exhibit high manufacturing variations, high parameter uncertainties and various nonlinear behaviors; MEMS systems have low signal to noise ratio (SNR) and dynamic range (DR) because miniaturized structures are more susceptible to various noises and disturbances.

Inertial measurement is a major application area of MEMS technology. Studies show that micromachined accelerometers and gyroscopes have wide range of automotive, industrial, consumer and military applications, and occupy more than 20% of the total MEMS market with more than one billion dollars in sales [1, 2, 3, 4].

A comparison of major accelerometer technologies is shown in Figure 1-1. Capacitive sensing [6 - 24] is the dominant sensing mechanism in MEMS inertial sensors. Among a variety of sensing mechanisms, there are two main alternatives to capacitive sensing in micromachined devices. Piezoresistive sensing [25 - 27] has inferior performance due to intrinsic resistor thermal noise and strong temperature dependency, hence, is mainly used in low-end products. Tunneling current sensing achieves sub-µg/rtHz noise floor [28 - 30]. However, because tunneling devices require an extremely small gap between tip and electrode (< 10 Angstrom) and high voltage (> 10 V), they are very expensive to fabricate and difficult to integrate. Capacitive sensing has the advantages of low temperature coefficients, low power dissipation, low noise, low-cost
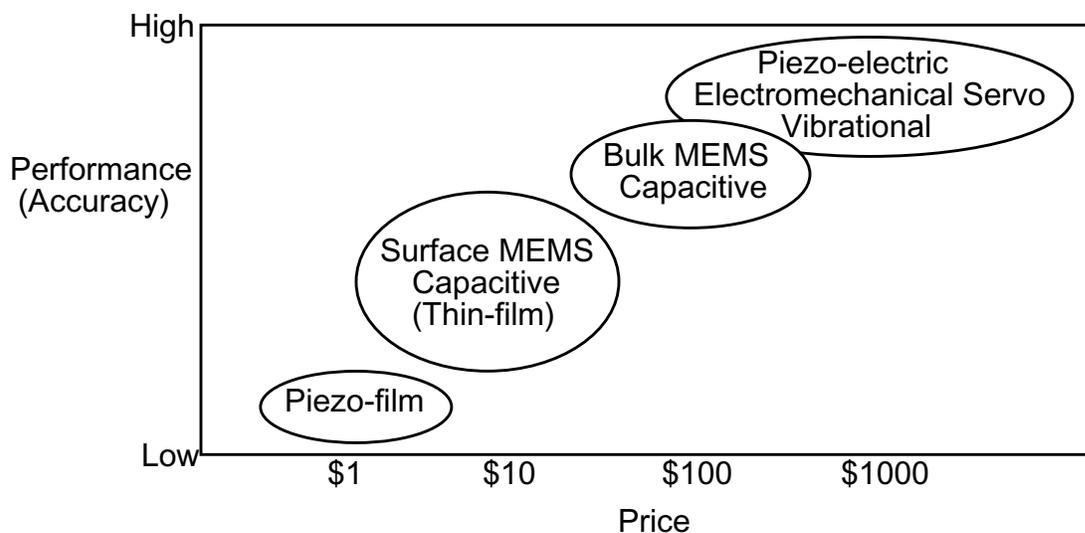
Figure 1-1: Cost and performance of accelerometer technologies [5].

fabrication, and compatibility with VLSI technology scaling. For these reasons, capacitive sensing has received the most attention and has been the most commercialized in recent years.

Based on fabrication methods, micromachined devices can be classified into two main categories: bulk micromachined devices and surface micromachined thin-film devices. The bulk capacitive sensors have higher sensitivity and lower noise floor than the thin-film devices because they have much larger mass and larger sensing capacitance. The main advantages of surface micromachining technology are low cost and easy integration of transducers and signal conditioning circuitry [2, 3, 4, 5]. In the last decade, thin-film capacitive accelerometers fabricated by polysilicon surface micromachining technology have been very successful in automotive and industrial applications. Commercial thin-film micro accelerometers achieve 200 µg/rtHz noise floor (ADXL105), have dual-axis sensing capability (ADXL202), and cost less than \$10 per unit [31]. However, almost all thin-film micro accelerometers have noise floor greater than 100 µg/rtHz. Many applications demand high-precision accelerometers with noise floor under 100 µg/rtHz in combination with good scale factor accuracy. For example, navigation applications generally require sub µg/rtHz noise floor and less than 0.1% overall scale factor error in acceleration measurement. Micro accelerometers fabricated by bulk micromachining and wafer bonding have reached µg/rtHz noise floor [11, 15, 19, 21, 29, 30]. However, the high manufacturing cost and the difficulty in integration make these devices less competitive. Today, the high-end inertial instrument market is still dominated by expensive non-MEMS electromechanical servo accelerometers and bulk piezoelectric accelerometers.

In many bulk and almost all thin-film MEMS accelerometers, the sensor resolution is limited by electronic noise from sensing circuit. Although all MEMS mechanical sensors have an intrinsic thermal-mechanical noise source called Brownian noise, the electronic noise floor is usually about one order of magnitude higher than the Brownian noise floor in both bulk and thin-film devices, even though the Brownian noise floor in bulk devices is several orders of magnitude lower. The circuit noise is more critical in thin-film accelerometers where the sensing capacitance is on the order of 10 - 1000 fF and the circuit noise usually greater than 100 μg/rtHz. The conventional sensor interface circuit designs are not optimized for noise and have become the performance bottleneck in MEMS inertial sensors. This calls for new capacitive sensing circuit design to significantly reduce the circuit electronic noise.

Besides noise, nonlinearities and variations of the transducers cause scale factor error in MEMS inertial sensors. This explains why feedback control is used in most high-end inertial sensors. In a closed-loop system, large loop gain can desensitize the closed-loop scale factor from nonidealities in the forward path, and make it solely depend on the feedback factor. Hence, the scale factor can be set accurately if linear and accurate feedback is established. In addition to improving scale factor accuracy, closed-loop control is also necessary for vacuum operation. Vacuum operation is important in many applications to improve the stability of MEMS devices, and is crucial for thin-film devices to overcome the Brownian noise barrier.

Compared to bulk micromachining, surface micromachining is not only less expensive, but also allows easier integration with electronics. One fundamental limitation of surface micromachining is that the thin-film devices have several orders of magnitude

higher Brownian noise because the available mass is very small, on the order of 10^{-10} kg. The Brownian noise of accelerometers is typically in the range of 10 - 100 µg/rtHz. The only way for surface micromachined sensors to overcome this limit is to operate the device in a vacuum environment to reduce the air damping, which is the main source of the Brownian noise. Low damping condition causes ringing in open-loop sensors. Therefore, closed-loop control must be employed to stabilize the transducer in any practical vacuum-packaged sensors.

The CMOS MEMS surface micromachining process developed at Carnegie Mellon University (CMU) is a typical example of surface micromachining [32]. On one hand, the fabrication process has very low cost and provides seamless integration with CMOS circuits. On the other hand, the device performance is severely limited. Because the device size is limited by the structural curling, both the mass and the sensing capacitance are smaller than in most polysilicon surface micromachining processes. The multi-layer structures have large fringe capacitance, which results in very low capacitance sensitivity. And both the manufacturing variation and the temperature variation are very large. The CMOS MEMS process provides an ideal testbed for advanced circuit and system design techniques which exploit the integration capability of MEMS to compensate the inherent weaknesses of the surface micromachining. In this work, techniques of low noise capacitive sensing circuit design and closed-loop control system design are explored to realize a low-noise high-precision micro accelerometer based on CMOS MEMS technology, thus, to prove that high-performance systems can indeed be realized by low-cost MEMS technology.

1.2 Research Direction

The performance of MEMS inertial sensors is determined by three fundamental issues: transducer design and fabrication; sensing circuit design; and control system design. The fabrication of the MEMS transducer is not the subject of this research. This work is based on the existing CMU CMOS MEMS surface micromachining process. This research focuses on the other two important aspects: sensing and control. The central problem of this project can be stated as the following: given the process limitations, how do we design the electronic subsystem to sense and control the motion of the MEMS transducer, in order to realize a high-performance acceleration sensor? Figure 1-2 shows a generic block diagram of the system under study.

The first goal of this research is to design a low noise capacitive sensing circuit that reduces the electronic noise floor to reach the level of Brownian noise. The noise floor of current thin-film capacitive MEMS accelerometers is in the range of 100 - 1000 µg/rtHz, about one order of magnitude higher than the Brownian noise floor, and is dominated by circuit noise. For CMOS MEMS accelerometers, the Brownian noise floor is around 30 µg/rtHz. Decreasing the circuit noise to this level brings the total noise floor below 50 µg/
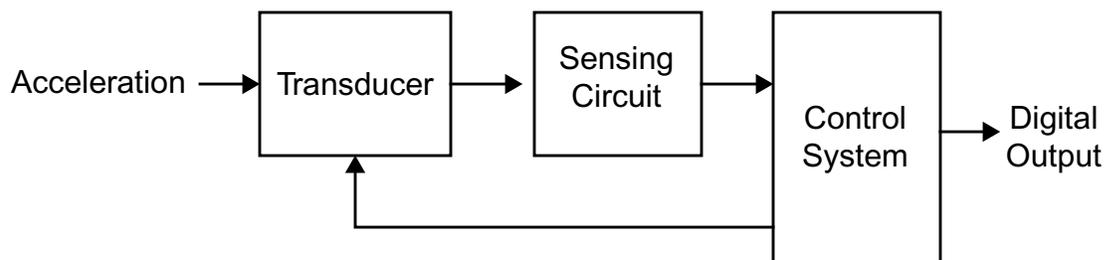
Figure 1-2: Generic block diagram of accelerometer system studied in this work.

rtHz, which is a significant improvement over the state of the art. To achieve this goal, we must first develop a better noise model for fF-range capacitive sensing. Based on this noise model, we will explore low noise circuit architectures and topologies to optimize the noise performance. In addition, other nonidealities, such as offset and charging, need to be suppressed for the sensor to function properly and robustly. In this work, we will demonstrate a CMOS MEMS accelerometer with 50 µg/rtHz noise floor and over 40 dB of offset reduction.

The other major goal of this work is to investigate closed-loop control system architectures for high-performance vacuum-packaged digital-output accelerometers. The feedback control must achieve three objectives: realize high linearity, low variation and good scale factor accuracy; stabilize the high-Q transducer in vacuum; and produce high-resolution digital output. Capacitive sensing is inherently nonlinear. The maximum dynamic range of an open-loop CMOS MEMS accelerometer is about 60 dB. Further improvement of linearity and dynamic range can only be achieved by closed-loop systems. To reduce the Brownian noise of CMOS MEMS accelerometer to µg/rtHz requires the Q of the transducer be greater than 1000. On the other hand, for the sensor to have the best settling behavior, the closed-loop Q of the system should be close to 0.5. Given the large variations of MEMS transducers, it is challenging to apply robust control to stabilize structures of such high Q. Finally, we also want the closed-loop system to function as an analog-to-digital (A/D) converter to provide digital output. In this work, the closed-loop system is expected to achieve 100 dB dynamic range, equivalent to 16 bit resolution. It also must be robust against variations and have low-cost hardware implementation.

The study of closed-loop MEMS systems requires extensive simulations. The multidisciplinary nature of MEMS systems and the complex behaviors of closed-loop systems dictate that behavioral simulation be used. The complexity of simulating a electromechanical feedback loop is often beyond the capability of circuit simulators. Therefore, we have a third goal in this research, that is to develop a behavioral macromodel for the CMOS MEMS accelerometer and to develop efficient behavioral simulation methods and tools for system-level simulations.

This work is based on CMOS MEMS accelerometers. However, the circuit and system techniques developed in this work are not restricted in one device or one process. The CMOS MEMS process has one of the smallest mass and capacitance sensitivity even among surface micromachining processes, therefore, poses a particularly challenging task for electronic subsystem design. The techniques that are proven effective in sensing and control of CMOS MEMS transducers will be valuable for MEMS systems in general. Most bulk and thin-film sensors are currently limited by electronic noise. Many bulk and thin-film devices are vacuum packaged for various reasons, hence, need closed-loop control. And a variety of applications other than inertial measurement require low-noise sensing and robust control of the motion of the micro structures. The ideas and results we present in this dissertation will have general significance in all these areas.

1.3 Previous Work

There are three major capacitive sensing circuit architectures: continuous-time voltage sensing using modulation/demodulation; continuous-time current sensing based on tran-

simpedance amplifier; and switched-capacitor charge sensing. The examples of continuous-time voltage sensing are Draper Lab's bulk vibration sensor reported by Bernstein [19] and Analog Devices' ADXL series polysilicon thin-film accelerometers [6, 31]. Fedder showed a transimpedance amplifier for capacitive sensing [8], however, he concluded that its noise performance is inferior. For this reason, current sensing is not often used in MEMS capacitive sensors. The switched-capacitor readout circuit techniques have been the most widely used approach in the past decade. Switched-capacitor ASICs for bulk accelerometer readout were reported by Smith [11] and Yazdi [15]. Motorola's accelerometer uses a similar approach [33]. Monolithic polysilicon surface micromachined accelerometers with integrated switched-capacitor circuit were reported by Lu [12] and Lemkin [13]. The specifications of these MEMS accelerometers are listed in Table 1-1.

Table 1-1: MEMS Capacitive Accelerometers

	Technology	Sensing method	Control method	Noise floor
Smith 94 [11]	Si-bulk + ASIC	switched capacitor	delta-sigma	1 µg/rtHz
Yazdi 99 [15]	Si-bulk + ASIC	switched capacitor	delta-sigma	3.7 µg/rtHz
Berstein 99 [19]	Si-bulk + ASIC	modulation/voltage	dc balance	1 µg/rtHz
Motorola [33]	Si-bulk + ASIC	switched capacitor	open-loop	2200 µg/rtHz
Lu 95 [12]	poly monolithic	switched capacitor	delta-sigma	1600 µg/rtHz
Lemkin 97 [13]	poly monolithic	switched capacitor	delta-sigma	110 µg/rtHz
ADXL05 [31]	poly monolithic	modulation/voltage	force balance	500 µg/rtHz
ADXL105 [31]	poly monolithic	modulation/voltage	open-loop	225 µg/rtHz

In the above table, the Draper vibration sensor [19] is dominated by Brownian noise, while all the other devices are dominated by electronic noise. Most bulk accelerometers

require a two-chip solution consisting of a sensor chip and a sensing/control ASIC, which is a major disadvantage. Despite large capacitance sensitivity, most bulk accelerometers are still limited by electronic noise. Comparing reference [19] to references [11] and [15], the Draper vibration sensor achieves the same noise floor with much smaller capacitance sensitivity and is the only device on the list that is limited by Brownian noise. This indicates that continuous-time sensing may be advantageous over switched-capacitor readout. In all thin-film accelerometers, the noise floor is above 100 μg/rtHz and dominated by electronic noise. Lemkin's work [13] achieves the lowest noise floor among thin-film devices, and probably the best relative noise performance among all, considering its sensing capacitance is more than 100 times smaller than bulk devices.

Some micro accelerometers listed in Table 1-1 employ closed-loop feedback control. Analog continuous-time force balanced feedback loops is used in ADXL05 where continuous-time sensing is used. The Draper vibration sensor is an ac acceleration sensor. It operates in open-loop in its sensing band but uses dc force feedback (< 2 Hz) to realize adaptive offset cancellation. In references [7 - 15, 34], sampled-data delta-sigma modulation is used in combination with switched-capacitor readout circuits. Delta-sigma modulation has been a focus of MEMS inertial sensor research in recent years because it offers a very attractive feature of direct digitization and can be implemented by simple CMOS switched-capacitor circuits. The combination of switched-capacitor readout and delta-sigma modulation control is widely used in research low-g MEMS accelerometers. A example of this trend is Lemkin's work [13] in which a low-Q underdamped polysilicon thin-film accelerometer is controlled by a second-order delta-sigma loop and produces digital output. The total noise including the quantization noise from A/D conversion is

110 µg/rtHz. However, all these examples of electromechanical delta-sigma modulation are restricted to simple second-order one-bit loops where the transducers are either over-damped or having low Q. It is interesting to notice that most commercial MEMS acceler-ometers are open-loop devices that do not use feedback. Analog Devices has given up force feedback in its recent products such as ADXL105. The closed-loop feedback increases the system complexity, sometimes results in significant increase of system cost. For most commercial MEMS accelerometers with < 80 dB dynamic range, the closed-loop operation is not necessary to achieve such performance.

All capacitive accelerometers in Table 1-1 have mechanical Q smaller than 10. High-Q MEMS transducers are considerably more difficult to control and require very robust control loop. For this reason, to ease the feedback loop design, the MEMS structures are sometimes intentionally overdamped (Q < 0.5) to split two poles in frequency [11]. While high Q being avoided in capacitive sensors, the robust control of high-Q micro structures has been demonstrated in tunneling accelerometers. Tunneling sensing requires the device be vacuum packaged to obtain Q greater than 100, while the tip and the electrode must be kept at a constant distance smaller than 10 Angstrom by a very stiff feedback loop with high loop gain. An advanced robust control technique, µ-synthesis, is used to design the robust controller for a 0.025 µg/rtHz tunneling accelerometer [29, 30, 35].

1.4 Our Approach

In this work, a chopper stabilized voltage readout architecture with noise optimization based on capacitance matching is used for low-noise capacitive sensing. We develop a

noise model showing the input-referred noise of capacitive sensor has strong frequency dependency with both an 1/f term and an $1/f^2$ term while the 1/f corner could exceed 10 MHz. Chopper stabilization is a continuous-time modulation/demodulation scheme that amplifies signal at high frequency where the noise is lower. We will show that continuous-time voltage sensing using chopper stabilization has superior noise performance than switched-capacitor charge sensing and transimpedance amplifier based current sensing and requires smaller circuit bandwidth. However, it was considered less reliable due to the problems of offset and charging. In this work, we use a switching biasing method with periodic reset at sensing nodes to suppress charging and active offset compensation based on differential difference amplifier (DDA), so that robust continuous-time voltage sensing circuit can be realized. Our noise model also shows the noise is dependent on transistor sizes and parasitic capacitance, and indicates there is an optimum transistor size that achieves capacitance matching of the sensor, the sensor/circuit interconnection and the circuit, which minimizes the input-referred noise, or equivalently, maximizes the signal-to-noise ratio (SNR). The front-end circuit is designed based on this noise matching technique.

At the system level, delta-sigma modulation is used to control the motion of the transducer for three reasons: direct digitization capability; better cost and power efficiency in hardware implementation than digital controller; better robustness than continuous-time analog controller. Based on previous work in this area, we extend the study of electromechanical delta-sigma modulation into high-order noise shaping, multi-bit feedback and the control of very high Q (> 1000) micro structures. The robustness of the feedback loop against parameter variations, disturbances and other nonidealities, particularly the position

offset and the undesirable vibration modes, is studied extensively. As multi-bit feedback is necessary to obtain high dynamic range and low proof-mass vibration, highly linear force-balanced feedback using micro electrostatic actuator is critical yet challenging, hence, becomes a focus of this research. A novel digital actuation method called complementary pulse density modulation (CPDM) is proposed and demonstrated to offer > 80 dB linearity and be insensitive to position offset.

The simulation of delta-sigma loops is a known challenging task for circuit simulators. Behavioral macromodels and custom simulator are needed to speed up the simulations. In the behavioral models, a table-based numerical modeling approach with spline interpolation evaluation is used to describe the nonlinearity that is difficult to capture by analytical expressions. The custom simulator employs clock-driven simulation and explicit numerical solver, therefore, is very efficient in simulating sampled-data closed-loop systems.

1.5 Dissertation Organization

This dissertation starts with an introduction of CMOS MEMS accelerometers. The following chapters all surround the two focus areas of this research: low-noise capacitive sensing circuit design and delta-sigma control system design. Each topic occupies two chapters. Our main results: the 50 μg/rtHz accelerometer noise floor by measurement, and 100 dB closed-loop system dynamic range by simulation, are presented in the ends of the discussions. The modeling and simulation techniques are also described along the way.

Chapter 2 gives an introduction to CMOS MEMS surface micromachining and CMOS MEMS accelerometers. The sensor nonidealities are discussed. And a behavioral model of the device is presented in the end.

The following two chapters discuss the low-noise sensing circuit design for fF-range capacitive sensors. In Chapter 3, a circuit noise model is given for capacitive accelerometers which provides insight to noise minimization. The existing sensing circuit architectures are reviewed and analyzed to show the superiority of continuous-time voltage-mode sensing. Other nonidealities, circuit offset, sensor offset and charging, are also discussed. In Chapter 4, the chopper-stabilized sensing amplifier with switching bias and DDA-based offset compensation, is described from architectural level down to detailed circuit design. The experiment results showing 50 μg/rtHz noise floor and >40 dB offset suppression are presented in the end of Chapter 4.

The next two chapters are devoted to the design of force-feedback delta-sigma modulators for robust control and high-resolution A/D conversion. Chapter 5 introduces the basic concepts of force-feedback delta-sigma modulation. The single-loop architecture, the loop filter topology, and its switched-capacitor circuit implementation, are described. Linear multi-bit force feedback using nonlinear micro actuators by complementary pulse density modulation (CPDM) is presented. Chapter 6 starts with a description of the simulation methodology. The simulation results are presented next. These results show the closed-loop system achieves 100 dB dynamic range, near-critical closed-loop damping, < 2 Angstrom proof-mass position error, and very good robustness.

The final chapter, Chapter 7 concludes the dissertation with a summary, suggestions for future work, and an analysis of future directions.

Chapter 2

CMOS MEMS Accelerometers

CMOS MEMS surface micromachining process developed at CMU enables MEMS devices to be fabricated at very low cost, and allows the seamless integration of MEMS sensor/actuators and CMOS analog/digital circuits. On the other hand, the performance of CMOS MEMS devices is severely limited by the low mass, low capacitance sensitivity and large manufacturing imperfections associated with the composite thin-film structures.

This chapter introduces the CMOS MEMS accelerometer, the device that is used in our study of sensing and control electronics. The chapter begins with a description of fabrication process flow and process characteristics in section 2.1. The design and the characteristics of the transducer are presented in sections 2.2 - 2.4. Section 2.5 discusses the behavioral macromodeling of this device for system-level simulations.

2.1 CMU CMOS-MEMS Process

The process flow of CMU CMOS-MEMS process [32, 36] is described in Figure 2-1. The standard CMOS fabrication process is followed by two dry etch steps to release the microstructures. An anisotropic reactive ion etch (RIE) with CHF_3 and O_2 is first performed to etch away SiO_2 that is not covered by any of the metal layers, resulting in vertical sidewalls. This step is followed by an isotropic RIE with SF_6 and O_2 to remove the

underlying silicon, thus releasing the microstructure. The metal layers, usually the top-most metal layer, are used to define the microstructures during the design and to protect the CMOS circuit region during the release. Therefore, no additional mask is required for MEMS fabrication.

The CMOS MEMS micromachining has been developed for Agilent 0.5 µm/0.8 µm, AMS 0.6 µm, TSMC 0.35 µm/0.5 µm and UMC 0.18 µm CMOS processes. The released microstructure consists of multiple layers of metal, SiO_2 and polysilicon. The minimum microstructure feature size is 0.9 µm for Agilent 0.5 µm technology. The thickness of release structures in a 3-metal process is about 5 µm. The released structures are sus-
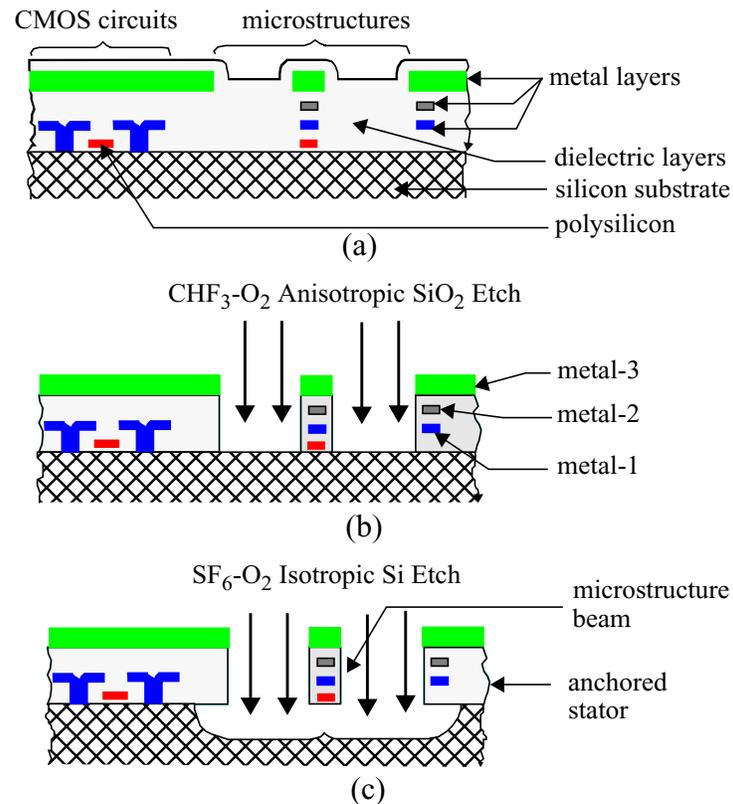
Figure 2-1: Process flow of CMOS MEMS surface micromachining.

pended with a gap of about 20 μm above the silicon substrate. The on-chip CMOS circuits can be integrated as close as 12 μm from the MEMS region, limited by silicon undercut of the isotropic etch. In practice, a conservative approach is to place the circuit about 40 μm from the MEMS region.

The foremost advantage of CMOS MEMS micromachining is the low cost. It does not require additional masks and lithography steps. And the whole process flow is completed by two simple dry etch steps within several hours. Another main advantage of this process is that it offers the tightest integration of MEMS and electronics, therefore allows on-chip signal detection, signal processing and control to be implemented. Complex system-on-chips (SOC) can be fabricated at low cost. The integration enhances the performance and functionality of MEMS systems, and reduces the system cost.

From performance point of view, the CMOS MEMS process provides metal interconnection with significantly lower resistance (0.07 Ω/square for Al) than the polysilicon interconnection used in polysilicon processes (30 Ω/square in reference [9]), thus, greatly reduces the interconnect thermal noise. Because the structures are suspended 20 μm above the substrate, and the circuits can be placed close to the transducers, the parasitic capacitance of the interconnection is also much smaller. This process offers multiple conductive layers which facilitates much more flexible and complex interconnections. This allows novel and complex devices, such as fully differential capacitive sensors, self-actuating springs and gimbaled gyroscopes, to be realized. The complexity of these devices prohibits them to be implemented by homogeneous structures of the polysilicon surface micromachining technology.

However, the thin-film structure of CMOS MEMS technology severely limits the device performance. The microstructures have small mass in the order of 10^{-10} kg, resulting in low sensitivity to outside force, and several orders of magnitude higher Brownian noise than bulk micromachined devices. In the 5 μm thick structures, less than 3 μm are conductive layers, therefore, the devices have low capacitance for sensing and actuation, less than 30 aF/μm for 1.5 μm gap. The total capacitance for a normal size device is less than 100 fF. The actual sensing capacitance is even smaller because 1/3 - 1/2 of the total capacitance is fringe capacitance due the small effective overlap area of the multi-layer capacitor. This leads to the low sensor sensitivity and low actuation force. This situation is further aggravated by the structural curling of the composite thin-film structures. The multi-layer structural material, composed of metal layers with interleaved dielectric layers, exhibits residual stress gradients that induce structural curling [37]. The typical radius of curvature of CMOS MEMS structures is as small as 4 mm, compared to 800 mm of polysilicon surface micromachining structures [10]. This curling limits the maximum proofmass size to be smaller than 400 μm x 400 μm, and maximum beam length to be less than 80 μm, hence, limiting the total available mass and capacitance. The different curvatures in different parts of the devices cause mismatches between electrodes, which further reduces the capacitance and capacitance sensitivity. Finally, the CMOS MEMS structures exhibit large lateral mismatch which causes large variable position offset in differential sensing devices [38]. The current CMOS MEMS devices also have large manufacturing variations among different processing runs, dice and devices.

2.2 CMOS MEMS Accelerometer Design

2.2.1 Sensor Structure

A CMOS MEMS lateral accelerometer is shown in Figure 2-2. This device senses the acceleration in parallel to the substrate surface. A proof-mass with folded-beam suspension is displaced by the acceleration of the substrate. The displacement of the proof-mass is sensed by a capacitive sensor consisting of multiple interdigitated capacitor fingers, and is converted into electrical signal. An electrostatic actuator, which is also formed by interdigitated fingers, is used to apply forces for offset adjustment and force-balanced feedback. On-chip CMOS circuit is integrated under the top-layer metal to detect, amplify and
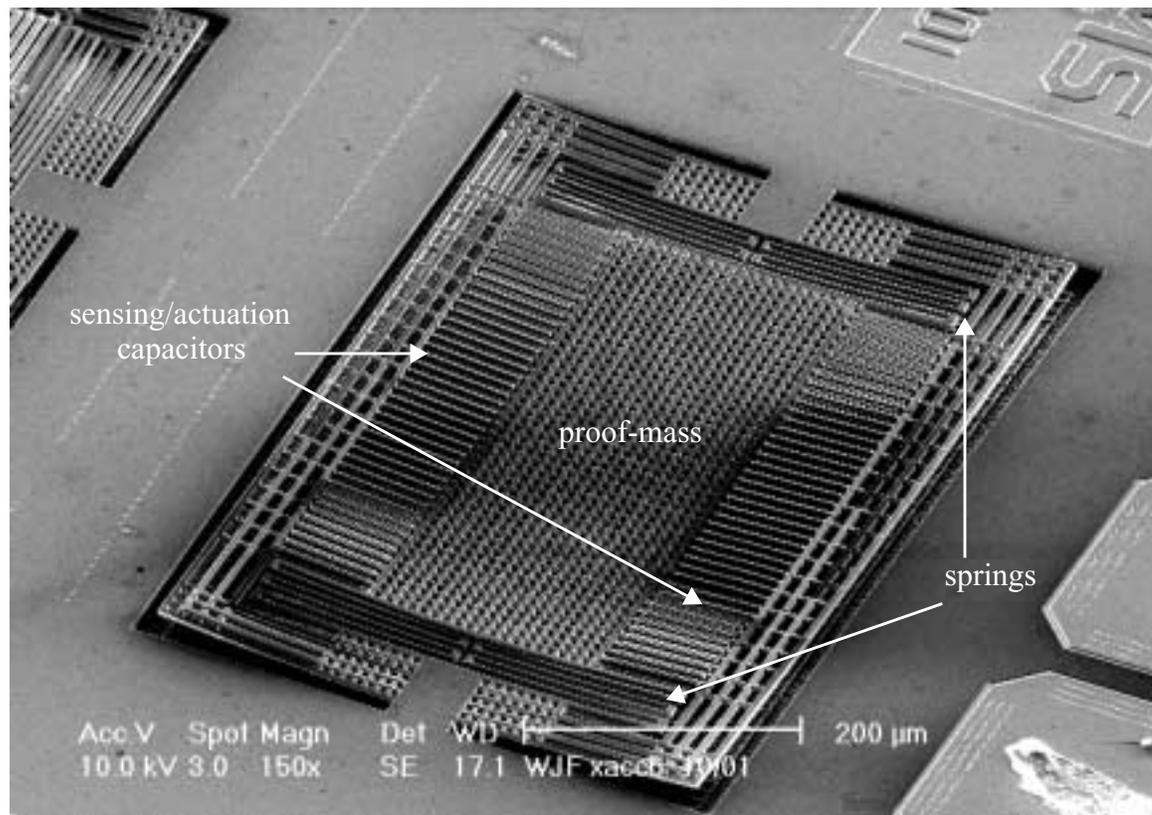
Figure 2-2: Scanning electron micrographs (SEM) of a CMOS MEMS accelerometer.

filter the signals. A detailed view of the multi-layer interdigitated capacitor fingers is pro-

vided in Figure 2-3. The major parameters of this device is listed in Table 2-1.
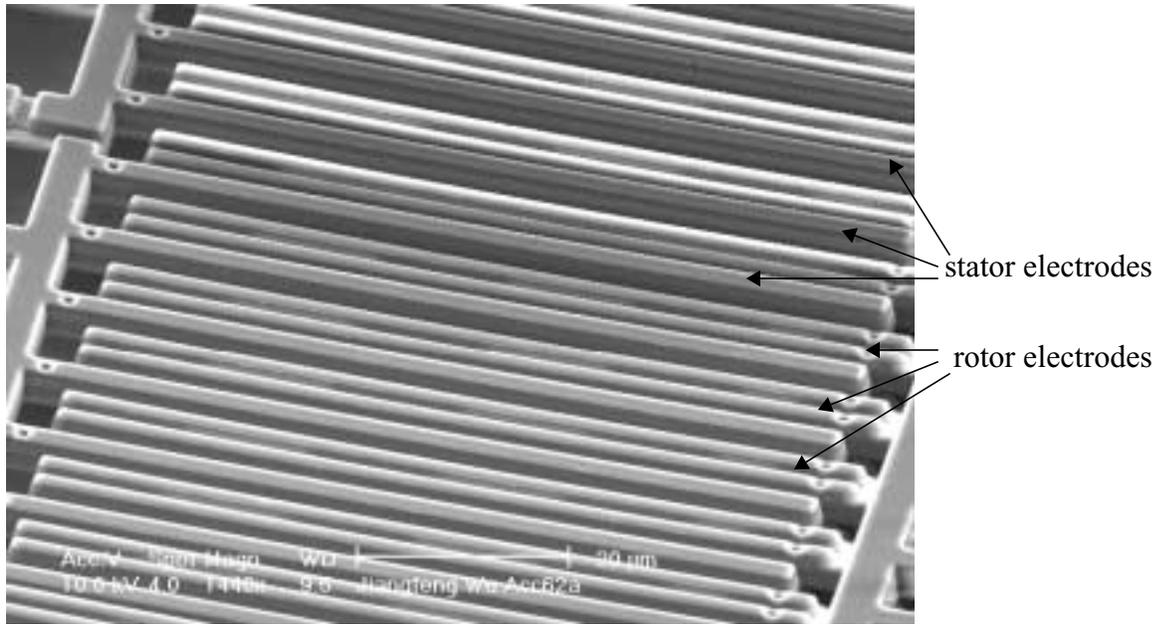
(a)
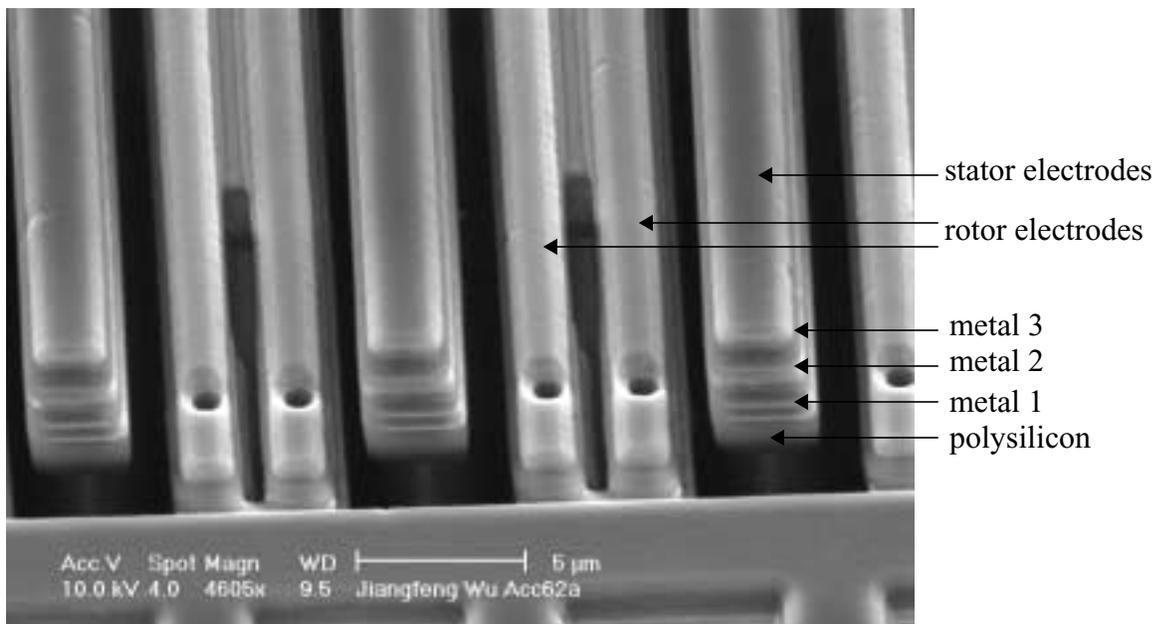
(b)

Figure 2-3: SEM of capacitor fingers for capacitive sensing and electrostatic actuation (a) and the close-up view of the multi-layer capacitor structure (b).

Table 2-1: Parameters of CMOS MEMS accelerometer

Size	600 µm x 450 µm
Proof-mass	0.63 µgram
Spring constant	0.86 N/m
Natural frequency	5.9 KHz
Quality factor (Q)	< 10
Capacitor gap	1.5 µm
Sensing capacitance	< 20 fF x 4
Capacitance sensitivity	< 0.4 fF/g
Interconnect Capacitance	100 fF
Sensitivity	1 mV/g

2.2.2 Structural Curling and Its Compensation

As we stated before, the structural curling is a particularly serious problem for composite CMOS MEMS structures. The radius of the curvature can be as small as 4 mm. The difference in curling of stator and rotor fingers causes mismatch between them, and results in loss of capacitance.

One technique to compensate the structural curling to the first order is to use curling matching frame [10, 22]. As depicted in Figure 2-4, both the suspension springs and the stator fingers are anchored to a rigid frame instead of the substrate. By making the frame, the springs, the proof-mass, the rotor fingers and the stator finger of the same composition of structural layers, the stator and rotor fingers are expected to curl in similar fashions, therefore, the mismatch can be compensated.

Figure 2-4: Curling matching frame.

Figure 2-5 shows the matching between stator and rotor fingers with and without frame matching. Curl matching frame generally improves the capacitance and capacitance sensitivity. However, the results vary with different processing runs and dice.

(a)   (b)
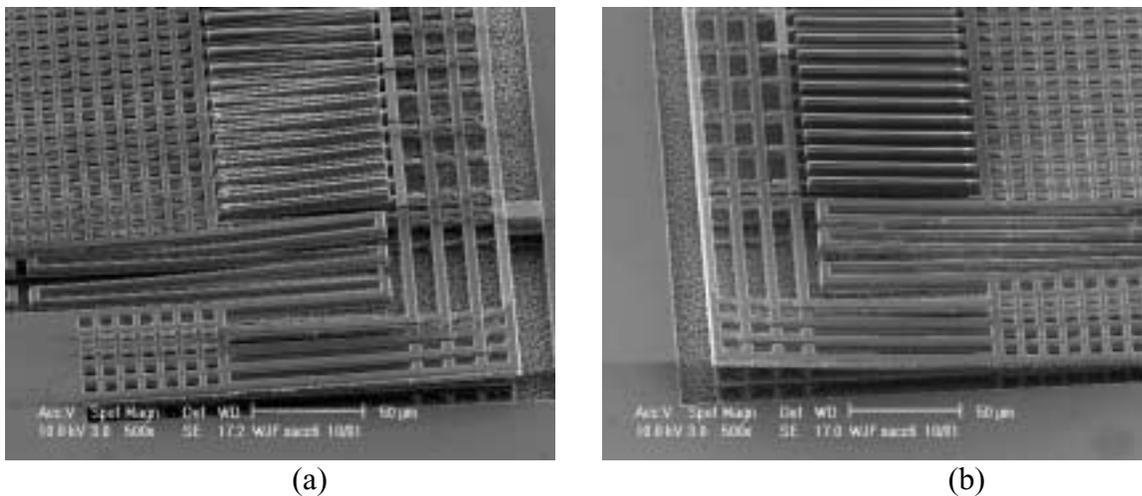
Figure 2-5: Finger mismatches without (a) and with (b) curling matching. frame.

2.3 Mechanical Sensing Element

2.3.1 Mechanical Sensing Principle

Acceleration measurement is achieved by a proof-mass, spring, and damper system made up of microfabricated structures. A lumped-parameter schematic of the system is shown in Figure 2-6.

An accelerometer is a force sensor. The substrate acceleration generates an inertial force on the proof-mass. The inertial force then induces the displacement of the proof-mass. In the operation range of the accelerometer, both the spring elastic force and the viscous damping force are linear with the displacement and the velocity of the proof-mass, respectively. Therefore, the differential equation in the sensing axis is given by:

$$m\ddot{x}(t) + b\dot{x}(t) + kx(t) \ = \ F_{in}(t) \ = \ ma_{in}(t),$$ (2-1)

Defining the natural frequency as:

$$\omega_n \ = \ \sqrt{\frac{k}{m}},$$ (2-2)
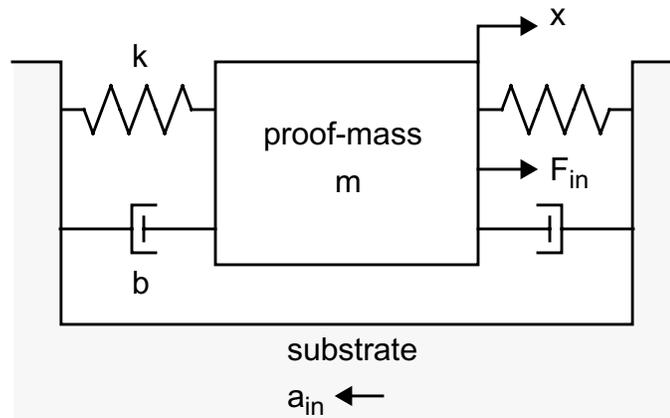
Figure 2-6: Mechanical lumped-parameter schematic of the accelerometer.

and the mechanical quality factor as:

$$Q = \frac{\sqrt{km}}{b},$$ (2-3)

the equation can be rewritten as:

$$\ddot{x}(t) + \frac{\omega_n}{Q}\dot{x}(t) + \omega_n^2 x(t) = F_{in}(t)/m = a_{in}(t).$$ (2-4)

A device is said to be underdamped if Q > 0.5, critically damped if Q = 0.5, and over-damped if Q < 0.5. For a underdamped device with Q > 0.5, the natural frequency is also the resonant frequency of the device. At frequencies much lower than the resonant frequency, the sensitivity of the accelerometer is given by:

$$\frac{x}{a_{in}} = \frac{m}{k} = \frac{1}{\omega_n^2}.$$ (2-5)

By Laplace transformation, the differential equation can be transformed into the s-domain. The transfer function of the accelerometer is:

$$T(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2}.$$ (2-6)

Based on this equation, the frequency responses of the accelerometer under different damping are plotted in Figure 2-7. High-Q MEMS structures exhibit ringing behavior and slow settling under shock. Bulk MEMS sensors are often overdamped to stabilize the proof-mass. However, large damping gives rise to high thermal-mechanical noise, also called Brownian noise, which is intolerable for surface-micromachined sensors. There-fore, thin-film MEMS accelerometers are usually underdamped to reduce the Brownian noise. Most accelerometers sense accelerations at frequency much lower than the resonant frequency. Resonant devices are used in some accelerometers, actuators and gyroscope.
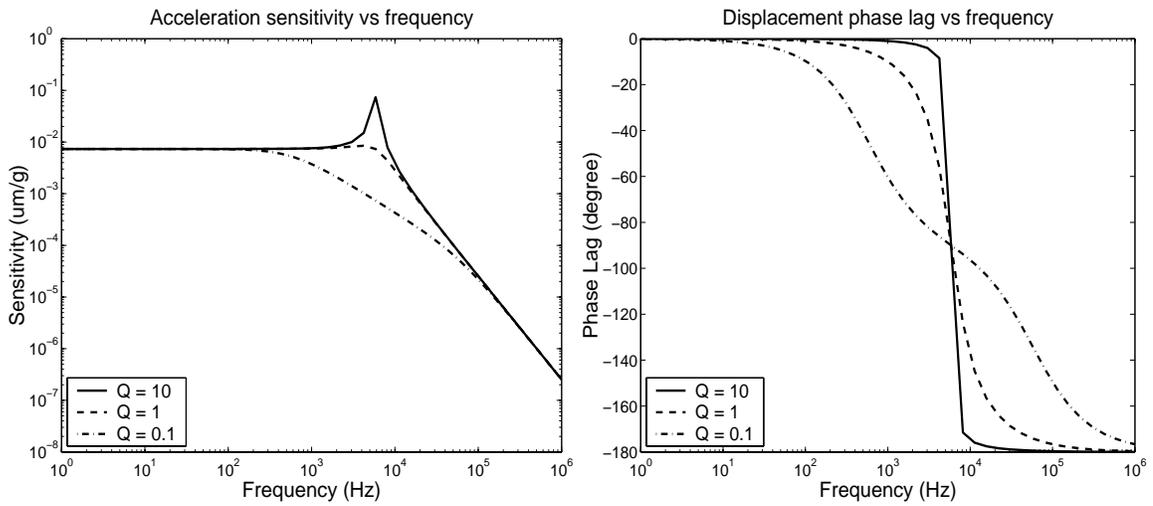
Figure 2-7: Amplitude and phase frequency response of the accelerometer.

2.3.2 Spring Design

Figure 2-8 shows the folded-beam spring used in the accelerometer. The spring constant in the x-axis is given by:

$$k_x = \frac{1}{N} Eh \left(\frac{w}{l} \right)^3, \tag{2-7}$$
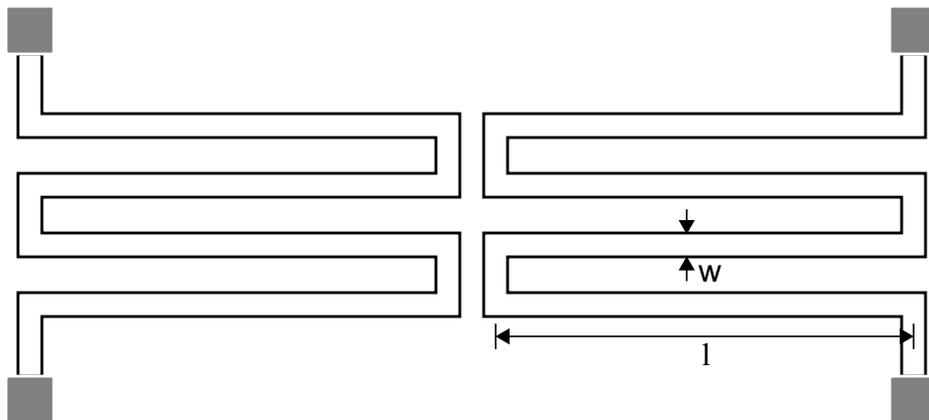
Figure 2-8: Multi-turn folded-beam spring.

where N is number of turns, E is the Young's modulus of elasticity, and l, w, h are the length, width and height (thickness) of the beam respectively. The spring constant in the z-axis is:

$$k_z = \frac{1}{N} Ew\left(\frac{h}{l}\right)^3 . \tag{2-8}$$

The accelerometer has 2-turn folded-beams on both ends. The two springs are in parallel configuration in z-axis. Therefore, the total spring constants are

$$k_x = 2 \cdot \frac{1}{2} \cdot Eh\left(\frac{w}{l}\right)^3 = Eh\left(\frac{w}{l}\right)^3 , \tag{2-9}$$

and

$$k_z = 2 \cdot \frac{1}{2} \cdot Ew\left(\frac{h}{l}\right)^3 = Ew\left(\frac{h}{l}\right)^3 , \tag{2-10}$$

In the accelerometer design, the beam width is 2.1 μm, and the beam height is the thickness of the composite structure, which is about 5 μm. This ensures that the structure has much larger stiffness hence smaller sensitivity in the z-axis than in the sensing axis.
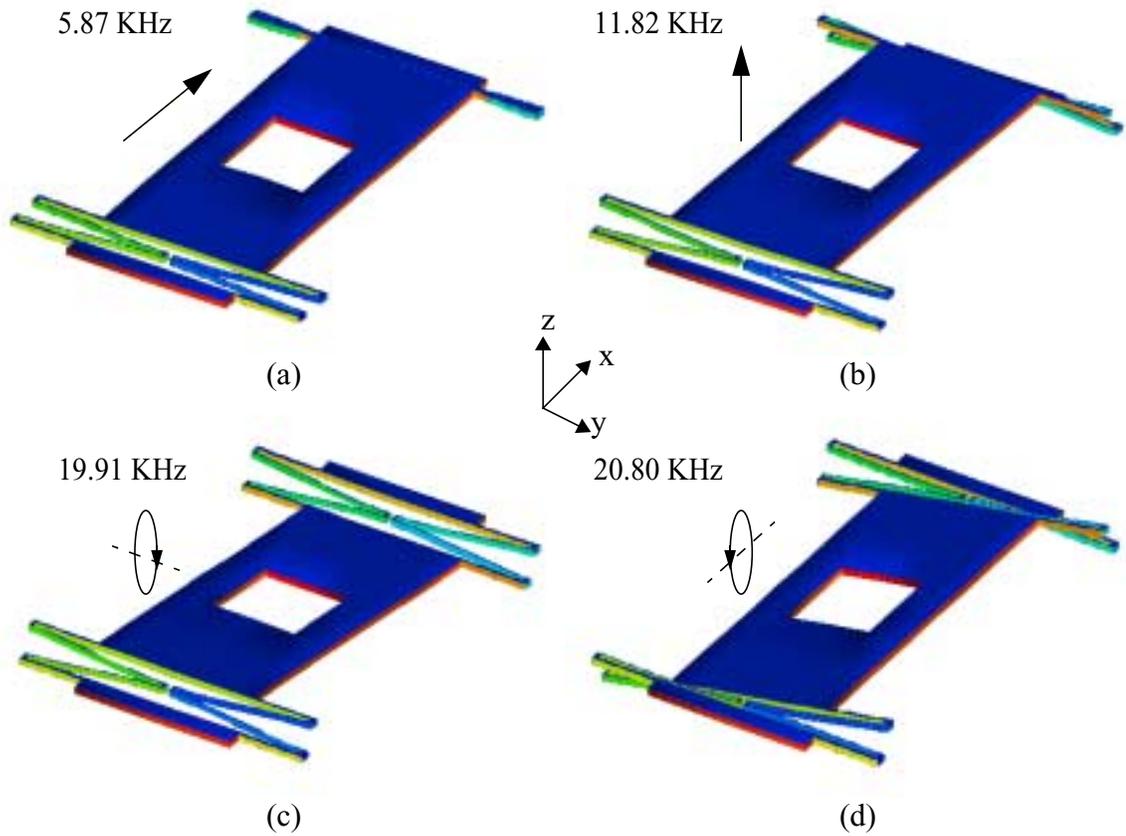
Figure 2-9: Resonant modes of the accelerometer structures (by MEMCAD).
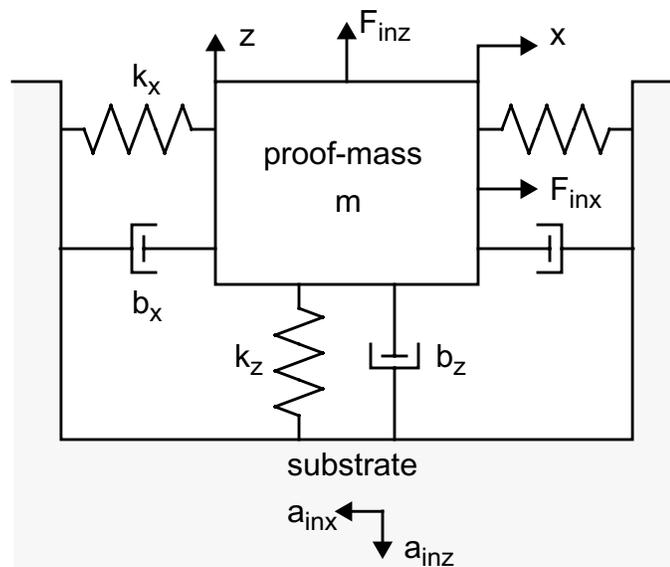
Figure 2-10: Two-axis lumped-parameter schematic of the accelerometer.

The single-axis schematic in Figure 2-6 is an ideal description of the accelerometer. In practice, the structure has other modes of motion, and responds to translational and rotational accelerations in other axes. Figure 2-9 shows the four most important modes with the lowest resonant frequencies. This result is obtained from finite element (FEM) simulations by MEMCAD. The mode in the sensing axis has the lowest resonant frequency, hence the highest sensitivity. The third and the fourth modes are rotational modes. They have lower sensitivities, and the rotational excitations are expected to be at much small scale under normal operating condition. Thus, only the z-axis mode has significant non-ideal effects such as cross-axis sensitivity and sensitivity fluctuation. A more realistic mechanical model of the accelerometer is shown in Figure 2-10.

2.3.3 Damping and Brownian Noise

There are two sources of mechanical damping: the structural damping; and the viscous damping by gas flows. The CMOS MEMS structures are made of Aluminum and SiO_2, both are high-Q materials with very low structural damping. The damping in CMOS MEMS devices is mainly caused by the viscous flow of gas surrounding the micro structures. The dominant damping mechanism in lateral accelerometer is squeeze-film damping between lateral parallel-plate capacitor fingers, which is approximately given by:

$$b \propto \mu_{eff} h \left(\frac{l}{d} \right)^3, \tag{2-11}$$

where l and h are the length and the height (thickness) of the fingers, d is the distance between the fingers, and μ_{eff} is the effective viscosity of the gas. The effective viscosity is dependant of the gas pressure [9]:

$$\mu_{eff} \propto \frac{P}{1 + P/P_0}, \tag{2-12}$$

where P_0 is on the order of 10^2 Torr and smaller than at atmospheric pressure. Experiment data shows that μ_{eff} increases linearly with the pressure between 100 mTorr and 100 Torr. Therefore, the mechanical Q of the structure can be increased by package the device in low-to-medium vacuum. Q value greater than 1000 is observed at pressure lower than 100 mTorr.

A direct consequence of air damping is the thermal-mechanical noise, a random force generated by the Brownian motion of ambient molecules. It is normally called Brownian noise. The power spectral density (PSD) of the Brownian noise force is given by:

$$\overline{F_n^2}(f) = 4kTb. \tag{2-13}$$

For accelerometers, the PSD of the input-referred Brownian noise is:

$$\overline{a_n^2}(f) = \frac{4kTb}{9.8^2 m^2} \qquad g^2/Hz, \tag{2-14}$$

and the input-referred Brownian noise floor is:

$$\sqrt{\overline{a_n^2}(f)} = \frac{\sqrt{4kTb}}{9.8m} \qquad g/\sqrt{Hz}. \tag{2-15}$$

In this CMOS MEMS accelerometer, the Brownian noise floor is about 30 μg/rtHz under normal air pressure. Although the circuit electronic noise is the dominant noise source in most surface micromachined thin-film sensors, we will show in chapter 5, that when the circuit noise is reduced, the Brownian noise could become a major performance limiting factor.

2.4 Capacitive Sensing and Electrostatic Actuation

Interdigitated multi-layer parallel-plate capacitors shown in Figure 2-3 are used in CMOS MEMS devices for both capacitive sensing and electrostatic actuation. The capacitance is extremely small and is difficult to measure directly. Accurate information about CMOS MEMS capacitors is obtained by simulations using 2D electrostatic field solvers. Two field simulators, Raphael and Maxwell, are used to study the multi-layer capacitor structure. The results are shown in Figure 2-11.
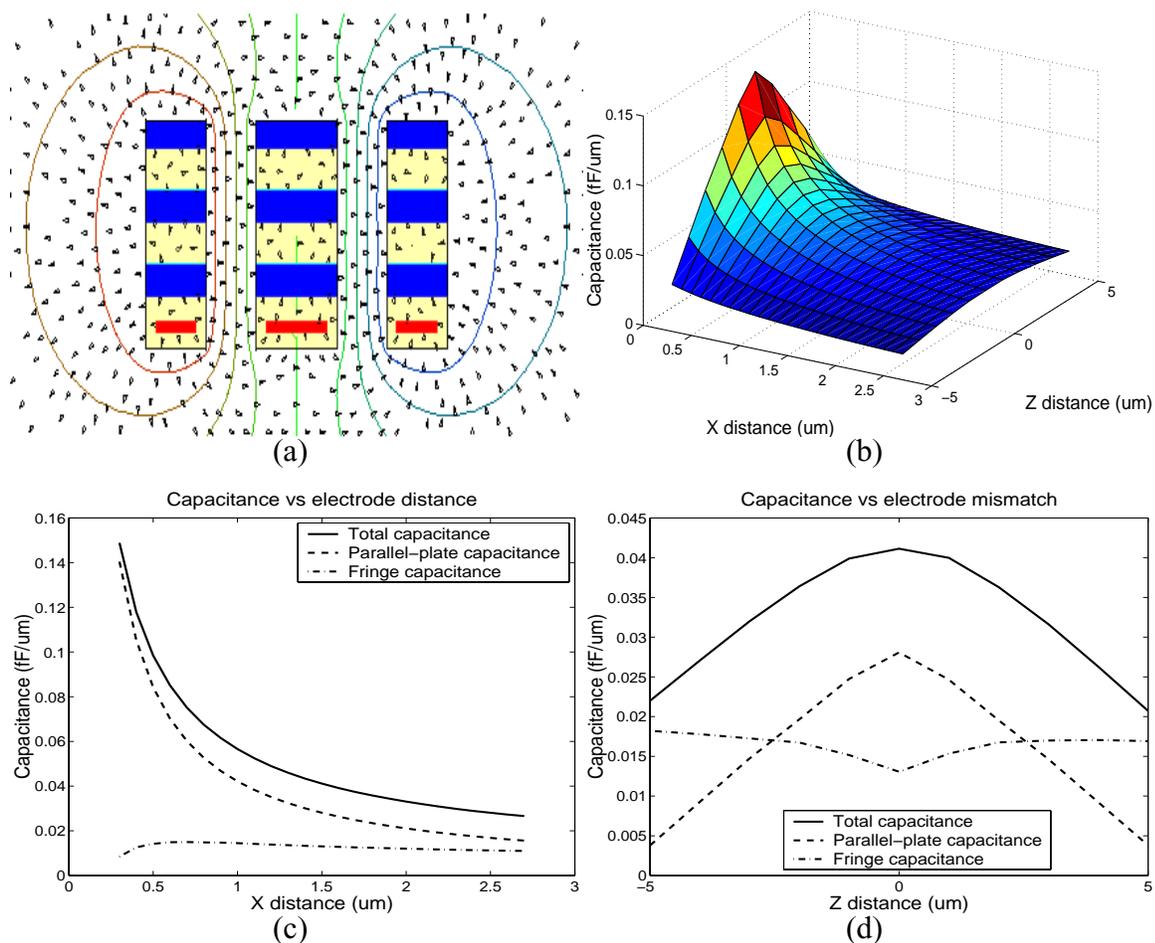
Figure 2-11: CMOS-MEMS multi-layer capacitor: (a) the cross section and the distribution of electrostatic field and potential; (b) the capacitance; (c) the capacitance versus x-axis distance at zero mismatch; (d) the capacitance versus z-axis mismatch at nominal position.

The simulations found a large portion of the total capacitance is from fringe field, as shown in Figure 2-12. The total capacitance can be decomposed into a parallel-plate capacitance term and a fringe capacitance term,

$$C(x,z) = \frac{C_p(z)}{x} + C_f(z),$$ (2-16)

where x and z are distances in the lateral sensing axis and the vertical axis respectively. Only the parallel-plate part is useful as the sensing capacitance, while the fixed fringe part adds to the parasitic capacitance. As shown in Figure 2-12(d), both are highly nonlinear functions of z which are difficult to describe with analytical expressions. This is partly due to the discontinuous nature of the multi-layer structures.

When there is no z-axis mismatch, the sensing capacitance is less than 30 aF/μm and 70% of the total capacitance. As the z-axis mismatch increases, both the value and the percentage of the sensing capacitance decrease. In actual devices, due to the structrural curling, it is not uncommon to observe average z-axis mismatch greater than 2 μm. Based on these results, the total sensing capacitance of a realistic device is estimated between 10 fF and 50 fF, depending on the design and the degree of structural curling. In CMOS-MEMS process, the circuits are usually placed 40 μm away from the sensor to be safe during the MEMS post processing. Therefore, the parasitic capacitance including the interconnect and the fringe capacitor is larger than 100 fF. The gate capacitance of the interface circuit also contributes significant amount of parasitic capacitance.

2.4.1 Capacitive Sensing Principle

In CMOS MEMS accelerometers, capacitive sensing converts the mechanical displacement into electrical signal. When the proof-mass moves in the sensing direction, the gap distances between the rotor and stator fingers change, and the capacitance of the parallel-plate capacitors changes accordingly. In a parallel-plate capacitor, the capacitance sensitivity to distance changes a gap distance x_0 is given by:

$$\frac{dC}{dx}\bigg|_{x=x_0} = \frac{d}{dx}\left(\frac{C_p}{x}\right)\bigg|_{x=x_0} = -\frac{C_p}{x_0^2} = -\frac{C(x_0)}{x_0}. \tag{2-17}$$

The capacitance change induces a charge transfer in the capacitors, which generates an ac voltage or an ac current.
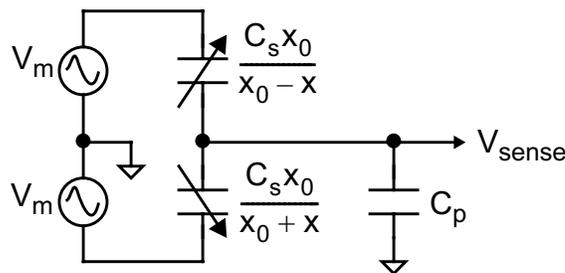
Figure 2-12: Capacitive sensing by a capacitive divider.

The capacitive sensing is based on the principle of the capacitive divider. Figure 2-12 shows a capacitive divider and provides a voltage-domain description of the sensing process. When the proof-mass moves in one direction, the capacitance of one sensing capacitor increases, while the capacitance of the other capacitor decreases. Thus, a voltage proportional to the displacement is generated. The sensitivity is limited by the parasitic capacitance which includes the fringe capacitance, the interconnect capacitance, and the

input capacitance of the interface circuit, for example, the gate capacitance of MOS transistors.

The sensed voltage is given by:

$$
\begin{aligned}
V_{sense} &= \frac{\dfrac{C_s x_0}{x_0 - x} - \dfrac{C_s x_0}{x_0 + x}}{\dfrac{C_s x_0}{x_0 - x} + \dfrac{C_s x_0}{x_0 + x} + C_p} \cdot V_m \\[2em]
&= \frac{2C_s}{2C_s + C_p} \cdot \frac{\dfrac{x}{x_0}}{1 - \dfrac{C_p}{2C_s + C_p}\left(\dfrac{x}{x_0}\right)^2} \cdot V_m
\end{aligned}
\qquad (2\text{-}18)
$$

The sensed voltage can be rewritten as a Taylor series as:

$$
V_{sense} = \frac{2C_s}{2C_s + C_p} V_m \left[\frac{x}{x_0} + \frac{C_p}{2C_s + C_p}\left(\frac{x}{x_0}\right)^3 - \left(\frac{C_p}{2C_s + C_p}\right)^2\left(\frac{x}{x_0}\right)^5 + \dots \right]. \qquad (2\text{-}19)
$$

The existence of the parasitic capacitance gives rise to the nonlinear terms. When the displacement is sufficiently small, as in the case of accelerometers, the above equation can approximated by a linear voltage-displacement relationship:

$$
V_{sense} = \frac{2C_s}{2C_s + C_p} \cdot \frac{x}{x_0} \cdot V_m. \qquad (2\text{-}20)
$$

Because the capacitive sensing is sensitive to electromagnetic interferences (EMI), the CMOS MEMS accelerometer employs a differential capacitive bridge consisting of two differential capacitive dividers to realize fully differential sensing, as shown in Figure 2-13.
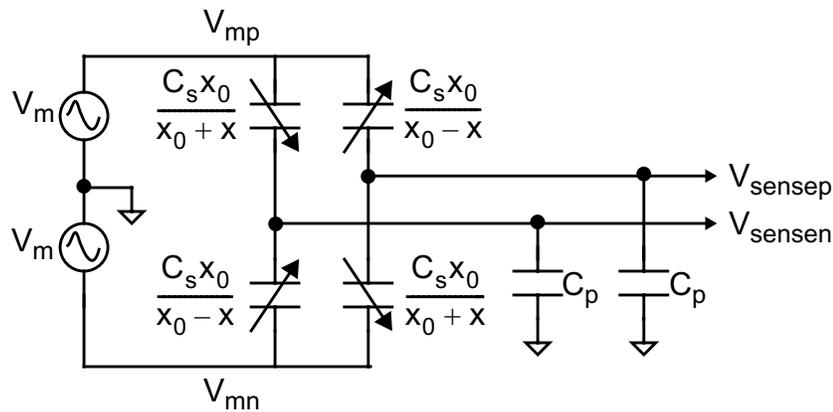
Figure 2-13: Fully differential capacitive sensor.

The fully differential topology significantly improves the interference rejection of the sensor with much higher common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The sensed voltage in a differential sensor can be written as:

$$V_{sense} = V_{sensep} - V_{sensen} = \frac{4C_s}{2C_s + C_p} \cdot \frac{x}{x_0} \cdot V_m. \qquad (2\text{-}21)$$

A common-centroid layout style is employed to compensate cross-axis manufacturing gradients and to achieve better cross-axis rejection [10, 22], as shown in Figure 2-14. However, it shall be noted that neither fully differential sensing nor common-centroid layout is able to compensate the sensor position offset that is caused by manufacturing mismatch in the sensing axis and that appears as a differential signal.
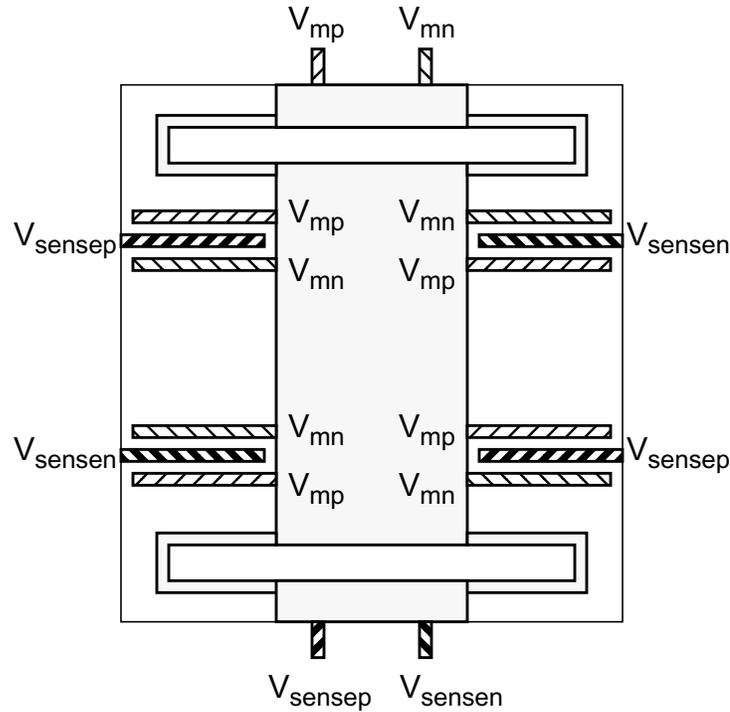
Figure 2-14: Connection schematic of the fully differential capacitive accelerometer.

Since capacitors can only sense ac signals, ac modulation sources are required for capacitive sensing. The sensed signal is an amplitude modulation (AM) signal with the acceleration signal modulated by a high frequency modulation carrier, and must later be demodulated. The sensitivity of the accelerometer is proportional to the amplitude of the modulation carrier, V_m. The V_m amplitude can not arbitrarily large due to sensor offset and electrostatic spring softening effect we will discuss in 4.3. The large position offset also limits the amplitude of V_m.

Combining equations (2-5) and (2-21), the overall sensitivity of the accelerometer is given by:

$$\frac{V_{sense}}{a_{in}} = \frac{4C_s}{2C_s + C_p} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega_n^2}.$$

(2-22)

With a resonant frequency around 6 KHz and V_m of 0.5 V, the accelerometer sensitivity is around 1 mV/g, with large manufacturing variations.

2.4.2 Nonideal Capacitive Sensor

Equation (2-20) - (2-22) give an ideal linear model of the capacitive accelerometer. The actual capacitive accelerometer is a nonlinear device, as shown in (2-19), therefore, the sensitivity varies with the sensor position offset. In addition, the sensing capacitances not only vary with proof-mass position in the sensing axis but also vary with proof-mass position or electrode mismatch in the vertical axis (z-axis).

The nonideal characteristics of the capacitive accelerometer is shown in Figure 2-15. Figure 2-15(a) and (b) show that the relationship between sensor output voltage and proof-mass position is not only nonlinear but also greatly affected by the mismatch is z axis. The sensitivity of the capacitive accelerometer is a function of both sensor position offset and z-axis mismatch. Figure 2-15(c) quantifies the open-loop sensor nonlinearity by total harmonic distortion (THD). It shows that in the best case where there is no position offset, the sensor nonlinearity with respect to 10 g input is a little better than -60 dB, equivalent to 0.1% or 10 bit, and it increases rapidly with the position offset. To achieve scale factor accuracy better than 0.1% and dynamic range better than 10 bit, closed-loop accelerometer with force balanced feedback must be used. The z-axis dependency of the capacitive sensor gives rise to a z-axis motion induced output voltage when the differential sensor is not in perfect balance due to both position offset or input signal. This is called cross-axis sensitivity. It is described in Figure 2-15(d).
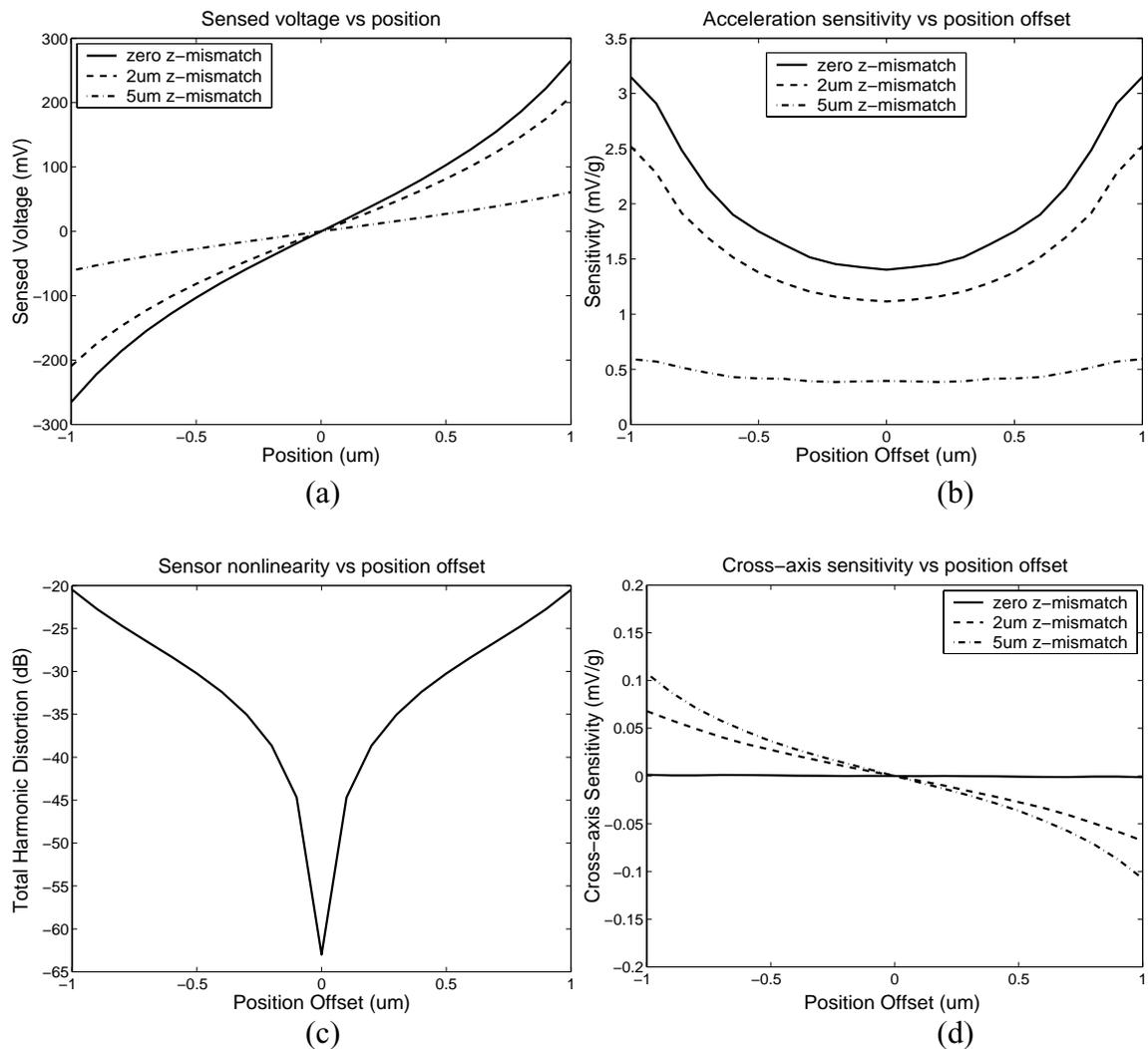
Figure 2-15: Nonideal capacitive accelerometer: (a) sensed voltage versus position with mismatch; (b) sensitivity versus position offset with mismatch; (c) sensor total harmonic distortion versus offset with 10 g input; (d) cross-axis sensitivity versus offset with mismatch.

2.4.3 Electrostatic Actuation

The same capacitor structures are used as electrostatic actuators. Electrostatic actuation has been the major actuation method in CMOS MEMS technology. In accelerometers, it is used to cancel the sensor offset and to realize force-balanced feedback.

When an electrical potential is applied across two plates of a capacitor, an attractive force is generated between the two plates (electrodes). The electrostatic force components in x and z-axis are given by:

$$F_x = \frac{1}{2}\frac{\partial}{\partial x}C(x, z)V^2,$$
(2-23)

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x, z)V^2.$$
(2-24)

For an ideal parallel plate capacitor, the force may be rewritten as:

$$F_x(x) = -\frac{1}{2}\frac{C(x)}{x}V^2.$$
(2-25)

where the negative sign indicates the force is attractive. For nonideal capacitor structures, by performing differentiation on the capacitance data, we can plot the electrostatic forces per square of volt in Figure 2-16. Obviously, the electrostatic actuator is a nonlinear actuator.
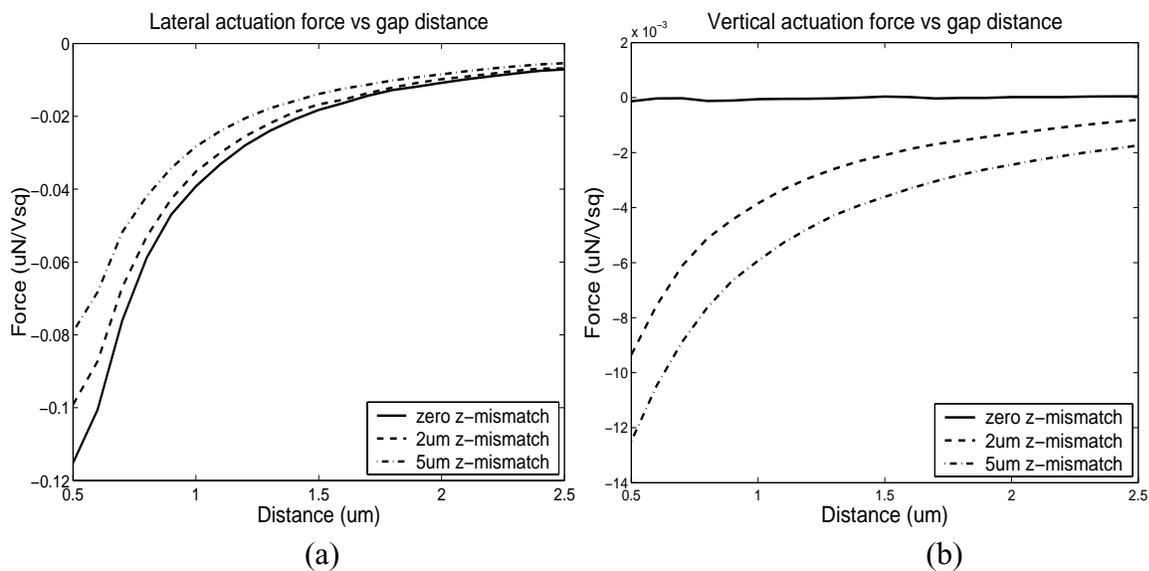
Figure 2-16: Electrostatic forces between two CMOS MEMS beams in lateral (a) and vertical (b) directions.

2.4.4 Electrostatic Spring Forces

Because voltage differences exist between stator and rotor fingers in the capacitive sensor, electrostatic forces are also generated there. The electrostatic forces in the capacitive sensor alters the sensitivity and the resonant frequency of the device. They have similar effects on the device characteristics as the mechanical spring, hence, are referred to as electrostatic spring forces.

In a differential capacitive sensor, the electrostatic spring forces in the lateral sensing axis (x axis) and the vertical axis (z axis) are given by:

$$F_{ex} = \frac{1}{2}\frac{\partial}{\partial x}C_{sp}(x, z)(V_m - V_{sense})^2 - \frac{1}{2}\frac{\partial}{\partial x}C_{sn}(x, z)(V_m + V_{sense})^2, \tag{2-26}$$

$$F_{ez} = \frac{1}{2}\frac{\partial}{\partial z}C_{sp}(x, z)(V_m - V_{sense})^2 + \frac{1}{2}\frac{\partial}{\partial z}C_{sn}(x, z)(V_m + V_{sense})^2. \tag{2-27}$$

The electrostatic spring force in the sensing axis has a positive sign, hence, having a destabilizing effect on the proof-mass. As the proof-mass move in one direction, this force tends to push the proof-mass further into this direction, thus, acting as a negative spring. This effect is called electrostatic spring softening. When the capacitive divider is in balance position, the effective electrical spring constant is given by:

$$k_e = -\frac{dF_{ex}}{dx} = -2\frac{C_{s0}}{x_0^2}V_m^2. \tag{2-28}$$

This effect is important in device design because it not only reduces the resonant frequency but also may potentially destabilize the device when the voltage across sensor plates is too large by causing the device to snap into one side. The total spring constant

must remain positive in order for the device to be stable. The largest modulation signal amplitude allowable is found to be:

$$V_{mmax} = \sqrt{\frac{kx_0^2}{2C_{s0}}}. \tag{2-29}$$

In reality, when the capacitive divider is not perfectly balanced, the electrostatic spring softening effect increases with the position offset. Therefore, design headroom is needed for adequate stability margin. The force in z-axis has a negative sign and causes a spring hardening effect. In general, the electrostatic spring forces should be minimized in accelerometer design, albeit they can be useful in applications such as resonant frequency tuning.

2.5 Macromodeling of CMOS MEMS Accelerometers

The accelerometer operates in multiple physical domains, primarily in mechanical domain and electrostatic domain. The thermal effect also has great undesirable impacts on the device [37, 38]. A physical model of the accelerometer is represented by a group of partial differential equations (PDE). Multi-domain dynamic simulations by numerically solving multiple PDEs with different characteristics are extremely computational intensive, and in many cases, impossible.

As MEMS technology enables the integration of sensing, actuation, signal processing and control, MEMS devices are often need to be studied in complex systems. This requires behavior-level macromodels with lumped parameters. A macromodel is represented by a group of coupled ordinary differential equations (ODE). Numerical solution of ODEs demands much less computation than solving PDEs. The PDEs are reduced to ODEs by

separating the spatial variables from the temporal variables, eliminating the spatial vari-

ables from the differential equations, and reducing the order by removing insignificant

modes.

The following simplifications are made to obtain the lumped-parameter macromodel

of the CMOS MEMS accelerometer: the proof-mass is treated as a solid body; the spring

stiffness and the damping are assumed to be linear; and only two modes in the sensing x

axis and the vertical z axis are included. With these treatments, this macromodel provides

a reasonably accurate behavior-level description of the device, in which major nonlineari-

ties and nonidealities are properly represented, including: the nonlinearity of the capaci-

tive sensor; the nonlinearity of the electrostatic actuator; the electrostatic spring forces; the

effect of parasitic capacitance; and the cross-axis sensitivity.

2.5.1 Model Equations

The equations of the models are:

$$m_x \ddot{x}(t) + b_x \dot{x}(t) + k_x x(t) = F_{inx}(t), \tag{2-30}$$

$$m_z \ddot{z}(t) + b_z \dot{z}(t) + k_z z(t) = F_{inz}(t), \tag{2-31}$$

$$F_{inx}(t) = m_x a_{inx}(t) + F_{espx}(x, z) + e_x(d - x, z)V_p^2 - e_x(d + x, z)V_n^2, \tag{2-32}$$

$$F_{inz}(t) = m_z a_{inz}(t) + F_{espz}(x, z) + e_z(d - x, z)V_p^2 + e_z(d + x, z)V_n^2, \tag{2-33}$$

$$V_{sense}(t) = S(x, z). \tag{2-34}$$

Equations (2-30) and (2-31) describe the motions in the sensing x axis and the vertical z

axis. Equations (2-32) and (2-33) give the total external forces, including the inertial

forces induced by substrate accelerations, the electrostatic actuation forces and electro-

static spring forces in x axis and z axis. Equation (2-34) gives the sensor output voltage in response to displacements in both x and z axes. The block diagram of this two-dimensional nonlinear macromodel is given in Figure 2-17.
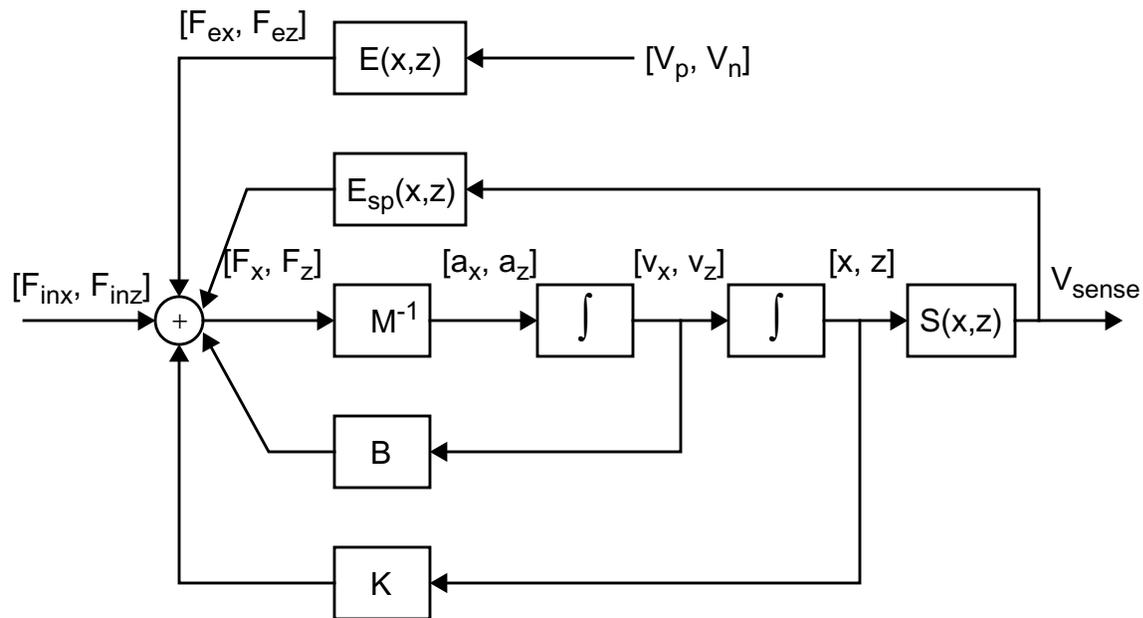
Figure 2-17: Behavioral macromodel of the accelerometer.

2.5.2 Table-Based Nonlinearity Modeling

The CMOS MEMS capacitor and the electrostatic force are both inherently nonlinear. Due to the discontinuity of the multi-layer structure, the nonlinearities in the fringe capacitance and the z-axis capacitance variation are difficult to describe by analytical functions. Therefore, we use a table-based numerical modeling approach to represent the capacitive sensor, the electrostatic actuator, and the electrostatic spring forces. This approach is depicted in Figure 2-18.
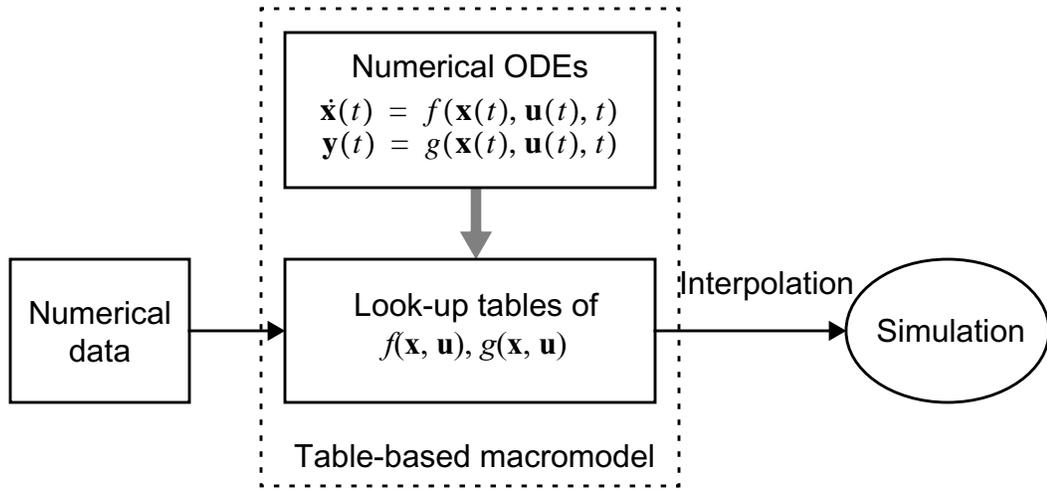
Figure 2-18: Generation and evaluation of table-based behavioral models.

A detailed analysis on capacitance and electrostatic forces is given in section 2.4. These data are organized into two dimensional tables with displacements in x and z axes as the references. In system-level simulations, the table-based model functions are evaluated by two-variable cubic spline interpolation. For simplicity, let us consider an one-dimensional cubic spline interpolation problem. The function value y at variable value x between x_i and x_{i+1} is computed by a cubic polynomial:

$$y = ay_i + by_{i+1} + cy''_i + dy''_{i+1}, \tag{2-35}$$

$$a = \frac{x_{i+1} - x}{x_{i+1} - x_i}, \tag{2-36}$$

$$b = \frac{x - x_i}{x_{i+1} - x_i}, \tag{2-37}$$

$$c = \frac{1}{6}(a^3 - a)(x_{i+1} - x_i)^2, \tag{2-38}$$

$$d = \frac{1}{6}(b^3 - b)(x_{i+1} - x_i)^2. \tag{2-39}$$

The cubic spline interpolation has good smoothness and stability, as demonstrated in Figure 2- 19, and requires simple computation. The equations show that it requires tables of second derivatives to be established in prior, but the computational overhead of building such tables is insignificant compared to the simulations. In simulations, since most functions change continuously, it takes little effort to locate the interpolation interval because consecutive data points usually fall into the same or the neighboring intervals. Therefore, although this numerical modeling method provides no insight to device design, it is very efficient in system-level simulations.
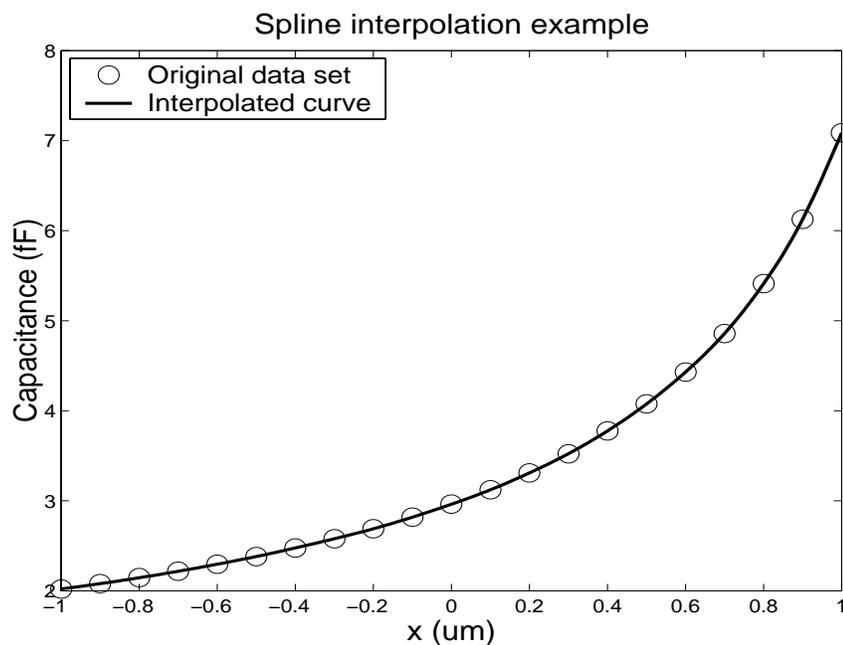
Figure 2-19: Cubic spline interpolation in one dimension.

2.6 Summary

In this chapter, we described the design, fabrication and modeling of the CMOS MEMS accelerometer. Several limitations of this device motivate the research work we will present in the rest of this dissertation. First, it is a low-sensitivity device with less then 20 fF x 4 total sensing capacitance, 0.4 fF/g capacitance change, and 1 mV/g overall sensitivity, therefore, optimization of noise is critical to obtain good resolution and dynamic range. Second, lateral position offset and vertical position mismatch have great impacts on the sensor, as the result, the device could have an offset more than 40 dB larger than the sensed signal. Third, the accelerometer is a nonlinear device with open-loop dynamic range no more than 60 dB, or scale factor accuracy worse than 0.1%, hence, it is necessary to use closed-loop feedback to achieve better performance. Finally, the large manufacturing and temperature variations of MEMS fabrication must be addressed in robust sensor system design.

Chapter 3

Noise, Offset and Charging in Capacitive Sensing

Because of the thin-film structure and the structural curling, the CMOS MEMS accelerometer has less than 20 fF x 4 total sensing capacitance, 0.4 fF/g motion-induced capacitance change, and 1 mV/g overall sensitivity. Consequently, a number of nonidealities become more critical issues than in capacitive sensors with larger capacitance sensitivity. These nonidealities not only degrade the performance of the sensor system, some of them also greatly affect the reliability, and even cause catastrophic device failure. The main nonidealities in fF-range capacitive sensors besides Brownian noise are: electronic noise; circuit offset; sensor offset; and undesirable charging activities. A successful design of electronic subsystem requires a careful consideration of all these factors. This chapter presents a complete analysis of these nonidealities, which provides guidance to interface circuit design. A review of capacitive sensor readout circuit architectures is also provided.

3.1 Electronic Noise

The electronic noise is the dominant noise source in most surface micromachined inertial sensors. The noise performance of accelerometers is measured by input-referred noise floor in g/rtHz. The input-referred noise floor determines the resolution of the sensor, and represents the signal-to-noise ratio (SNR). The input-referred electronic noise is deter-

mined by both the sensitivity of the sensor and the absolute amount of noise generated in the circuit.

The CMOS MEMS capacitive sensors have ultra small sensing capacitance, hence, have very high impedance, according to the following relationship:

$$Z = \frac{1}{2\pi f C}.$$

(3-1)

With most systems operating at modulation frequency between 100 KHz and 10 MHz, the impedance of CMOS MEMS capacitive sensor is in the range of 10^6 - 10^8 Ω. To avoid substantial attenuation of the signal, the interface circuit must have comparably high input impedance, which excludes bipolar junction transistors (BJT) to be used. Field effect transistors (FET), such as MOSFETs, should be used in capacitive sensing for thin-film MEMS devices.

In CMOS circuits, the flicker (1/f) noise and the thermal noise are two main noise sources. Because the signal is modulated at 100 KHz - 10 MHz, it was often assumed that the thermal noise is the dominant circuit noise. However, estimation based on this assumption yields a noise floor up to more than one order of magnitude lower than the actual measurement results. In this section, we provide a more accurate noise model for capacitive sensing circuit design, which is validated by experimental results presented in the next chapter.

3.1.1 Noise Sources

Figure 3-1 is a generic schematic of capacitive sensing showing all noise sources and parasitic devices. The sensitivity of a capacitive accelerometer is given by

$$V_{sense} = \frac{2C_s}{2C_s + C_p} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega_n^2}. \tag{3-2}$$

Regardless of the input biasing methods, the reverse-biased diode exists at the sensing node in most cases, either being placed intentionally as the bias device, or as a parasitic PN junction in the bias device, such as a turned-off MOS switch, or a subthreshold MOS-FET. Electronic noise comes from the following five sources: the thermal noise of the input MOSFET, the 1/f noise of the input MOSFET, the shot noise of the diode leakage, the noise from the modulation signal, and the noise from other parts of the circuit. In a differential topology, the modulation noise enters the two differential inputs equally, thus being cancelled. By designing the circuit properly, the noise contributions by the load and the following stages can be minimized so that the total noise will be dominated by the input device. Therefore, the last two sources are neglected in the following discussions.
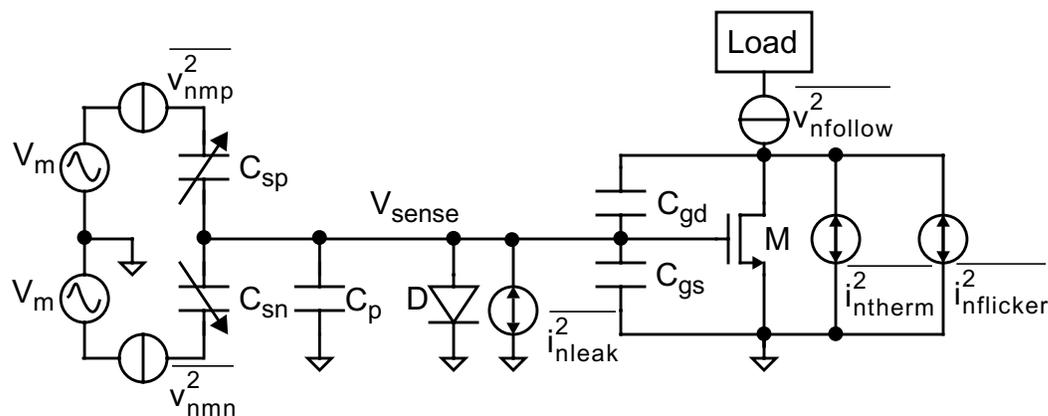
Figure 3-1: Noise sources and parasitic devices in capacitive sensing.

Under long channel approximation, the power spectral densities (PSD) of the thermal, the 1/f and the shot noise current are given by [39, 40, 41]:

$$\overline{i^2_{ntherm}}(f) \;=\; 4\gamma kT g_m \;=\; 4\gamma kT \sqrt{2\mu_n C_{ox}(W/L)I_D}, \tag{3-3}$$

$$\overline{i^2_{nflicker}}(f) \;=\; \frac{K_f I_D}{C_{ox} L^2 f}, \tag{3-4}$$

and

$$\overline{i^2_{nleak}}(f) \;=\; 2q I_{leak}, \tag{3-5}$$

where W and L are the channel width and length of the MOSFET, g_m is the transconductance of the MOSFET, I_D is the bias current of the MOSFET, k the Boltzmann's constant, T is the temperature in Kelvins, μ_n is the carrier mobility, C_{ox} is the gate capacitance per unit area, K_f is the flicker noise coefficient, q is the electron charge, I_{leak} is the leakage current of the diode, and f is the frequency at which the circuit is operated. The MOSFET thermal noise coefficient γ is 2/3 for long channel transistors and can be as large as 2 - 3 for short channel transistors.

3.1.2 Input-Referred Noise Floor

The sensing capacitance of CMOS-MEMS accelerometers is estimated to be less than 20 fF. Since capacitive sensors detect signals using capacitive dividers, the parasitic capacitance is a very important factor in determining the sensitivity. Because the noise performance, measured either by the signal-to-noise ratio (SNR) or by the input referred noise floor, is a function of the sensitivity, the parasitic capacitance also has a great impact on noise and resolution. In CMOS MEMS technology, as the interconnect capacitance is rela-

tively small than polysilicon and other surface micromachining processes, the gate-to-source and gate-to-drain capacitance are important components of the total parasitic capacitance. For the sensor to have reasonable sensitivity, the size of the input MOSFET must be kept small. On the other hand, the thermal noise and the 1/f noise of the MOSFET at the sensing node are inversely proportional to the channel width and the channel area, respectively:

$$\overline{v_{ntherm}^2}(f) = \overline{i_{ntherm}^2}/g_m^2 = \frac{4\gamma kT}{g_m} = \frac{4\gamma kT}{\sqrt{2\mu_n C_{ox}(W/L)I_D}}, \tag{3-6}$$

$$\overline{v_{nflicker}^2}(f) = \overline{i_{nflicker}^2}/g_m^2 = \frac{K_f}{2\mu_n C_{ox}^2 WLf}. \tag{3-7}$$

Long channel approximation is used in the expression of thermal noise (3-6). For small MOS devices, the 1/f noise dominates in a wide frequency range. In fact, the 1/f noise corner could extend beyond 10 MHz for typical transistor sizes used in CMOS MEMS capacitive sensors.

The shot noise current is proportional to the leakage current. The leakage current is usually smaller than 1 pA and can be ignored in most cases. However, because surface micromachined devices have very small capacitance, the effects of the leakage shot noise become much more significant. The noise voltage at the input node due to leakage shot noise is given by:

$$\overline{v_{nleak}^2}(f) = \frac{\overline{i_{nleak}^2}}{(2\pi C_{total}f)^2} = \frac{qI_{leak}}{2\pi^2 C_{total}^2 f^2}. \tag{3-8}$$

This noise is strongly dependent on the frequency. It dominates at the very low frequency, and determines how low the modulation frequency can be.

The total voltage noise PSD at the sensing node is given by:

$$
\begin{aligned}
\overline{v_n^2}(f) &= \overline{v_{ntherm}^2}(f) + \overline{v_{nflicker}^2}(f) + \overline{v_{nleak}^2}(f) \\
&= \frac{4\gamma kT}{\sqrt{2\mu_n C_{ox} I_D (W/L)}} + \frac{K_f}{2\mu_n C_{ox}^2 WLf} + \frac{qI_{leak}}{2\pi^2 C_{total}^2 f^2}
\end{aligned}
\quad (3\text{-}9)
$$

Thus, according to equation (3-2), the PSD of the total input referred noise for an acceler-

ometer is

$$
\begin{aligned}
\overline{a_n^2}(f) &= \overline{a_{ntherm}^2}(f) + \overline{a_{nflicker}^2}(f) + \overline{a_{nleak}^2}(f) \\
&= \frac{\omega_n^4 x_0^2 \gamma kT (2C_s + C_p + C_{gs} + C_{gd})^2}{C_s^2 V_m^2 \sqrt{2\mu_n C_{ox} I_D (W/L)}} + \\
&\quad \frac{\omega_n^4 x_0^2 K_f (2C_s + C_p + C_{gs} + C_{gd})^2}{8C_s^2 V_m^2 \mu_n C_{ox}^2 WLf} + \frac{\omega_n^4 x_0^2 qI_{leak}}{8\pi^2 C_s^2 V_m^2 f^2}
\end{aligned}
\quad , \quad (3\text{-}10)
$$

where C_s is the sensing capacitance, C_p is the combination of the interconnect capacitance

and the fringe capacitance, x_0 is the nominal gap between electrodes, and w_n is mechanical

resonant frequency of the accelerometer. The gate capacitances of the MOSFET are deter-

mined by the area of the channel,

$$
C_{gs} = \frac{2}{3} C_{ox} WL + C_{ox} WL_{ov},
\quad (3\text{-}11)
$$

and

$$
C_{gd} = C_{ox} WL_{ov}.
\quad (3\text{-}12)
$$

And the input-referred noise floor is given by:

$$\sqrt{\overline{a_n^2}(f)} = \sqrt{\frac{\omega_n^4 x_0^2 \gamma kT (2C_s + C_p + C_{gs} + C_{gd})^2}{C_s^2 V_m^2 \sqrt{2\mu_n C_{ox} I_D (W/L)}} + \frac{\omega_n^4 x_0^2 K_f (2C_s + C_p + C_{gs} + C_{gd})^2}{8C_s^2 V_m^2 \mu_n C_{ox}^2 WLf} + \frac{\omega_n^4 x_0^2 q I_{leak}}{8\pi^2 C_s^2 V_m^2 f^2}} \quad g/\sqrt{Hz}. \quad (3\text{-}13)$$

In the above derivation, velocity saturation effect of short-channel devices is ignored in thermal noise model. The MOS transistor with carrier velocity saturation is characterized by following equations [40, 41, 42]:

$$I_D = \frac{\mu_n C_{ox}}{2[1 + (V_{gs} - V_{th})/(LE_c)]} \frac{W}{L} (V_{gs} - V_{th})^2, \quad (3\text{-}14)$$

$$g_m = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \cdot \frac{V_{gs} - V_{th}}{1 + (V_{gs} - V_{th})/(LE_c)} \cdot \frac{2 + (V_{gs} - V_{th})/(LE_c)}{1 + (V_{gs} - V_{th})/(LE_c)}, \quad (3\text{-}15)$$

where E_c is the critical electric field. The transconductance of actual short-channel devices is lower than predicted by long-channel approximation. In deep velocity saturation region, equation (3-15) becomes:

$$g_{msat} = \mu_n C_{ox} WE_c, \quad (3\text{-}16)$$

the transconductance reaches a saturated value and can no longer be increased by increasing bias current or bias voltage. The thermal noise of the velocity saturated transistor is given by [42]:

$$\overline{v_{ntherm}^2}(f) = \frac{4\gamma kT g_{d0}}{g_m^2} = \frac{4\gamma kT}{\alpha g_m}, \quad (3\text{-}17)$$

α is a parameter smaller than 1 for short channel devices and is dependent on transistor size and bias condition. Compared to long channel approximation, the thermal noise is larger, has stronger dependency on channel width W, and weaker dependency on channel

length L. For both long and short channel input MOS transistors, the accelerometer input-referred electronic noise can be expressed as:

$$\sqrt{\overline{a_n^2(f)}} = \sqrt{\frac{K_T T (1 + c_1 W + c_2 WL)^2}{W^\beta L^{\beta-1}} + \frac{K_F (1 + c_1 W + c_2 WL)^2}{WLf} + \frac{K_L I_{leak}}{f^2}}, \quad (3\text{-}18)$$

where K_T, K_F and K_L are the lumped coefficients for the three noise components, c_1 and c_2 are given by:

$$c_1 = \frac{2 C_{ox} L_{ov}}{2 C_s + C_p}, \quad (3\text{-}19)$$

and

$$c_2 = \frac{2 C_{ox}}{3 (2 C_s + C_p)}. \quad (3\text{-}20)$$
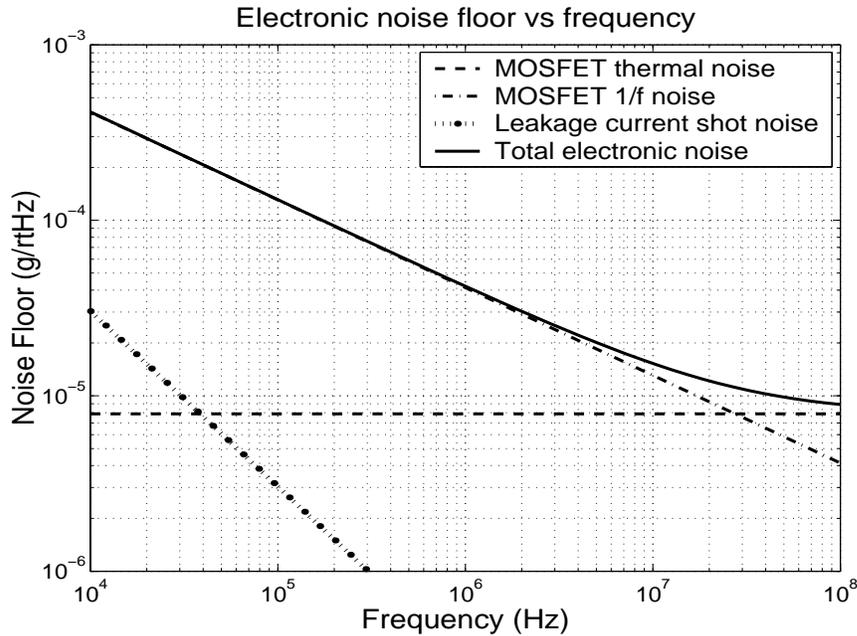
Figure 3-2: Input-referred electronic noise floor and its three components versus frequency.

β is 0.5 without velocity saturation, and increases to 1 for devices in deep velocity satura-

tion region. The input-referred electronic noise and its three components are plotted in

Figure 3-2 versus frequency.

In addition, if the voltage gain across the input MOSFET is *A*, the transducer gain is

given by:

$$G = \frac{2C_s V_m A}{\omega_n^2 x_0 [2C_s + C_p + C_{gs} + (1 + A)C_{gd}]} . \tag{3-21}$$

The Miller effect of the feedback capacitor C_{gd} is reflected in the denominator.

3.1.3 Noise Optimization with 1/f Noise

According to equation (3-18), if all other parameters are given, there is an optimum

input MOS transistor size that minimizes the input-referred noise floor at each frequency.

Similarly based on (3-19), there is also an optimum input transistor voltage gain that max-

imizes the overall transducer gain. The noise and gain usually cannot be optimized simul-

taneously. This is similar to the noise matching and power matching in RF front-end

circuits. Unlike in RF design though, the circuits following the capacitive sensing front-

end can easily achieve much lower noise due to low operating frequency. Thus, the gain

optimization is not necessary and the front-end circuit should be designed based on the

noise optimization.

In conventional low noise circuit design, large transistors are always used because the

transistor thermal noise and 1/f noise decrease with channel width and channel area

respectively. This is not the case in capacitive sensing. When the channel width and chan-

nel area of the MOSFET are made larger, the absolute values of both the thermal noise and

the 1/f noise become smaller. However at the same time, the gate capacitances also

increase which reduces the sensitivity of the capacitive sensor based on equation (3-2). At

any given frequency and channel length, the minimum noise floor, or the maximum SNR,

is achieved by an optimum channel width. This optimum width is found by setting the fol-

lowing derivative to zero:

$$\frac{\partial}{\partial W} \overline{a_n^2}(f) = 0. \tag{3-22}$$

If the noise floor is dominated by 1/f noise, the optimum width is:

$$W_{opt} = \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}}, \tag{3-23}$$

which leads to:

$$C_{gs} + C_{gd} = 2C_s + C_p. \tag{3-24}$$

If both the 1/f noise and thermal noise need to be considered, the optimum width of the

transistor is smaller than the value given by (3-23) and the exact expressions become com-

plex. Simplified expressions of the optimum width and the capacitance relationship are

given by:

$$W_{opt} = \eta \cdot \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}}, \tag{3-25}$$

$$C_{gs} + C_{gd} = \eta(2C_s + C_p), \tag{3-26}$$

where $1/3 < \eta < 1$ is a coefficient dependent on W_{opt}. Equation (3-24) and (3-26) show that

the minimum input-referred noise floor is achieved when the gate capacitance of the tran-

sistor is at a value equal to or smaller than the total capacitance of the sensor and the inter-

connection. Thus, the noise optimization is referred to as optimum capacitance matching.

In some polysilicon processes, because the large interconnect capacitance dominates, it is not meaningful to optimize the sizing of input MOSFETs, and the input transistors are often made as large as permitted by area and power constraints. In CMOS MEMS technology, with the interconnect parasitics significantly reduced, choosing the optimum size for input MOSFETs to achieve capacitance matching is important to minimize noise floor.

With relatively small overlap capacitances, a given channel area *WL* fixes both the 1/f noise and the gate capacitance, and a large *W/L* ratio reduces the thermal noise. Therefore, it is usually preferred to use minimum channel length *L*. Figure 3-3 show the relationship between noise and the channel width at 100 KHz and 10 MHz, respectively, with minimum channel length of 0.5 μm. The minimum noise and the optimum channel width versus the modulation frequency are plotted in Figure 3-4. These plots are calculated using the typical parameters of CMOS MEMS accelerometers with 20 fF sensing capacitance and 100 fF total parasitic capacitance including the interconnect capacitance and the fringe capacitance. They show that given transducer and interconnect parameters, which is limited by the fabrication process and is not decided by the circuit designers, there is a limit on the minimum achievable noise floor and this limit decreases with the frequency. The optimum channel width of input MOSFETs to achieve matching is in the range of 50 - 100 μm for 0.5 μm channel length. Forced to use these relatively small devices, the 1/f noise is significant in entire frequency range of 100 KHz - 10 MHz. An obvious way to reduce noise is to modulate the signal at higher frequency. However, higher frequency means more power consumption and difficulties in circuit implementation. Therefore, understanding the limit and the trade-offs of noise performance is very important.
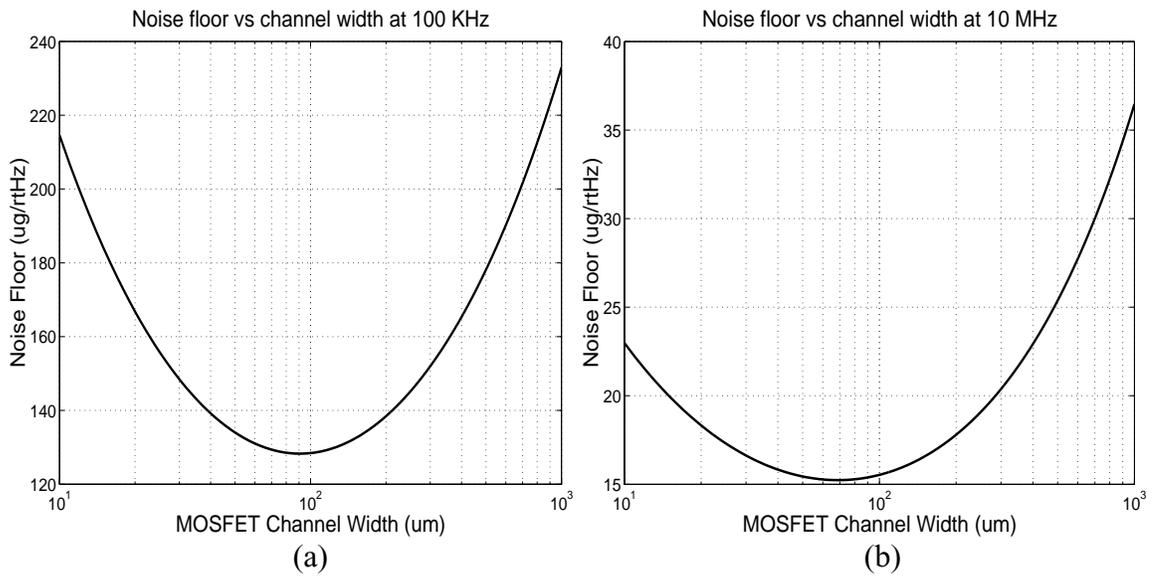
Figure 3-3: Input-referred electronic noise floor: (a) noise versus MOSFET channel width at 100 KHz; (b) noise versus MOSFET channel width at 10 MHz. Channel length is 0.5 μm. Bias current is 0.5 mA. Long channel model is used in calculation.
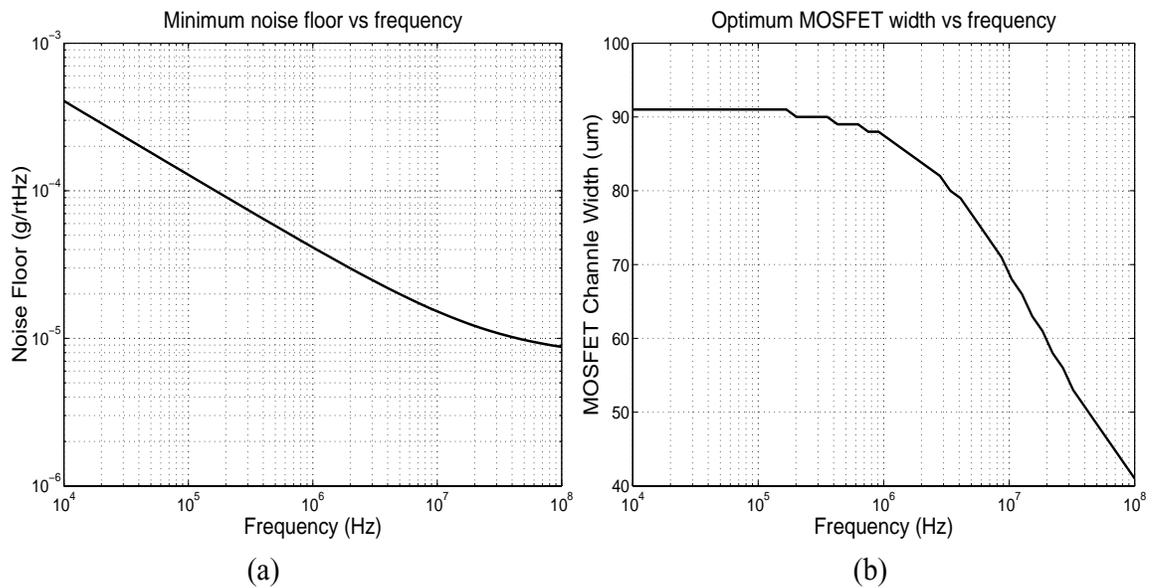
Figure 3-4: Input-referred noise optimization: (a) minimum noise floor versus frequency; (b) optimum MOSFET channel width versus frequency. Channel length is 0.5 μm. Bias current is 0.5 mA. Long channel model is used in calculation.

The 1/f noise is usually not sensitive to the bias current. In some processes, the 1/f noise actually increases with the bias current. When the 1/f noise is significant, the bias current or voltage of the MOS transistors has relatively small impact on the circuit noise performance.

3.1.4 Noise Optimization without 1/f Noise

If sufficiently large bandwidth can be achieved, the electronic noise floor is ultimately limited by the thermal noise of the MOS transistors. Under the dominance of the thermal noise, the equation (3-18) is reduced to:

$$\sqrt{\overline{a_n^2}(f)} = \sqrt{\frac{K_T T(1 + c_1 W + c_2 WL)^2}{W^\beta L^{\beta-1}}}. \tag{3-27}$$

Since the expression is simplified, closed-form expressions for optimum transistor width and minimum accelerometer input-referred noise can be obtained by setting the following derivative to zero:

$$\frac{\partial}{\partial W}\overline{a_n^2}(f) = \frac{\partial}{\partial W}\left[\frac{K_T T(1 + c_1 W + c_2 WL)^2}{W^\beta L^{\beta-1}}\right] = 0. \tag{3-28}$$

This results in an optimum transistor width of:

$$W_{opt} = \frac{\beta}{2-\beta} \cdot \frac{1}{c_1 + c_2 L}, \tag{3-29}$$

and a minimum input-referred noise floor of:

$$\sqrt{\overline{a_n^2}(f)} = \sqrt{\frac{4K_T T}{\beta^\beta(2-\beta)^{2-\beta}}L^{1-\beta}(c_1 + c_2 L)^\beta}. \tag{3-30}$$

According to equation (3-11), (3-12), (3-19) and (3-20), the optimum transistor width can be rewritten as:

$$W_{opt} = \frac{\beta}{2-\beta} \cdot \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}}, \tag{3-31}$$

and it gives an optimum capacitance matching condition of:

$$\frac{C_{gs} + C_{gd}}{2C_s + C_p} = \frac{\beta}{2-\beta}. \tag{3-32}$$

The optimum conditions given by (3-29), (3-30), (3-31) and (3-32) need to be considered separately in two regions: long channel region with large critical electric field and relatively small bias current or voltage; and short channel region where MOS transistors are in deep velocity saturation, because the expressions for K_T are different in these two regions.

In the long channel region, β is 0.5, and the optimum transistor width and optimum capacitance matching are given by:

$$W_{opt} = \frac{1}{3} \cdot \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}}, \tag{3-33}$$

$$C_{gs} + C_{gd} = \frac{2C_s + C_p}{3}. \tag{3-34}$$

The minimum noise floor is:

$$\sqrt{\overline{a_n^2(f)}} = \sqrt{\frac{16\omega_n^4 x_0^2 \gamma k T (2C_s + C_p)^{3/2}}{3^{3/2} C_s^2 V_m^2 (2\mu_n I_D)^{1/2}} L^{1/2} \left(\frac{2}{3}L + 2L_{ov}\right)^{1/2}}. \tag{3-35}$$

Equation (3-35) suggests that increasing bias current (or voltage) reduces the noise floor. However, increasing the current is the least effective way to reduce noise. For example, a 2x reduction of noise floor requires 16x larger current. Furthermore, excessively large current will drive the sub-micron MOS transistors into velocity saturation.

In the deep velocity saturation region, β becomes 1, and the optimum width of the transistors is given by:

$$W_{opt} = \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}}. \tag{3-36}$$

This leads to the optimum matching condition of:

$$C_{gs} + C_{gd} = 2C_s + C_p. \tag{3-37}$$

The minimum input-referred noise floor in deep velocity saturation region is:

$$\sqrt{\overline{a_n^2(f)}} = \sqrt{\frac{4\omega_n^4 x_0^2 \gamma kT(2C_s + C_p)}{\alpha C_s^2 V_m^2 \mu_n E_c}\left(\frac{2}{3}L + 2L_{ov}\right)}. \tag{3-38}$$

The noise floor is no longer affected by the bias current or voltage.

Both (3-35) and (3-38) show that the noise floor is reduced by smaller channel length. This seems to suggest that minimum length should always be used in input transistors. However, one should be aware that deep sub-micron MOS transistors are more noisy because γ is larger due to hot electron effect, α is less than unity due to velocity saturation, and μ_n is smaller due to mobility degradation [40, 42]. For the same reason, one should also be cautious to over-drive the transistors into deep velocity saturation region. For CMOS processes with relatively long channel, such as the 0.5 µm technology, minimum channel length and large bias current are effective in minimizing the thermal noise floor. In more advanced deep sub-micron CMOS technologies, the optimum length and bias current must be carefully chosen by simulations, and often by experiments due to the lack of accurate noise models for deep sub-micron transistors.

Based on the long channel model without hot electron effect ($\gamma = 2/3$), the minimum thermal noise floor is 8 µg/rtHz for 0.5 µm NMOS transistor biased at 0.5 mA, and it will be reduced to 4 µg/rtHz in a 0.13 µm technology. Due to various short channel effects which result in higher thermal noise, both numbers underestimate the actual noise. A more realistic estimate of the optimum thermal noise floor is about 10 µg/rtHz. There are four ways to further reduce the noise floor: reducing the natural frequency; reducing the gap width; increasing the total sensing capacitance; and reducing the interconnect capacitance.

3.2 Noise Folding and Capacitive Sensing Architectures

Capacitive sensing operates based on motion-induced charge transfer. This charge transfer generates an ac voltage or an ac current. Therefore, there are three ways to read out the sensed signal: reading the charge, reading the voltage, and reading the current. The noise performances of these three methods are different.

3.2.1 Review of Capacitive Sensing Circuit Architectures

There are three types of readout circuits for capacitive sensing: switched-capacitor (SC) charge integration; continuous-time (CT) current readout with transimpedance amplifier (TIA); and continuous-time voltage readout. The continuous-time voltage readout can be realized by two approaches: capacitive feedback architecture; and open-loop architecture. The generic noise model in Figure 1 and the noise analysis in the previous section, although obtained from a voltage-domain description, apply universally to all four types of circuits. However, capacitive sensing generates an AM signal that needs to be

sampled or demodulated in some way to extract its envelop, and noise folding may be introduced during this process. The three circuit architectures differ in the noise folding process, which has a great influence on overall noise performance. Furthermore, in the SC charge sensing circuits and the TIA current sensing circuits, there are noise sources other than the ones described in Figure 1, introducing additional noises.

The switched-capacitor readout is the most widely used architecture for capacitive sensing [9, 11 - 15, 43]. The switched-capacitor circuit is widely used in realizing robust and accurate MOS analog signal processing circuits [44]. The capacitive sensing is based on charge-voltage relationship, the same foundation on which the SC circuit operates. Thus, the capacitive sensor can be integrated very well with the SC interface circuits. The SC circuit provides a virtual ground and robust dc biasing at the sensing node so that the sensed signal is insensitive to parasitic capacitance and undesirable charging. The SC circuit also offers a wide range of techniques to suppress offset and low-frequency noise, such as correlated double sampling (CDS) and programmable capacitor array (PCA) [9].
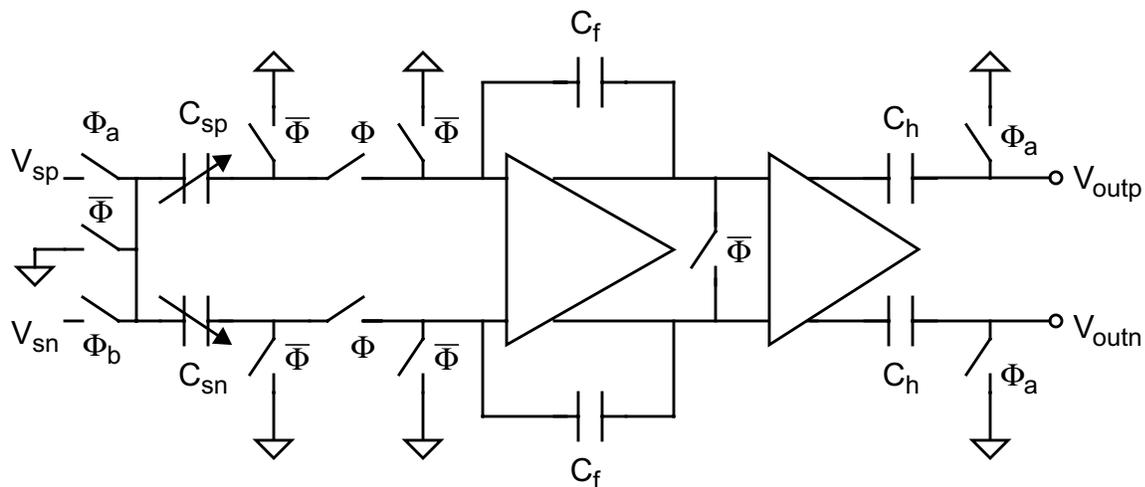
Figure 3-5: Switched-capacitor charge integrator with correlated double sampling (CDS) for capacitive sensing [9, 13, 43].

A SC charge integrator for polysilicon surface micromachined accelerometer is shown in Figure 3-5. The output voltage of this circuit is given by:

$$V_{out} = \frac{C_{sp} - C_{sn}}{C_f} V_s.$$ (3-39)

The transimpedance amplifier is widely used in optical receivers for sensing photocurrent from photodiodes. In capacitive sensors, the charge transfer generates an ac current which can be sensed by the TIA [8]. This is shown in Figure 3-6. The circuit output is given by:

$$V_{out}(f) = j2\pi f R_f (C_{sn} - C_{sp}) V_m.$$ (3-40)

For capacitive sensing, the TIA circuit is a differentiator that has high-pass frequency response. The TIA architecture provides a virtual ground and robust dc biasing at the sensing node in continuous-time.

The capacitance change can also be sensed by reading the ac voltage in continuous-time. A capacitive feedback voltage sensing amplifier [6, 16] is shown in Figure 3-7. And an open-loop differential voltage sensing amplifier [17, 23] is shown in Figure 3-8.
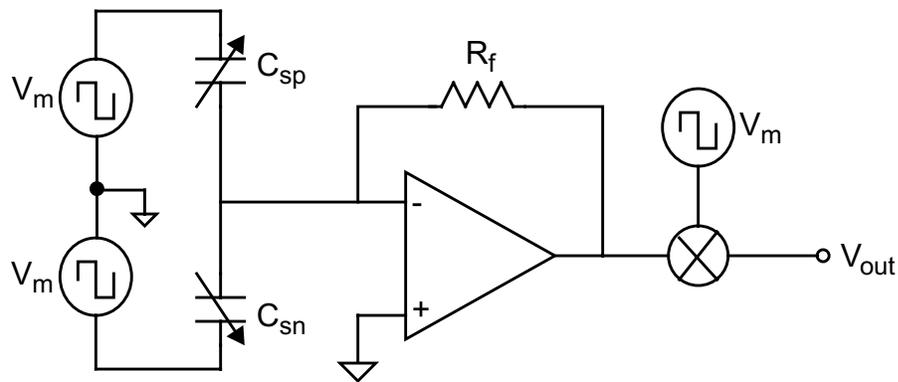
Figure 3-6: Transimpedance amplifier for continuous-time current-mode capacitive sensing [8].
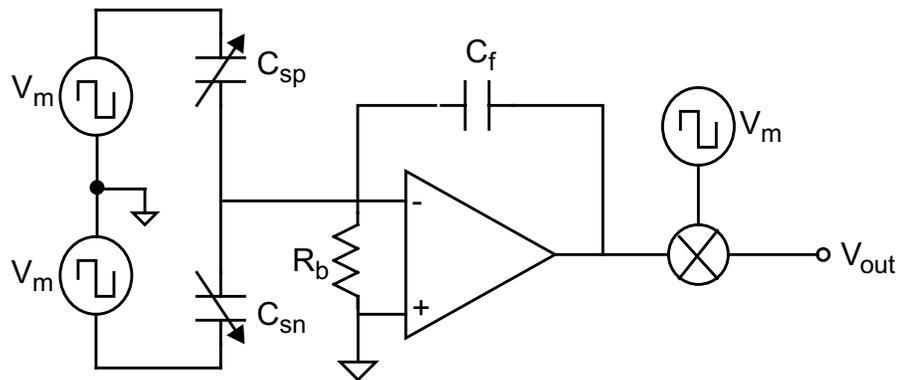
Figure 3-7: Continuous-time voltage-mode capacitive sensing with a capacitive feedback topology [6, 16].
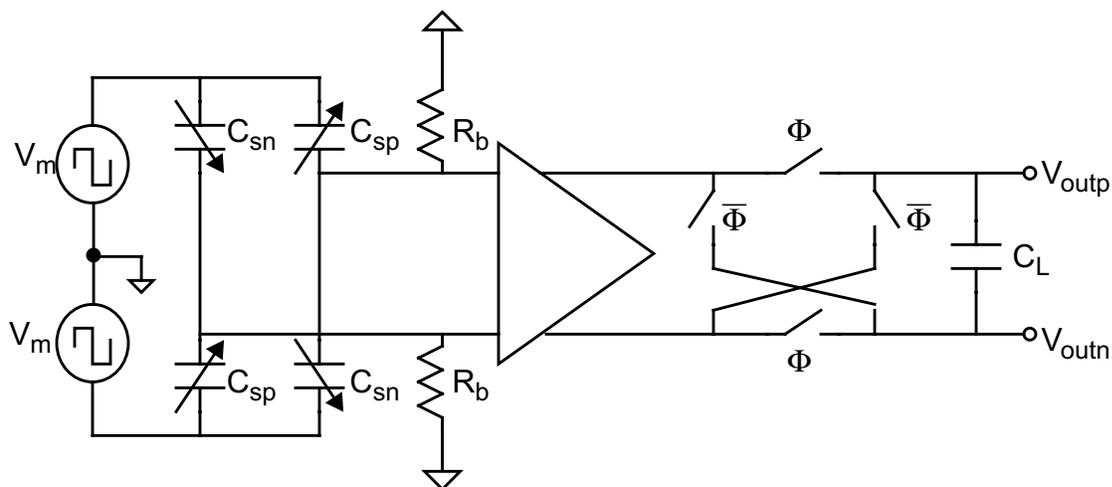
Figure 3-8: Continuous-time voltage-mode capacitive sensing with a open-loop fully differential topology [17, 23].

Continuous-time voltage sensing requires a biasing circuit to provide dc bias at the sensing node. In Figure 3-7 and 3-8, resistors are drawn to represent the biasing devices. To avoid attenuating the signal, they must have very large resistance, orders of magnitude higher than the ac impedance of the sensor, which itself is in the range of 10^6 - 10^8 Ω. In practice, real resistors are rarely used because the large resistors not only occupy large silicon area but also possess large parasitic capacitance. For ultra-small capacitance devices such as in CMOS MEMS, it is simply impossible to use resistor biasing that requires GΩ

resistors. A number of devices with high ac impedance are used as the bias devices, including: reverse-biased diodes; sub-threshold MOSFETs; and MOS switches that are normally turned off, as we will described in next chapter. Robust and reliable dc biasing at the sensing nodes is a major challenge for continuous-time voltage sensing circuits.

The output voltage of the capacitive feedback amplifier in Figure 3-7 is given by:

$$V_{out} = \frac{C_{sp} - C_{sn}}{C_f} V_m.$$

(3-41)

An ac virtual ground is provided by this circuit so that the sensed signal is parasitic-insensitive. The input voltage of the open-loop amplifier in Figure 3-8 is given by (3-2). It is a parasitic-sensitive signal. For this reason, the open-loop architecture is undesirable when there exists a large varying parasitic capacitance, such as in some polysilicon surface micromachining technologies where diffusion interconnect is used. This disadvantage, along with the difficulties in dc biasing and offset control, the open-loop continuous-time voltage readout has been considered the least robust and has been much less popular than the SC architecture.

3.2.2 Comparison of Noise Performances

Despite its popularity, the SC circuit has much higher circuit noise for two reasons. First, it uses MOS switches to connect the sensor and the circuit input. The on-resistance of the MOS switches give rise to additional thermal noise that is amplified by the following circuits. The thermal noise of MOS switches is referred to as kT/C noise because the noise power is proportional to kT/C. Second, it is a sampled-data system and a SC front-end prohibits any anti-aliasing filter to be used prior to sampling, therefore, severe noise

folding causes the output noise power to multiply. According to sampling theorem, the spectrum of a sampled signal is given by:

$$X_s(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X(f - nf_s).$$

(3-42)

During the sampling process, the power of the narrow-band signal remains the same, while the power of the wide-band noise increases by aliasing. This is equivalent to folding noises outside the signal band into the signal band. Because the circuit bandwidth must be several times higher than the sampling rate to allow the circuit to settle properly, the noise folding causes the in-band noise to multiply. Assuming the bandwidth of the circuit is N times of the sampling rate:

$$BW = Nf_s,$$

(3-43)

the spectrum of the signal and the noise are given by:

$$
\begin{aligned}
s_s(f) &= \frac{1}{T_s} \sum_{n=-N}^{N} s_0(f - nf_s) \\
&= \frac{1}{T_s} s_0(f), \qquad -\frac{f_s}{2} < f < \frac{f_s}{2}
\end{aligned}
$$

,

(3-44)

and

$$n_s(f) = \frac{1}{T_s} \sum_{n=-N}^{N} n_0(f - nf_s).$$

(3-45)

Thus, the power of in-band signal is given by:

$$S_s = \frac{1}{T_s^2} S_0,$$

(3-46)

and the power of in-band noise is given by:

$$N_s = \frac{1}{T_s^2} N N_0.$$
(3-47)

The signal-to-noise ratio (SNR) after sampling is reduced by a factor of *N*:

$$\frac{S_s}{N_s} = \frac{1}{N} \frac{S_0}{N_0}.$$
(3-48)

This is shown in Figure 3-8.

SC readout circuits have been used extensively in polysilicon MEMS processes because the polysilicon interconnection generates a large amount of thermal noises, hence, the circuit noise is less important. With the device size shrinking, the capacitance becoming smaller, the kT/C noise grows larger. As the interconnect noise source is eliminated by metal routing, the kT/C noise plus noise folding has become a major limitation of sensor resolution.

With sinusoidal carrier signal, the demodulation in continuous-time does not cause noise folding. However, the circuit implementation is more difficult for sinusoidal carriers,
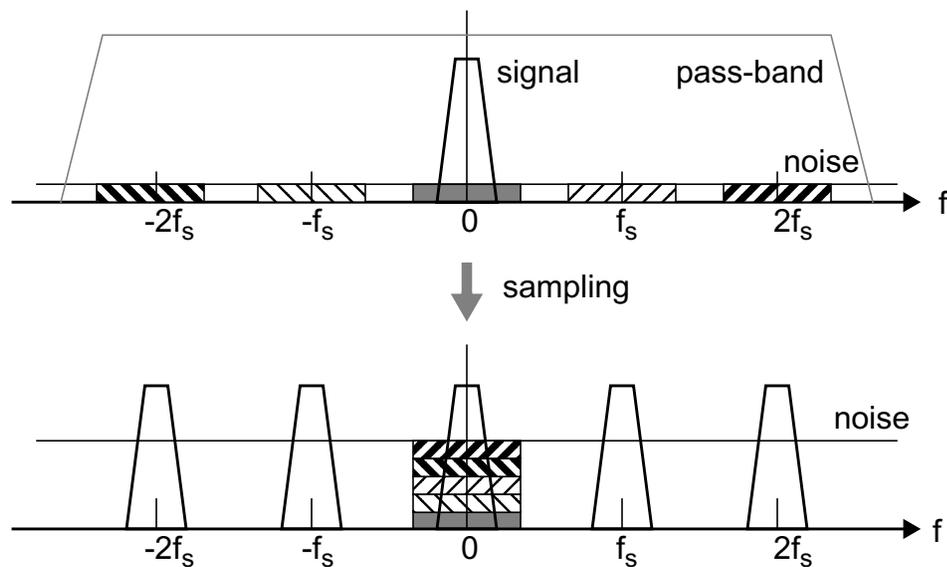
Figure 3-8: Noise folding in sampling process.

particularly in the demodulator. The demodulation using square-wave carrier, does give rise to noise folding, but at lesser level than the sampling. It is shown in Figure 3-9.

To understand the effect of demodulation on the noise, the balanced square-wave signal can be written in Fourier expansion:

$$u(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2\pi(2n-1)f_m t)}{2n-1}$$
$$= \frac{4}{\pi} \left[\sin 2\pi f_m t + \frac{1}{3} \sin 6\pi f_m t + \frac{1}{5} \sin 10\pi f_m t + \dots \right]$$

(3-49)

The whole process of modulation and demodulation can be expressed by:

$$s_{out}(t) = [(s_0(t)u(t) + n_0(t)) \bullet h(t)]u(t)$$
$$= s_0(t)u^2(t) + (n_0(t) \bullet h(t))u(t) \quad ,$$
$$= s_d(t) + n_d(t)$$

(3-50)
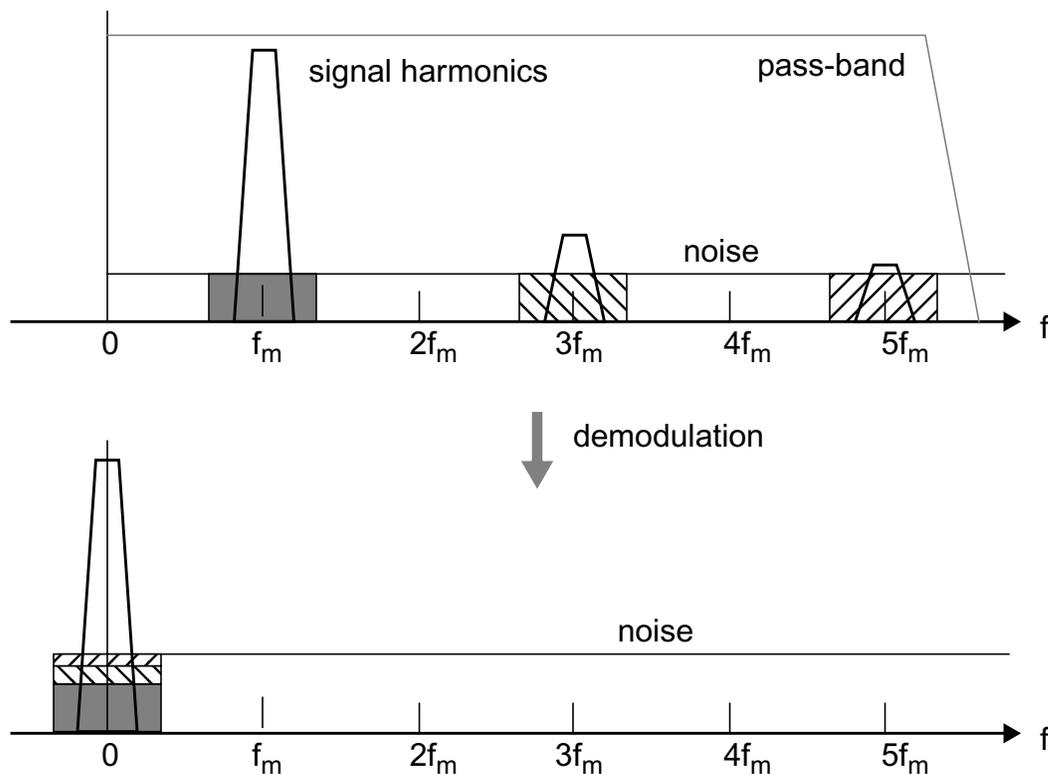
Figure 3-9: Noise folding in square-wave demodulation process.

where $h(t)$ is the inverse Fourier transform of the circuit frequency response.

If the circuit frequency response is flat and low-pass bandwidth of:

$$BW = (2N - 1)f_m,$$
(3-51)

according to (3-49) and (3-50), the demodulated signal is given by:

$$s_d(t) = s_0(t)\left[\frac{4}{\pi}\sum_{n=1}^{N}\frac{\sin(2\pi(2n-1)f_m t)}{2n-1}\right]^2$$

$$= s_0(t)\frac{16}{\pi^2}\sum_{n=1}^{N}\frac{[\sin(2\pi(2n-1)f_m t)]^2}{(2n-1)^2} .$$
(3-52)

$$= s_0(t)\frac{16}{\pi^2}\sum_{n=1}^{N}\frac{1-\cos(4\pi(2n-1)f_m t)}{2(2n-1)^2}$$

Since only the dc part is kept after demodulation, the signal can be written as:

$$s_d(t) = s_0(t)\frac{8}{\pi^2}\sum_{n=1}^{N}\frac{1}{(2n-1)^2},$$
(3-53)

and its Fourier transform in the frequency domain is given by:

$$s_d(f) = s_0(f)\frac{8}{\pi^2}\sum_{n=1}^{N}\frac{1}{(2n-1)^2}.$$
(3-54)

And the total signal power after demodulation is given by:

$$S_d = S_0\left[\frac{8}{\pi^2}\sum_{n=1}^{N}\frac{1}{(2n-1)^2}\right]^2$$

$$\leq S_0\left[\frac{8}{\pi^2}\sum_{n=1}^{\infty}\frac{1}{(2n-1)^2}\right]^2 .$$
(3-55)

It is known that:

$$\sum_{n=1}^{\infty}\frac{1}{(2n-1)^2} = \frac{\pi^2}{8}.$$
(3-56)

Therefore, in the ideal case where the bandwidth is infinity, the demodulated signal power is:

$$\lim_{N \to \infty} S_d = S_0 \left[\frac{8}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{(2n-1)^2} \right]^2 = S_0. \tag{3-57}$$

On the other hand, assuming the noise is a white wide-band stationary random process, the power of the noise after demodulation is given by:

$$N_d = N_0 \frac{16}{\pi^2} \sum_{n=1}^{N} \frac{1}{(2n-1)^2}, \tag{3-58}$$

and in ideal case, by:

$$\lim_{N \to \infty} N_d = N_0 \frac{16}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{(2n-1)^2} = 2N_0. \tag{3-59}$$

The SNR after demodulation is then given by:

$$\frac{S_d}{N_d} = \frac{S_0}{N_0} \frac{\left[\dfrac{8}{\pi^2} \displaystyle\sum_{n=1}^{N} \dfrac{1}{(2n-1)^2} \right]^2}{\dfrac{16}{\pi^2} \displaystyle\sum_{n=1}^{N} \dfrac{1}{(2n-1)^2}}. \tag{3-60}$$

With infinite bandwidth, the SNR is:

$$\lim_{N \to \infty} \frac{S_d}{N_d} = \frac{S_0}{N_0} \frac{1}{2}. \tag{3-61}$$

The SNR loss by demodulation is 3 dB in ideal case. This SNR loss can be understood intuitively as the following: the signal power is not changed by demodulation, while the noise power is increased by folding the noise at odd harmonic frequencies into the base-band, therefore, the total SNR is decreased. As shown in Figure 3-10, the additional SNR

loss caused by finite circuit bandwidth is smaller than 1 dB. Therefore, the total SNR loss by square-wave demodulation is less than 4 dB in continuous-time voltage sensing.

While also operating in continuous-time, the current sensing approach exhibits much high SNR loss because its frequency response is not flat. The transimpedance amplifier is inherently a differentiator and has high-pass frequency response. The high-frequency noises are amplified by the TIA and folded into the signal band. According to Figure 3-11, the SNR loss are given by,

$$\frac{S_{dc}}{N_{dc}} = \frac{S_0}{N_0} \frac{\left[\dfrac{8}{\pi^2} \displaystyle\sum_{n=1}^{N} \dfrac{1}{(2n-1)}\right]^2}{\dfrac{16}{\pi^2} \displaystyle\sum_{n=1}^{N} 1} . \tag{3-62}$$

With the feedback resistor also adding noise, the CT current sensing also has worse noise performance than the CT voltage sensing [8].
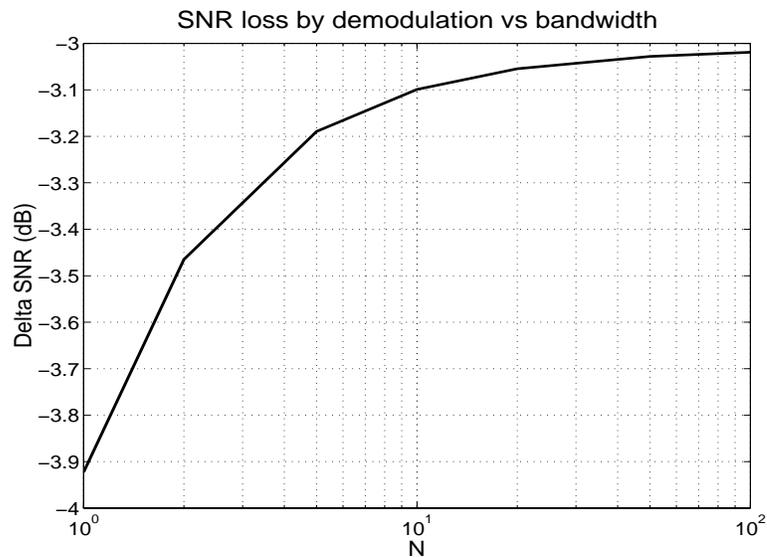
Figure 3-10: SNR loss versus bandwidth in square-wave demodulation.
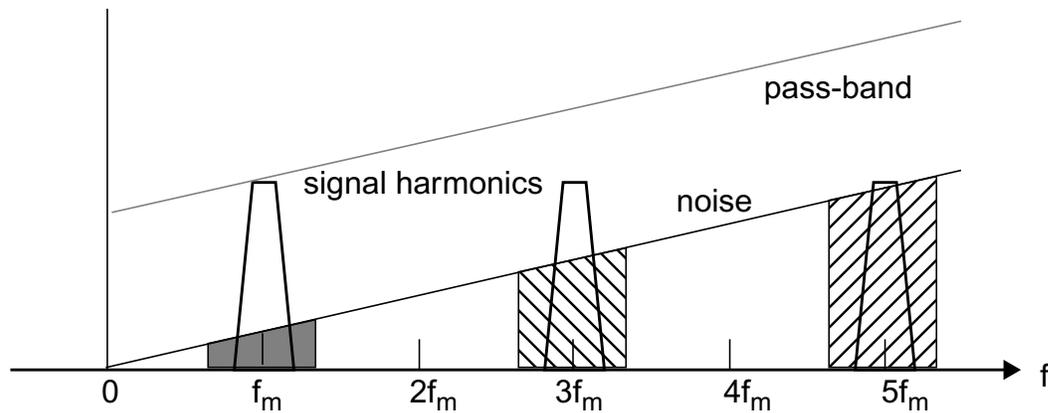
Figure 3-11: Noise folding in demodulation after high-pass filtering.

A properly designed TIA will apply bandwidth limiting of some kind to reduce the folding of high-frequency noise. However, a key advantage of the TIA architecture is that it provides a virtual ground in continuous-time so that the sensed signal (but not the noise) is insensitive to parasitic capacitance. To maintain the virtual ground requires the circuit to have very high gain at the modulation frequency. As a result, the closed-loop bandwidth is much larger than the modulation frequency, which causes greater noise folding.

A similar approach to TIA is to use feedback capacitor instead of feedback resistor to form a capacitive voltage amplifier. This capacitive feedback continuous-time voltage sensing architecture does not suffer from the amplification of high-frequency noise. However, just like TIA, it requires large bandwidth to obtain an ac virtual ground at the modulation frequency. Therefore, compared to the open-loop architecture, it consumes more power while provides less gain.
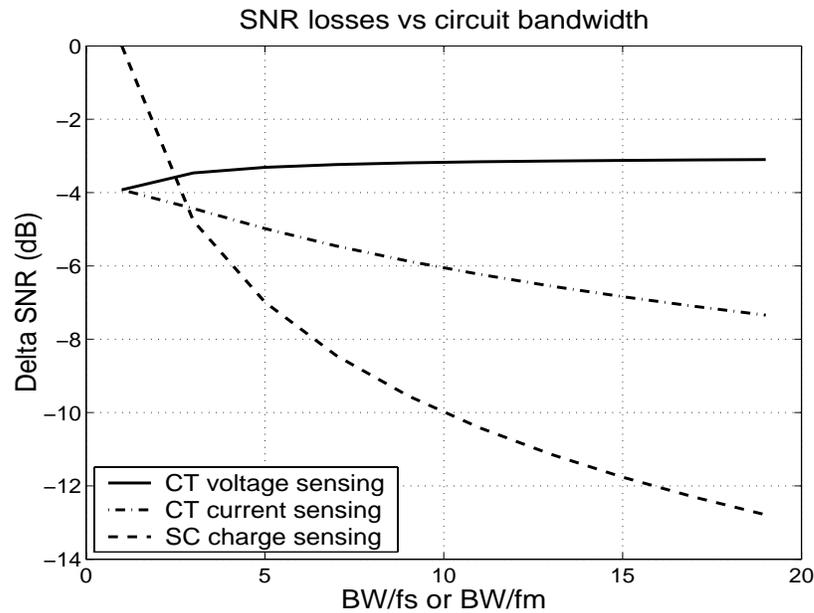
Figure 3-12: SNR loss versus bandwidth in three sensing architectures with square-wave modulation signal for CT voltage and current sensing.

The SNR degradation caused by noise folding versus the ratio between the circuit bandwidth and the modulation or sampling frequency are shown in Figure 3-12. The SNR loss is less than 4 dB and is insensitive to the bandwidth in continuous-time voltage sensing. The circuit can operate at bandwidth three times of the clock frequency with little SNR degradation. The SNR decreases rapidly with increasing bandwidth in the SC charging sensing and CT current sensing. On the other hand, all the feedback architectures must have bandwidth much higher than the clock frequency for proper operation, therefore, severe noise folding is inevitable for SC and TIA circuits. The continuous-time voltage sensing approach has the best noise performance. In particular, the open-loop CT voltage sensing architecture not only has good noise performance but also requires much smaller bandwidth than the other architectures, which implies savings in power and area.

3.2.3 A Time-Domain Noise Simulation Study

The above analysis is verified by a time-domain Monte-Carlo simulation study. In this study, additive white Gaussian noise (AWGN) sequences are used as noise sources. Transient simulations are performed by HSPICE on three circuit architectures which do not include the capacitive feedback voltage amplifier, then the simulation data are processed in MATLAB to calculate the normalized noise power and noise root mean square (RMS) value. The noise sequence is band-limited to 10MHz, and sampled at 20 MHz (50 ns). The circuits are modulated or sampled at 1 MHz. The anti-aliasing filter for continuous-time circuits has 3-dB bandwidth of 500 KHz.

Figure 3-13 shows the normalized input-referred RMS noise values. It is obvious that the open-loop continuous-time voltage readout has far superior noise performance compared to the other two architectures.
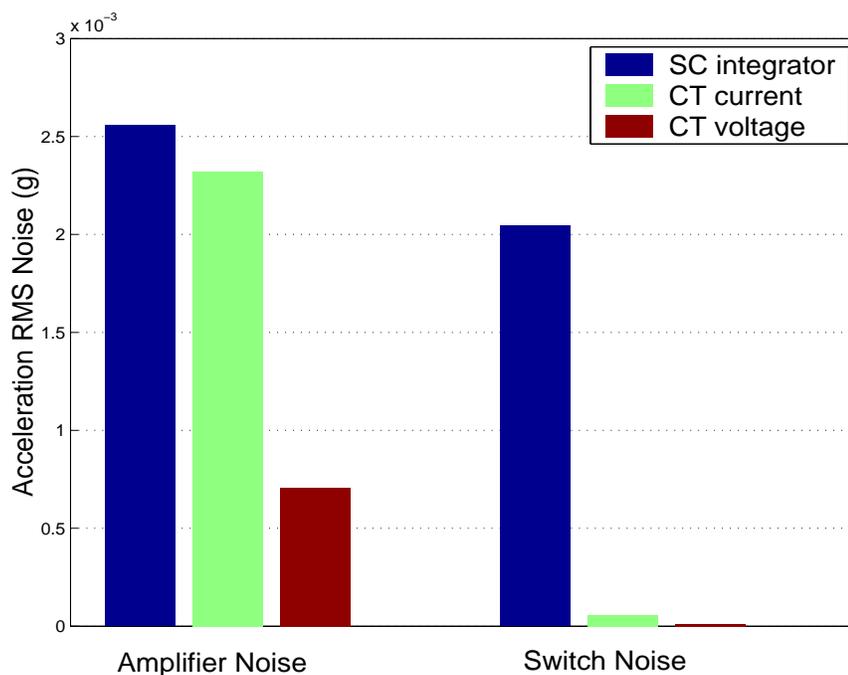
Figure 3-13: Simulated input-referred noise RMS values in three sensing architectures.

3.2.4 Summary of Noise Folding

The previous analyses and simulations conclude that demodulation with square-wave signal increases the output noise power by noise folding. The output noise PSD is given by:

$$N_o = N(f_m)F, \tag{3-63}$$

where F is the noise folding factor. In all analyses and simulations, the noise is assumed to be white with constant PSD across all frequencies. As we discussed in section 3.1, the circuit noise is in fact frequency dependent. Therefore, the result of noise folding should be expressed more accurately by:

$$\begin{aligned}N_o &= \frac{16}{\pi^2}\sum_{n=1}^{N}\frac{N((2n-1)f_m)}{(2n-1)^2}\\&= \frac{16}{\pi^2}\left[N(f_m)+\frac{1}{9}N(3f_m)+\frac{1}{25}N(5f_m)+\ldots\right]\end{aligned}. \tag{3-64}$$

Because the noise decreases with frequency, the noise folding factor is little smaller than the 3 dB predicted by (3-40). If the noise is an ideal 1/f noise, the noise folding factor is:

$$F = \frac{16}{\pi^2}\sum_n\frac{1}{(2n-1)^3} \approx 1.7, \tag{3-65}$$

which is about 2.3 dB. In practice, the actual noise folding factor F is between the white noise assumption and the ideal 1/f noise assumption.

3.3 Circuit and Sensor Offsets

The sensitivity of the CMOS MEMS accelerometer is lower than 1 mV/g. The offsets of the circuit and the sensor itself could be more than 40 dB larger than the sensed signal.
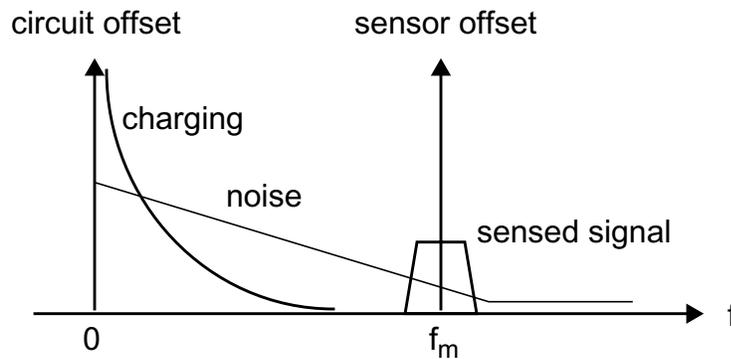
Figure 3-14: Spectrum of signal, noise, sensor offset, circuit offset and charging.

Without proper offset suppression, these offsets reduce the signal dynamic range in good cases, while in the worst situations, they may saturate the amplifier and completely block the useful signal. Figure 3-14 shows the spectrum locations and the possible relative magnitudes of sensed signal, noise, circuit offset, sensor offset, and charging, which we will describe in the next section. Due to the large magnitudes of nonideal components, the sensing circuit must be able to reject these components while amplifying the useful signal.

3.3.1 Circuit Offset

The CMOS circuits have offset on the order of 10 mV. For small minimum-length devices necessary for minimizing input-referred noise floor, the circuit offset is worse than in normal differential amplifiers, and could possibly approach 100 mV. The circuit offset appears as a dc signal at the circuit output. While gain of 100 - 1000 is required to amplify the sensed signal, the amplified dc offset can easily saturate the circuit and completely block the useful ac signal.

(a)   (b)
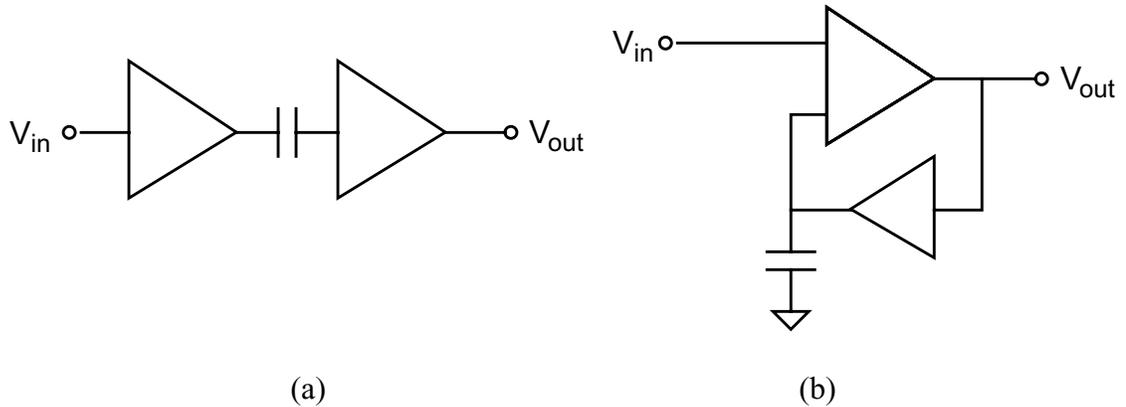
Figure 3-15: Methods of dc offset cancellation: (a) ac coupling; and (b) dc feedback.

In SC circuits, the dc offset is often cancelled by correlated double sampling (CDS) technique [45]. In continuous-time circuits, there are two methods to block the offset: capacitive ac coupling and dc feedback. As shown in Figure 3-15, the capacitive coupling directly blocks the dc offset, while the dc feedback method employs a low-pass feedback loop to attenuate the dc offset.

3.3.2 Sensor Offset

In CMOS MEMS accelerometer, the lateral manufacturing mismatch causes a position offset in the sensor. For 1.5 μm gap between stator and rotor fingers, the mismatch offset can be as large as 0.1 - 1.0 μm, which is equivalent to 15 - 150 g of acceleration. This sensor position offset is sensed by capacitive sensors and appears as an ac offset signal at the modulation frequency indistinguishable to the sensed signal.

Since the sensor offset is modulated (or sampled in SC circuit) at the same clock frequency as the signal, it can not be cancelled by ac coupling or dc feedback shown in Figure 3-15, as the circuit offset. In vibration sensors, or ac accelerometers, the sensor offset can be cancelled by employing a dc feedback loop with very narrow bandwidth using

demodulated signal [23]. This is not possible if the dc acceleration needs to be sensed. For dc accelerometers, the sensor offset could only be removed by trimming or calibration.

The sensor offset cancellation can be done in mechanical domain by using electrostatic actuators to pull the proof-mass back to the center position. However, since the sensor offset can be very large, large actuator area and high voltage are often needed. It is therefore very desirable to have electronic cancellation of sensor offset. An offset cancellation scheme using programmable capacitor array (PCA) is introduced in [9, 13, 43]. We will present a different scheme based on differential difference amplifier (DDA) in the next chapter.

3.4 Charging in Ultra-Small Capacitive Sensors

Capacitive sensing relies on charge transfer to detect capacitance variations. Besides the charge transfer induced by the capacitance variation, there are inevitably unwanted charge transfer activities. These undesirable charge transfer activities are referred to as charging throughout this dissertation. There are two main mechanisms of undesirable charging: the accumulation of charges from the surrounding air on the electrodes; the charge leakage of bias devices. When MOS switches are used, charge injection is also introduced, and will be discussed in the next chapter. According to the charge-voltage relationship

$$V = \frac{Q}{C},\tag{3-66}$$

when the capacitance is very small, the charging could have significant impacts.

Sensing Electrode
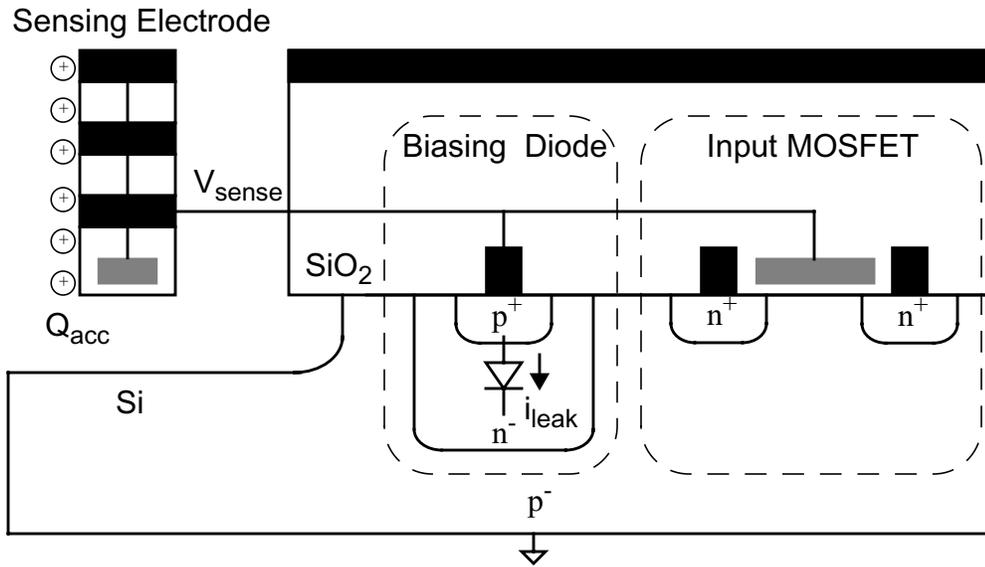
Figure 3-16: Very-high-impedance sensing node and undesirable charging mechanisms.

$V_{mp}(t) = V_b + V_m(t)$

$Q_c(t)$ charging

$Q(t) = Q_0 + Q_c(t)$

$V_{sense}(t) = V_b + \Delta V_{sense}(t) + \Delta V_c$

$V_{mn}(t) = V_b - V_m(t)$
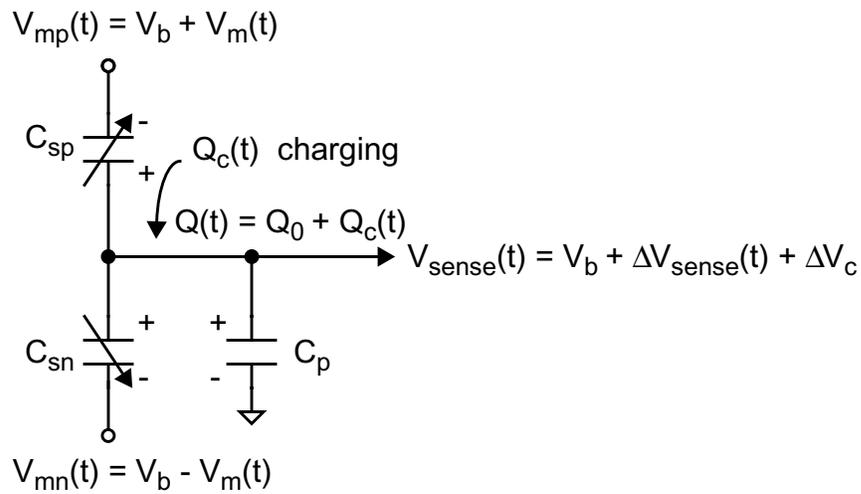
Figure 3-17: Charging and charging induced voltage error in a capacitive sensor.

As shown in Figure 3-16, the sensing node is surrounded by air and SiO_2, both are dielectric, and reverse-biased diodes. Therefore, the input sensing node has very high impedance on the order of $G\Omega$, and is very sensitive to charge. Figure 3-17 depicts the capacitive sensing from the viewpoint of charge transfer. Q_c is the total charge caused by

any undesirable charging activities. At any given time, the total charge on the sensing node

is given by:

$$Q(t) = C_{sp}[V_{sense}(t) - V_{mp}(t)] + C_{sn}[V_{sense}(t) - V_{mn}(t)] + C_p V_{sense}(t). \quad (3\text{-}67)$$

The sensing voltage is then:

$$V_{sense}(t) = \frac{C_{sp}V_{mp}(t) + C_{sn}V_{mn}(t) + Q(t)}{C_{sp} + C_{sn} + C_p}. \quad (3\text{-}68)$$

The voltages at the modulator input are given by:

$$V_{mp}(t) = V_b + V_m(t), \quad (3\text{-}69)$$

$$V_{mn}(t) = V_b - V_m(t). \quad (3\text{-}70)$$

where V_b is the dc bias voltage and $V_m(t)$ is the ac modulation signal. Based on charge

conservation, the total charge on the sensing node is given by:

$$Q(t) = Q(0) + Q_c(t). \quad (3\text{-}71)$$

where $Q(0)$ is the initial charge. Without charging, the charge on the sensing node should

be a constant. In the initial condition, there is no ac modulation, and all voltages equal to

the dc bias voltage:

$$V_{mp}(0) = V_b, V_{mn}(0) = V_b, V_{sense}(0) = V_b. \quad (3\text{-}72)$$

The initial charge is then given by:

$$Q(0) = V_b C_p. \quad (3\text{-}73)$$

Thus, the sensing voltage can be rewritten as:

$$
\begin{aligned}
V_{sense}(t) &= \frac{C_{sp}(V_b + V_m(t)) + C_{sn}(V_b - V_m(t)) + V_b C_p + Q_c(t)}{C_{sp} + C_{sn} + C_p} \\
&= V_b + \frac{C_{sp} - C_{sn}}{C_{sp} + C_{sn} + C_p} V_m(t) + \frac{Q_c(t)}{C_{sp} + C_{sn} + C_p}
\end{aligned}
\quad (3\text{-}74)
$$

The first term is the dc bias voltage, the second ac term is the actual sensed signal, and the third term shows that the charging gives rise to a voltage error at the sensing node.

The total amount of charge transferred by charging over the time is given by:

$$Q_c(t) = \int_0^t i_c(\tau)d\tau.$$
(3-75)

where i_c is the charging current. The charging current is usually very small. For example, the leakage current of reversed-biased diode is much less than 10^{-13} A. When the capacitance is large, the effects of charging can often be neglected. However, in CMOS MEMS, because the capacitance is only about 20 fF, the charging may cause large error voltage. According to equation (3-75), the amount of charge displaced by charging, hence the charging error, is an integral over time. Therefore, uncontrolled charging may grow over time be become infinitely large, or equivalently, has an infinite dc magnitude as shown in Figure 3-14. In such cases, charging could saturate the circuit from the input. Charging with lower magnitude would cause the drift of circuit input bias point and input capacitance, and result in variations of sensitivity and gain. Other than swamping the circuit, charging induced voltage error has another effect that might cause system failure. The charging could give rise to an electrostatic force between sensing fingers. With larger charging error, the large force might cause the fingers to snap. Smaller charging induced force will be sensed and give an error output.

The continuous-time voltage readout circuit is particularly vulnerable to charging. Without a dc virtual ground, the input sensing nodes have very high impedance all the time, hence is particularly sensitive to charging. In a continuous-time voltage sensing circuit, the sensing nodes must be provided robust dc biasing to prevent the charging. In the

next chapter, we will show that by combining continuous-time operation and reset, robust continuous-time voltage sensing could be realized.

3.5 Summary

This chapter provides a thorough analysis of nonidealities in capacitive sensing in fF-range and lays a theoretical foundation for the circuit implementation we will describe in the next chapter. A model of electronic noise is presented. This model reveals the strong frequency dependency of the noise. It also suggests that the input-referred noise could be minimized by choosing input transistor size to achieve optimum capacitance matching at each frequency. A review of capacitive sensing circuit architectures is given and noise folding in these architectures is analyzed. It concludes that continuous-time voltage-mode sensing has superior noise performance over switched-capacitor readout and current-mode sensing. Finally, the origins and consequences of circuit offset, sensor position offset and undesirable charging, are described. These nonidealities could cause error signals much larger than the sensed signal and could block the useful signal if not suppressed.

Chapter 4

Chopper Stabilized Capacitive Readout Circuit

A CMOS chopper stabilized amplifier for capacitive readout of CMOS MEMS accelerometers is presented in this chapter. Based on the analyses in the previous chapter, a set of circuit techniques are applied to an open-loop continuous-time voltage amplifier to minimize noise, offset and charging. This circuit uses chopper stabilization to reduce frequency-dependant noise and dc offset, and uses capacitance matching to minimize input-referred noise floor. Periodic reset is used to establish robust dc bias at the sensing nodes and prevent undesirable charging, while the circuit as a whole operates in continuous time. A differential difference amplifier (DDA) topology is employed for offset compensation, wherein the circuit offset are cancelled by dc feedback and the sensor offset are cancelled by ac correction signal. Integrated with a CMOS MEMS accelerometer, the circuit achieves 50 µg/rtHz input-referred noise floor with only 0.4 fF/g acceleration-induced capacitance change. The measured total noise is close to the Brownian noise floor. This device achieves one of the lowest noise floor results ever reported in thin-film MEMS accelerometers.

This chapter consists of five sections. Section 4.1 introduces the circuit architecture. Section 4.2 describes the detailed circuit design. Section 4.3 and 4.4 present the chip implementation and experimental results. Section 4.5 is the summary.

4.1 Circuit Architecture

MEMS capacitive sensor interface circuits have been primarily implemented by switched capacitor (SC) circuit because of its robustness and its capability of compensating sensor offset [9, 11 - 15, 43]. However, for ultra-small capacitance sensing applications such as in CMOS MEMS technology, the SC implementation becomes more and more difficult and is fundamentally limited by kT/C noise. Electronic noise is currently the dominant noise source in most surface micromachined inertial sensors. To advance the noise performance with shrinking device size, alternatives to the SC readout scheme must be investigated.

In CMOS MEMS technology, with low capacitance (20 fF x 4) and low sensitivity (< 0.4 fF/g and 1 mV/g), sensors are more susceptible to noise, offset, charging and other nonidealities. The signal-to-noise ratio (SNR) is more sensitive to the capacitance matching of the sensor, the interconnect and the interface circuit. Therefore, the interface circuit design for CMOS MEMS sensors is challenging and the noise optimization is necessary.

4.1.1 Choice of Circuit Architectures

An open-loop continuous-time voltage readout architectures is used in this work. As shown in the previous chapter, by reducing noise folding, continuous-time voltage readout is superior in noise performance over switched-capacitor charge integration and TIA-based current sensing.

There are two ways to implement continuous-time voltage sensing: capacitive feedback amplifier [6, 16] and open-loop voltage amplifier [17, 23]. The main advantage of feedback topologies including SC circuits and TIAs is that a virtual ground is provided so

that sensed signal is insensitive to parasitic capacitance. This advantage is crucial in many technologies where the wiring capacitance is large and has large variations. For example, some polysilicon MEMS processes use diffusion as interconnect layer between sensors and circuits, which has very large temperature variations. However, although a virtual ground ensures the parasitic insensitivity of the signal, the noise is still parasitic sensitive and follows the analysis in section 3.1. Thus, feedback topologies can only reject variations, but cannot improve the signal-to-noise ratio (SNR). The main disadvantage of the feedback topologies is that in order to maintain an ac virtual ground at the clock frequency, the circuit must has bandwidth considerably greater than the clock frequency. Therefore, in order to obtain the same gain, the feedback topologies are less efficient in power and area compared to open-loop topologies. Furthermore, in the case of SC circuits and TIA circuits, more bandwidth results in more noise folding, hence, degrades the noise performance.

In CMOS MEMS technology, metal interconnection is used to connect the sensor to the circuit. Hence, both the scale and the variation of the parasitic capacitance are considerably smaller than most other MEMS technologies. We can therefore afford to use open-loop topology to achieve better power and area efficiency. The main concerns for an open-loop continuous-time readout circuit are reliability and robustness because a dc virtual ground is not available. It is more difficult to control undesirable charging activities and the offsets of the sensor and the circuit. In particular, the reliable biasing of the high-impedance sensing nodes is a main challenge for continuous-time voltage readout.

4.1.2 Chopper Stabilization

Chopper stabilization is a noise reduction technique that modulates the signal to higher frequency where there is no dc offset and less 1/f noise, then demodulates it back to the baseband after amplification [45, 46, 47]. The reduction of noise and offset is depicted in Figure 4-1. The name of chopper stabilization was given more than 50 years ago when high-precision dc amplifier was realized by ac-coupled gain stages. Because the capacitance change must be detected with an ac source, modulation is natural for continuous-time capacitive sensing.

The circuit noise in capacitive accelerometers is frequency dependent. The minimum input-referred circuit noise floor decreases with the frequency and the thermal-mechanical Brownian noise is white. According to Figure 4-2, the circuit noise and the Brownian noise cross at modulation frequency between 1 - 2 MHz. Beyond this point, further increase of modulation frequency will not significantly reduce the total noise floor, while requiring the circuit to have higher speed and more power consumption. Thus, in this design, the circuit will be optimized to operate at 1 MHz modulation frequency.
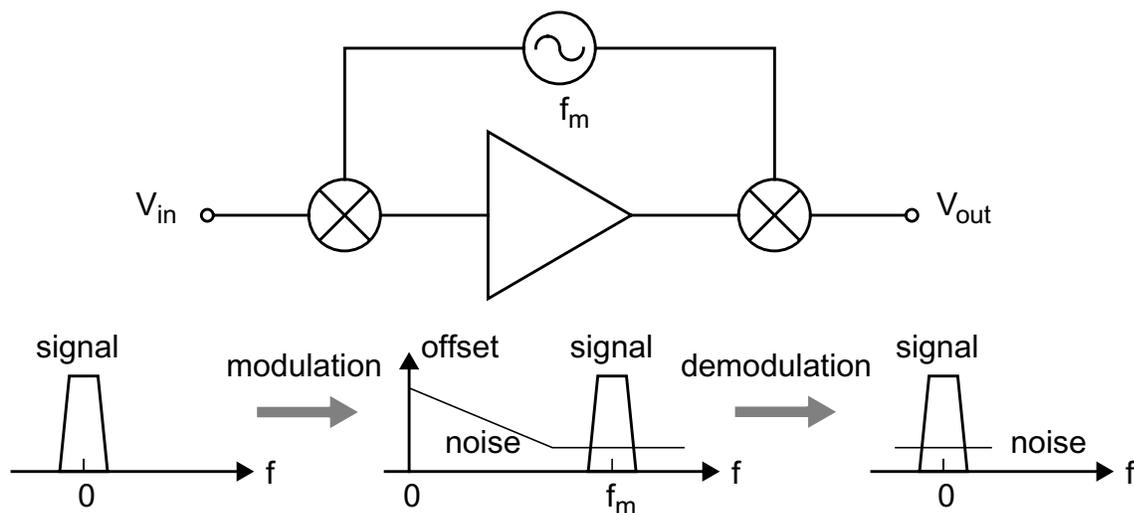

Figure 4-1: Chopper stabilization.
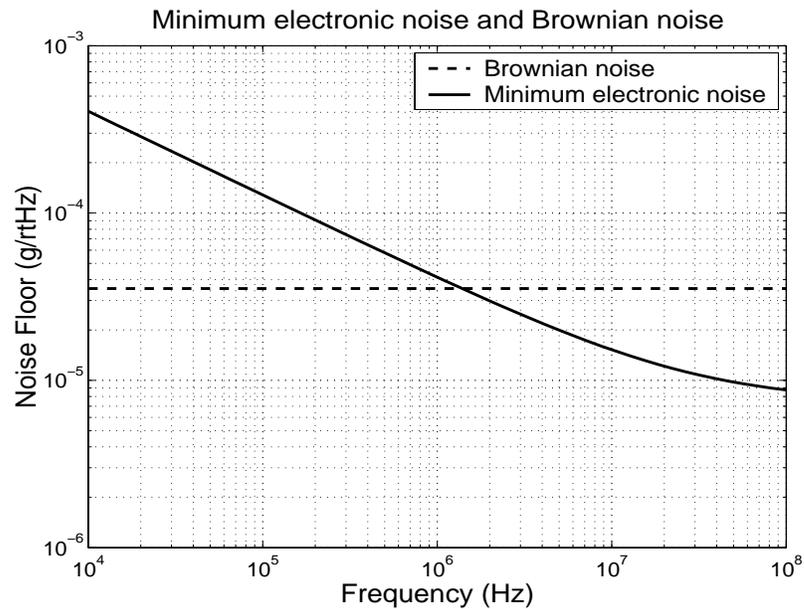
Figure 4-2: Minimum electronic noise and Brownian noise versus modulation frequency.

4.1.3 Circuit Architecture

The block diagram of the circuit architecture is depicted in Figure 4-3. To minimize the total noise, the continuous-time voltage readout method is used to reduce noise fold-ing; the chopper stabilization is employed to avoid large low-frequency noise; the signal paths on the sensor, and between the sensor and the circuit, are carefully laid out to mini-mize the interconnect capacitance; the circuit input is designed with minimum number of noise contributing devices and is optimized using the optimum capacitance matching; the fully differential topology is used to reject common-mode and power supply noise; and the modulation signals are generated on chip using clean dc source to minimize the noise in the modulation signals. Both the sensor position offset and the circuit offset are cancelled using a differential difference amplifier (DDA). And the effect of charging is minimized by a switching dc biasing method using reset.
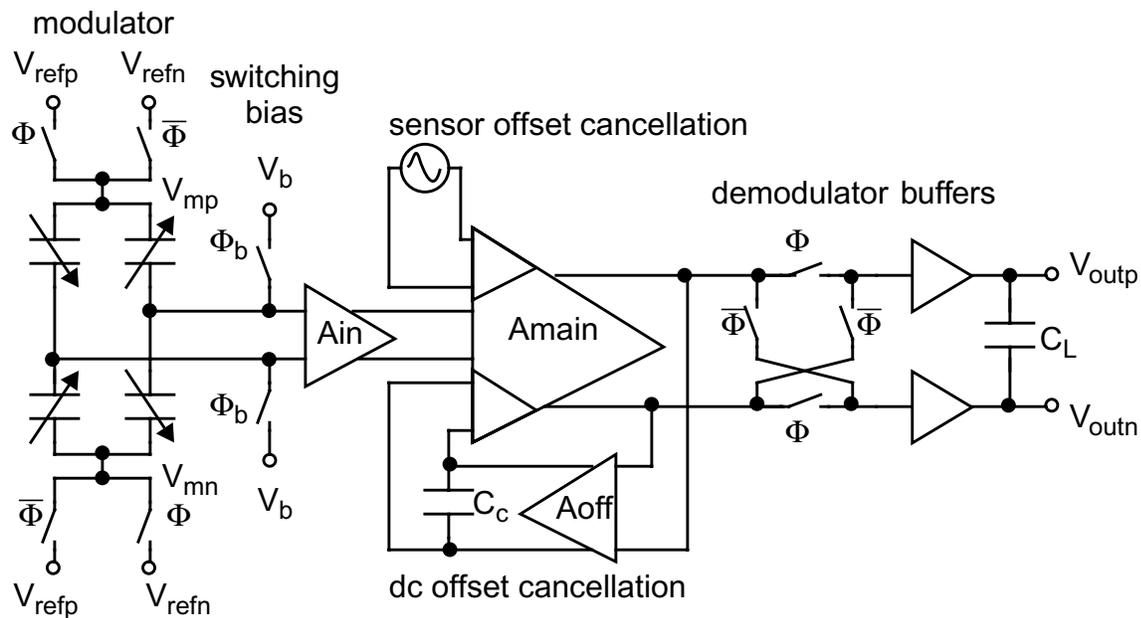
Figure 4-3: Block diagram of the fully differential chopper stabilized capacitive readout amplifier with switching input bias and dc/ac offset cancellations.

The entire signal path from the sensor to the output pads is fully differential. The chopper stabilization is provided by a pair of differential square-wave modulation signals generated by MOS switches using clean reference voltages from off chip. The dc bias at the input sensing nodes is established by turning on the MOS reset switches every 16 clock cycles to reset the input nodes to a clean dc voltage source. By releasing charge periodically, the effect of charging is minimized. A two-stage three-input wide-band differential difference amplifier (DDA) provides gain of 40 - 50 dB in 3-dB bandwidth greater than 3 MHz. In this two-stage architecture, the first buffer stage is optimized for noise performance, and the second gain stage provides the main amplification and offset cancellations. The amplifier has two auxiliary input ports for offset compensation. The dc circuit offset is cancelled by a dc feedback loop employing a narrow-band offset amplifier and a large off-chip capacitor. The ac signal is not affected by the loop due to its narrow bandwidth. The

electronic cancellation of sensor offset is realized by sensing an ac correction signal into another input port of the DDA. Because large gain is provided by the amplifier, a passive mixer is used to demodulate the signal. Figure 4-4 is a signal flow diagram of this circuit.

This circuit is to be fabricated by a digital CMOS process that does not provide high-quality passive components. One design goal is to avoid any on-chip passive components. The whole system uses only one off-chip capacitor for dc offset cancellation. In this design, an open-loop architecture which has large gain variation is adopted because by acknowledging that the sensor sensitivity has large manufacturing variation, there will not be much benefit to design a feedback amplifier with accurate gain. The open-loop topology avoids the use of large and accurate feedback resistors or capacitors which are not available in most digital CMOS processes. This topology also makes it possible to provide
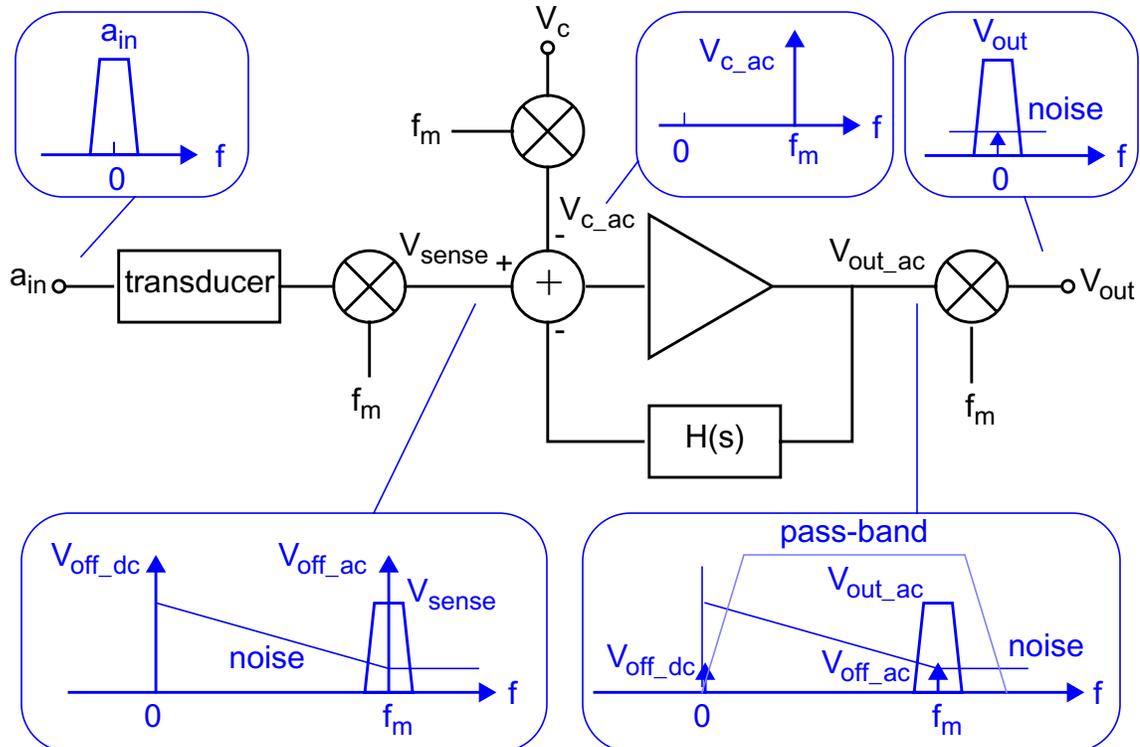
Figure 4-4: Suppression of low frequency noise, circuit offset and sensor offset.

sufficiently large gain in a single stage amplifier. Since most of the gain is provided by the

second stage of the DDA, the use of ac coupling that requires large capacitors is avoided,

the circuit design is simplified, and the silicon area is reduced. The accuracy of the system

scale factor can only be obtained by enclosing the transducer in a feedback loop and then

trimming or calibrating the closed-loop system. The open-loop readout amplifier

described in this chapter provides a low-noise front-end for such a system.

4.1.4 Modulation and Input Biasing

Figure 4-5 shows the schematic of the modulation generation and input biasing circuit.

The timing of the signals is shown in Figure 4-6. All clock signals are generated from a
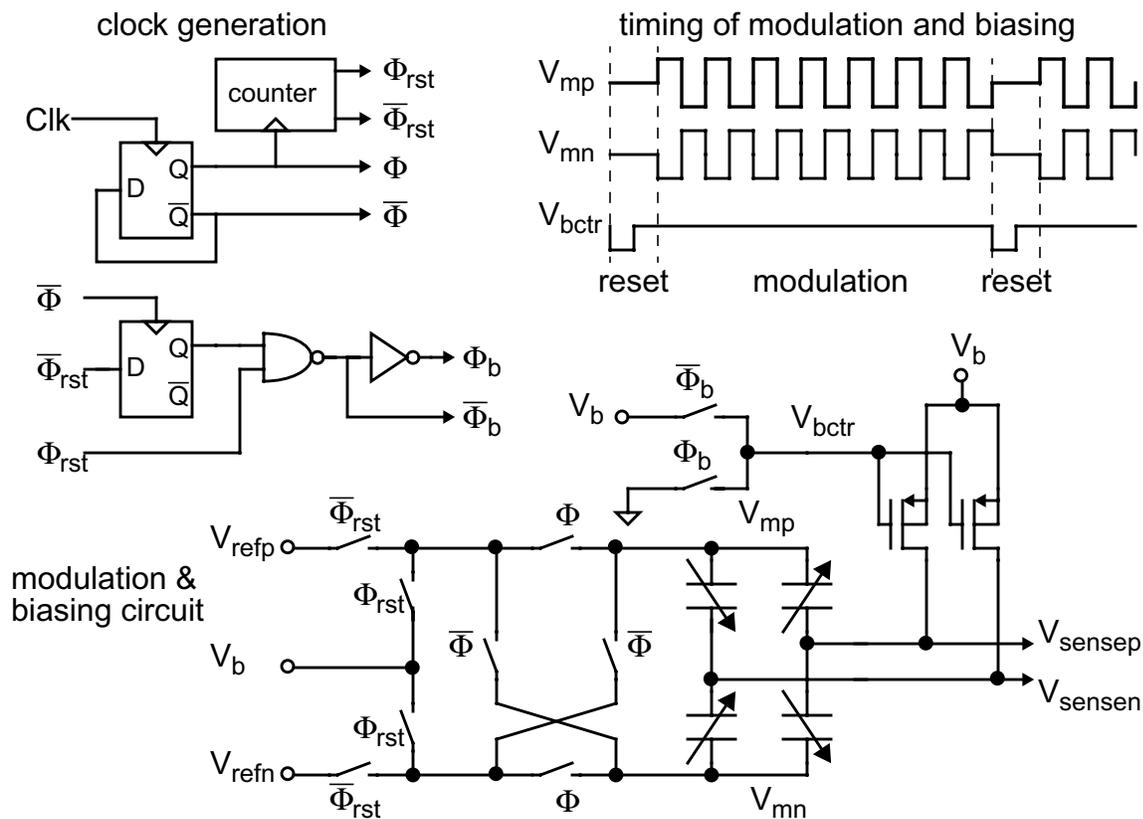
Figure 4-5: Schematic of the modulation generation and input biasing circuit.

single digital clock. This clock timing scheme is designed to prevent undesirable charging

and to eliminate charge injection error.

In a perfectly balanced differential capacitive bridge, the noise from the input modula-

tor will be completely cancelled. However in practice, the existence of the signal and the

offset, as well as the circuit mismatch, cause imbalance in the capacitive bridge, resulting

in leakage of modulation noise into the circuit input. To minimize the modulation noise,

the switches in the modulator are realized by large CMOS transmission gates, and clean dc

reference voltage sources with large bypass capacitors are used.
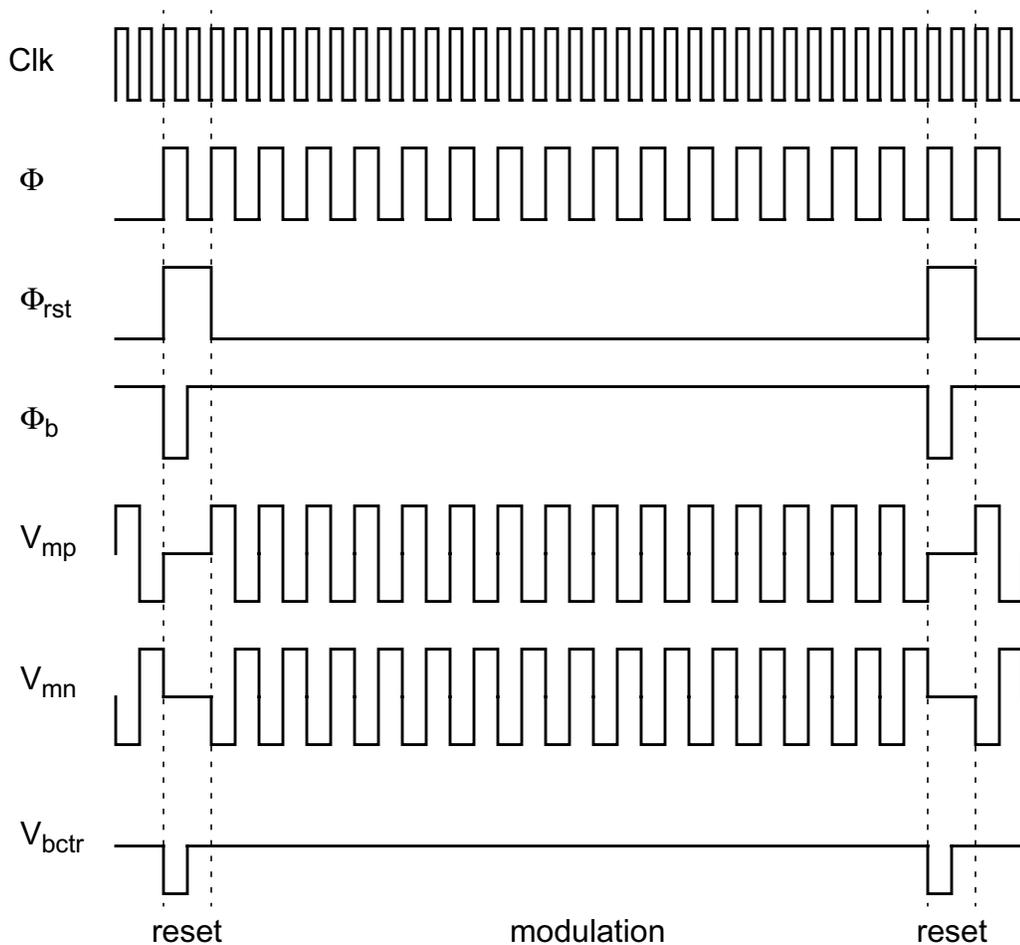
Figure 4-6: Timing diagram of clock, modulation and reset signals.

The purpose of the input biasing is to establish the dc voltage at the input nodes and to prevent unwanted charging activities. Every 16 clock cycles (8 cycles are shown in Figure 4-5 for simplicity), the bias MOS switch is turned on and connects the input sensing nodes directly to a dc voltage source. The periodic reset scheme re-establishes the dc bias voltage periodically and prevents caregiver accumulation. The sensed error voltage due to charging is given by:

$$V_{error} = \frac{Q_c(t)}{C_{sp} + C_{sn} + C_p},$$

(4-1)

where the total charge due to charging is given by:

$$Q_c(t) = \int_0^t i_c(\tau)d\tau.$$

(4-2)

As shown in (4-1) and (4-2), if we reset the dc bias often enough, we can reduce the time in which the charge is accumulated, hence minimizing the voltage drift caused by the charging. On the other hand, during most of the time, the bias switch is off and has negligible impact on the circuit operation. The periodic reset biasing scheme is more robust than the previous biasing methods using diodes and subthreshold MOSFETs and does not require any tuning. Because the reset frequency is far greater than the signal bandwidth, glitches and errors due to the reset could be completely filtered after demodulation, and would not affect the output signal.

In this switching bias scheme, two types of charge transfers occur to the sensing node during the reset. First, the dc voltage source charges the sensing node to the bias voltage as the MOS switches are on. Second, charge injection occurs when the MOS switches are instantaneously turned off. These charge transfers do not cause any errors in a perfectly balanced capacitive bridge. However in reality, a signal-dependent error may be intro-
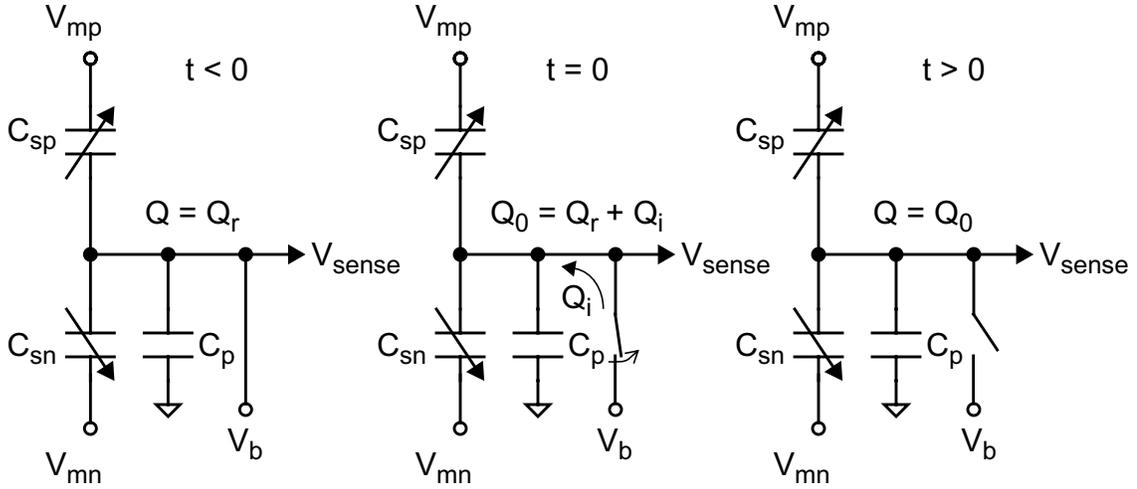
Figure 4-7: Total charge at the sensing node before, at and after the reset is turned off.

duced by the reset charge transfers as the balance is disturbed by the signal and the sensor position offset. To better understand this charge-related reset error, let us take a close look at the charge transfers in the capacitive bridge, as shown in Figure 4-7.

According to the analysis of charging in section 3.4, the sensed voltage is given by:

$$V_{sense}(t) = \frac{C_{sp}V_{mp}(t) + C_{sn}V_{mn}(t) + Q(t)}{C_{sp} + C_{sn} + C_p}. \tag{4-3}$$

Assuming there is no undesirable charging, based on charge conservation, the total charge $Q(t)$ on the sensing node at any given time should remain constant, being equal to the amount at the time when reset is just turned off, Q_0. When the reset has settled, and the reset switches and the modulation are still on, the voltages at the sensing node and the modulator inputs are:

$$V_{sense} = V_b,\ V_{mp} = V_b - V_M,\ V_{mn} = V_b + V_M. \tag{4-4}$$

And the total charge then is:

$$\begin{aligned} Q_r &= C_{sp}(V_b - V_{mp}) + C_{sn}(V_b - V_{mn}) + C_p V_b \\ &= (C_{sp} - C_{sn})V_M + C_p V_b \end{aligned}. \tag{4-5}$$

where V_b is the dc bias voltage, and V_M is amplitude of the square-wave modulation signal. At the moment when the MOS switches are turned off, an additional charge Q_i is injected. Therefore, the total charge after the reset is given by:

$$Q_0 = Q_r + Q_i = (C_{sp} - C_{sn})V_M + C_p V_b + Q_i, \qquad (4\text{-}6)$$

Using (2), the sensed voltage can be written as:

$$V_{sense}(t) = V_b + \frac{C_{sp} - C_{sn}}{C_{sp} + C_{sn} + C_p}V_m(t) + \frac{C_{sp} - C_{sn}}{C_{sp} + C_{sn} + C_p}V_M + \frac{Q_i}{C_{sp} + C_{sn} + C_p}. \quad (4\text{-}7)$$

The third term is a signal-dependent offset error and is a differential error in a fully differential sensor, as shown in Figure 4-8(a). The fourth term is a signal-independent offset error caused by the charge injection.

The signal-dependent reset error can be eliminated by disabling the modulation during the resident turning the modulation back on after the reset. In this case, instead of (4-3), the voltages after reset are given by:

$$V_{sense} = V_{mp} = V_{mn} = V_b. \qquad (4\text{-}8)$$

Therefore, the sensed voltage is:

$$V_{sense}(t) = V_b + \frac{C_{sp} - C_{sn}}{C_{sp} + C_{sn} + C_p}V_m(t) + \frac{Q_i}{C_{sp} + C_{sn} + C_p}. \qquad (4\text{-}9)$$

The signal-dependent term no longer exists. The elimination of this error is shown in Figure 4-8(b). The charge injection error given by the last term is a common-mode error, thus, can be reduced by a fully differential sensor topology. The residual charge injection error is modulated at the reset frequency, thus, can be completely filtered after demodulation.
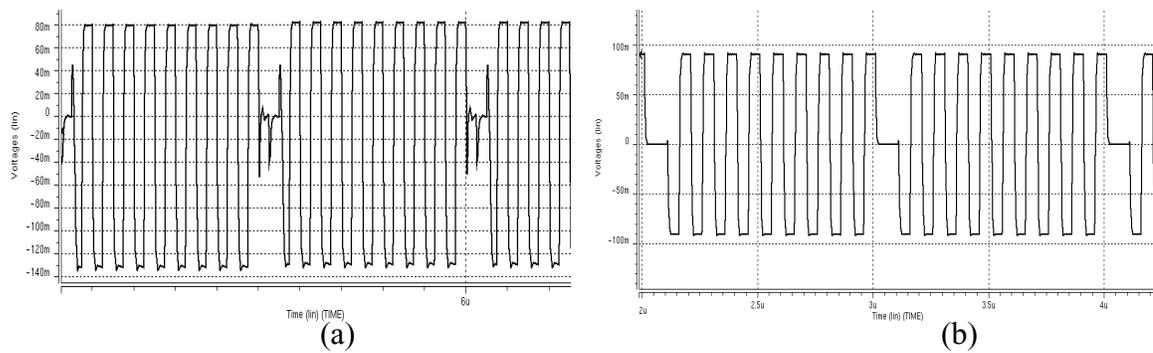
Figure 4-8: Charge error due to reset: (a) offset error with the modulation always on; (b) offset error is eliminated by turning off modulation during reset.

When the bias switches are turned off, the drain current in the subthreshold MOS switches changes the amount of charge on the sensing nodes, hence causing voltage drift. The drain current is a combination of the leakage current across the reverse-biased drain-base junction, and the subthreshold drain-source current. Because in the off-state, the gate voltage is much lower than the threshold voltage and there is no source to provide sustained current to the drain, the subthreshold current is insignificant. The junction leakage current is a main source of charging. In addition, the leakage current gives rise to the shot noise at low modulation frequency.

The leakage current across the drain-body junction is typically very small, in the range of 10^{-15} - 10^{-14} A/um^2, for most CMOS processes. However, early experiment results indicate the leakage in the process we are using, may be much worse due to the low quality of the drain-body junction. Therefore, careful attention is paid during the design to minimize the leakage of bias switches. In a N-well CMOS process, NMOS transistors could have relatively large leakage current because its base is the substrate that is fixed at the ground. There exists a potential up to a few volts across the reverse-biased diode formed by the N+ source and the P- substrate. The leakage of PMOS transistors can be made smaller by

tying up the source and the N-well body. As shown in Figure 4-9, body, source and drain are all biased at the same voltage, and there is approximately zero potential between the drain and body. According to equation [48]:

$$I_{db} = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)\left(\exp\left(\frac{qV_{db}}{kT}\right) - 1\right), \tag{4-10}$$

where D_p and D_n are the carrier diffusion coefficients, L_p and L_n are the average diffusion lengths, p_n and n_p are the minority carrier concentrations, and A is the junction area, the drain-body leakage current is minimized by zero drain-body voltage. For this reason, PMOS transistors with tied source and body are used as the bias reset switches. The sizes of these switches are kept minimum for two reasons: to reduce the temperature-dependent parasitic capacitance, and to reduce the junction area hence the junction leakage.
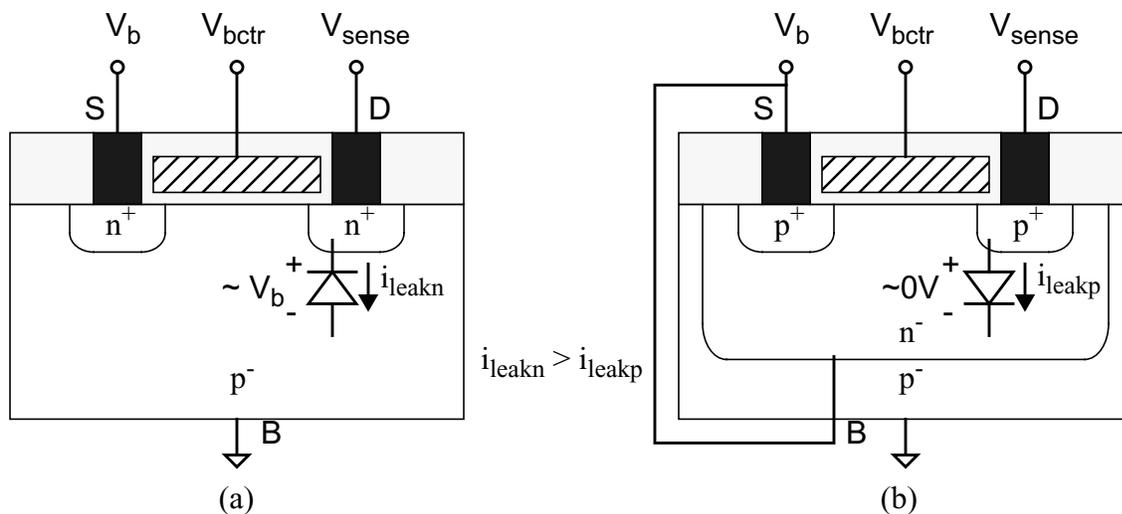
Figure 4-9: Leakage in bias switch: (a) NMOS switch; (b) PMOS switch with source connected to the body.

4.2 Circuit Design

The schematic of the two-stage three-input DDA is shown in Figure 4-10. This amplifier consists of two stages so that design optimization can be performed separately. The input buffer stage is optimized for noise performance. The second gain stage provides main amplification and dc/ac offset cancellations and is optimized for gain and bandwidth. Gain around 35 dB is provided by the open-loop operational transconductance amplifier (OTA) in the second stage. This configuration requires no on-chip passive components, simplifies the circuit design and minimizes the silicon area, but at the expense of relatively high power dissipation.
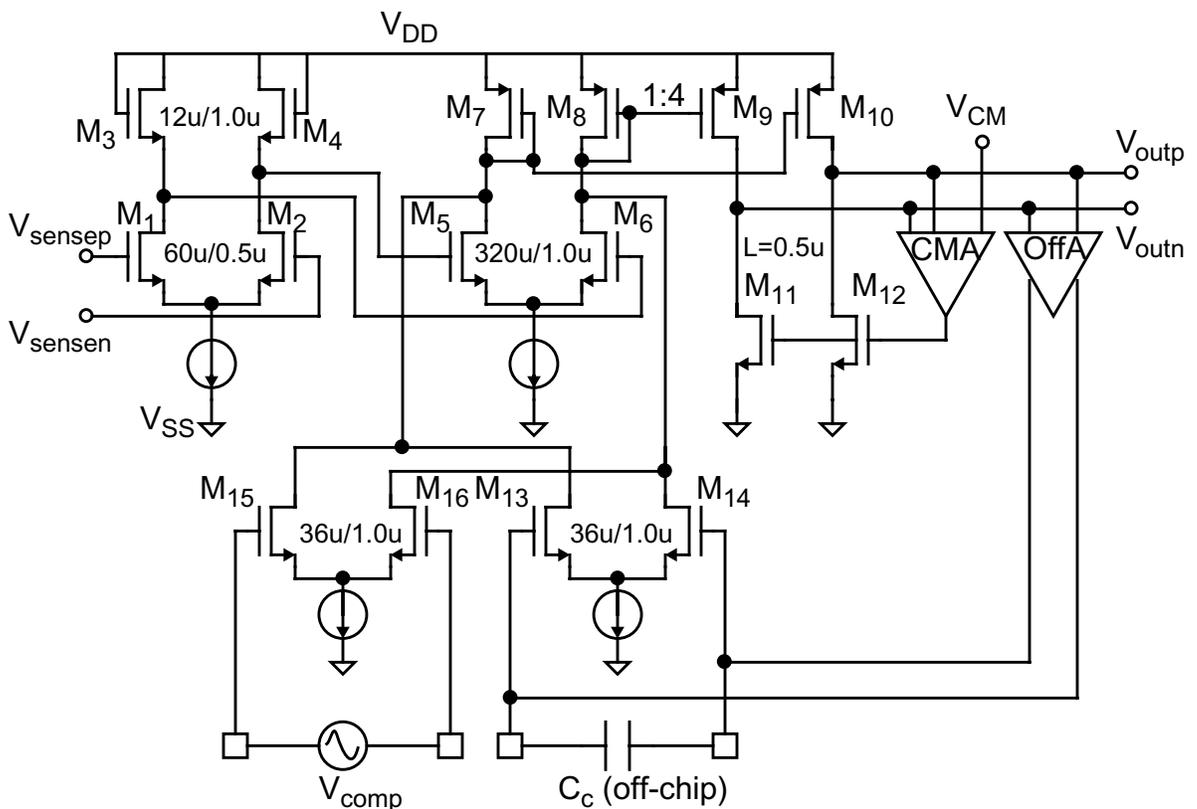
Figure 4-10: Schematic of the two-stage wide-band differential difference amplifier with offset cancellation.

The two-stage topology is preferred to the single-stage topology with cascode devices for the following reasons. First, the noise optimization requires the input transistors to have small size, therefore, they do not have sufficiently large transconductance to drive the entire high-gain wide-band amplifier. Second, the two-stage topology makes it easy to implement offset compensation and minimizes the noise contributed by offset compensation circuits. Finally, a low-gain input stage could achieve four goals at once: minimizing the number of main noise contributing devices; amplifying signal to attenuate noise from the following circuits; limiting gain to prevent large sensor position offset from saturating the circuit from the beginning; limiting gain to reduce Miller effect.

4.2.1 Input Stage Noise Optimization

The buffer stage is a simple differential low-gain amplifier. Due to their high carrier mobility, NMOS transistors have higher transconductance, lower thermal noise and higher 1/f noise corner than PMOS transistors of the same size. Although the PMOS transistors have lower 1/f noise corner, calculations conclude that NMOS transistors achieve lower total input-referred circuit noise floor. Hence, NMOS transistors are used as input devices. The diode-connected NMOS transistors are used as the load device so that the circuit has a predictable gain determined by the ratio of transconductances

$$A_{in} = g_{m1}/g_{m3}. \tag{4-11}$$

The gain is designed to be about 3.3 in order to attenuate the noise from following stages by a factor of 10. The minimum channel length of 0.5 μm is used for input transistors to minimize the gate capacitance. Based on the noise analysis in the previous chapter, the input-referred noise from the input MOS transistor is given by:

$$\overline{a_n^2}(f) = \overline{a_{ntherm}^2}(f) + \overline{a_{nflicker}^2}(f)$$

$$= \frac{K_T T(1 + c_1 W + c_2 WL)^2}{W^\beta L^{\beta-1}} + \frac{K_F(1 + c_1 W + c_2 WL)^2}{WLf} \cdot \qquad (4\text{-}12)$$

The width of the input transistors is chosen to minimize the input-referred noise. The 60 μm channel width is relatively small compared to the transistor sizes in conventional low noise amplifiers.

The noise contributions by the load devices at the input sensing nodes are given by

$$\overline{v_{n3}^2} = \frac{\overline{i_{n3}^2}}{g_{m1}^2}$$

$$= \frac{\overline{i_{ntherm3}^2}}{g_{m1}^2} + \frac{\overline{i_{nflicker3}^2}}{g_{m1}^2}$$

$$= \frac{4kT g_{m3}}{g_{m1}^2} + \frac{K_f L_1}{2\mu_n C_{ox}^2 W_1 L_3^2 f} \qquad (4\text{-}13)$$

$$= \overline{v_{ntherm1}^2} \cdot \frac{g_{m3}}{g_{m1}} + \overline{v_{nflicker1}^2} \cdot \frac{L_1^2}{L_3^2}$$

Given a gain of 3.3, the thermal noise of the load devices is 1/3.3 of that of the input transistors. The 1/f noise of the load transistors is reduced to 1/4 by using 2x larger channel length of 1.0 μm.

4.2.2 Differential Difference Amplifier Design

With a preceding buffer stage, the main gain stage can be optimized to achieve higher gain and bandwidth with less constraints. This stage is a three-input DDA with a wide-band operational transconductance amplifier (OTA) topology. The OTA is designed to
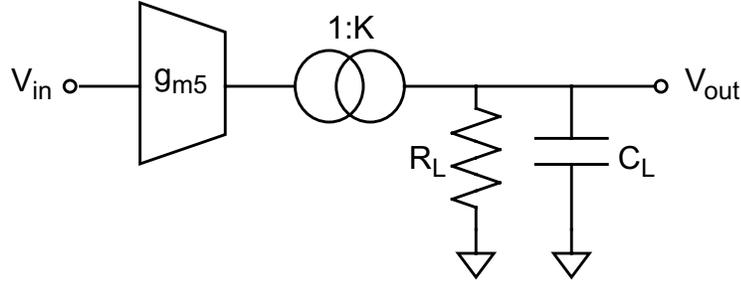
Figure 4-11: Simplified schematic of main signal path in the 2nd stage OTA.

have a gain around 35 dB in the main signal path, a 3-dB bandwidth greater than 3 MHz

and a reasonable output swing range of at least 2.5 V under 5 V supply.

A simplified diagram of the main signal path in the second stage OTA in shown in Fig-

ure 4-11. The voltage gain in the main signal path is given by:

$$A_{main} = Kg_{m5}R_L, \tag{4-14}$$

where g_{m5} is the transconductance of the 2nd-stage input transistor, K is the current gain of

the current mirror formed by M7-M10, and R_L is the load impedance. The current mirror

provides additional current gain by using $K = 4$. The 3-dB bandwidth of the OTA is given

by:

$$\omega_{-3dB} = \frac{1}{R_L C_L}. \tag{4-15}$$

The gain-bandwidth product of the amplifier is determined in part by g_m:

$$GBW = A_{main}\omega_{-3dB} = \frac{Kg_{m5}}{C_L}. \tag{4-16}$$

Thus, maximizing g_m not only improves the gain but also help improving the bandwidth.

The g_m of long channel transistors is:

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}. \tag{4-17}$$

To maximize g_m, the main input NMOS transistors M5 and M6 are NMOS transistors not only have large channel width of 320 μm, but also have 2x minimum channel length of 1 μm to prevent g_m loss caused by velocity saturation. The large input transistors also minimize both 1/f and thermal noise. The noise contribution of these devices is negligible compared to the buffer stage.

The OTA does not use any cascode devices in the output stage because high output resistance increases the RC constant and limits the 3-dB bandwidth. The output resistance is provided by the drain-source resistances of the output PMOS and NMOS transistors, M9 - M12:

$$R_L = r_{ds10} \| r_{ds12}. \tag{4-18}$$

This is shown in Figure 4-12.

Since the load capacitance is partially determined by the following circuits and the interconnection, the output resistance must be reduced to maximize the bandwidth, at the expense of gain loss. The large g_m provided by large M5 and M6 compensates the relatively low load resistance and maintains a reasonable gain.
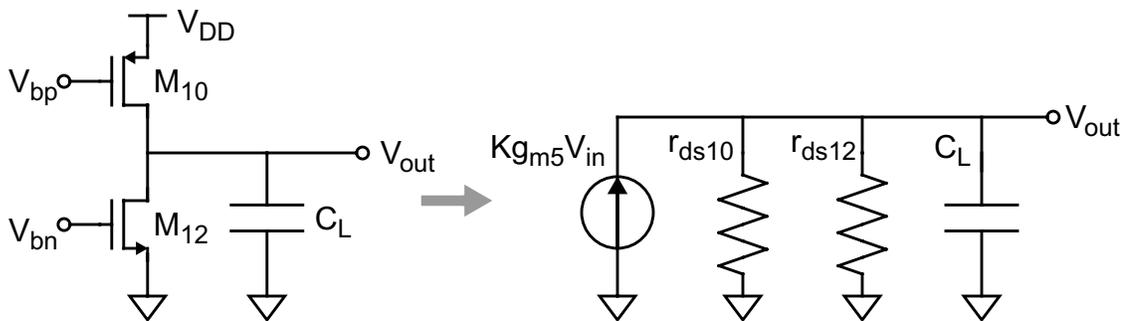

Figure 4-12: Output impedance of the single-stage OTA.

The drain-source resistance of MOS transistors is given by:

$$r_{ds} = \frac{\partial V_{ds}}{\partial I_{ds}} = \frac{V_A}{I_D}, \tag{4-19}$$

where V_A is the Early voltage. The finite output resistance is the result of two main physical mechanisms: channel-length modulation (CLM) and drain-induced barrier lowing (DIBL), both are functions of channel length:

$$r_{ds} = r_{dsCLM} \| r_{dsDIBL} = \frac{V_{ACLM}(L)}{I_D} \| \frac{V_{ADIBL}(L)}{I_D}. \tag{4-20}$$

The resistance due to CLM is given by:

$$r_{dsCLM} \propto \frac{L}{I_D}. \tag{4-21}$$

The resistance due to DIBL decreases more rapidly with shrinking length. The length of PMOS transistor M9 and M10 should be at least 1 µm to obtain high output impedance and accurate current gain of the current mirror. Therefore, minimum channel length is used in NMOS transistors M11 and M12, and the OTA output impedance is mainly determined by these two transistors.

The majority of the total bias current is supplied to the output stage to boost the gain and improve the speed. The current mirrors of M7 - 10 have 1:4 current ratio ($K = 4$). The CMOS process used to fabricate this chip is not particularly suitable for implementing high-speed circuit, and the use of the top layer metal as etch mask further increases the parasitic capacitance. The output stage requires 4 mA bias current to obtain the proper output resistance. And the large current ratio K help to boost the gain by compensating the lowered resistance R_L. Thus, total of 5 mA current is consumed to achieve gain about 35 dB in 3 MHz bandwidth.
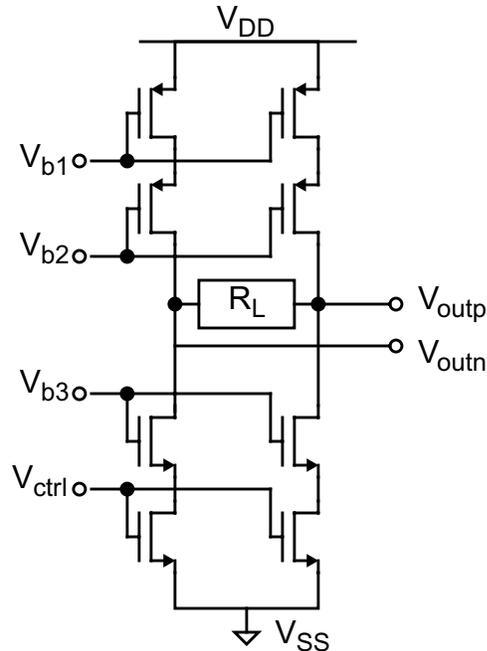
Figure 4-13: Alternative implementation of the wide-band amplifier.

A low-power alternative without the use of passive components is to use MOS resistor as the differential output load, as shown in Figure 4-13. By having low output impedance, two cascade gain stages are needed instead of one. The main difficulty is that the MOS resistor must have large linear range to ensure good output swing. Since power dissipation is not a major concern in this project, the simple open-loop OTA is used in implementation. This circuit achieves output swing range greater than 3 V.

In the DDA, two auxiliary input pairs are included for offset control. For large offset compensation range, the current supplied to the compensation input ports must be comparable to the current consumed by the main input pair. The inclusion of the compensation input pairs reduces the gain in the main signal path, but helps to improve the bandwidth as more current is poured into the output stage. The noise contributed by the auxiliary input transistors referred to the main signal input is given by:

$$\overline{v_{n13 \to 5}^2} = \frac{\overline{i_{n13}^2}}{g_{m5}^2}$$

$$= \frac{\overline{i_{ntherm13}^2}}{g_{m5}^2} + \frac{\overline{i_{nflicker13}^2}}{g_{m5}^2}$$

$$= \frac{4kT g_{m13}}{g_{m5}^2} + \frac{K_f L_5}{2\mu_n C_{ox}^2 W_5 L_{13}^2 f} \qquad (4\text{-}22)$$

$$= \overline{v_{ntherm5}^2} \cdot \frac{g_{m13}}{g_{m5}} + \overline{v_{nflicker5}^2} \cdot \frac{L_5^2}{L_{13}^2}$$

Therefore, these MOS transistors should have small g_m and large channel length to minimize their noise contribution. In this design, the auxiliary input transistors have considerably smaller channel width hence smaller transconductance than the main input transistors. Since the flicker noise of the second stage is negligible compared to the input stage, channel length of 1.0 μm is used in the auxiliary input transistors to reduce the die area. As result, the voltage gains of compensation signals are much smaller than the main signal gain. which is not a problem for offset cancellation. Therefore, the output voltage of the two-stage DDA is given by:

$$V_{out} = A_{in} A_{main} V_{in} + A_{aux} V_{dccmp} + A_{aux} V_{accmp}$$

$$= K \frac{g_{m1}}{g_{m3}} g_{m5} R_L V_{in} + K g_{m13} R_L V_{dccmp} + K g_{m15} R_L V_{accmp} \qquad (4\text{-}23)$$

4.2.3 Offset Cancellations

The circuit offset appears as a dc signal. Chopper stabilization separates the ac signal and the dc offset in the frequency domain, therefore, the offset can be minimized by blocking the dc signal path. To avoid the use of on-chip coupling capacitors, a dc feedback loop
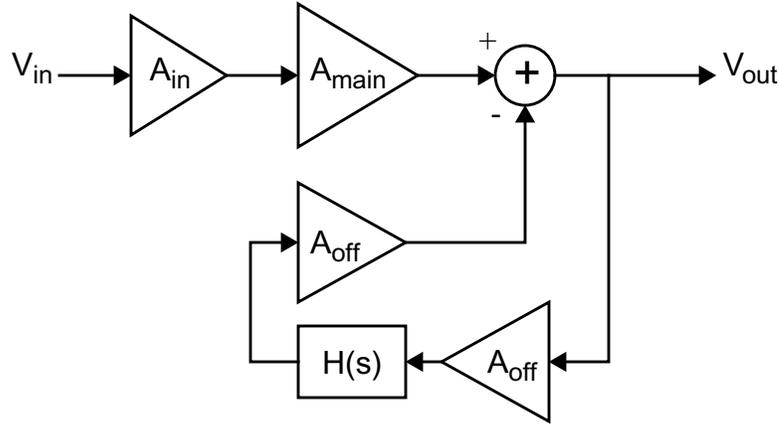
Figure 4-14: Block diagram of the 2-stage amplifier with dc feedback.

is employed to cancel the circuit offset. Figure 4-14 is the block diagram of the 2-stage amplifier with dc feedback.

In Figure 14, the closed-loop transfer function of the feedback loop is:

$$T(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{A_{in}A_{main}}{1 + A_{aux}A_{off}H(j\omega)}. \tag{4-24}$$

If a low-pass filter is used, the system has a high-pass frequency response. The dc gain is given by

$$A_{dc} = \frac{A_{in}A_{main}}{1 + A_{aux}A_{off}}. \tag{4-25}$$

while the high-frequency gain is:

$$A_{ac} = A_{in}A_{main}. \tag{4-26}$$

By using the high-frequency gain as the reference, the input-referred dc offset is found to be reduced by a factor of $1 + A_{aux}A_{off}$.

An on-chip narrow-band offset amplifier and a large off-chip capacitor provide the low-pass filtering to ensure that only the low frequency signal is attenuated and the modu-

lated sensing signal is not affected. The schematic of the offset amplifier is shown in Figure 4-15. The offset amplifier directly drives a pad and is loaded with an 1 nF off-chip capacitor. With the feedback offset cancellation, the offset amplifier output is measured at 0.1 V, using designed gain values, the input-referred offset of the DDA is 10 µV.

Since the sensor offset appears as an ac signal and occupies the same frequency band as the desired signal, it can not be blocked by filtering. Thus, calibration is required to tune out this offset based on measurement. In this circuit, the electronic cancellation of the sensor offset is provided by sending an ac correction signal into the second auxiliary input port. In this implementation, the ac correction signal is generated off-chip using the same clock signal and modulation scheme. By supplying sufficient current into the ac compensation pair, the electronic sensor offset cancellation provides much larger compensation range than the mechanical method using electrostatic actuators. It not only avoids the high voltage and related reliability issues, but also pull the high-offset devices which are previous regarded as failed devices back into usable region.
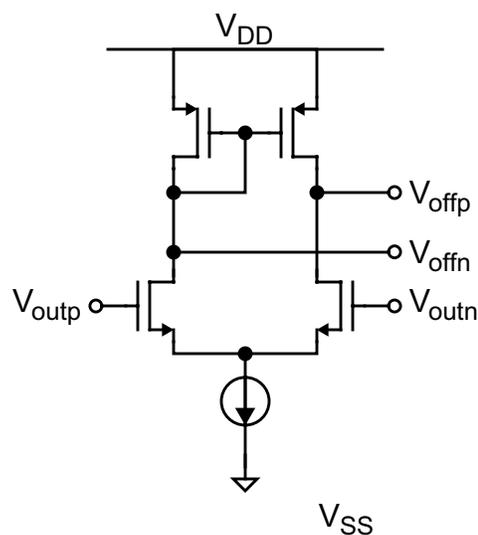

Figure 4-15: Narrow-band offset amplifier.
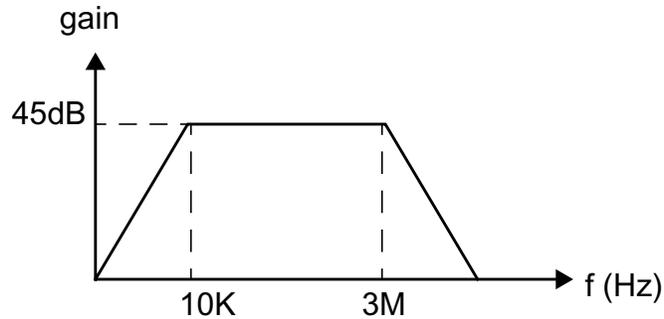
Figure 4-16: Amplifier frequency response.

As shown in Figure 4-16, the amplifier has a band-pass frequency response in which the lower frequency corner is determined by the dc feedback loop, and the high frequency corner is limited by the circuit output resistance and the load capacitance.

4.2.4 Common-Mode Feedback Circuit

The output of the DDA still has relatively high impedance and a common-mode feedback loop is needed to stabilize the output common-mode voltage. Unlike in most operational amplifier where the output impedance is very high, the dominant pole of the common-mode feedback loop cannot be provided by the wide-band amplifier which has 3 MHz 3-dB bandwidth. The common-mode amplifier (CMA) must provide the dominant pole while still being sufficiently fast to control high-frequency common-mode signals. The common-mode amplifier is shown in Figure 4-17. The CMA has much lower 3-dB bandwidth than the DDA itself and employs lead compensation to improve the unity gain frequency. The lead compensation using an on-chip capacitor and triode-region MOSFET resistor achieves greater than 80 degree phase margin and 60 MHz unity gain frequency, according to HSPICE simulations. To maximize swing range of differential signals, source degeneration with triode-region MOSFET resistor is used in this CMA design. The DDA has 3V output swing range under 5V supply.
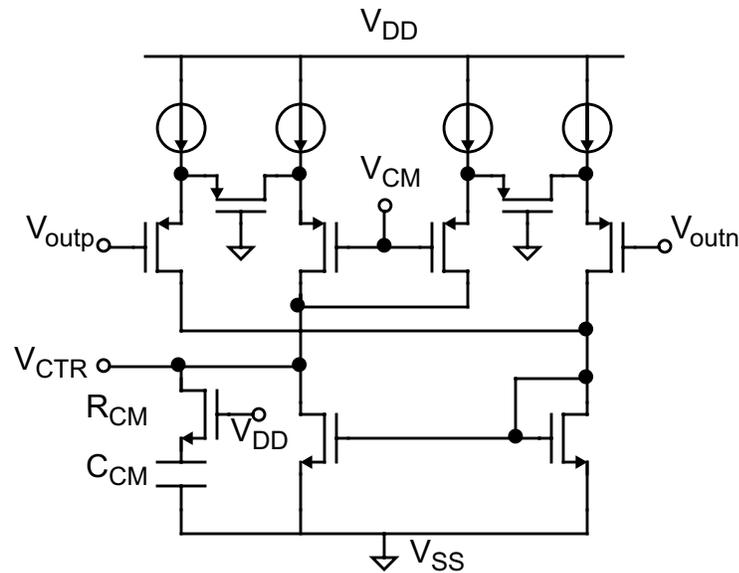
Figure 4-17: Common-mode amplifier with source degeneration and lead compensation.

4.2.5 Biasing Circuit

Cascode current mirrors are used in both stages of the DDA to boost the output imped-
ance of the tail current sources, thereby improving the common-mode rejection ratio
(CMRR) and power supply rejection ratio (PSRR) of the differential amplifier. The current
biasing of the entire circuit is provided by the bias circuit shown in Figure 4-18. To main-
tain the voltage headroom, NMOS wide-swing cascode current mirror are used for tail
current sources. Simple NMOS and PMOS mirrors are also used to bias various buffers.
Because we intended to study the effects of bias current on the noise performance, instead
of using an on-chip bandgap reference, an off-chip programmable current source is
employed to provide the reference current.

Figure 4-18: Bias network with off-chip adjustable current source.

4.3 Implementation of Integrated CMOS MEMS Accelerometer

An integrated CMOS MEMS dual-axis accelerometer prototype chip was implemented. This chip includes three regular-size accelerometers in two orthogonal orientations and one larger accelerometer. The design of CMOS MEMS accelerometers is detailed in chapter 3. Each of the sensors is integrated with an on-chip capacitive readout amplifier just described. All four integrated sensors share the same clock generation circuit and the bias circuit.

Because the interconnect capacitance directly affects the noise floor, the signal paths on the sensor, and between the sensor and the circuit, are very carefully laid out to minimize the interconnect capacitance. On the sensor, the signal paths are located on the outer frame which is more than 20 μm above the substrate. In the 3-metal process, due to the top metal shield and silicon undercut, the lowest metal layer is used to carry signals between

the sensor and the circuit to minimize the interconnect capacitance. Windows are placed in the top metal shield above the signal lines to further reduce the capacitance between the metal1 lines and the metal3 shield. In the circuit, careful attention is paid to the symmetry of the differential signal paths throughout the layout. All circuits are shielded by guard rings, and the signal paths are carefully isolated from lines of power supply, clock signals and actuator drive signals. The power supply is distributed by a star network to minimize the interferences between circuit blocks. The top layer metal shield is connected to a clean ground separated from Vss. And long analog signal lines are placed above N-well shield that is also connected to the clean ground. These measures, in addition to the high CMRR and PSRR design, minimize the influences of power supply noise, substrate noise, cross talk, and outside interferences. Because the process is not very good for implementing high-speed circuits, and the grounded top layer metal mask increases the parasitic capacitance, buffers are inserted in various places to drive on-chip and off-chip loads.

The prototype chip was fabricated in Agilent 0.5 μm 3-metal 1-poly N-well CMOS process. The MEMS structures were released by SiO_2/Si dry etching. The CMOS MEMS processing was performed in CMU cleanroom. The die size is 3.5 mm by 2.5 mm. Figure 4-19 shows the layout and the die photograph of the chip. Figure 4-20 shown the SEM of the released and bonded die and the close-up view of the CMOS MEMS accelerometer. To protect the circuits in the MEMS processing, the circuit area is covered by the top metal layer and can not be seen in the die photo and the SEM. The layout of the readout amplifier is shown in Figure 4-21.
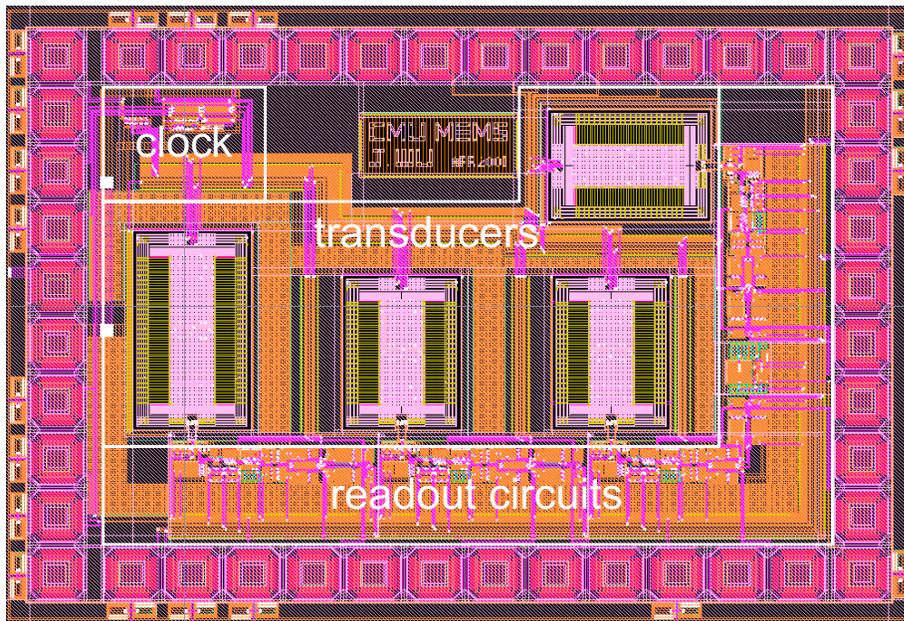
(a)
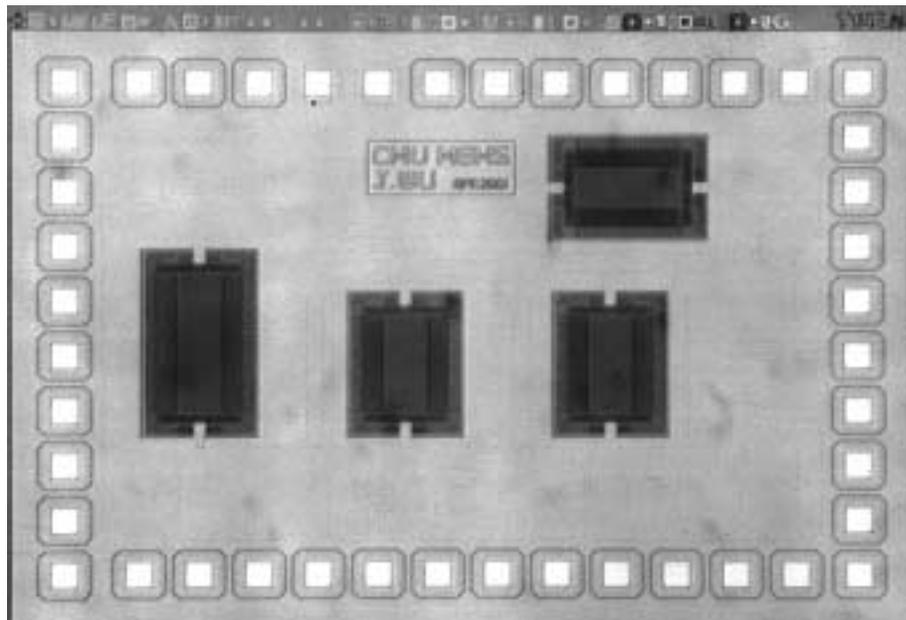
(b)

Figure 4-19: Chip implementation: (a) chip layout showing the circuit area; (b) micrograph of the unreleased die with circuit covered by top metal layer.
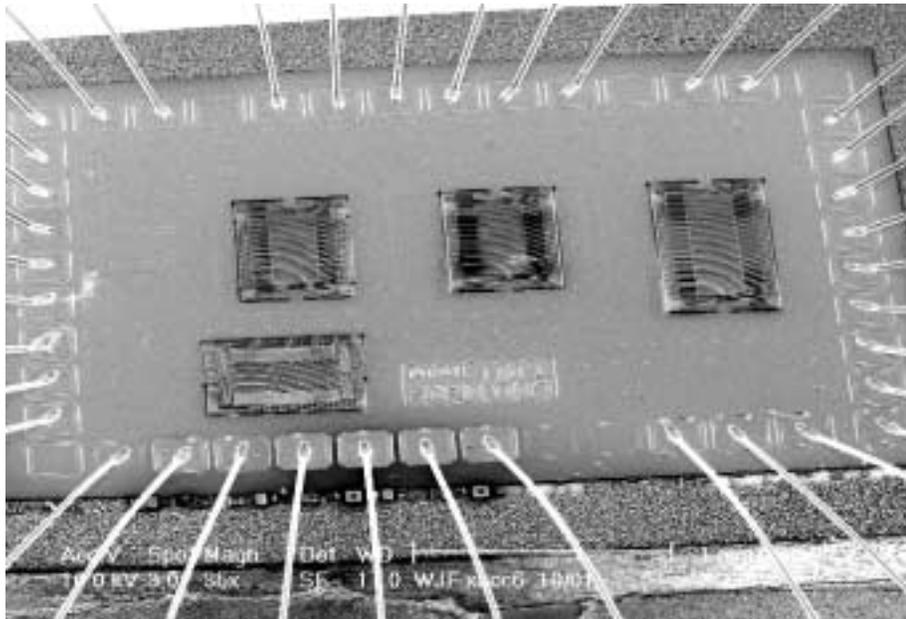
(a)
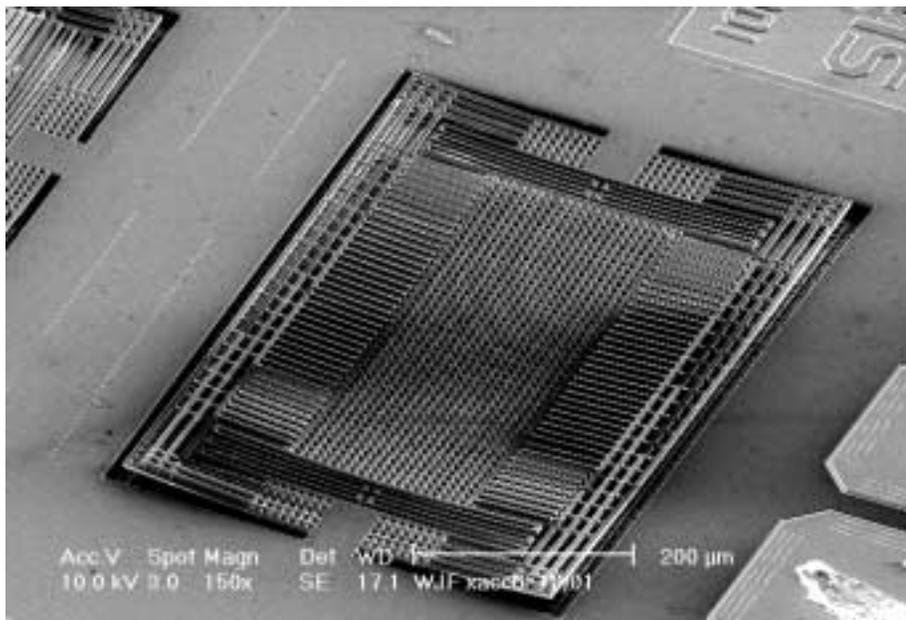
(b)

Figure 4-20: Scanning electron micrograph of: (a) the die after MEMS post-processing and wire bonding; (b) one of the four lateral accelerometers.
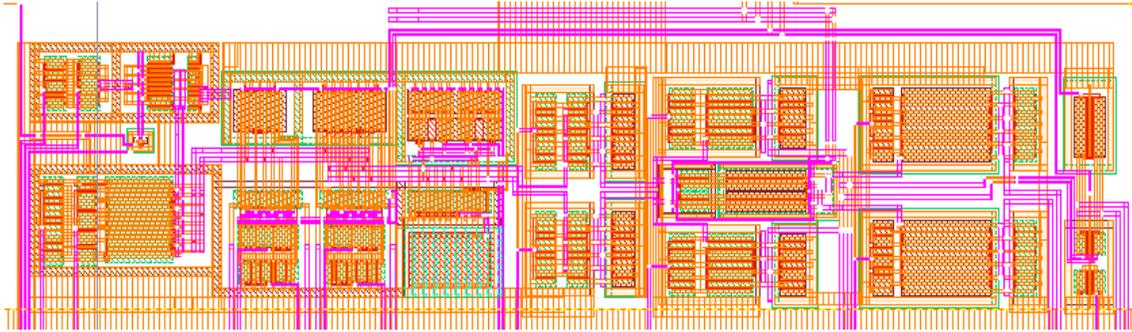
Figure 4-21: Layout of a chopper stabilized capacitive sensing amplifier.

4.4 Experimental Results

4.4.1 Experiment System

A photograph of the experiment setup for acceleration measurement is shown in Figure 4-22. The prototype chip is tested on a vibration table. This vibration table generates a single-frequency acceleration signal.

The die is attached on a 40-pin DIP package and wire-bonded. The package is mounted on a small adaptor board which is mounted on the vibration table during the experiment. The measurements take place on the main test board off the vibration table. Power supply, dc bias and clock signals are also fed in or generated on the test board. A shielded 40-connector ribbon cable is used to carry signals between the test board and the adaptor board.

On the main test board, a low-noise instrumentation amplifier converts the differential output signals from the test chip into a single-ended signal. Measurement is performed at
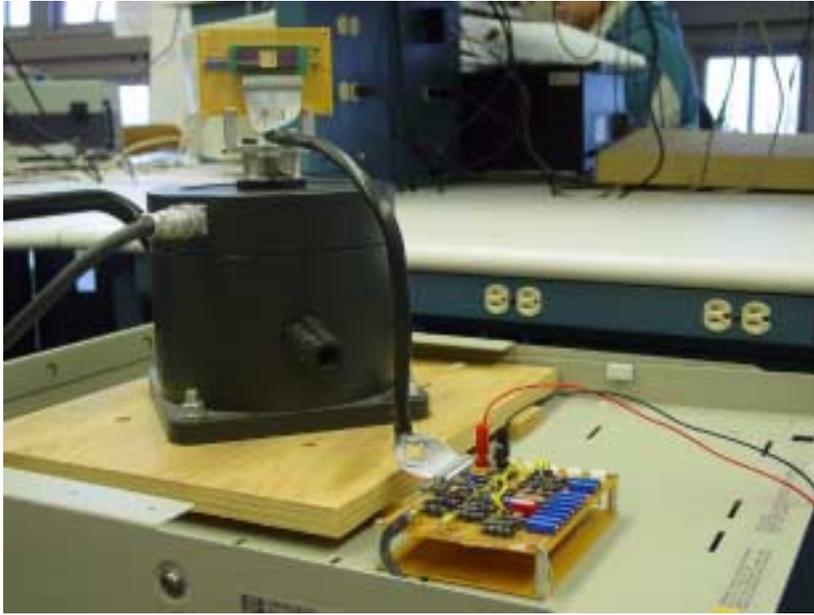
Figure 4-22: Test setup for acceleration measurement.

the output of the instrumentation amplifier so that differential probes are not needed. The instrumentation amplifier has programmable gain in the range of 2 - 50. Since noise is the main objective of measurement, the gain is set to maximize the output signal magnitude so that the measurement noise can be minimized. Since large signal gain is provided on chip, the noises from off-chip circuits and the measurement instruments are negligible.

A reference accelerometer is installed on the vibration table. The sensitivity of the reference signal is 1 V/g. By comparing the measured output signal to the reference, the sensitivity and the input-referred noise floor of the integrated CMOS MEMS accelerometer can be calculated.

4.4.2 Time-Domain Measurements

Figure 4-23 shows the measured output signal and the reference signal in response to a 0.5 g 400 Hz sinusoidal acceleration. The overall sensitivity of the test system is 3.2 V/g.

A gain of 25 is used in the off-chip amplifier. Therefore, the sensitivity of the integrated accelerometer is 130 mV/g.

The differential pre-demodulation signals are shown in Figure 4-24. The waveforms show the timing of the modulation and the reset, as well as the large signal transient
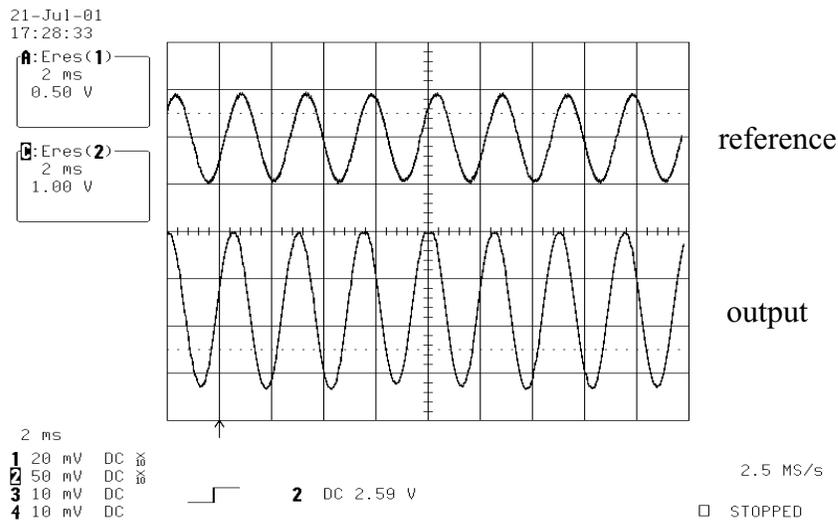
Figure 4-23: Output and reference waveforms under 0.5 g 400 Hz input.
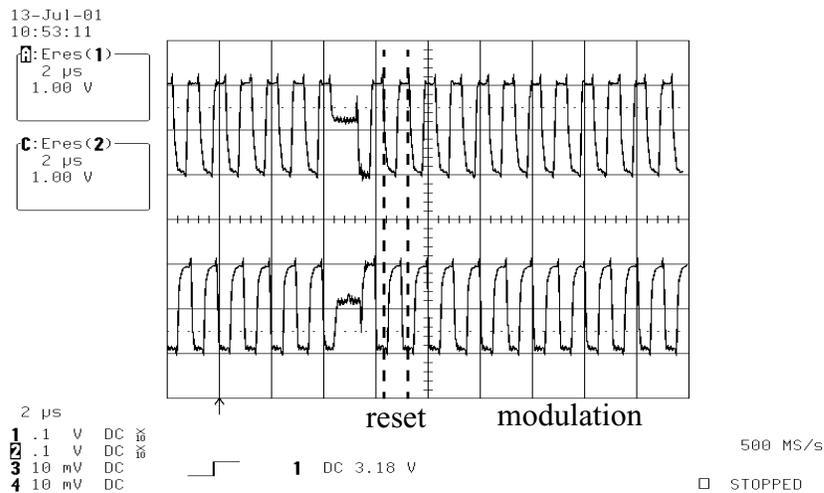
Figure 4-24: Differential pre-demodulation signals showing modulation and reset.

response of the circuit to an 1 MHz square wave signal. The settling time is less than 30 ns. The differential signal swing range is greater than 3 V.

4.4.3 Noise Measurements

The minimum noise floor is measured at modulation frequency of 1 MHz. A 0.5 g 400 Hz sinusoidal acceleration is provided by the vibration table. Thus, the signal power is -9 dBg. The output spectrum in response to the -9 dBg input acceleration is shown in Figure 4-25. In the spectrum, the output signal power is -7 dBm, and the power spectral density (PSD) of the output noise is -84 dBm/Hz. Therefore, the accelerometer input-referred noise PSD is -86 dBg/Hz, and the input-referred noise floor is about 50 μg/rtHz.

The total input-referred noise floor is close to the calculated Brownian noise floor of about 30 μg/rtHz. This is demonstrated by testing a half-released device. This device is released by an incomplete Si etch, so that the structure can be moved by large electrostatic force, but has very low sensitivity to both the acceleration signal and the random forces generated by the Brownian motion of ambient molecules. By desensitizing the device to Brownian noise, the real electronic noise floor can be revealed. The structure is driven by a 5 V sinusoidal voltage with +/- 25 V dc bias on the differential electrostatic actuator, which generates a force equivalent to a few hundred g. The output spectrum is shown in Figure 4-26. The output noise PSD is 2 - 3 dB lower than the result obtained from a fully released device on a vibration table. This proves that the integrated CMOS MEMS accelerometer is approaching the Brownian noise limit.

The relationship between noise and modulation frequency is measured and plotted in Figure 4-27 and 4-28. These tests show that the total noise decreases with the modulation frequency up to 1 MHz, as predicted by (3-18) and Figure 4-2. This proves that the 1/f

noise is the most significant noise source in this modulation frequency range. The SNR and the input-referred noise floor get worse beyond 1 MHz because the signal is limited by incomplete settling due to finite circuit bandwidth which is about 3 MHz. The minimum noise floor is achieved at 1 MHz modulation. As discussed earlier, the total electronic noise floor crosses over the Brownian noise around 1 - 2 MHz, therefore, the 50 µg/rtHz noise floor measured at 1 MHz modulation frequency is close to the best achievable noise floor without vacuum packaging.

The experiments also show that the input-referred noise floor of the accelerometer is dependent on the signal frequency. As shown in Figure 4-29 and Figure 4-30, the noise is higher at lower signal frequency. The noise decreases more than 10 dB from dc to 500 Hz while the sensitivity remains constant. In Figure 4-30, the noise versus signal frequency is plotted for four different measurements performed on this prototype at 1 MHz chopping frequency and a previous prototype at 50 KHz, 200 KHz and 1 MHz, each having a differ-ent electronic noise floor. From Figure 4-30, the correlation between the signal-frequency-dependent noise and the electronic noise at the modulation frequency is obvious. This leads us to conclude that this signal-frequency-dependent noise originates from the elec-tronic noise in the sensed signal, not from other additive noise sources in the sensor or other parts of the circuit. All measurements consistently give the following approximate equation of output noise PSD:

$$N_o(f, f_m) = N(f_m)F\left(1 + \frac{K}{f^n}\right),\qquad(4\text{-}27)$$

where f is the signal frequency, f_m is the modulation frequency, $N(f_m)$ is the noise PSD at the modulation frequency, F is noise folding factor, K is the coefficient of signal-frequency

dependency, and *n* is number between 1 and 2. This equation captures both the modulation-frequency dependency and the signal-frequency dependency of the output noise.

Equation (4-27) indicates that the electronic noise undergoes some kind of noise shaping that is not predicted by the analyses in Chapter 3 based on stationary random processes. These analyses predict that the demodulated output noise should be almost white regardless whether the circuit noise is dominated by 1/f noise or by white noise. All hypotheses based on independent additive noise sources, such as baseband circuit 1/f noise or sensor 1/f noise, fail to explain the correlation between the output frequency-dependent noise and the electronic noise floor at the chopping frequency. Because of the use of synchronous demodulation, this noise shaping could not be the result of the clock jitter (the phase noise that decreases with the offset frequency). This leaves us only one possibility, that is, the frequency dependency of the noise PSD is the result of the noise being a nonstationary random process. In fact, the 1/f noise is indicated by many to be a nonstationary process that exhibits fractal behaviors such as self-similarity [94, 95, 96, 97]. A nonstationary random process could not be properly modeled by its PSD because its autocorrelation function varies with time. When observed by a spectrum analyzer at very low frequency (< 500 Hz), these nonstationary or fractal properties could make the Fourier transform of the measured noise sequence appear to decrease with the frequency. Because the frequency dependency is the result of the nonstationary properties of the high-frequency noise at the modulation frequency, minimizing the noise floor at the modulation frequency would lower the entire curve of the output noise. Furthermore, because the white thermal noise is more close to a stationary random process, the frequency dependency may disappear when the thermal noise dominates, as in ADXL accelerometers [31].
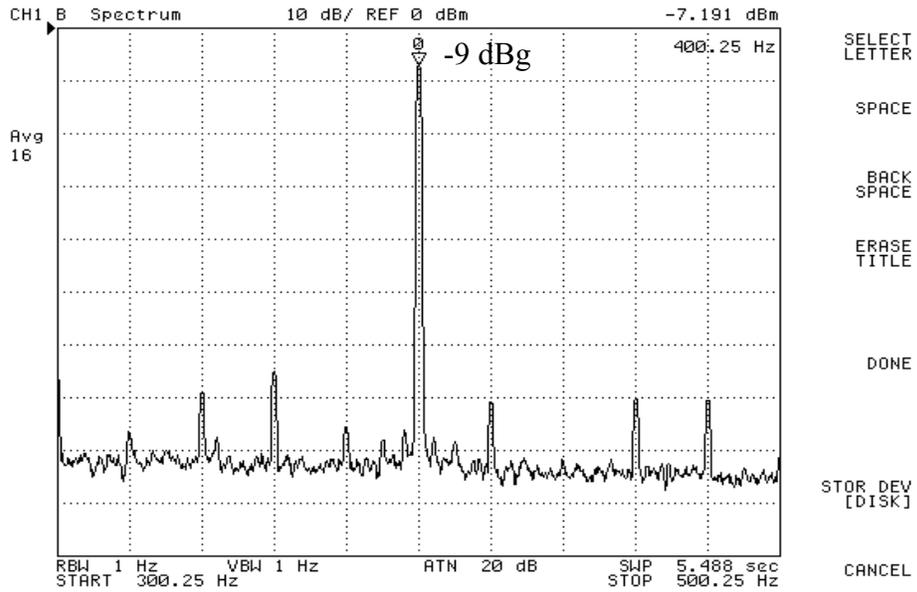
Figure 4-25: Output spectrum with -9 dBg 400 Hz input acceleration.
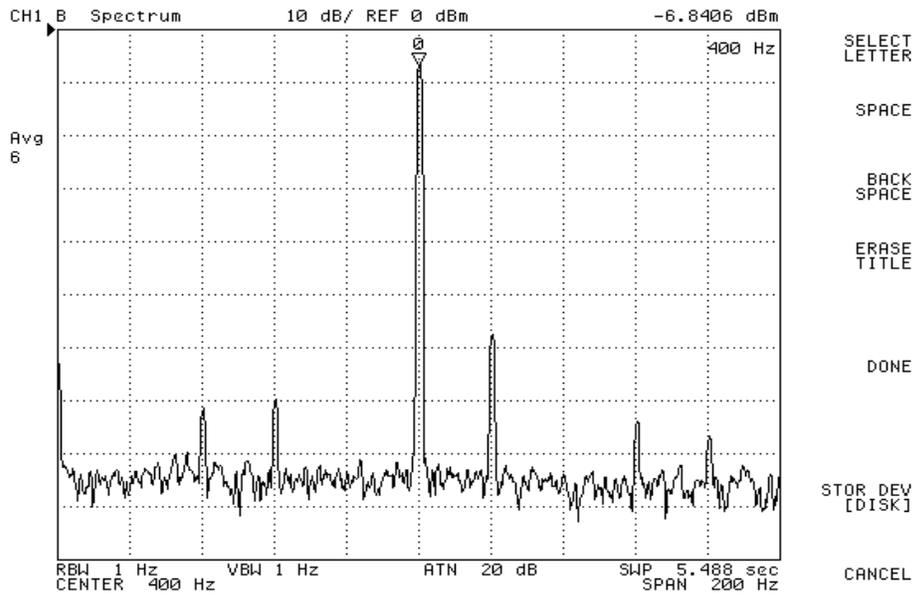
Figure 4-26: Output spectrum of self-test without Brownian noise.
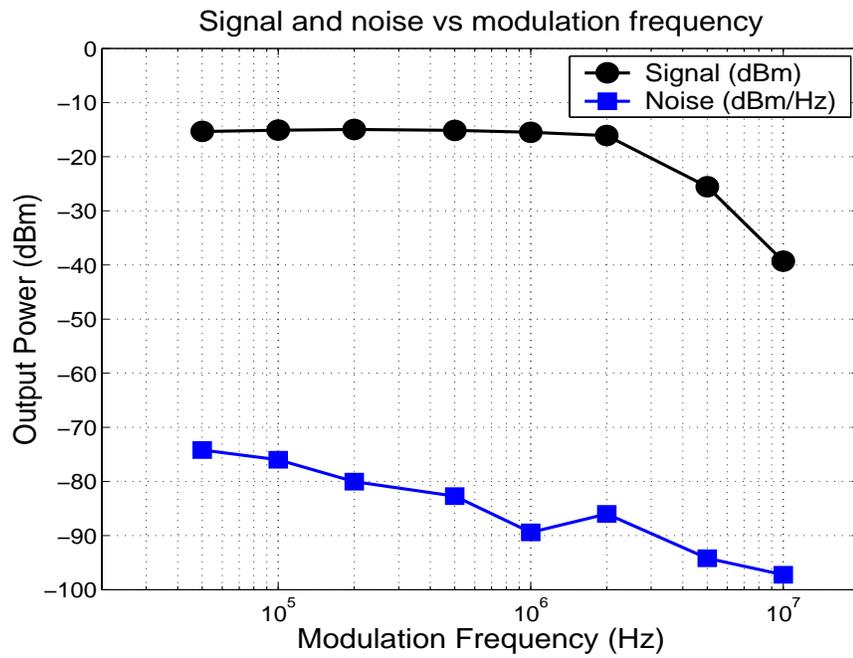
Figure 4-27: Output signal power and noise power spectral density versus modulation frequency.
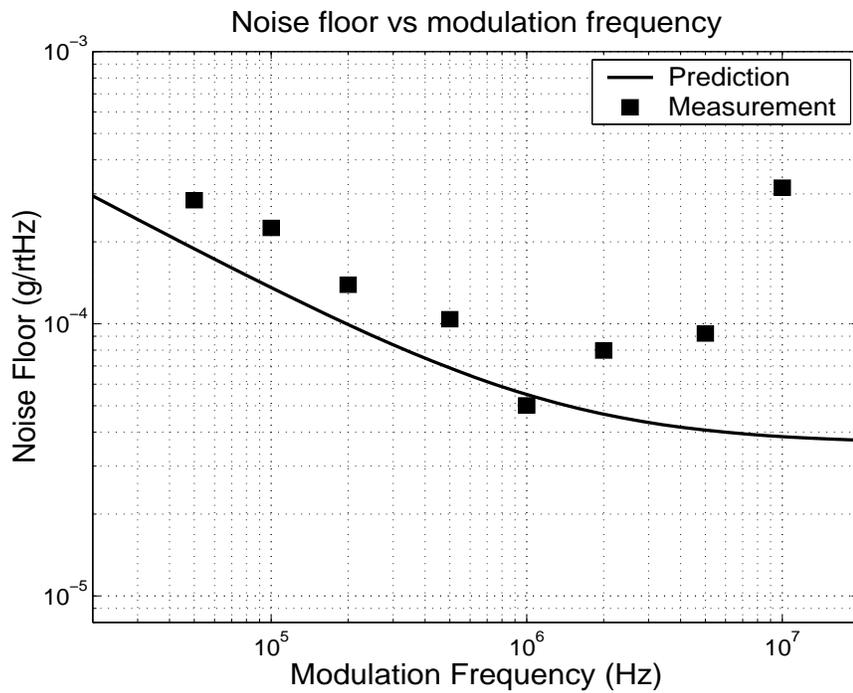
Figure 4-28: Accelerometer input-referred noise floor versus modulation frequency.
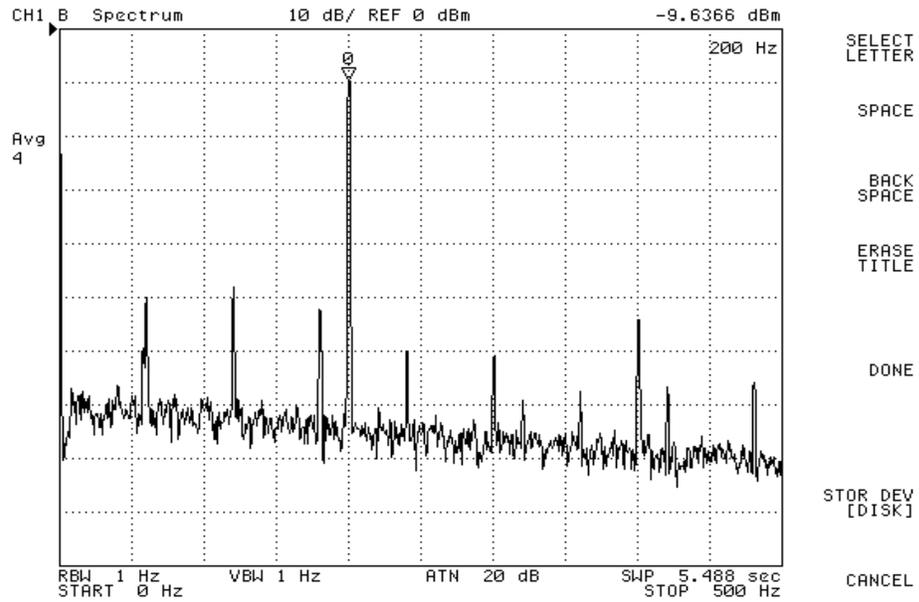
Figure 4-29: Output spectrum from 0 - 500 Hz showing noise decreases with frequency.
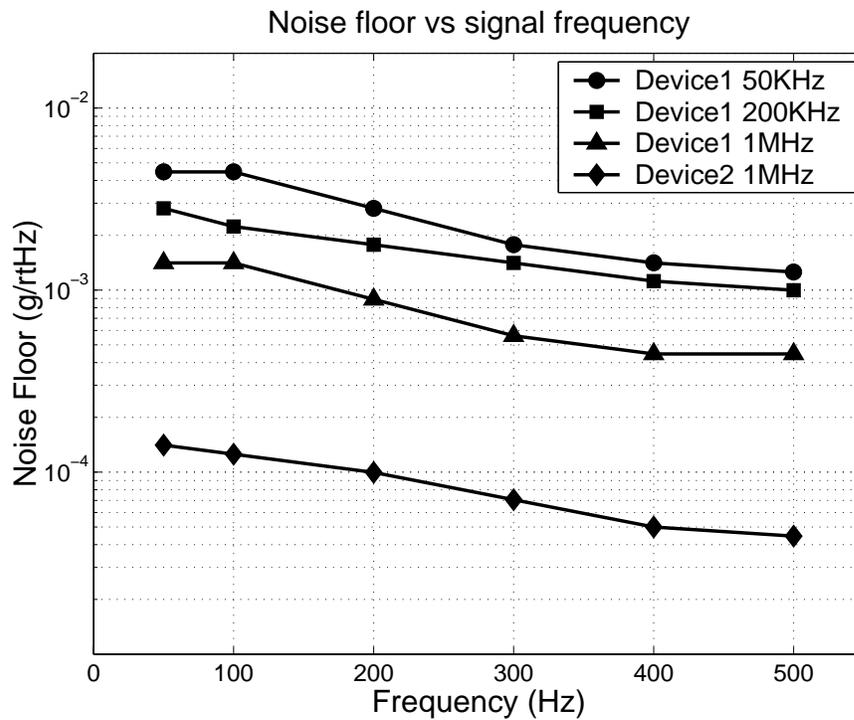
Figure 4-30: Input-referred noise floor versus input signal frequency at four measurements on different prototypes with different modulation frequencies.

4.4.4 Offset Measurements

Figure 4-31 shows the time-domain results of dc/ac offset cancellation. In Figure 4-31(a), the ac differential signals exhibit large dc offset voltage greater than 1 V. Divided by the designed gain of the circuit, the input-referred dc offset voltage is about 10 mV. By enabling the dc offset cancellation, this offset is eliminated in Figure 4-31(b). The output voltage of the offset amplifier is measured at 0.1 V. The input-referred offset is reduced to 10 µV. Figure 4-31(c) shows the waveforms with dc offset control but without ac offset control. The ac signal is mainly due the sensor position offset. In Figure 4-31(d), this ac offset is also significantly reduced by ac offset cancellation.

The spectrum of pre-demodulation ac signal is shown in Figure 4-32. The modulation frequency is 200 KHz and the signal frequency is 400 Hz. Therefore, the ac offset appears as the peak at 200 KHz, and the signal appears as the two peaks at 196.6 KHz and 200.4 KHz, respectively. In Figure 4-32(a), where there is no ac offset control, the offset signal at 200 KHz due to position offset saturates the circuit and completely blocks the sensing signals. In Figure 4-32(b), with the ac offset cancellation enabled, the offset signal is reduced by 40 dB, and the sensing signal peaks emerge. Figure 4-32 demonstrates the importance and effectiveness of the DDA-based electronic offset cancellation. The sensor offset is often much greater than 15 g, large enough to completely block any sensing signals, and difficult for electrostatic actuator to compensate. The electronic offset cancellation is more effective than the mechanical method based on electrostatic actuators, offering large offset control range while avoiding the high voltage required to pull back the proof-mass.
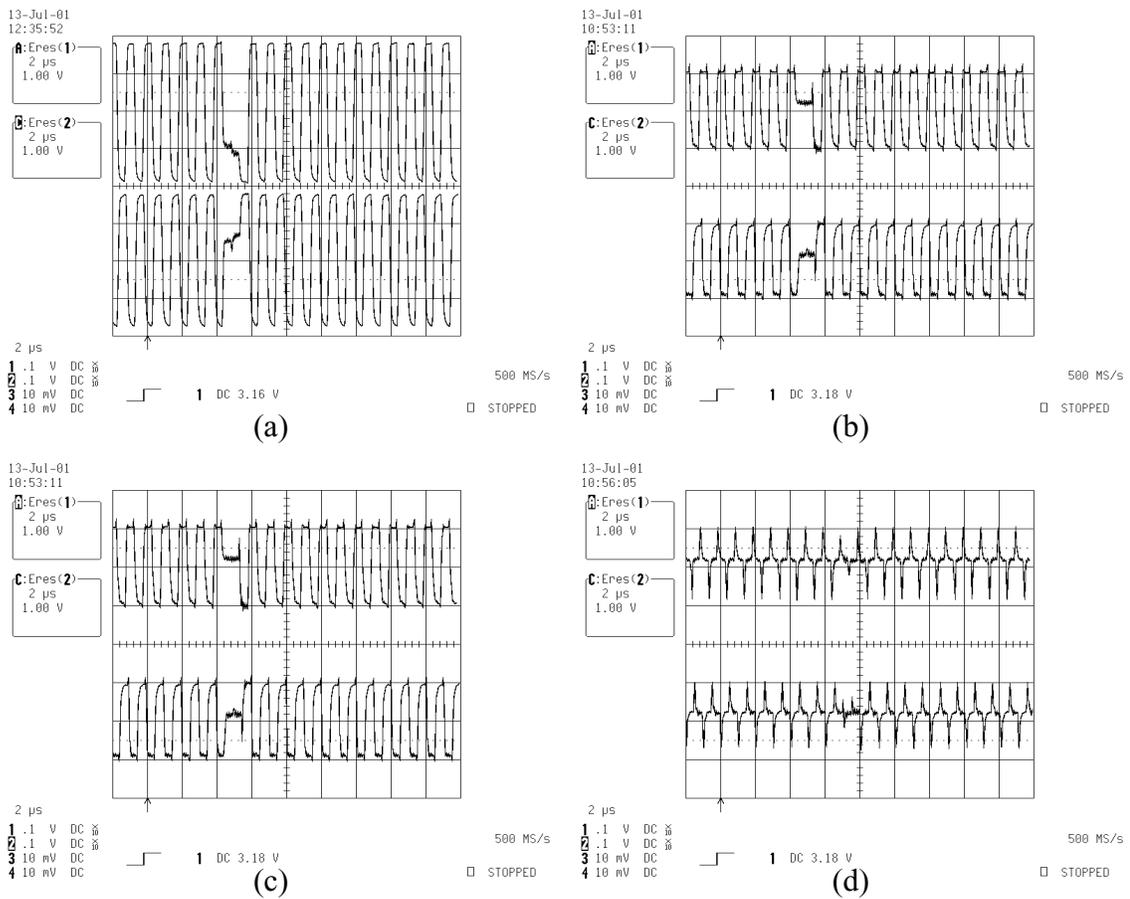
Figure 4-31: Time-domain waveforms of pre-demodulation signals: (a) with ac and dc off-set; (b, c) after dc offset is cancelled; (d) after both dc and ac offset is cancelled.
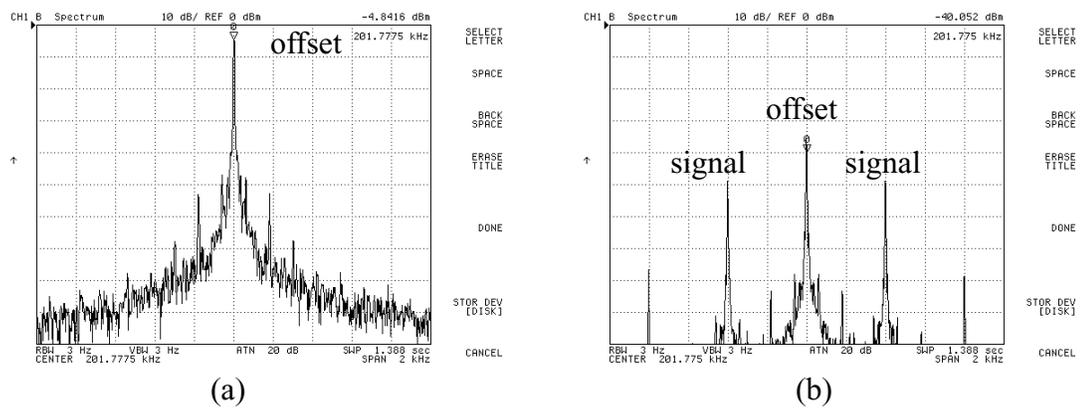
Figure 4-32: Spectrum of pre-demodulation signals: (a) the signal is blocked by ac sensor offset greater than 100 g; (b) signal appears after the sensor offset is reduced by 40 dB.

4.4.5 Comparison to Previous Work

Table 4-1 compares this integrated CMOS MEMS accelerometer to some other MEMS capacitive accelerometers reported recently. Among thin-film MEMS accelerometers using polysilicon or CMOS MEMS technologies, the 50 µg/rtHz input-referred noise floor achieved by this device is one of the best noise performances ever reported. On the other hand, the CMU CMOS MEMS technology has the smallest capacitance sensitivity while having lower manufacturing cost.

Micro-g noise floor has been realized by bulk micromachined devices. These devices have several orders of magnitude larger proof-mass and sensing capacitance, hence lower noise floor. However, they are much more expensive to fabricate and difficult to integrate with electronics. In fact, all silicon bulk accelerometers listed in Table 4-1 use a two-chip solution with one sensor chip and one ASIC for signal pickup and processing.

The accelerometer noise floor versus capacitance sensitivity of recently reported MEMS accelerometers is plotted in Figure 4-33. One figure of merit to quantify the performance of capacitive accelerometer readout circuits is the product of the capacitance sensitivity and the input-referred noise floor:

$$CNP = C_s \cdot \sqrt{\overline{a_n^2(f)}}. \tag{4-28}$$

This product describes how sensitive the interface circuit is to detect the capacitance changes. The line in Figure 4-33 indicates the average capacitance-noise products of all devices shown in Table 4-1 and Figure 4-33. Among them, this integrated CMOS MEMS accelerometer achieves the lowest capacitance-noise product.

Table 4-1: Comparison of accelerometer capacitances and noise floors

	Technology	Sensing method	Capacitance	Noise floor
Smith 94 [11]	Si-bulk + ASIC	switched cap.	80 pF/g	1 µg/rtHz
Yazdi 99 [15]	Si-bulk + ASIC	switched cap.	20 pF/g	3.7 µg/rtHz
Berstein 99 [19]	Si-bulk + ASIC	CT voltage	0.48 pF/g	1 µg/rtHz
Lu 95 [12]	poly monolithic	switched cap.	500 fF, 2.5 fF/g	1600 µg/rtHz
Lemkin 97 [13]	poly monolithic	switched cap.	101 fF x 2	110 µg/rtHz
ADXL105 [31]	poly monolithic	CT voltage	-	225 µg/rtHz
Zhang 00 [22]	CMOS MEMS	CT voltage	20 fF, 0.4 fF/g	1000 µg/rtHz
This work	CMOS MEMS	CT voltage	20 fF, 0.4 fF/g	50 µg/rtHz
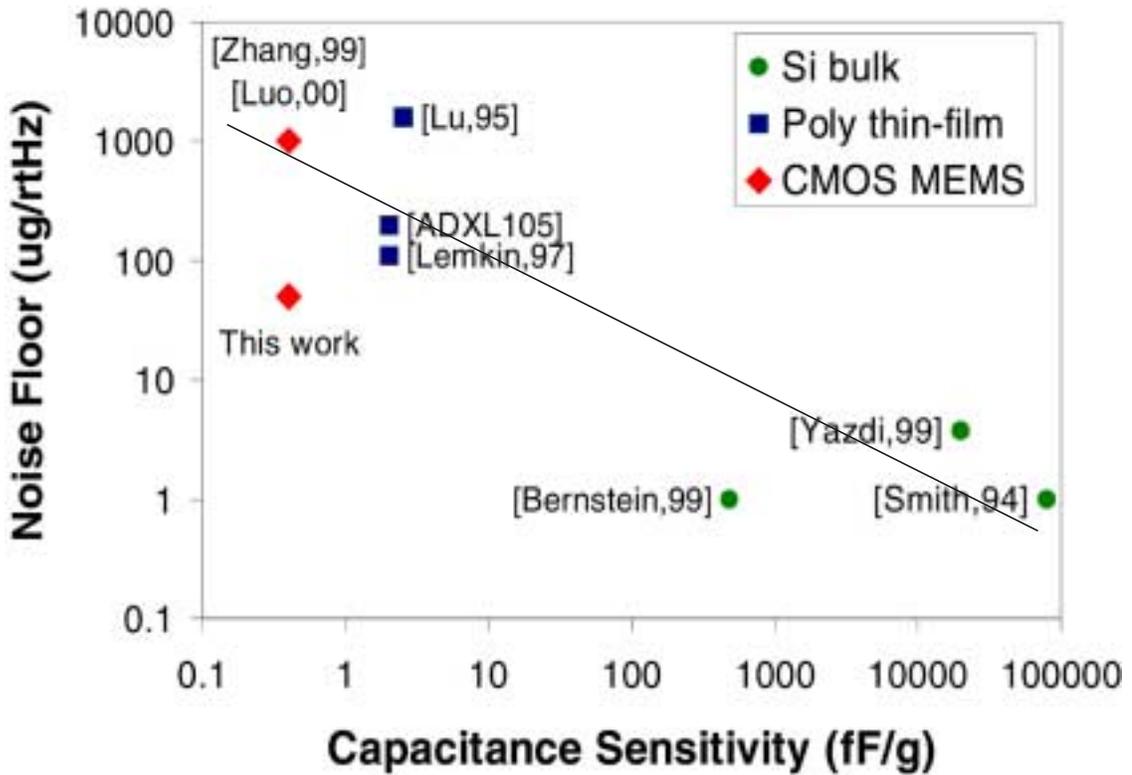
Figure 4-33: Comparison of noise floor versus capacitance sensitivity among recently reported MEMS accelerometers.

4.5 Summary

This chapter describes a low-noise low-offset chopper stabilized capacitive readout amplifier and an integrated CMOS MEMS accelerometer chip using this circuit. The low noise is obtained by chopping the signal at MHz frequency and sizing the input transistors based on optimum capacitance matching. The suppression of charging is accomplished by a switching biasing method which uses periodic reset to establish robust dc bias at the input sensing nodes. The low offset is achieved by dc/ac offset cancellation based on differential difference amplifier (DDA).

Table 4-2: Performance summary

Sensitivity	130 mV/g
Noise floor	50 µg/rtHz @ 400 Hz (1 MHz modulation)
Acceleration range	> 15 g (> 4 V output swing)
Sensor offset reduction	> 40 dB
Circuit DC offset	10 µV
Resonant frequency	5.8 KHz
Sensor bandwidth	1 KHz
Modulation frequency	20 KHz - 2 MHz
Supply voltage	5 V
Current consumption	6 mA/sensor
Die area	3.5 mm x 2.5 mm
Sensor area	600 µm x 450 µm (4 sensors)
Technology	0.5 µm 3M1P CMOS + CMOS MEMS

A summary of the integrated CMOS MEMS accelerometer with the chopper stabilized capacitive readout amplifier is given in Table 4-2. The integrated CMOS MEMS accelerometer achieves 50 µg/rtHz noise floor and > 40 dB of sensor offset reduction. The total measured noise floor is very close to the estimated Brownian noise floor of 30 µg/rtHz. The measurements also show that the accelerometer noise floor is dependent on the chopping frequency and the noise model presented in Chapter 3 gives good noise estimation.

Chapter 5

Electromechanical Delta-Sigma Modulation for High-Q MEMS Structures

This chapter describes the electromechanical delta-sigma modulation. By applying delta-sigma ($\Delta-\Sigma$) modulation on thin-film MEMS accelerometers, it is possible to accomplish three tasks at once: producing high-resolution digital output; providing feedback linearization to suppress sensor nonlinearities and variations; and applying closed-loop control to enable high-Q operation to reduce Brownian noise. $\Delta-\Sigma$ modulation have been used in previous works to achieve the first two goals. In this work, it is extended to control the high-Q MEMS structures, which is critical for the thin-film devices to reach the performance currently only attainable by other more expensive technologies.

5.1 Motivations

5.1.1 Brownian Noise and Settling Time

In inertial sensors, the thermal-mechanical noise commonly known as the Brownian noise is given by

$$\overline{a_n^2}(f) = \frac{4kTb}{m^2} = \frac{4kT\omega_n}{mQ} \ . \tag{5-1}$$

The mechanical quality factor is defined as

$$Q = \frac{m\omega_n}{b}. \tag{5-2}$$

Two ways to reduce the Brownian noise are decreasing the damping b and increasing the mass m. As the resonant frequency w_n must be large enough to maintain sufficient sensor bandwidth, both means increase the Q factor of the transducer. In thin-film MEMS devices, because large mass is not available, the Brownian noise is particularly large, usually in the range of 10 to 100 µg/rtHz. As we have seen in the previous work, the circuit electronic noise can be significantly reduced by good interface circuit design, the Brownian noise is a major obstacle for thin-film devices to achieve higher performance. To obtain lower noise floor, the transducer must be underdamped and must have high mechanical Q. Since silicon and other materials used in semiconductor processes have high intrinsic Q factor, the Q of the device is determined by the air damping. Therefore, a high mechanical Q can be obtained by placing the devices in low-to-medium vacuum. Experiments showed that CMOS-MEMS structures can achieve Q over 1000 at 10 mTorr air pressure [49].

A high-Q underdamped device is critically stable. It oscillates at sudden changes in acceleration, such as an impulse or a step signal, and settles very slowly. This oscillation is called ringing. The relationship between the settling time and the Q of an underdamped 2nd-order system is given by [50]:

$$T_s \propto \frac{Q}{\omega_n}. \tag{5-3}$$

Thus, the higher the quality factor is, the slower the system settles after a step input. Practical sensors are required to have none or minimum ringing and settle as fast as possible. Thus, the device must be controlled and stabilized in a closed-loop with negative feedback

in order to damp the ringing while adding no noises. To achieve the fastest settling, the closed-loop system should have critical damping with closed-loop Q of 0.5, or equivalently, closed-loop damping factor of unity. The step responses of the underdamped accelerometer to 5 g step input with Q from 1 to 1000 are shown in Figure 5-1.
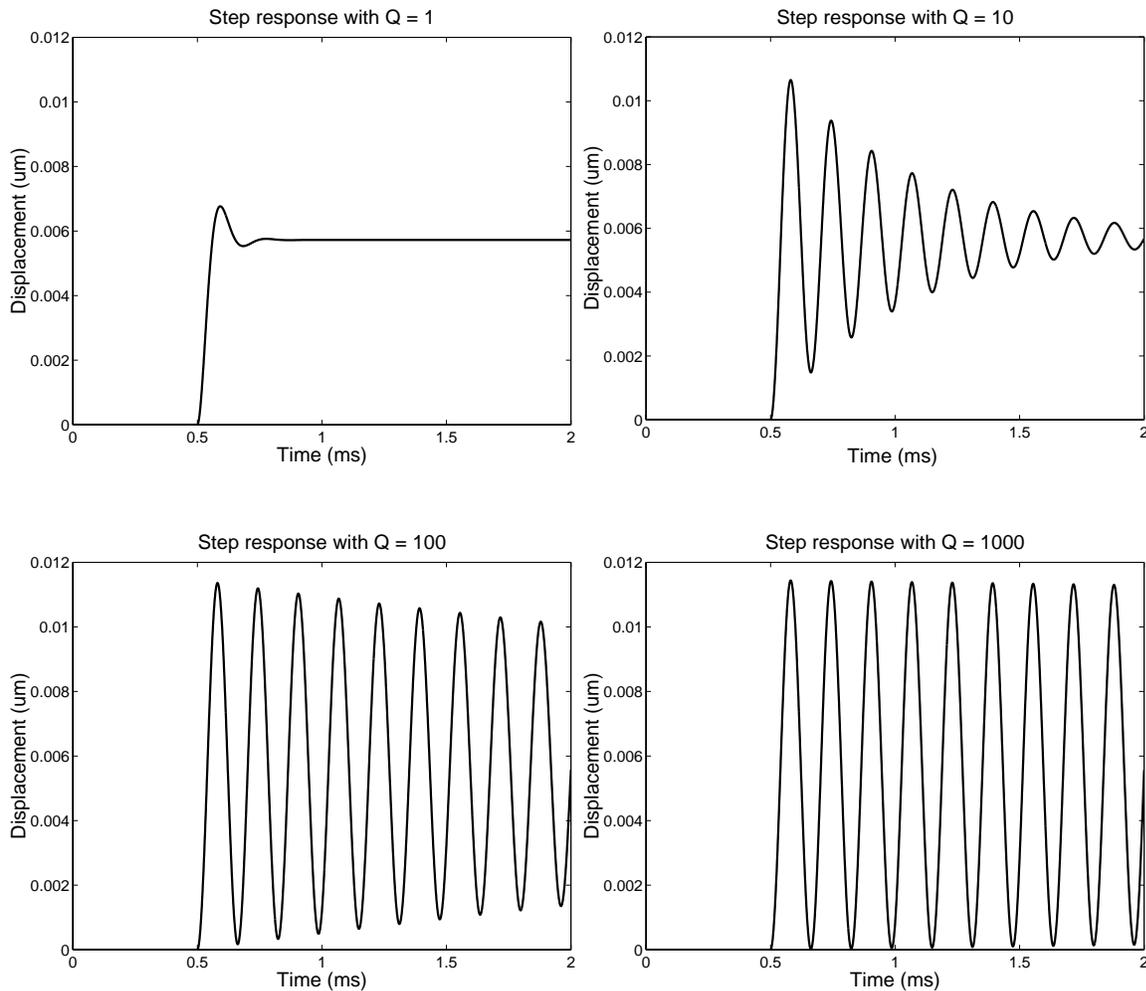
Figure 5-1: Ringing of an open-loop underdamped MEMS structure.

5.1.2 Feedback Linearization

The closed-loop control also provides feedback linearization to suppress the nonlinearities and variations of the transducer. As shown in Chapter 2, the linearity of an open-loop capacitive accelerometer is 60 dB at best. The only way to achieve dynamic range greater than 60 dB is to use closed-loop sensors.

In the closed-loop system shown in Figure 5-2, function $S(f)$ describes the sensor sensitivity including nonlinearities and variations,

$$
\begin{aligned}
S(f) &= (S_0 + \Delta S_0)f + (S_1 + \Delta S_1)f^2 + \ldots \\
&= S_0 f + \Delta S(f)
\end{aligned}
\tag{5-4}
$$

With linear feedback, the output of the closed-loop system is given by:

$$
\begin{aligned}
V_{out} &= \frac{S_0 f_{in}}{1 + S_0 F} + \frac{\Delta S(\Delta f)}{1 + S_0 F}, \\
&= V_0 + \Delta V
\end{aligned}
\tag{5-5}
$$

in which the difference force is:

$$
\Delta F = \frac{f_{in} + \Delta S(\Delta f)}{1 + S_0 F}.
\tag{5-6}
$$

If the loop gain is sufficiently large and the following condition is satisfied:

$$
S_0 F \gg 1,
\tag{5-7}
$$
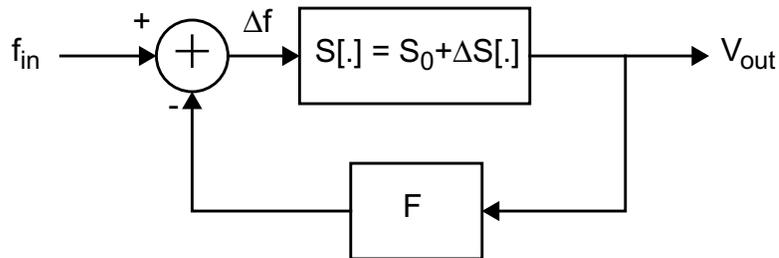
Figure 5-2: Suppression of nonlinearities and variations by feedback linearization.

we have:

$$V_{out} \approx \frac{f_{in}}{F}, \tag{5-8}$$

with:

$$\Delta f \approx 0, \tag{5-9}$$

$$\Delta V = \frac{\Delta S(\Delta f)}{1 + S_0 F} \approx 0. \tag{5-10}$$

Therefore, with the feedback, the system is desensitized to nonlinearities and variations, so that these nonidealities have very little effects on the system output.

5.1.3 Digital Accelerometer

Most modern applications of inertial sensors use computers, microprocessors and other digital devices. To process the signals in digital domain, the sensors must be followed by analog-to-digital (A/D) converters. The digital processing also allows easier and more accurate trimming, calibration and adjustment of the sensors. Therefore, it is very desirable to integrate A/D converters with the transducers and the sensing circuitry on a single micro chip, as shown in Figure 5-3. Such integrated digital sensor systems-on-chip (SOC) not only provide more functionality, but also reduce the overall system cost.

The delta-sigma (Δ–Σ) modulation technique is attractive because it provides direct digitization and closed-loop feedback control at the same time. It has long been the prominent technique for high-resolution analog-to-digital conversion of low-speed signals. The sensing bandwidth of most mechanical sensors is smaller than 10 KHz, well within the applicable range of Δ–Σ techniques. If a Δ–Σ modulator can be designed to control a high-Q mechanical transducer, three objectives could be accomplished at once: producing high-
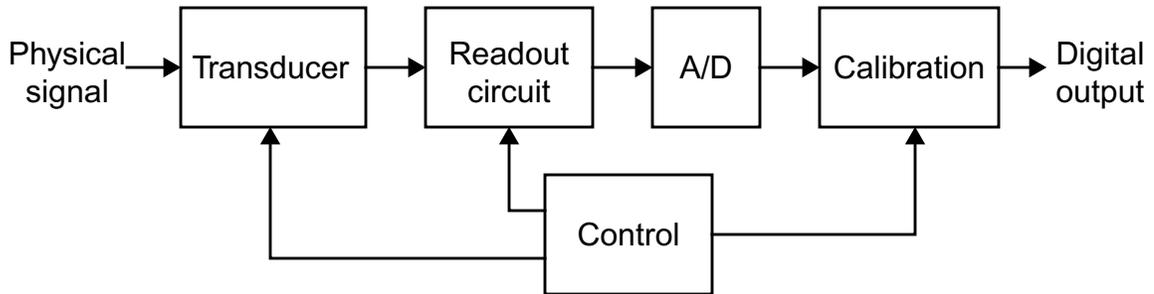
Figure 5-3: Integrated digital sensor system with on-chip digital control and calibration.

resolution digital output; providing feedback linearization to suppress sensor nonlineari-ties and variations; and enabling high-Q operation to reduce thermal-mechanical noise.

Compared to other feedback control strategies, the main advantage of $\Delta-\Sigma$ modulation is the simplicity and robustness of its implementation. It has much lowest cost and con-sumes much less power than digital controllers which require A/D, D/A converters and microprocessors. The system is insensitive to imperfections in the circuit elements, there-fore, is more accurate and robust than pure analog implementations. It is also most suit-able for CMOS implementation, thus, facilitates the integration with transducers and sensing circuitry.

The $\Delta-\Sigma$ modulation has been used in A/D converters for 20 years [51 - 60], and has been applied in MEMS inertial sensors and other sensors in the past decade [7 - 9, 11 - 15, 43]. However, the $\Delta-\Sigma$ modulation has been used mainly as a mean of A/D conversion, but not much as a control method. And no work has been done on using it to control very lightly damped resonators with Q exceeding 100. On the other hand, the high-Q operation is necessary for surfaced micromachined devices to overcome the Brownian noise barrier in order to achieve the performance currently only attainable by bulk micromachining and

other more expensive technologies. Due to this status, the research on MEMS applications of $\Delta-\Sigma$ techniques has been limited to second-order one-bit systems, because there has been no need to explore more advanced techniques to minimize quantization noise when the overall noise is dominated by the Brownian noise and the electronic noise.

In this work, the application of $\Delta-\Sigma$ modulation in high-Q MEMS structures is investigated. The goal is to study the $\Delta-\Sigma$ modulation both as a A/D conversion technique and as a control method on micromechanical resonators with high Q and low dc gain. Both high-order noise shaping and multi-bit feedback are included in this study. And special emphasis is given to the robustness of the $\Delta-\Sigma$ feedback loop because the manufacturing and environmental variations are particularly large in micro-fabricated devices.

5.2 Review of Delta-Sigma Modulation

The $\Delta-\Sigma$ modulation have been widely used in low-to-medium speed A/D and D/A converters. Examples of $\Delta-\Sigma$ A/Ds include very-low-speed 24 bit A/Ds for instrumentation applications and Mb/s 10 bit A/Ds for wireless communications. It is the dominant technique to realize data converters with resolution higher than 14 bit [51 - 60]. In the past decade, this technique has been applied in integrated MEMS sensors to provide direct digitization [7-9, 11 - 15, 43]. Although there are now many variations of $\Delta-\Sigma$ modulation, discussions in this work are restricted to sampled-data low-pass analog-to-digital $\Delta-\Sigma$ modulators.

5.2.1 Oversampling and Noise Shaping

The quantization errors introduced in analog-to-digital conversion could be modeled as an additive noise source referred to as the quantization noise. With a few exceptions, the quantization noise could be approximated by a white noise signal with reasonable accuracy. Under the white quantization noise assumption, the power spectral density (PSD) of the quantization noise is constant over frequency in a range from dc to the sampling frequency f_s. Therefore, if we oversample the signal at much higher rate than its Nyquist frequency, $f_s \gg 2f_0$, and then perform low-pass filtering on the quantized data, we can reduce the total power of in-band quantization noise, as shown in Figure 5-4.

Defining the oversampling ration as

$$OSR = \frac{f_s}{2f_0},$$
(5-11)

the maximum signal-to-noise ratio (SNR) of an N-bit quantizer is given by [41, 51],

$$
\begin{aligned}
SNR_{max} &= 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR) \\
&= 1.76 + 6.02N + 10\log(OSR)
\end{aligned}
$$
(5-12)
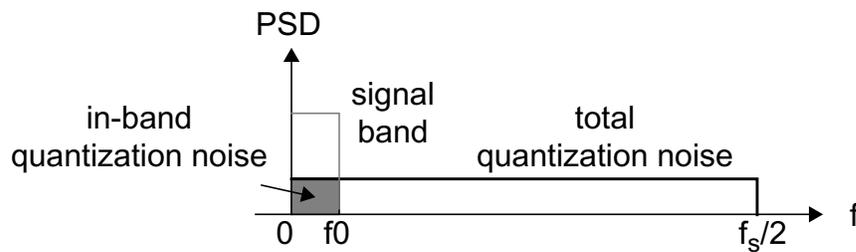
Figure 5-4: Reduction of in-band quantization noise by oversampling.
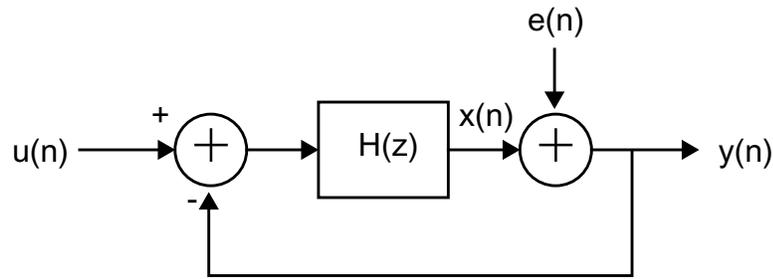
Figure 5-5: Noise shaping using feedback.

With oversampling, the SNR could be further improved by noise shaping. Considering the system in Figure 5-5, the closed-loop signal transfer function $S_{TF}(z)$ and the noise transfer function $N_{TF}(z)$ are derived as [41, 51]:

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)}. \tag{5-13}$$

and

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}. \tag{5-14}$$

If H(z) has low-pass frequency response and large dc gain, the quantization noise power within the Nyquist frequency could be reduced as shown in Figure 5-6.
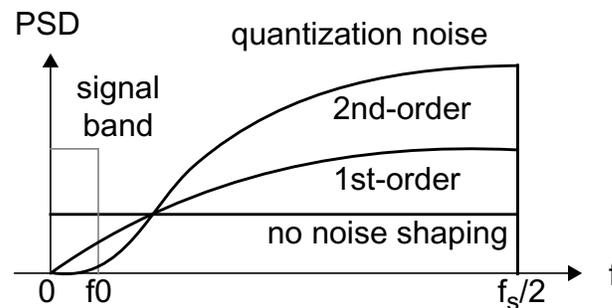
Figure 5-6: Reduction of in-band quantization noise by noise shaping

The closed-loop system should be followed by a digital low-pass filter with higher order than H(z) to remove enhanced out-of-band noise and reduce the total noise power. This filter is called decimation filter in Δ–Σ modulators. In conventional Δ–Σ A/D converters, the loop filter consists of one or more integrators, so that H(z) goes to infinity at DC, and the maximum SNR is given by

$$
\begin{aligned}
SNR_{max} &= 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{2L+1}{\pi^{2L}}OSR\right) \\
&= 1.76 + 6.02N + 10(2L+1)\log(OSR) + 10\log(2L+1) - 9.94L
\end{aligned}
\qquad (5\text{-}15)
$$

where L is the order of the modulator which equals the number of integrators in the loop filter.

A generic diagram of Δ–Σ modulator is shown in Figure 5-7. Another advantage of Δ–Σ modulator is that the linearity of the system is determined solely by the feedback D/A, thus, is insensitive to the circuit imperfections on the forward path, including the loop filter and the low-resolution A/D. Many Δ–Σ converters use 1-bit D/A and simple comparator. Because 1-bit D/A has only two output levels, the D/A and thereby the system are inherently linear.
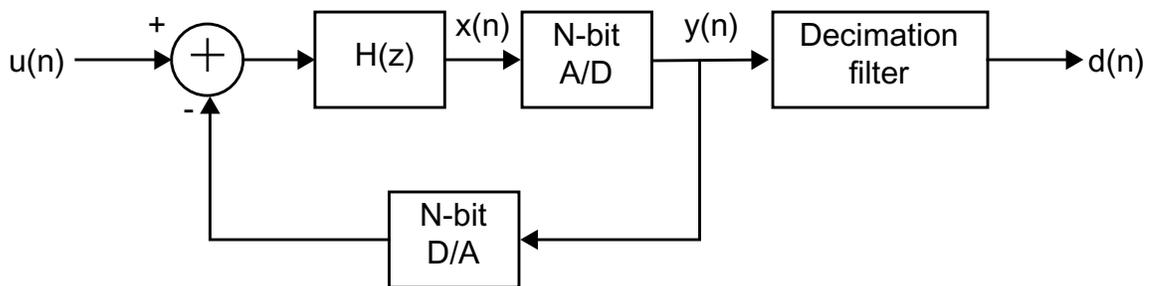
Figure 5-7: Generic block diagram of delta-sigma modulators.

According to (14), the theoretical peak SNR of Δ–Σ modulators at OSR of 256 is given in Table 5-1. The practical Δ–Σ converters have somewhat lower performance than these ideal values. Particularly, because multi-bit D/A does not have the inherent linearity, the performance of multi-bit modulators may be degraded by nonlinear distortions.

Table 5-1: Calculated peak SNR of Δ–Σ modulator with OSR of 256.

	1-bit	2-bit	3-bit
No noise shaping	31.9 dB	37.9 dB	43.9 dB
1st-order	74.9 dB	80.9 dB	86.9 dB
2nd-order	115.3 dB	121.3 dB	127.3 dB
3rd-order	155.0 dB	161.0 dB	167.0 dB

5.2.2 Delta-Sigma Analog-to-Digital Converters

The Δ–Σ A/D converters employ one or more switched-capacitor integrators in the loop filter to provide noise shaping. Figure 5-8 shows a second-order Δ–Σ converter. The first-order and the second-order are inherently stable.
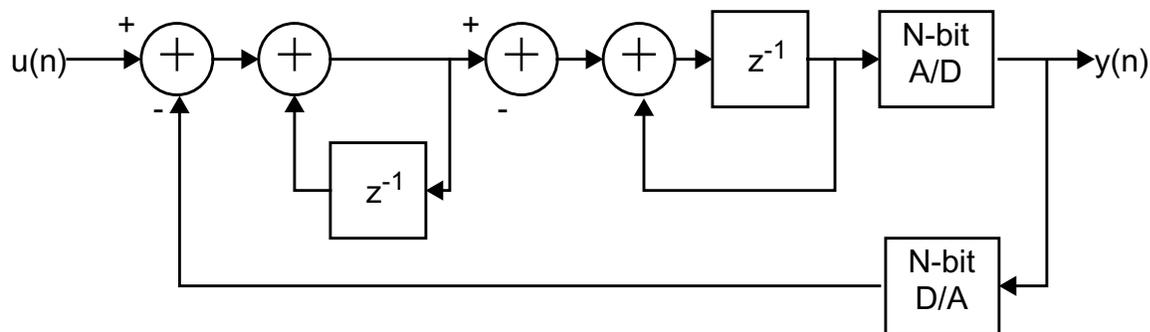
Figure 5-8: Second-order Δ–Σ modulator.

According to equation (5-7), the maximum SNR and the dynamic range (DR) of the converter can be improved by three ways: increasing oversampling ratio (OSR); increasing the order (L); and increasing the forward-path A/D resolution (N). Single-bit modulator has the advantage of better linearity, and the OSR can not be arbitrarily high due to circuit speed and power consumption constraints. For high-resolution and high-speed converters, high-order modulators with more than two integrators are widely used. The stability of high-order modulators is a challenging problem. There are two popular architectures of high-order $\Delta{-}\Sigma$ modulators: interpolative architecture [41, 51, 53]; and cascade architecture, or multi-stage noise shaping (MASH) architecture [41, 51, 60]. The interpolative structure implements a high-order filter with the zeros of the noise transfer function spreading over the frequency-of-interest band, thus, reduces the sensitivity to component variations. The interpolative modulators must be carefully designed to ensure its stability. The cascade or MASH architecture constructs the high-order modulators using the inherently stable first and second-order loops, thus, ensuring the system is stable. However, the high-order noise shaping is achieved by perfect cancellation of terms in the noise transfer functions of the consecutive loops. Therefore, mismatches of circuit components degrade the system performance.
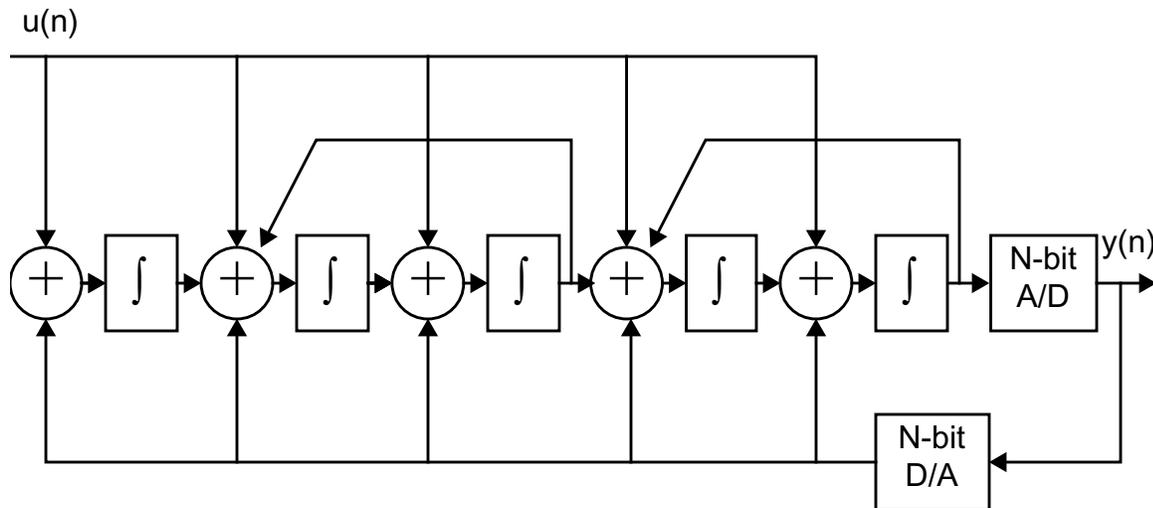
Figure 5-9: Interpolative high-order Δ–Σ modulator.
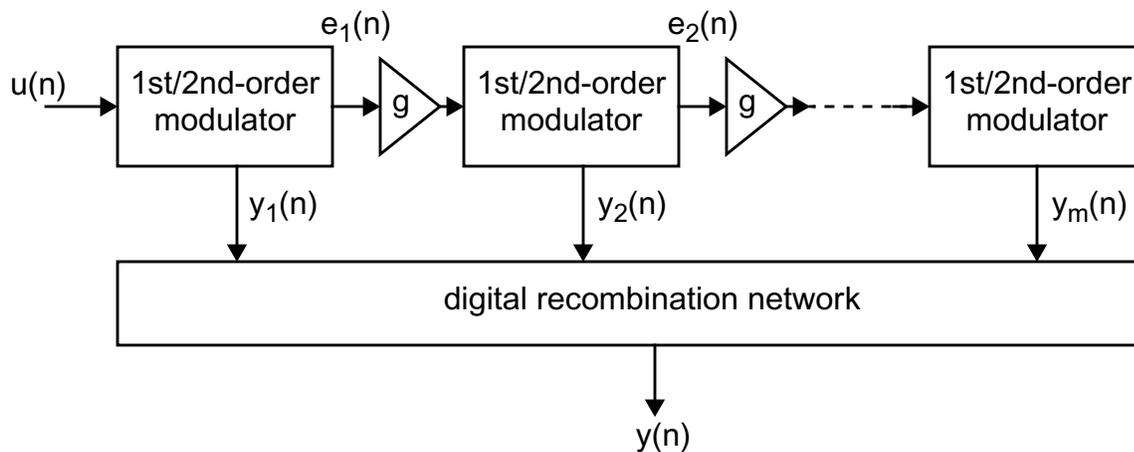
Figure 5-10: Cascade high-order Δ–Σ modulator with multi-stage noise shaping (MASH).

The alternative way to improve SNR and DR is to use multi-bit quantization. Multi-bit quantization not only reduces the quantization noise, but also makes high-order modulators more stable. The linearity of multi-bit modulator depends on the feedback D/A. And it is challenging is to realize multi-bit D/A with high linearity. The most popular approach to highly linear D/A is dynamic element matching (DEM) [46 - 48]. DEM uses a variety of coding schemes to randomize the D/A element mismatch nonlinearity from dc to f_s, there-

fore, reducing the in-band nonlinearity in the same way as the quantization noise. Furthermore, mismatch shaping similar to noise shaping can be performed to further minimize the in-band nonlinearity. Many recent high-performance $\Delta-\Sigma$ A/D converters use a combination of high-order noise shaping and multi-bit quantization with DEM to achieve both high-resolution and high-speed.

5.2.3 Delta-Sigma Modulation in MEMS

In the past decade, the $\Delta-\Sigma$ modulation has been employed in MEMS capacitive sensors, specially in inertial sensors [7-9, 11 - 15, 43]. One reason of its popularity is that the $\Delta-\Sigma$ feedback loop can be implemented with only a little additional complexity based on the switched-capacitor readout scheme. However, most works in this area are limited to second-order single-bit modulators using the mechanical transducer itself to provide noise shaping. Because of the noise folding nature of switched-capacitor circuits, the circuit noise often dominates the overall noise floor. And in surface micromachined devices, the mechanical noise is also prominent. Thus, there has not been a great demand to investigate more advanced $\Delta-\Sigma$ techniques to minimize the quantization noise.
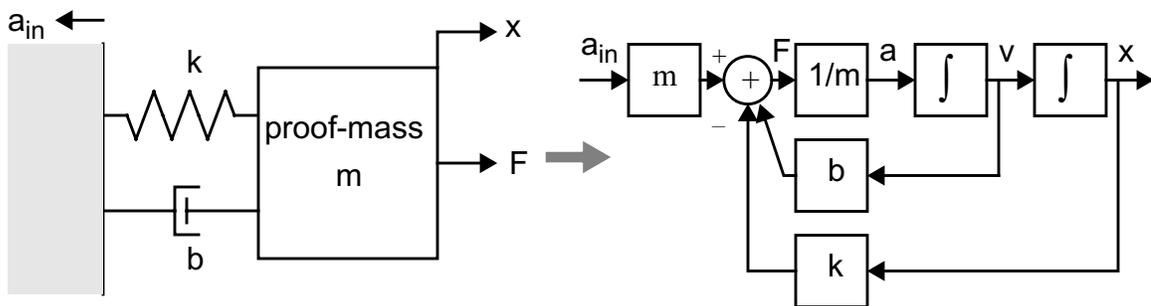
Figure 5-11: Second-order proof-mass/spring/damper system.

The mechanical sensing element of an accelerometer can be modeled as a proof-mass/ spring/damper system in Figure 5-11, which has a second-order transfer function:

$$T(s) = \frac{X(s)}{F(s)} = \frac{1}{ms^2 + bs + k} = \frac{1/m}{s^2 + \frac{\omega_r}{Q}s + \omega_n^2}. \tag{5-16}$$

It has two poles and has low-pass frequency response. Obviously, if enclosed in a $\Delta-\Sigma$ feedback loop, the mechanical transducer can provide noise shaping.

Reference [11] uses an overdamped bulk micromachined transducer to split two poles to high and low frequencies. The first-order noise shaping is realized by operating the $\Delta-\Sigma$ loop below the high frequency pole. Gas is filled into the package to achieve the over-damping. 15 b resolution in 5 Hz bandwidth is reported by this work. Surface microma-chined devices can not afford the overdamping, because the Brownian noise will be too large as the proof-mass is small. Reference [13] uses an underdamped transducer with Q of 1.6, fabricated by polysilicon surface micromachining, to provide noise shaping. A 2-tap FIR lead compensator is employed to stabilize the feedback loop. Dynamic range of 84 dB is reported in 100 Hz bandwidth. Both works are based on switched-capacitor sensor interface circuits and use 1-bit feedback. Multi-mode 1-bit $\Delta-\Sigma$ control is demonstrated by Fedder [8, 34] on a suspended polysilicon microstructure. In this work, a continuous-time unity-gain buffer is used for sensing and the total noise floor is dominated by quantization noise. Multi-mode control is very important for vacuum-packaged devices where undesir-able vibration modes must be suppressed.

5.3 Force-Balanced Delta-Sigma MEMS Accelerometer

5.3.1 Architecture

Figure 5-12 is the generic architecture of Δ–Σ force-balanced accelerometers. The loop filter H(z) provides compensation to the two-pole proof-mass/spring/damper structure to ensure the loop have sufficient stability margin. The loop filter could also provide additional noise shaping by incorporating integrators in the filter. The order of the modulator is defined as the total number of open-loop poles in the system. Since the mechanical structure has two poles, the systems without additional integrators are second-order modulators. If the loop filter contains L integrators, the modulator order is $L+2$. In electromechanical Δ–Σ modulators, the order of the system indicates the number of poles in the forward path transfer function, and does not reflects the order of noise shaping. This will be demonstrated in the simulation results presented in the next chapter. A single loop structure is shown because it is arguably the only practical configuration for electromechanical force-balanced feedback systems. The velocity of the proof-mass is not controlla-
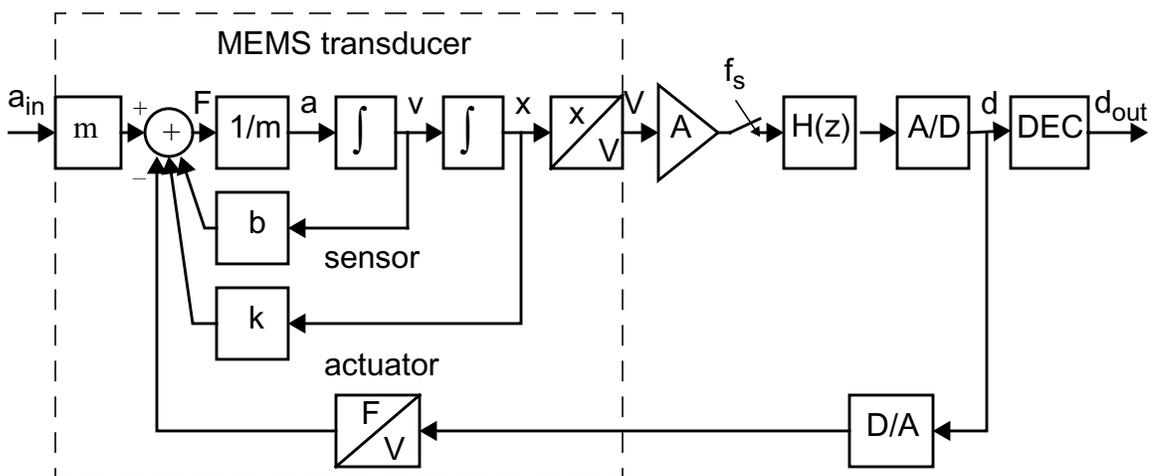
Figure 5-12: Generic architecture of Δ–Σ force-balanced accelerometers

ble. And because the sensor produces a weak signal, feedback at the sensing node is not desirable due to noise injection. Thus, interpolative structure with multiple feedback paths is not applicable. On the other hand, the micro-fabricate transducer exhibits large manu-facturing variations, and variations due to temperature, ambient charge and other environ-mental factors. The characteristics of the transducer are not precisely known during the design phase. Therefore, cascade structure (MASH) relying on accurate quantization noise cancellation cannot be used.

In this single-loop architecture, the loop filter must first provide compensation to the high-Q micromechanical resonator, therefore, it should have the following form:

$$H(z) = K \cdot (1 - \alpha_0 z^{-1}) \cdot \frac{1 - \alpha_1 z^{-1}}{1 - z^{-1}} \cdot \ldots \cdot \frac{1 - \alpha_n z^{-1}}{1 - z^{-1}} . \qquad (5\text{-}17)$$

The first term is a gain factor, the second term is a lead compensator that provides phase lead to the 2nd-order transfer function of the micromechanical transducer, and the other terms are integrators with lead compensation for additional noise shaping. With each pole being added at dc by an integrator, additional lead compensation is necessary to keep the loop conditionally stable. The loop filter must provide robust control to the proof-mass against parameter variations. The loop filters should be placed on the forward path so that the overall linearity of the system is not affected.

In a 2nd-order system, the sole function of the loop filter is providing compensation to ensure stability. The loop filter has a z-domain transfer function:

$$H(z) = K \frac{1 - \alpha z^{-1}}{1 - \alpha} . \qquad (5\text{-}18)$$

It is a lead compensator, or equivalently, a proportion-derivative (PD) controller [50]. The scaling factor is to normalize the system dc gain. The loop filter for the 3rd-order modulator has a transfer function in the form of:

$$H(z) = K\frac{(1 - \alpha z^{-1})(1 - \beta z^{-1})}{(1 - \alpha)(1 - z^{-1})}. \tag{5-19}$$

In the 3rd-order system, the loop filter also provides noise shaping. An integrator boosts the dc gain, while the two compensators are required to keep the loop stable. This is equivalent to a proportion-integral-derivative (PID) controller [50]. The design of the loop filter is more similar to linear feedback controllers than to conventional Δ–Σ converters.

As we have shown in the previous chapters, by eliminating noise folding, chopping signal at high frequency, and matching capacitance, the circuit noise in CMOS MEMS micromachined devices can be significantly reduced. The key to further improve the resolution of thin-film sensors is decreasing the ambient squeeze-film damping to obtain high Q. High-Q sensing elements have been avoided in previous works due to stability and settling concerns. In some cases, gas is deliberately filled into the package to reduce the Q. In this work, the Δ–Σ modulator is specifically designed for MEMS structure with Q over 100.

5.3.2 Challenges

The micromechanical transducer in the Δ–Σ feedback loop has high quality factor, low dc gain, and large variations. The high Q coupled with the large variations make the robust control of the transducer a challenging control problem. Due to the low dc gain, the equations in section 5.2.1 governing conventional Δ–Σ modulators are no longer valid and the

quantization noise is significantly higher than conventional Δ–Σ converters with the same order and OSR.

A high-Q underdamped system has two conjugate poles in the S-plane very close to the imaginary axis, as shown in Figure 5-13, and exhibits large peaking in its frequency response, as shown in Figure 5-14. The feedback control of such a plant is not trivial as the stability margin is very limited. Because of the inclusion of A/D nonlinearity, the linear control theory is not completely applicable to Δ–Σ feedback systems. This situation is further aggravated by the large manufacturing and environmental variations. The robust stability and robust performance must be achieved with an uncertain plant. Nevertheless, despite all these difficulties, we will demonstrate in the next chapter that the Δ–Σ modulation in fact provides very robust control to the high-Q MEMS structures.

Unlike conventional Δ–Σ converters which use integrator to obtain ideally infinite dc gain, the dc gain of the mechanical transducer is given by:

$$T_{dc} = \frac{1}{m\omega_n^2}. \tag{5-20}$$

The resonant frequency of the transducer is usually between 1 KHz and 10 KHz to get reasonable sensing bandwidth, hence, the dc gain is quite small. Given the same modulator order and OSR, the SNR of an electromechanical Δ–Σ modulator is much lower than predicted by equation (5-14). To achieve higher SNR or lower OSR, high-order modulators with integrators in the loop filter may be used to give additional noise shaping. As the implementation is restricted to single-loop architecture, higher-order modulators are more difficult to stabilize and have significantly reduced design space, which we will show in
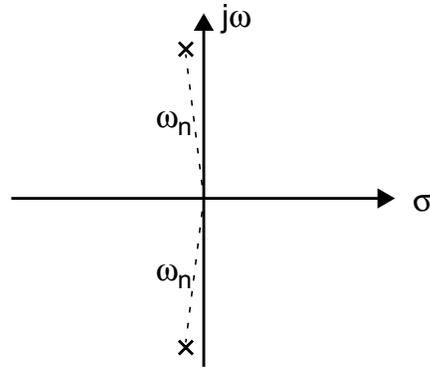
Figure 5-13: Two conjugate poles of a high-Q 2nd-order structure in S-plane.
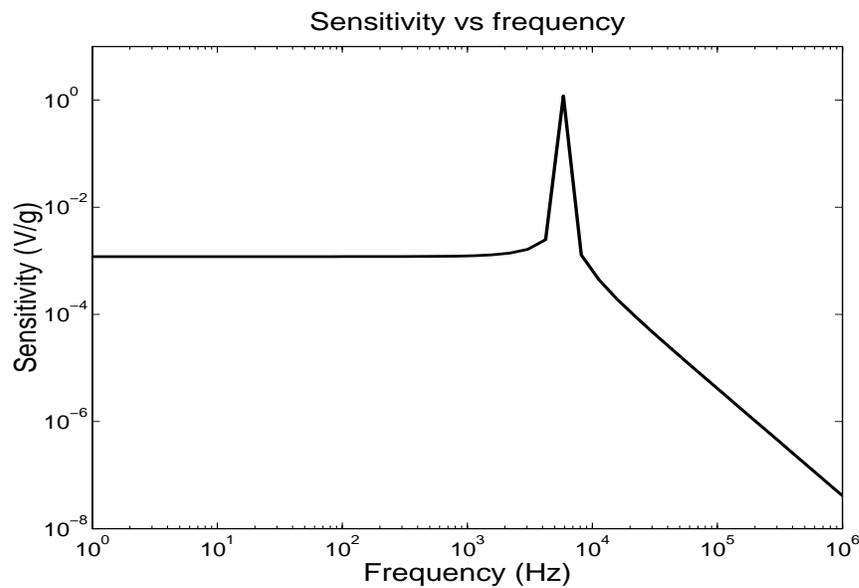
Figure 5-14: Peaking in frequency response of a high-Q 2nd-order structure.

the next chapter. Consequently, multi-bit feedback is very attractive because it lowers the quantization noise and improves the stability.

5.3.3 Design

The single-loop force-balanced Δ–Σ loop is similar to a linear feedback control loop except that a nonlinear quantizer is included in the loop. Therefore, techniques for designing and analyzing linear feedback control system could be used to aid its design.
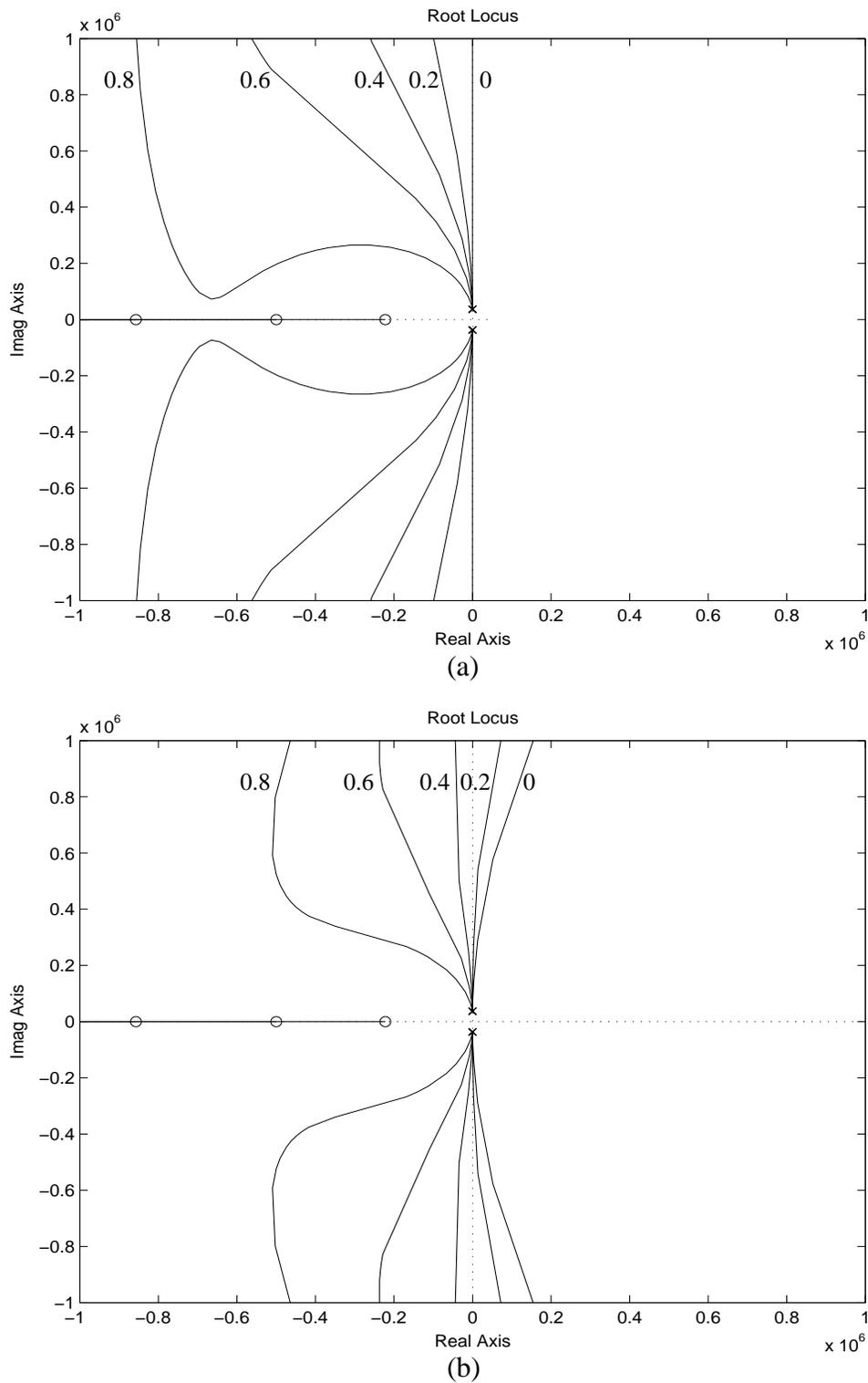
Figure 5-15: Root loci of the 2nd-order loop with compensation coefficient $\alpha = 0$, 0.2, 0.4, 0.6 and 0.8: (a) ideal 2nd-order system; (b) 2nd-order system with a 500 KHz 1st-order anti-aliasing filter. The open-loop Q is 1000.

Figure 5-15 shows the root loci of the 2nd-order loop with a lead compensator described by (5-18). Because the open-loop poles are effectively located on the imaginary axis, even a small perturbation will cause the system to become unstable. This is demonstrated in Figure 5-15(a), where an anti-aliasing filter with bandwidth of 500 KHz, about 100 times larger than the natural frequency, is sufficient to drive the system into instability. Therefore, deep compensation with α greater than 0.4 is required to stabilize the loop. The stability of the 3rd-order system is more difficult to achieve. With the anti-aliasing filter, the system is in fact a 4th-order system which is conditionally stable (so are 3rd-order systems) and becomes unstable when the loop gain is either too low or too high, as shown in Figure 5-16. Because the loop gain in $\Delta-\Sigma$ systems is signal dependent, very heavy compensation with β around 0.98 must be used to ensure stability in low gain condition.
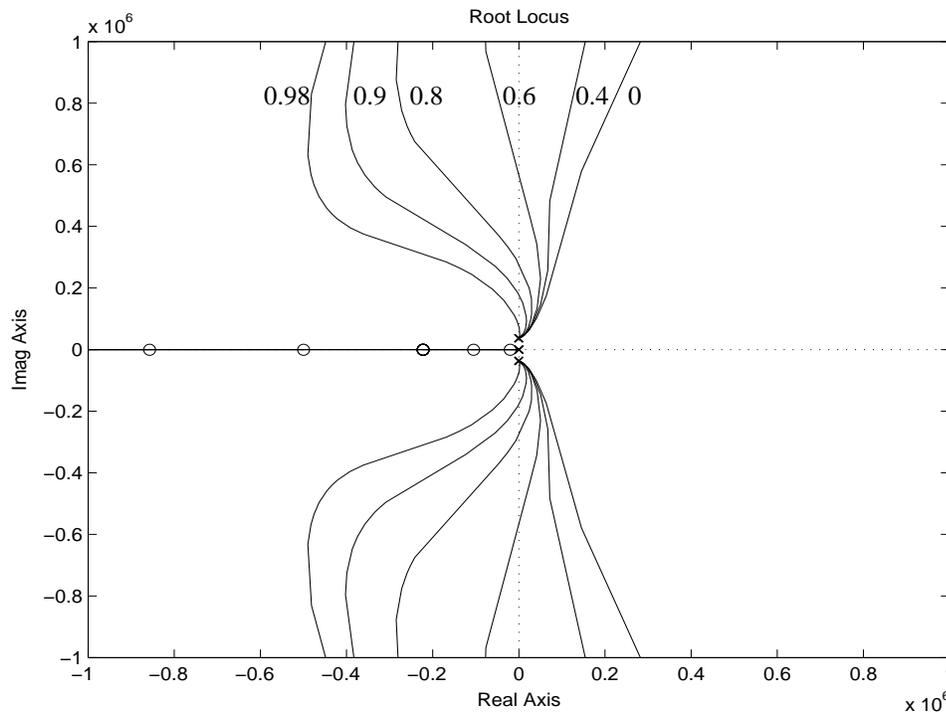
Figure 5-16: Root loci of the 3rd-order loop with compensation coefficients α = 0.8, and β = 0, 0.4, 0.6, 0.8, 0.9 and 0.98; a 500 KHz 1st-order anti-aliasing filter is included. The open-loop Q is1000.

The issue with limited stability margin due to very high open-loop Q is further compli-

cated by two other factors: the uncertain plant. e.g., the micromachined structure; and the

nonlinear element, e.g., the quantizer. Due to the nonlinear quantizer, the actual loop gain

is dependent on the input signal magnitude and is time varying. Therefore, even though

the linear analysis provides a starting point and some important insights to the loop design,

it could not fully predict the behavior of the Δ–Σ loop. The actual design of a force-bal-

anced Δ–Σ loop must be completed with in exhaustive simulations, combined with aggres-

sive robustness tests.

5.3.4 Quantization Noise Spectrum
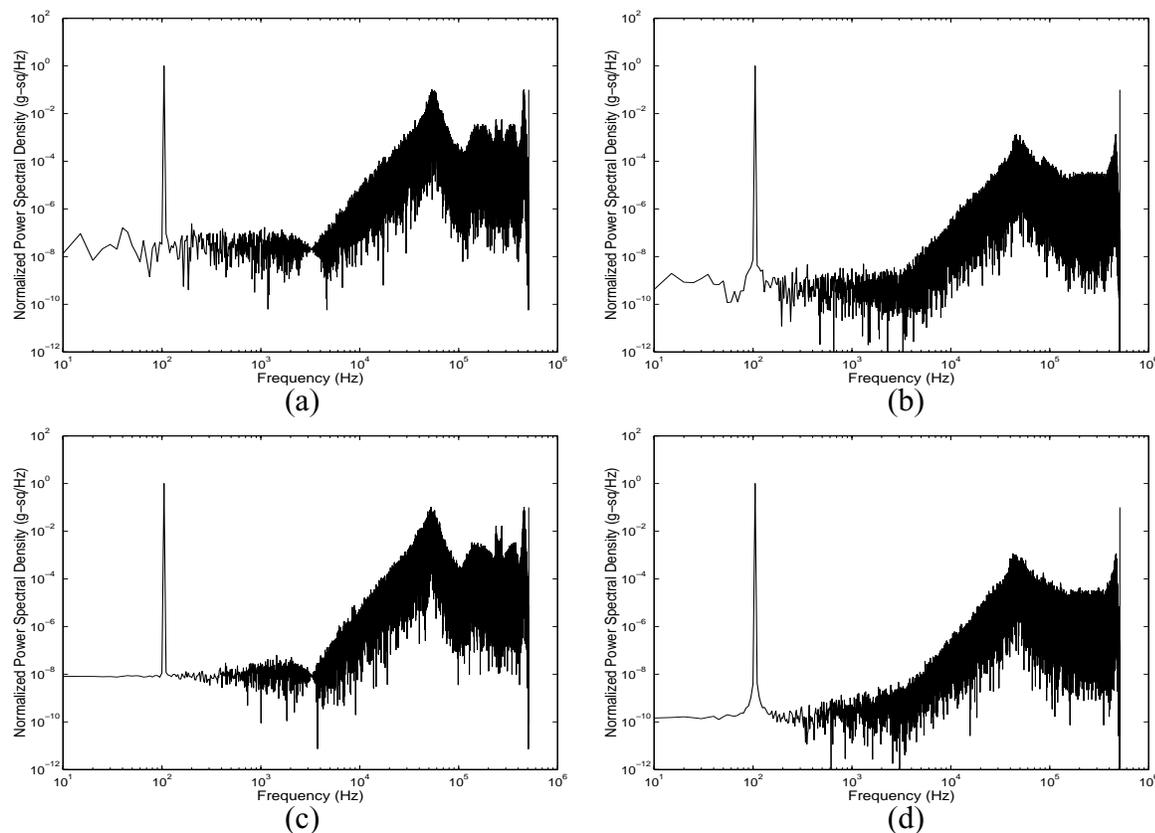
Figure 5-17:   Normalized power spectral density (PSD) of pre-decimation output bit stream of: (a) the 2nd-order 1-bit system; (b) the 2nd-order 3-bit system; (c) the 3rd-order 1-bit system; (d) the 3rd-order 3-bit system.
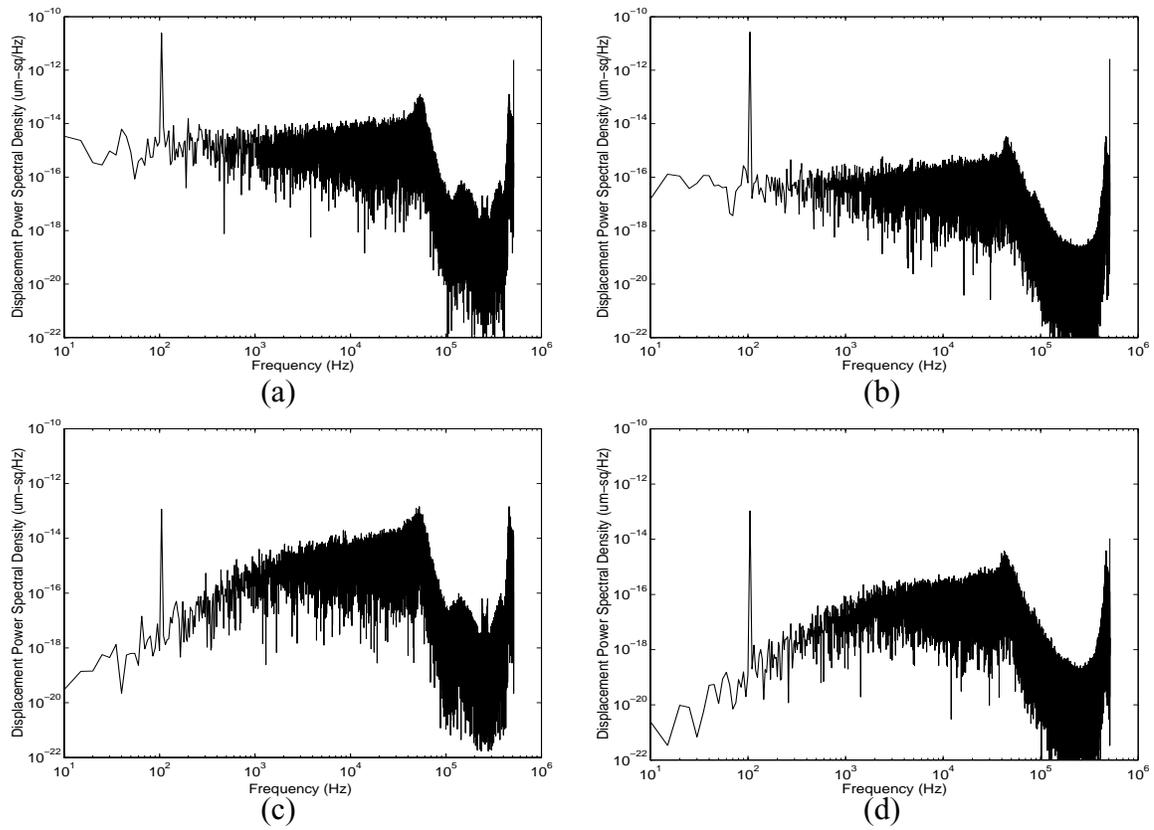
Figure 5-18: Power spectral density (PSD) of the proofmass displacement of: (a) the 2nd-order 1-bit system; (b) the 2nd-order 3-bit system; (c) the 3rd-order 1-bit system; (d) the 3rd-order 3-bit system.

The power spectral densities (PSD) of the output bit stream and the proofmass displacement are plotted in Figure 5-17 and Figure 5-18, respectively, for 2nd-order and 3rd-order modulators with 1-bit and 3-bit feedback. Effects of noise shaping can been seen clearly from these PSD plots.

5.3.5 Performance Metrics

The performance of $\Delta-\Sigma$ modulators are measured by signal-to-noise-and-distortion ratio (SNDR). When the input signal is small, the SNDR is determined by quantization noise power. When the signal approaches the full-scale of the modulator, the SNDR is dominated by harmonic distortions caused by nonlinearity.

The SNDR can be computed on decimated output data using the sinusoidal minimum error method [9, 52]. In this method, the input to the system under test is a sinusoidal signal, thus, the output is a sinusoidal signal plus distortions and noises:

$$
\begin{aligned}
s(t) &= \hat{s}(t) + e(t) \\
&= A\sin(2\pi ft + \Phi) + e(t)
\end{aligned} \tag{5-21}
$$

The least square estimation is used to find the best-fit sinusoidal signal that minimizes the mean square error between the actual output samples and this sinusoidal signal

$$
\begin{aligned}
\|e(n)\|_2 &= \|s(n) - \hat{s}(n)\|_2 \\
&= \sum_{n=1}^{N} (s(n) - A\sin(2\pi fnT_s + \Phi))^2
\end{aligned} \tag{5-22}
$$

The mean square error is minimized when its partial derivatives with respect to A and Φ are zero,

$$
\frac{\partial}{\partial A}\left(\sum_{n=1}^{N} (s(n) - A\sin(2\pi fnT_s + \Phi))^2 \right) = 0, \tag{5-23}
$$

$$
\frac{\partial}{\partial \Phi}\left(\sum_{n=1}^{N} (s(n) - A\sin(2\pi fnT_s + \Phi))^2 \right) = 0. \tag{5-24}
$$

Thus, the amplitude and the phase of the best-fit sinusoidal signal are given by

$$
A = \frac{2\sqrt{\left(\sum_{n=1}^{N} s(n)\sin(2\pi fnT_s) \right)^2 + \left(\sum_{n=1}^{N} s(n)\cos(2\pi fnT_s) \right)^2}}{N}, \tag{5-25}
$$

$$
\Phi = \operatorname{atan}\left(\frac{\sum_{n=1}^{N} s(n)\cos(2\pi fnT_s)}{\sum_{n=1}^{N} s(n)\sin(2\pi fnT_s)} \right). \tag{5-26}
$$

The difference between the system output and the best-fit signal is then the total error signal, which includes the harmonic distortions and noises. The signal power is calculated from the best-fit sinusoidal signal. And the total power of noises and distortions is computed from the error signal, which in the absence of dc offset, equals to the variance of the error signal. Therefore, the SNDR is given by

$$SNDR = 10\log\left(\frac{A^2/2}{var(e(n))}\right). \tag{5-27}$$

Based on SNDR, the input-referred power of noise and distortion in dB is calculated by

$$ND = 10\log(a_{in}^2/2) - SNDR. \tag{5-28}$$

and the average quantization noise floor is given by

$$\sqrt{\overline{n^2}} = \sqrt{10^{\frac{ND}{10}}/f_{BW}}. \tag{5-29}$$

In the accelerometer, the power of 1 g sinusoidal acceleration is used as the reference to measure the power of noise and distortion. Thus, the input-referred quantization noise uses dBg as its unit. In situations when the modulator is unstable, these performance specifications no longer have proper meaning. Sudden decrease of SNDR often indicates the modulator becomes unstable.

The performance metrics discussed above measure the quality of analog-to-digital conversion. The electromechanical $\Delta-\Sigma$ modulation has another main objective that is to provide feedback control to the MEMS transducer to achieve the optimum settling performance. The settling performance of a system is characterized by the overshoot of its step response and the settling time. For an underdamped 2nd-order system, the overshoot of the step response is given by [50]:

$$\text{Overshoot} = e^{-\dfrac{\pi}{\sqrt{4Q_c^2 - 1}}}.$$

(5-30)

The settling time to reach within 2% of the steady-state value is given by:

$$T_s = \frac{8Q_c}{\omega_n}.$$

(5-31)

Q_c is the overall quality factor of the system, which in our electromechanical $\Delta-\Sigma$ feed-back system, is the closed-loop quality factor. In systems with higher Q_c, the step responses have more overshoot and ringing, and settle slower. At very high Q_c, the over-shoot is equal to 1, meaning the amplitude of the ringing is equal to the final steady-state value, and the settling of the ringing is very slow, as shown in Figure 1. When $Q_c < 0.5$, the system becomes an overdamped system in which the settling time increases with decreasing Q_c because lower Q_c makes the system slower to follow the step input. The optimum settling occurs at $Q_c = 0.5$, which is called the critical damping point where there is no overshoot and the settling time is minimized. This relationship among overshoot, set-tling time and quality factor could be generalized to higher order systems. Therefore, the control performance of the electromechanical $\Delta-\Sigma$ modulator is characterized by its closed-loop quality factor, Q_c, which could be measured from the overshoot of its step response. The goal for the control system design is to make Q_c as close to 0.5 as possible.

5.4 Loop Filter Implementation

5.4.1 Loop Filter Structure

The loop filter described by (5-16) could be implemented by the structure shown in Figure 5-19. It is a cascade of a gain stage, a lead compensator and a series of integrators with lead compensation. Each stage is a discrete-time block that can be implemented by a switched-capacitor circuit with only one opamp. The capacitor matching accuracy in modern CMOS processes is about 0.1%, which corresponds to 10-bit coefficient accuracy [74]. To realize the loop filter by analog circuits in practice, we must be able to represent the loop filter coefficients by fewer than 10 bits. Filters with higher coefficient accuracy requirement can only be realized by digital hardware, such as 16-bit DSPs. This is a major subject that we will discuss in the next chapter.

5.4.2 Switched-Capacitor Circuit Implementation

Two key building blocks of the loop filter are the lead compensator and the compensated integrator. Both blocks could be realized by switched-capacitor circuits with single opamp. To realize accurate loop filter transfer function, correlated double sampling (CDS) could be used to minimize errors due to offset, 1/f noise and finite opamp gain [9, 41, 43 - 45, 61 - 63]. The lead compensator and the compensated integrator with CDS are shown in Figure 5-20 and Figure 5-21.

$$V_{in} \longrightarrow \boxed{K} \longrightarrow \boxed{1 - \alpha_0 z^{-1}} \longrightarrow \boxed{\frac{1 - \alpha_1 z^{-1}}{1 - z^{-1}}} \dashrightarrow \boxed{\frac{1 - \alpha_n z^{-1}}{1 - z^{-1}}} \longrightarrow V_{out}$$
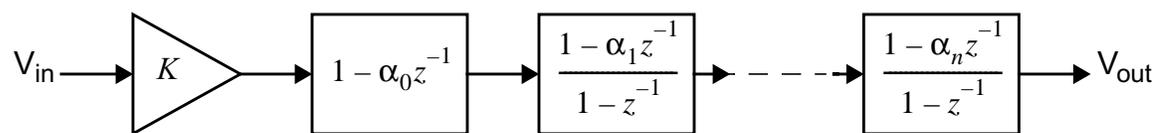
Figure 5-19: Loop filter structure for the single-loop Δ–Σ architecture.
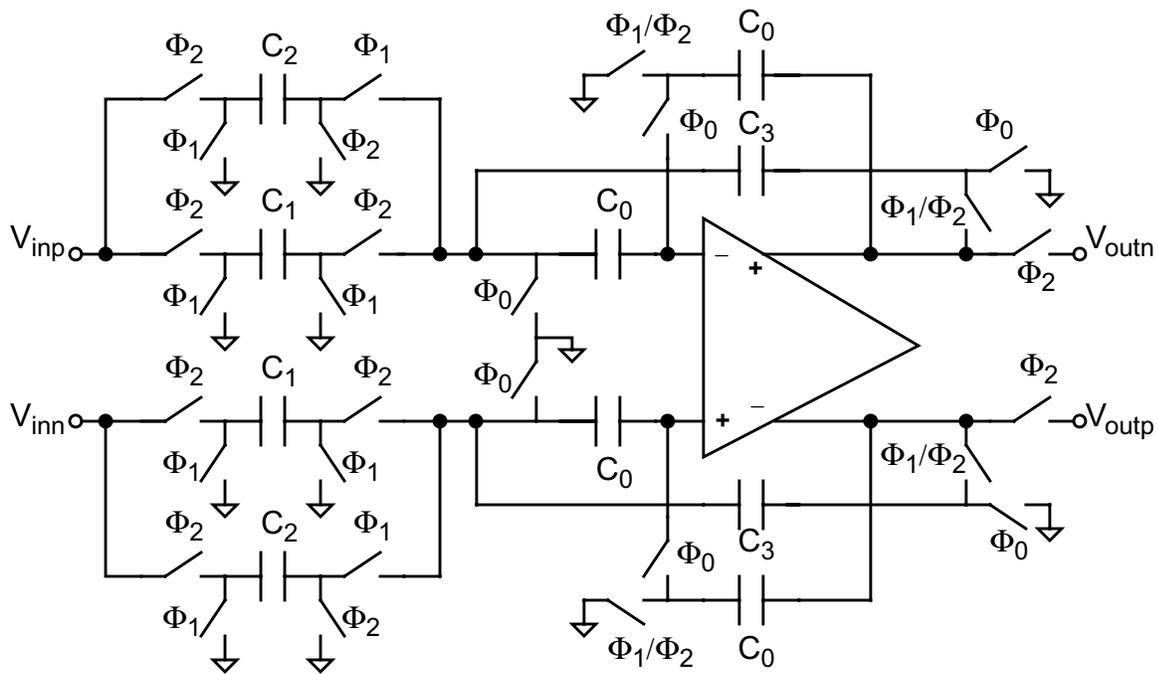
Figure 5-20: Switched-capacitor lead compensator with CDS.
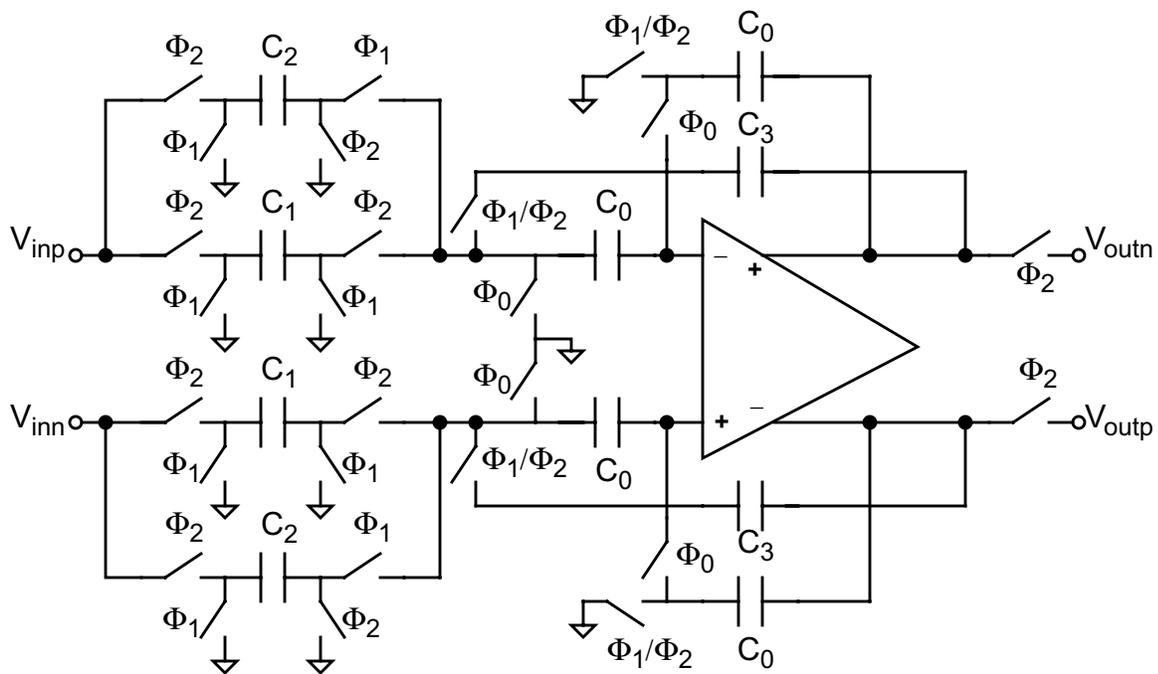
Figure 5-21: Switched-capacitor integrator with lead compensation and CDS.

The circuits in Figure 5-20 and 5-21 use a 3-phase clock scheme so that only one opamp is needed for each stage while the CDS can be performed. In the reset phase F_0, the charge due to error charge due to offset and other low frequency errors is stored on C_0 and an error-free virtual ground is created for C_3 in the rest of the clock cycle. In F_1, the charge stored on C_2 from the previous sample is pushed to C_3. And in F_2, a new sample is added to C_3 and stored on C_2 for the next clock cycle, while the output voltage stored on C_3 is sampled. The output voltages at the sampling time (F_2) are given by:

$$V_{out}(n) = \frac{C_1}{C_3} V_{in}(n) - \frac{C_2}{C_3} V_{in}(n-1), \tag{5-32}$$

and

$$V_{out}(n) = V_{out}(n-1) + \frac{C_1}{C_3} V_{in}(n) - \frac{C_2}{C_3} V_{in}(n-1), \tag{5-33}$$

respectively, for the lead compensator and the compensated integrator. The corresponding z-domain transfer functions are:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_3} - \frac{C_2}{C_3} z^{-1}, \tag{5-34}$$

and

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\frac{C_1}{C_3} - \frac{C_2}{C_3} z^{-1}}{1 - z^{-1}}. \tag{5-35}$$

By adding the previous sample to C_3 (F_1) before the current sample (F_2), an unit delay element is realized without employing another opamp. The lead compensator is basically a 2-tap finite impulse response (FIR) filter and is implemented by a 2-input switched-capacitor gain stage with a delay element in one signal path. The only difference between the

lead compensator and the compensated integrator is that the charge stored on C_3 is cleared in the reset phase (F_0) in the lead compensator, while in the integrator, the charge is accumulated across clock cycles to realize integration.

Because the CDS also minimizes the error due to finite opamp gain, and the use of CDS capacitor in the feedback path relaxes the opamp slew-rate requirement, low-power single-stage OTAs with gain of 40 - 60 dB and low slew-rate can be used. Since the feedback in the CDS reset phase is provided by CDS capacitors, the CDS capacitors C_0, could be significantly smaller than C_3 to save the circuit area. The fully differential topology reduces the common-mode noise, power supply noise and even-order distortions. However, the fully differential opamp requires a common-mode feedback circuit which is not shown in Figure 5-20 and 5-21. Also not shown are the small deglitching capacitors added to provide a continuous-time feedback even as all switches are off.

5.5 Multi-Bit Force-Balanced Feedback

5.5.1 Multi-Bit Control of Electrostatic Actuators

Compared to conventional Δ–Σ converters, the multi-bit feedback is more advantageous in MEMS sensor systems. Electromechanical Δ–Σ modulator requires much higher OSR to achieve the same SNR, which results in higher power consumption. The practical implementation issues dictate the use of single-loop architecture with design style similar to linear feedback controller. In such a single-loop structure, the high-order modulator has very limited stability margin and design space. Although theoretically feasible, we will see

that modulators with order higher than 3 are difficult to implement in practice. Alternatively, the multi-bit force-balanced feedback eases the stability problem, reduces the quantization noise, and makes the system closer to linear system so that linear feedback control theory can be better applied.

Realizing highly linear multi-bit feedback D/A is a challenging task that has motivated a great amount of research in dynamic element matching (DEM) [54 - 56]. This matter is further complicated in MEMS by the nonlinear nature of the feedback actuators. MEMS capacitive sensors use various types of electrostatic actuators. In CMU CMOS-MEMS process, the electrostatic actuator is formed by multi-layer parallel-plate capacitors, as shown in Figure 5-22. The actuation force has a square law relationship with the voltage across the two electrodes:

$$F = \frac{1}{2}\frac{\partial C}{\partial x}V^2.$$ (5-36)

This is a nonlinear actuation force which is also a function of the actuator offset. Designing a D/A to control the nonlinear actuator and realize robustly linear feedback is considerably more difficult than in conventional Δ–Σ converters.
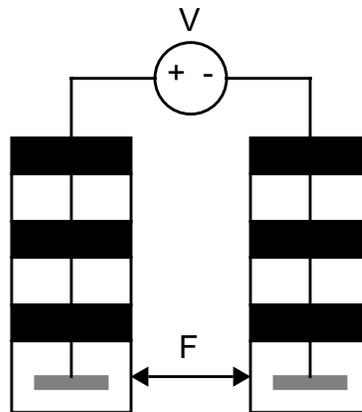
Figure 5-22: CMOS MEMS parallel-plate actuator
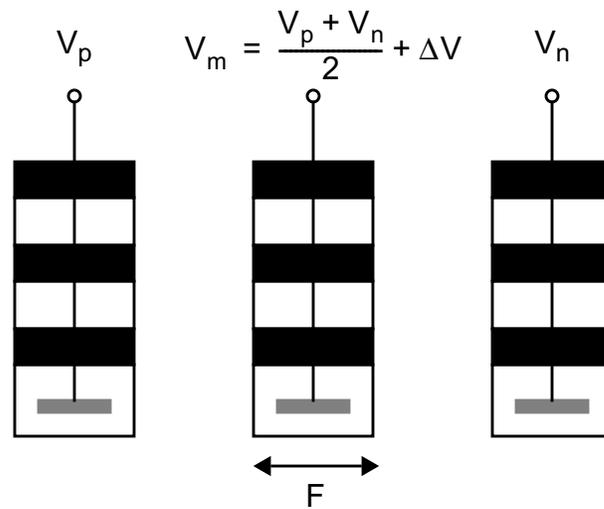
Figure 5-23: Differential CMOS MEMS parallel-plate actuator.

There are several ways to implement multi-bit force balanced feedback, including pulse amplitude modulation (PAM), pulse width modulation (PWM), and pulse density modulation (PDM). The PAM is most straightforward method in which the feedback force is controlled by applied voltage on the actuator. It requires a D/A to provide the actuation voltage. In parallel-plate electrostatic actuators, the force and the voltage have a square law relationship. When there is no offset, a differential actuator can be used to generate a force that is proportional to the voltage:

$$
\begin{aligned}
F &= \frac{\partial C}{\partial x}(V_P - V_N)\left(V - \frac{V_P + V_N}{2}\right) \\
&= \frac{\partial C}{\partial x}(V_P - V_N)\Delta V
\end{aligned}
\tag{5-37}
$$

The linearity of such a actuator is limited because it relies on perfect matching between two actuators to cancel the square term. This differential actuator is sensitive to offset and offset variation, thus, is not robust. The nonlinearity of the differential PAM actuator is shown in Figure 5-24.
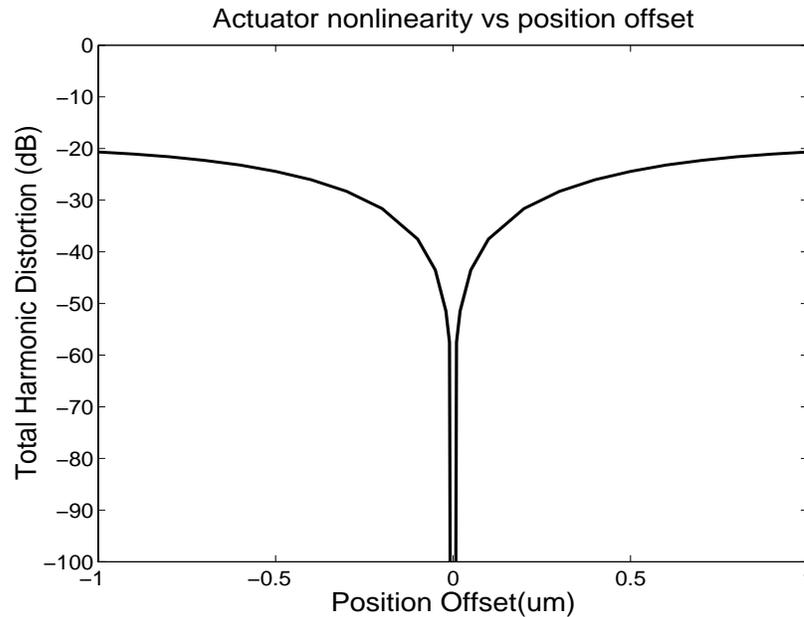
Figure 5-24: Nonlinear distortion versus position offset in differential actuator.

The fact that the differential electrostatic actuator is inherently bi-level can be exploited to realize linear multi-bit force-balanced feedback using time as the reference. Figure 5-25 shows such a bi-level digital actuator. Both the PWM and the PDM schemes use 2-level applied voltage to turn on and off the two sets of electrodes. The multi-bit actuation is realized by controlling the time duration for which one set of actuator electrodes are turned on within unit time period, thus, controlling the average actuation force. The linearity of the actuation depends on the timing accuracy. Since clock frequency can be set very precisely by crystal oscillators, highly linear actuators can be realized. Even when the clock has large timing jitter, or phase noise, due to its wide-band spectral characteristics, the effect of the jitter on system performance is minimized by oversampling and noise shaping in Δ–Σ systems. As shown in Figure 5-26, the PWM suffers from nonlinearity induced by finite rising and falling times of the pulses, specially when the clock frequency

is high and settling time is large compared to the clock period. Therefore, the PDM scheme is preferred because the number of rising and falling edges is proportional to the number of pulses, hence, no nonlinearity is generated as long as complete settling can be achieved between clock edges.
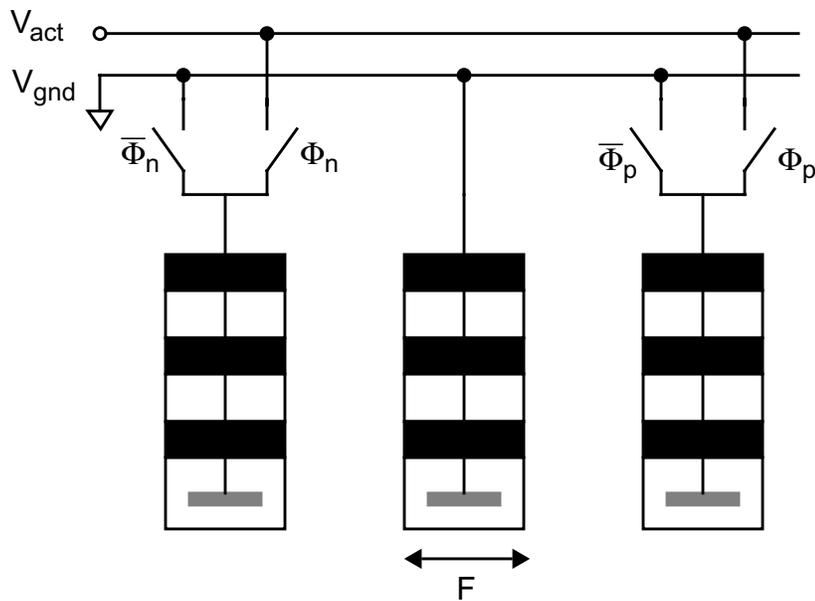
Figure 5-25: Bi-level digital actuator for PWM and PDM actuation.
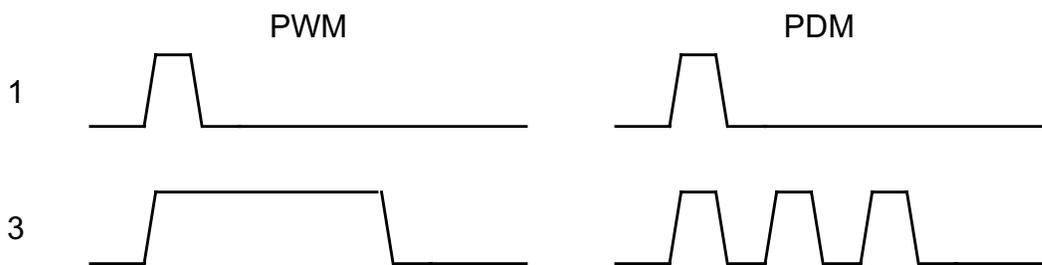

Figure 5-26: PWM and PDM.

5.5.2 Pulse Density Modulation

The PDM controls the number of unit return-to-zero (RZ) pulses within unit time period to realize multi-bit actuation. It can be easily implemented by digital circuit. Because the parallel-plate actuator is sensitive to the distance between the electrodes, the PDM still suffers from nonlinearities caused by the actuator offset and the displacement of the proof-mass when the input signal is large.

For multi-bit feedback, it is important to keep the displacement small even with large input signals. In a closed-loop system, this is done by increasing the gain on the forward path. A feedback system with large loop gain tends to go unstable more easily. It is design trade-off to choose a forward gain that minimizes the signal-dependent nonlinearity while maintaining sufficient stability margin. This will be clearly demonstrated in the next chapter.

Surface micromachined devices exhibit large offset and offset variation. It is often the case that it is impossible to pull the proof-mass back to zero-offset position while the sensor offset is cancelled by electronics. In such situations, the imbalance of actuation forces provided by two sets of actuator electrodes results in nonlinearity. One obvious solution is to calibrate the electrostatic actuator by applying different voltages across the two sets of electrodes to cancel the imbalance. However, the offset may change over time and it can be difficult to perform calibration in some situations. A actuation scheme less sensitive to the offset is very desirable.

We propose an electrostatic actuator driving scheme that is less sensitive to proof-mass position and is more robust against actuator offset. It is named complementary pulse density modulation (CPDM). As shown in Figure 5-27, the CPDM uses a combination of RZ

pulses of opposite polarities to compensate the offset nonlinearity. Denote F_P and F_N as the forces given by the two sets of electrodes, m as the N-bit input data, T_a and T_s as the pulse width and the sampling period, the average actuation force of regular PDM is:

$$\overline{F_a} = mF_P\frac{T_a}{T_s} \qquad (m > 0)$$
$$= mF_N\frac{T_a}{T_s} \qquad (m < 0)$$

(5-38)

and the average actuation force of CPDM is:

$$\overline{F_a} = m\frac{F_P + F_N}{2}\frac{T_a}{T_s} + (2^N - 1)\frac{F_P - F_N}{2}\frac{T_a}{T_s}.$$

(5-39)

The CPDM enables us to drive the two sets of electrodes with the same voltage while maintaining high linearity in a large range of offset. Simulations show that the 3-bit CPDM is able to maintain relatively high SNDR with offset up to 30% of the total actuator gap width. The side effect of CPDM is that it introduces an offset actuation force that is independent of the input data and this results in a dc offset at the output of the Δ–Σ modulator.

Although the CPDM is robust against actuator offset, it does not eliminate the signal-dependent nonlinearity. It is not possible to apply dynamic element matching (DEM) to differential electrostatic actuators and the spectral characteristics of this signal-dependent nonlinearity are not known. Nevertheless, a third PDM variation, named randomized PDM (RPDM), is proposed which randomly selects feedback pulse configuration between PDM and CPDM. By introducing some randomness, the RPDM attempts to whiten the signal-dependent nonlinearity and then reduce it as quantization noise. The signal-dependent nonlinearity apparently has different spectral characteristics than the white noise as the

RPDM scheme does not improve the SNDR by significant margin. The 3-bit RPDM does

though, achieves the best peak SNDRs for both 2nd-order and 3rd-order modulators.
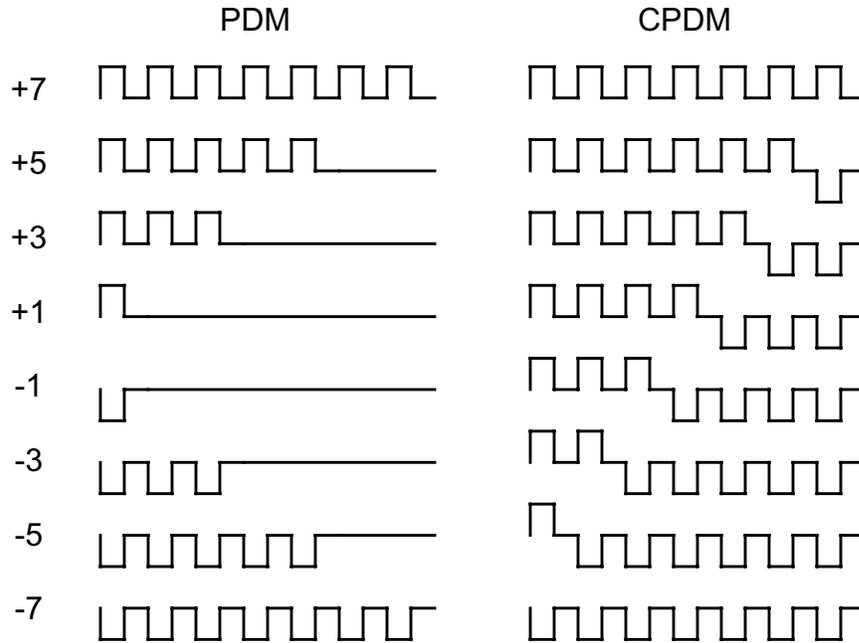
(a)
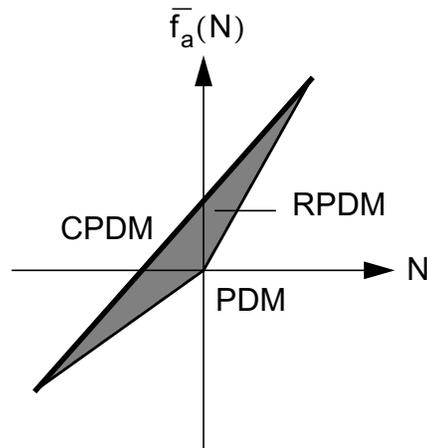
(b)

Figure 5-27: Multi-bit force feedback using pulse density modulation (PDM): (a) actuation pulse sequences of 3-bit regular PDM and complementary PDM (CPDM); (b) average actuation force per sampling period as a function of driving digital signal for PDM, CPDM and randomized PDM (RPDM).

5.6 Summary

This chapter introduces the force-balanced electromechanical delta-sigma modulation for high-Q MEMS structures. The $\Delta-\Sigma$ feedback loop needs to achieve three goals: high-resolution A/D conversion; suppression of nonlinearities and variations; and robust control of high-Q MEMS structures. It also faces three challenges: low dc gain; large frequency response peaking due to high Q; and nonlinear feedback actuators. A single-loop architecture with lead compensator and compensated integrators and its switched-capacitor circuit implementation are described to solve the first two issues. Offset-insensitive complementary pulse width modulation (CPDM) is proposed is to realize linear force feedback using nonlinear actuators.

Chapter 6

Simulation of Delta-Sigma MEMS Accelerometer

This chapter presents a simulation study on $\Delta-\Sigma$ accelerometers. This study aims to investigate the performance, the stability and the robustness of $\Delta-\Sigma$ systems with high-Q MEMS structures, and to explore the design space for practical implementation. A custom simulator is developed for this purpose. Systems with high-order noise shaping and multi-bit feedback are included in this study. The simulation results conclude that a practically realizable $\Delta-\Sigma$ modulator could achieve micro-g quantization noise floor and 100 dB dynamic range at oversampling ratio of 256, stabilize transducer with Q of 1000 to obtain near optimum settling behavior, and be very robust against parameter variations. The study proves that $\Delta-\Sigma$ modulation could accomplish three tasks: enabling high-Q operation to reduce thermal-mechanical noise; generating high-resolution digital output; and providing feedback linearization to suppress sensor nonlinearities and variations.

In the chapter, the simulation methods are introduced in section 6.1. Section 6.2 - 6.6 present the simulation results and discussions. A summary is given in 6.7.

6.1 Simulation Methods

6.1.1 Challenges

A $\Delta-\Sigma$ modulator is a nonlinear system that cannot be fully described by analytical models. Simulations are necessary to fully understand the operation of $\Delta-\Sigma$ modulators

and to design a practical system. In an oversampled system, the sampling frequency is much higher than the signal bandwidth. To simulate such as systems, the time step must be sufficiently small compared to the sampling period, while the time span must be large enough for the low-frequency signal. Hence, the simulation of $\Delta-\Sigma$ systems often requires extremely long transient runs. This is specially true for MEMS applications where the OSR is required to be larger than conventional converters. For example, if the OSR is 1000, the system bandwidth is 10 times of test signal frequency in order to find the harmonic distortions, and 10 signal periods are observed for the system to reach steady state, then the simulation will need to compute 10^5 samples, while the simulation step must be even smaller than the sampling period. It is not surprising for a simulation run to take more than 10^6 steps. The large amount of computation required when simulating $\Delta-\Sigma$ modulators demands that the simulation tool be very efficient. Circuit simulators such as SPICE and SPECTRE are very inefficient in simulating oversampled systems. General-purpose numerical simulation tools such as MATLAB also cannot meet the demand of efficiency.

6.1.2 Simulation Methods

Efficient time-domain simulation of $\Delta-\Sigma$ systems is realized by two approaches: behavioral macromodeling to simplify the system representation; and efficient numerical algorithm for solving the differential equations. A macromodel of CMOS MEMS accelerometer is described in Chapter 3. This is the most important component in electromechanical $\Delta-\Sigma$ modulator and has the most significant effects on the system behaviors. Simple behavioral models of other loop components, such as the amplifier, the loop filter,

the A/D converter and the feedback D/A are used [64, 65, 66]. Because the system is sampled, these components are described by difference equations.

To simulate the system in time-domain is to solve the ordinary differential equations (ODE) of the MEMS transducer and the difference equations of other components. Circuit simulators such as SPICE use implicit methods to solve the differential equations. The implicit methods employ a combination of numerical integration and nonlinear equation solving using Newton-Raphson iterations to ensure numerical stability. If the time step is automatically controlled, a stable implicit ODE solver can be quite efficient. But for oversampled systems such as Δ–Σ modulators, the time step must be smaller than the sampling period, and much smaller than the system time constants. This is main reason why SPICE is very slow in dealing with oversampled systems.

The oversampling nature of Δ–Σ modulators can be exploited to allow efficient simulation. First, because of the small time step, explicit methods with only numerical integration are employed to solve the ODEs with sufficient stability [67]. By eliminating the Newton-Raphson iterations, explicit ODE solvers not only improve the computation speed but also avoid the convergence problem. Second, because the circuit behaviors within the clock period have no significant impact on the overall system behavior, instant settling approximation [68] is used to reduce the number of simulation steps. Without simulating the circuit in detail within each clock period, the time step is chosen to be comparable to the clock period. The system is simulated in a clock driven fashion with each integration triggered by a clock event, as shown in Figure 6-1.
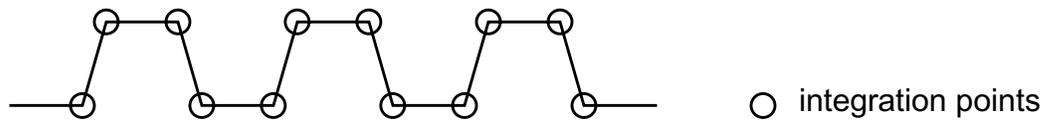
Figure 6-1: Clock driven simulation.

These methods are validated by small simulation examples. Compared to MATLAB simulations with implicit solvers plus automatic step control, they give the identical simulation output in much less time.

6.1.3 A Custom Simulator

The goals for this simulation study demand the simulation tool to be efficient and flexible. Custom tools can achieve high efficiency by avoiding all overhead, and be easily modified for different simulation tasks. Therefore, a custom simulator is developed in C++
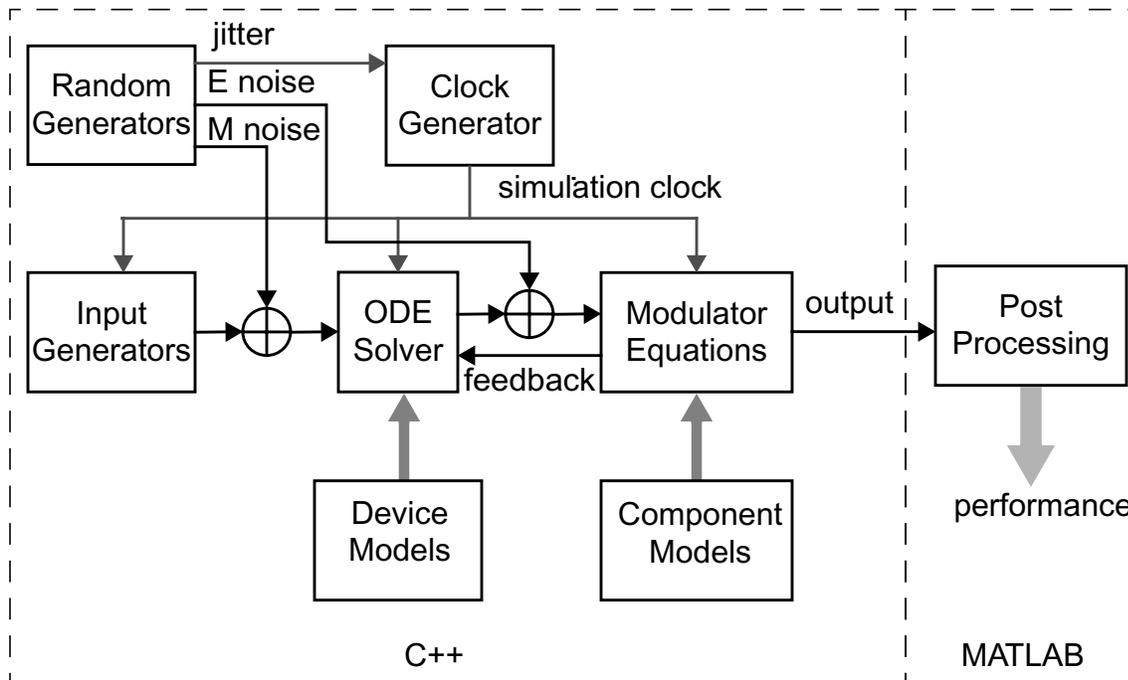
Figure 6-2: Block diagram of the behavioral simulator for electromechanical $\Delta-\Sigma$ systems.

programming language. The accelerometer model described in chapter 3, system compo-

nents such as amplifiers, continuous-time and discrete-time filters, A/Ds and D/As, vari-

ous signal sources and noise sources, and numerical solvers for differential equations and

nonlinear equations, are all written in C++ classes. These classes form an extensible

library of components and tools. Within this framework, nonidealities such as electronic

noise, Brownian noise, position offset and clock jitter, can all be modeled. The block dia-

gram of the simulator is shown in Figure 6-2.

After initial simulation test, a 4th-order explicit Runge-Kutta solver is chosen for all

simulations. For a system of ODEs in the general form of:

$$y' = f(t, y), \qquad (6\text{-}1)$$

where $y(t)$ and $y'(t)$ are vectors, the 4th-order Runge-Kutta method uses the following

formula to calculate the solution:

$$k_1 = f(t, y(t))\Delta t, \qquad (6\text{-}2)$$

$$k_2 = f(t + \Delta t/2, y(t) + k_1/2)\Delta t, \qquad (6\text{-}3)$$

$$k_3 = f(t + \Delta t/2, y(t) + k_2/2)\Delta t, \qquad (6\text{-}4)$$

$$k_4 = f(t + \Delta t, y(t) + k_3)\Delta t, \qquad (6\text{-}5)$$

$$y(t + \Delta t) = y(t) + \frac{1}{6}(k_1 + 2k_2 + 2k_3 + k_4). \qquad (6\text{-}6)$$

This simulator is able to compute 50,000 clock cycles in 280 CPU seconds on a 200

MHz Sun UltraSparcII workstation. The 64-bit double-precision float-point data format is

used throughout the computation, therefore, the numerical noise has no effect on the simu-

lation results, which is the case in some SPICE simulators. The efficiency and flexibility

offered by this simulator has been proven crucial in conducting this study. The following sections present the simulation results obtained by this simulator.

6.2 Stability

The z-domain transfer functions of the 2nd-order and 3rd-order modulators are given by:

$$H(z) = \frac{1 - \alpha z^{-1}}{1 - \alpha}, \qquad (6\text{-}7)$$

and

$$H(z) = \frac{(1 - \alpha z^{-1})(1 - \beta z^{-1})}{(1 - \alpha)(1 - z^{-1})}. \qquad (6\text{-}8)$$

The coefficients of lead compensation, α and β, directly affects the stability of the feedback system. At low values of compensation coefficients, the system is undercompensated and less stable, thus, limit cycles move to lower frequencies causing degradation of performance. If the coefficients are too small, the modulator becomes unstable. At high values of these coefficients, the system is overcompensated and the noise shaping is reduced with the quantization noise floor increased. And there are optimum values of compensation coefficients that achieve the lowest quantization noise.

Simulations are performed to find out how the compensation affects the stability and performance, specially under high Q condition. The noise and distortion power versus compensation coefficient of 2nd-order modulators is plotted in Figure 3 for Q of 1, 10, 100, and 1000. When the system is unstable, the noise and distortion power can no longer be properly calculated, and shows abnormally high values. As shown in Figure 3, the opti-
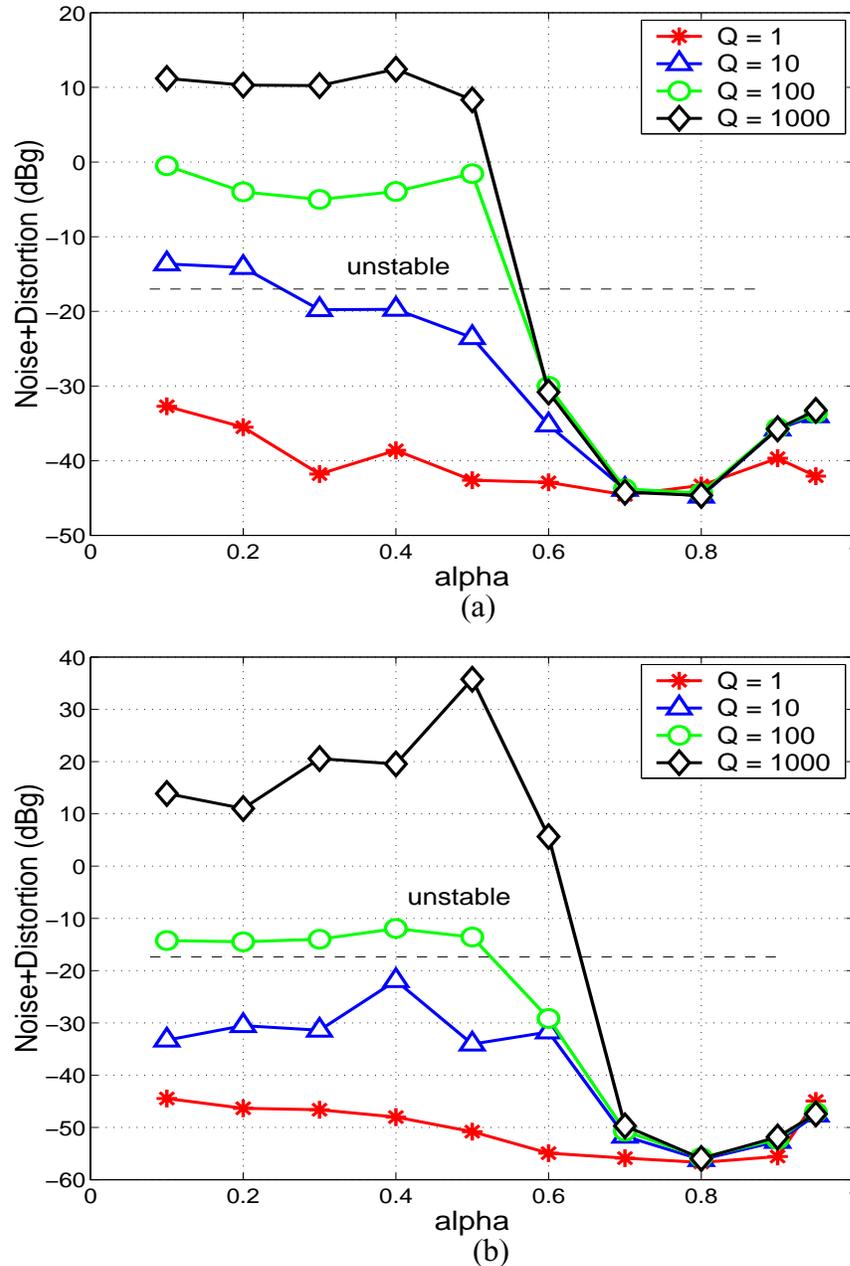
Figure 6-3: Total power of noise and distortion versus lead compensation coefficient (alpha) at different Q factors of: (a) the 2nd-order 1-bit system; (b) the 2nd-order 3-bit system.

mum compensation is achieved at α value close to 0.8. The system performance is much more sensitive to the compensation at high Q value. When Q is high, deviation from the optimum compensation causes the system to go unstable rapidly, while at low Q, it just

results in moderate increase of quantization noise. This result is expected. It proves that

for systems with high-Q transducers, finding the optimum compensation point is very

important. It is also found that the stability and performance of the system are similar at Q

of 100 and 1000, suggesting the results would be valid for even higher Q factors.

   The results of the 3rd-order modulator is shown in Figure 6-4. The first lead compen-

sator is fixed at optimum compensation coefficient (α) of 0.8. The inclusion of the integra-

tor boosts the optimum performance but further reduces the design space. For high Q

structures, there is a very sharp transition from stable to unstable. The system needs to be

compensated more deeply with value of β greater than 0.92 to maintain stability. This

result is predicted by the root locus analysis in section 5.3.3. Although the design space is

more limited, a compensation coefficient between 0.92 and 0.99 could still be accurately

implemented by analog integrated circuits with 0.1% matching accuracy or 8-bit digital
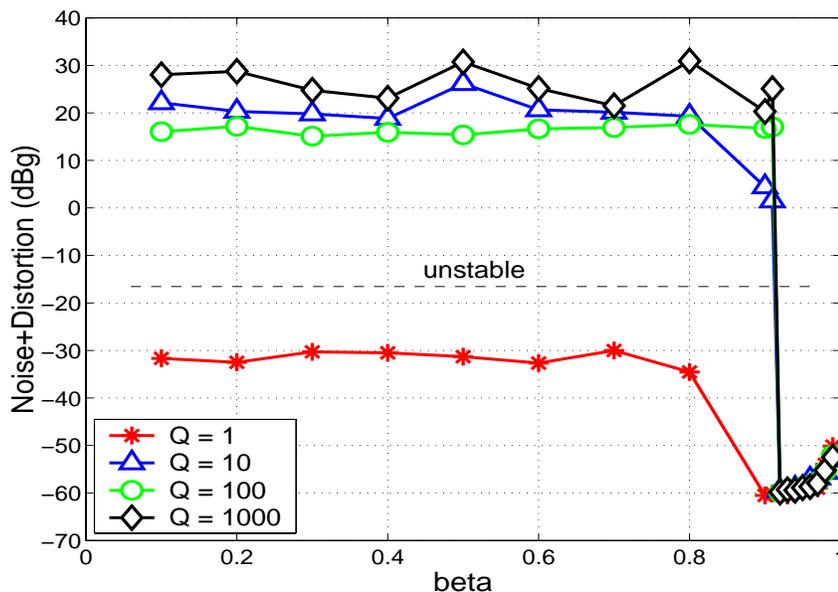
Figure 6-4: Total power of noise and distortion versus second lead compensation coefficient (beta) at different Q factors of the 3rd-order 1-bit system.

hardware. However, for 4th or higher order system, the design space is expected to shrink further, and hardware implementation will become increasingly difficult.

6.3 SNDR and Dynamic Range

In this study, the signal-to-noise-plus-distortion ratio (SNDR) is plotted versus magnitude of input acceleration. The dynamic range (DR) and the peak SNDR are found from the simulation data. These parameters determine how well the $\Delta-\Sigma$ accelerometer converts the analog acceleration signal into the digital output data and define its performance. The SNDR of the system is determined by quantization noise at low signal level, and by non-linear distortions when the signal level approaches the full scale.

In all simulations, the input signals are 200 Hz sinusoidal signals. The decimation filter bandwidth is 2 KHz. The resonant frequency of the MEMS accelerometer is 5.87 KHz. The system sampling frequency is 1.024 MHz, therefore, the OSR is 256. The system is simulated for 0.1 second, which includes 20 signal clock cycles, 400 decimated data points and 10^5 sampling periods. Mechanical Q of 1000 is used in all simulations. The actuation voltage for digital force feedback is 5 V.

6.3.1 SNDR of 1-Bit Modulators

The SNDR versus input acceleration of 1-bit modulators are plotted in Figure 6-5. The peak SNDRs of the 2nd-order and the 3rd-order modulators are 62.6 dB and 74.9 dB, respectively, significantly lower than the ideal value of 74.9 dB and 115.3 dB predicted by equation (5-15). The SNDR gain by 3rd-order modulator is smaller than prediction by a very large margin. For 1-bit modulators that are inherently linear, the SNDR loss can only be attributed to higher quantization noise. This can be explained by the low dc gain of the
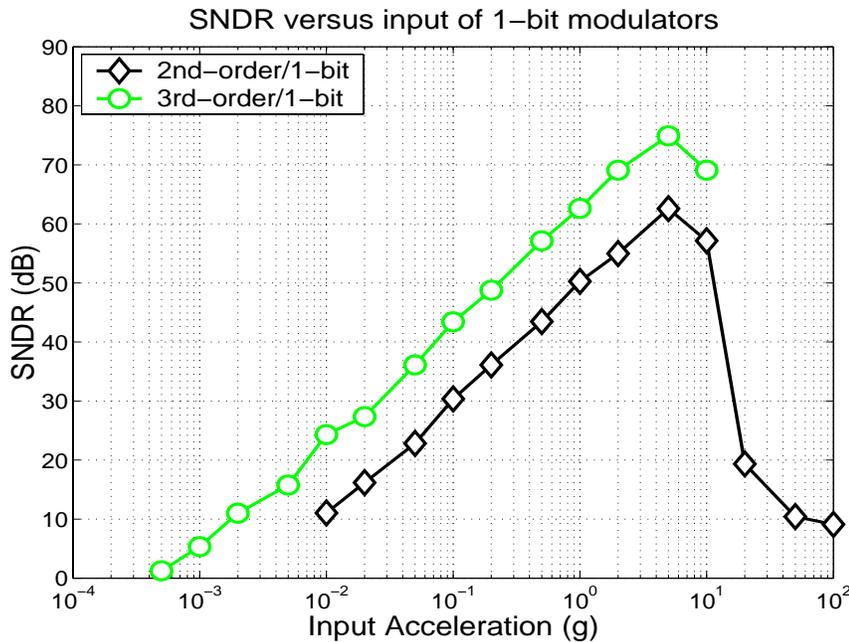
Figure 6-5: SNDR versus input acceleration of: the 2nd-order 1-bit system; the 2nd-order 3-bit system; the 3rd-order 1-bit system; and the 3rd-order 3-bit system. The loop gain is 200. The Q is 1000. The decimation filter bandwidth is 2 KHz.

MEMS accelerometer. Although the MEMS structure has two poles, these poles are not located at dc frequency, but at 5.87 KHz. Therefore, the 2nd-order proof-mass, spring, damper system provides less than the first order noise shaping. By including an integrator in the loop, the 3rd-order modulator just realizes the full 1st-order noise shaping.

The 1-bit modulators show very good linearity until saturation. The 3rd-order modulator becomes unstable when the input signal is larger than 10 g. The 3rd-order system is conditionally stable, and stability is affected by the magnitude of the input signal [51, 58].

6.3.2 SNDR of Multi-Bit Modulators

The SNDR curves of 3-bit modulators are shown in Figure 6-6. In section 5.5, we introduce the pulse density modulation (PDM) method and its variations to realize digital force feedback. The 3-bit modulators studied here use PDM, CPDM and RPDM feedback.

At small signal level, the 3-bit modulators improve the SNDR by 10 - 15 dB over 1-bit systems. The peak SNDRs of the 2nd-order and the 3rd-order modulators are 76.4 dB and 79.4 dB, respectively, gains of 13.8 dB and 4.5 dB over 1-bit systems. The 3-bit quantization reduces the quantization noise floor and the minimum detectable signal (MDS) by about 12 dB and extend the dynamic range in the lower end by the same amount. The minimum detectable signal for 3rd-order 3-bit modulator is 100 ug (RMS). This translates to a 2.3 µg/rtHz quantization noise floor. As in the 1-bit case, the 3rd-order modulator becomes unstable with input signal magnitude greater than 10 g.

With the multi-bit feedback, harmonic distortions are introduced by nonlinear feedback force. From the SNDR curves, the nonlinearity becomes obvious when the amplitude of input signal is greater than 0.5 g. As the result, the gains in peak SNDR and total dynamic range are less than the predicted value of 12 dB. When the gain in the forward path is not sufficiently large, the system exhibit a sharp SNDR drop between 1 g and 5 g input levels. This performance degradation due to nonlinear distortions is intolerable.

The nonlinearity of feedback actuation force is displacement-dependent, hence, is also signal-dependent. This nonlinearity is more complex than element mismatch in conventional converters and is more difficult to compensate. Figure 6 shows that the three PDM variations, PDM, CPDM and RPDM, differ little in distortion performances, while the RPDM scheme yields the best peak SNDRs in both examples. The effective way to reduce the distortion is to minimize the displacement in response to the input acceleration. This is done by increasing the gain in the forward path. It should be noted that higher-order noise shaping cannot achieve the same objective because what needs to be maximized is not just the dc gain but the gain at all frequencies. A 10x increase of forward gain yields substan-
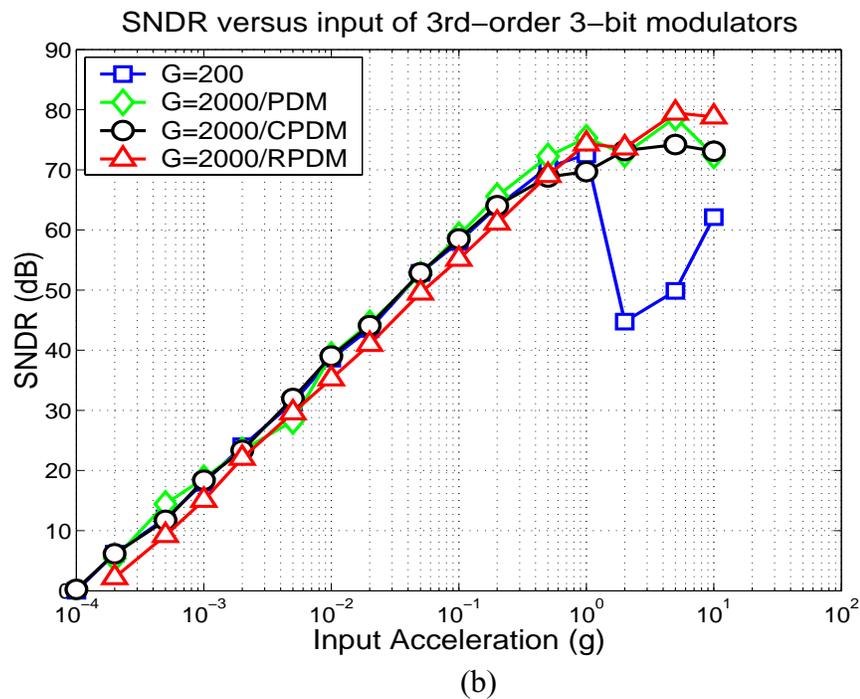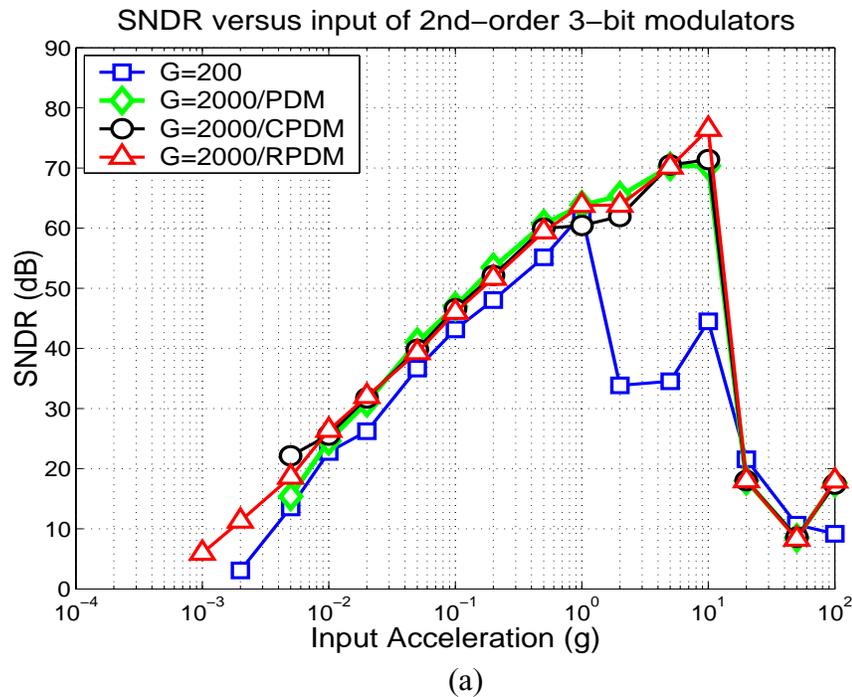
Figure 6-6:   SNDR versus input acceleration with different loop gain and PDM coding schemes of: (a) the 2nd-order 3-bit system; (b) the 3rd-order 3-bit system. The Q is 1000. The decimation filter bandwidth is 2 KHz.

tial improvement in distortion performance, eliminating the SNDR drop and obtaining 30

dB SNDR gain at 5 g input. Since too large a gain will destabilize the system, design

trade-off must be made between distortion performance and stability margin.

6.3.3 Comparison

All four SNDR curves of the 2nd-order and the 3rd-order modulator with 1-bit and 3-bit feedback are re-plotted in Figure 6-7. The performance of electromechanical Δ–Σ modulator is limited by two factors: inadequate noise shaping resulted from low dc gain of the transducer; and displacement-dependant nonlinearity of multi-bit actuation force. The peak SNDRs and the dynamic ranges of the four systems are listed in Table 6-1 and Table 6-2. The dynamic range is defined as the range between the MDS and the input level where the SNDR starts decreasing rapidly due to saturation. The performance gains of both higher-order noise shaping and multi-bit quantization are significantly smaller than
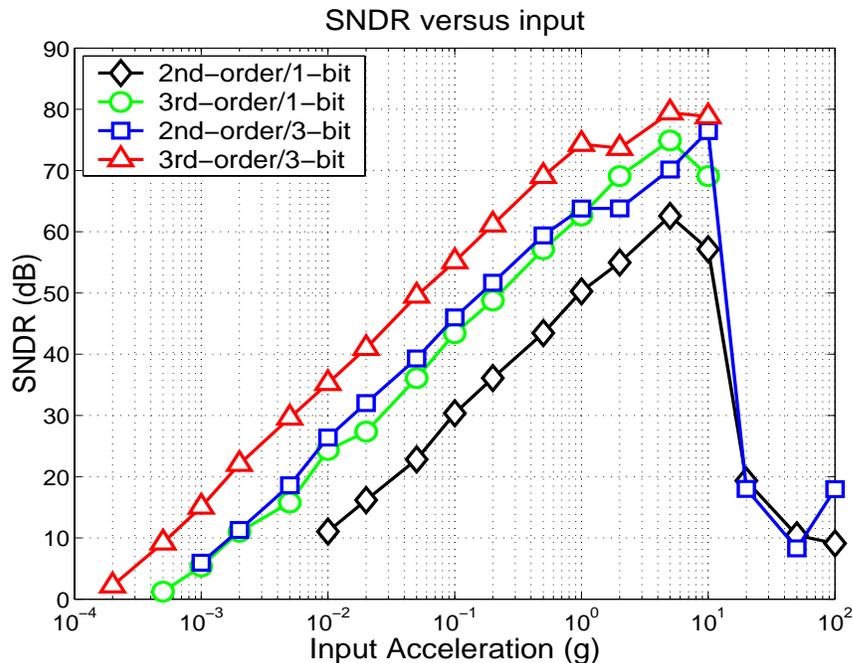
Figure 6-7: SNDR versus input acceleration of: the 2nd-order 1-bit system; the 2nd-order 3-bit system; the 3rd-order 1-bit system; and the 3rd-order 3-bit system. The loop gain is 2000. The RPDM is used for multi-bit systems. The Q is 1000. The decimation filter bandwidth is 2 KHz.

the predicted values in Table 5-1. Nevertheless, the 3rd-order 3-bit modulator achieves 100 dB dynamic range, equivalent to 16 bit resolution. Considering the difficulties in implementing high-order modulators, multi-bit feedback is a more proper approach to further performance improvement.

Table 6-1: Peak SNDR of $\Delta-\Sigma$ accelerometer with OSR of 256.

	1-bit	3-bit
2nd-order	62.6 dB	76.4 dB
3rd-order	74.9 dB	79.4 dB

Table 6-2: Dynamic range of $\Delta-\Sigma$ accelerometer with OSR of 256.

	1-bit	3-bit
2nd-order	60 dB	80 dB
3rd-order	86 dB	100 dB

6.4 Robustness

MEMS devices suffer from a plethora of nonidealities, such as: nonlinearities, offsets, parameter uncertainties caused by manufacturing variations and environmental factors, and undesirable modes of motion. The utmost goal of closed-loop feedback is to enhance the performance by desensitizing the system from some of the nonidealities, in another word, suppressing these nonidealities. On the other hand, since the closed-loop system has the potential to become unstable, it may be more sensitive to some nonidealities. Thus, robustness against all nonidealities is extremely important for closed-loop systems. In fact, one major concern over the practicality of closed-loop MEMS systems, particularly the oversampled loops, is their robustness.

The $\Delta-\Sigma$ loop is effective in desensitizing the system from nonlinearities other that the nonlinearity in the feedback actuator. The effects of mechanical Q variations are studied in section 2. In this study, we investigate how the system stability and performance are affected by: the offset, the variations of the resonant frequency and the transducer gain; the bandwidth of anti-aliasing filter; and the motion in z-axis. As in section 3, Q of 1000 is used throughout the study. The results show that the 2nd and 3rd-order $\Delta-\Sigma$ modulators are very robust against various nonidealities. These systems function very well over a large range of parameter variations. And the CPDM digital feedback scheme introduced in section 5.5 shows superior robustness against sensor offset.

6.4.1 Effect of Offset

The large position offset of thin-film devices poses a challenge to closed-loop systems. An additional offset cancelling actuator is often needed to pull the proof-mass back to cen-

ter position, which not only competes for limited device area with sensing and feedback functionality, but also often requires high voltage. The electronic offset cancellation described in chapter 4 makes it possible for devices to operate under relatively large position offset. It is then very desirable for closed-loop systems to also operate robustly under position offset.

The modulators are simulated with position offset from 0 to 1 μm under 1.5 μm nominal gap distance. This offset range is realistic for CMOS MEMS accelerometers. Electronic offset cancellation is implemented to prevent the electronic components from saturation. 3-bit modulators with PDM, CPDM and RPDM feedbacks are tested to compare their offset tolerances. The electrostatic actuators on two opposite sides are driven by 5 V. The SNDR versus position offset is plotted in Figure 6-8. As expected, the CPDM digital actuation scheme has far superior offset tolerances, maintaining good linearity and high SNDR at offset up to 0.5 μm. On the contrary, the other two methods are not robust against offset. Even at 0.1 μm offset, they experience 30 - 50 dB SNDR loss due to the nonlinearity described in section 5.5. If the devices are expected to operate under offset, the CPDM method should be used to realize digital force-balanced feedback.

Not only does the position offset introduce nonlinear distortions into the system, the imbalance of actuation forces may destabilize the loop. When the offset is greater than 0.5 μm, the modulators become unstable. In such situation of excessive offset, the actuators on opposite sides must be driven by different voltages such that they can provide forces of the same magnitude in the opposite directions. Calibration is needed to set the driving voltages. The SNDR results with calibration is shown in Figure 6-9. The calibration signifi-

cantly improves the SNDR and the stability of the modulators. However, additional

resources are required and it is not always possible to perform calibration.

(a)

(b)
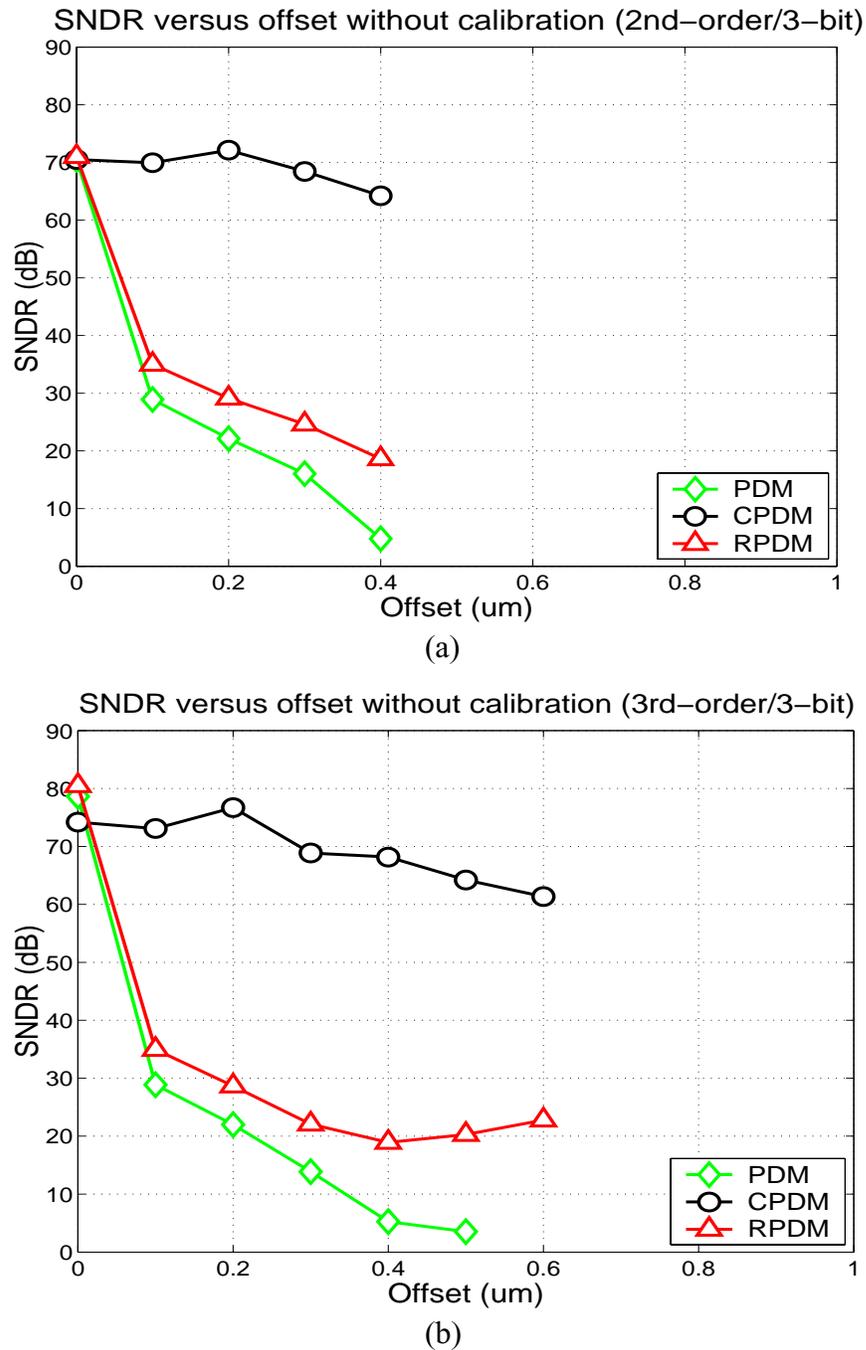
Figure 6-8: SNDR versus position offset without calibration for: (a) 2nd-order/3-bit modulators; (b) 3rd-order/3-bit modulators. The input acceleration is 5 g. The Q is 1000. The actuation voltage is 5 V.
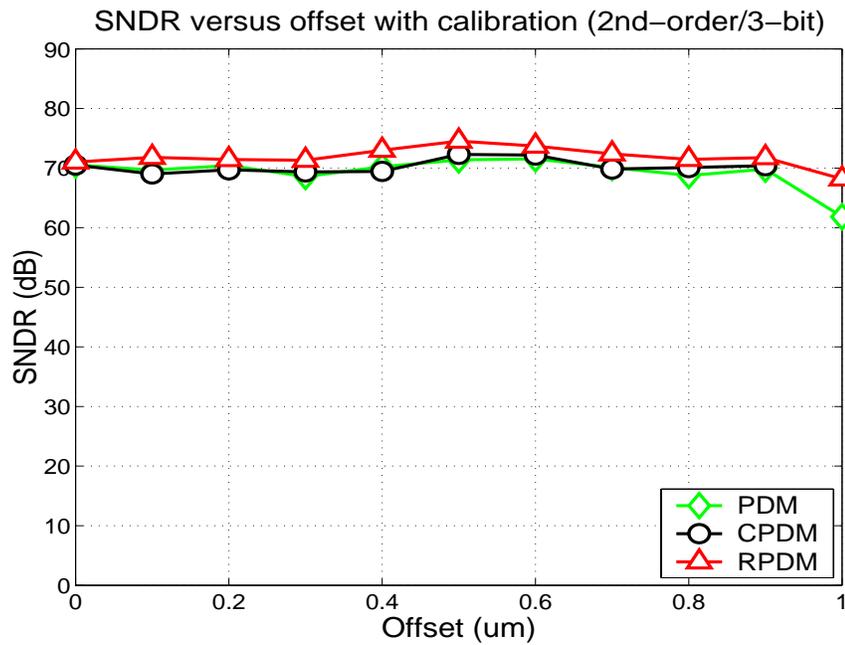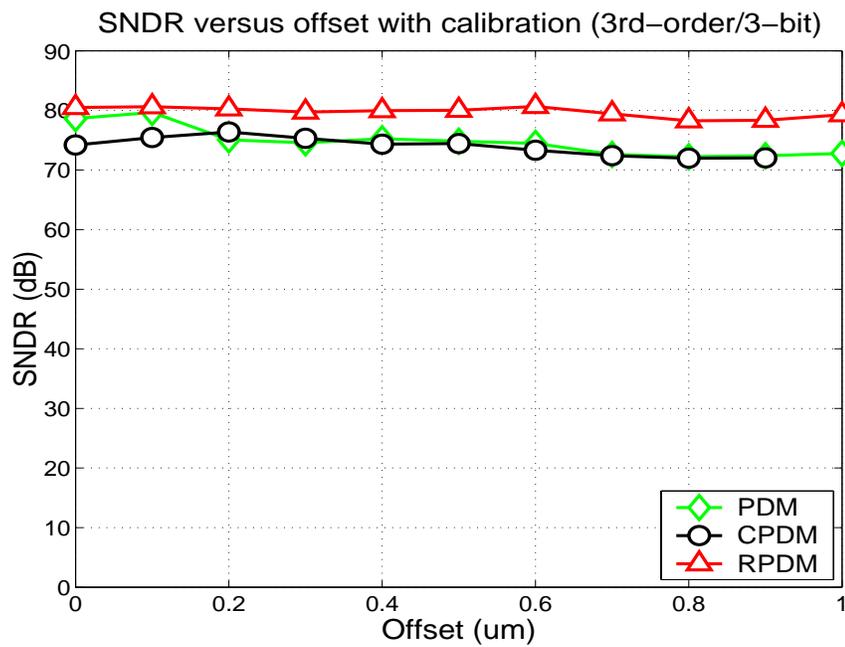
Figure 6-9: SNDR versus position offset with calibration for: (a) 2nd-order/3-bit modulators; (b) 3rd-order/3-bit modulators. The input acceleration is 5 g. The Q is 1000. The actuation voltage is calibrated.

6.4.2 Effect of Transducer Gain

The gain on the forward path is determined by both the transducer sensitivity and the gain of the interface circuit. Micromachined transducers and analog integrated circuits have large manufacturing and temperature variations. Single-bit modulators are not sensitive to the gain due to the existence of the 1-bit comparator. For multi-bit systems, the gain has great influence on the distortion performance and the loop stability. The SNDR versus forward gain for 3-bit modulators with 5 g input signal is shown in Figure 6-10. The 5 g excitation is chosen because it is close to full-scale so that large-signal nonlinear effects can be revealed. At low gain, the displacement is large, causing large harmonic distortions. At high gain, the SNDR increases as nonlinearity decreases. When gain is excessively high, the compensation becomes insufficient and the system becomes unstable. Considering the importance of the forward gain and its large variations, it is desirable to have gain programmability for optimizing the performance.
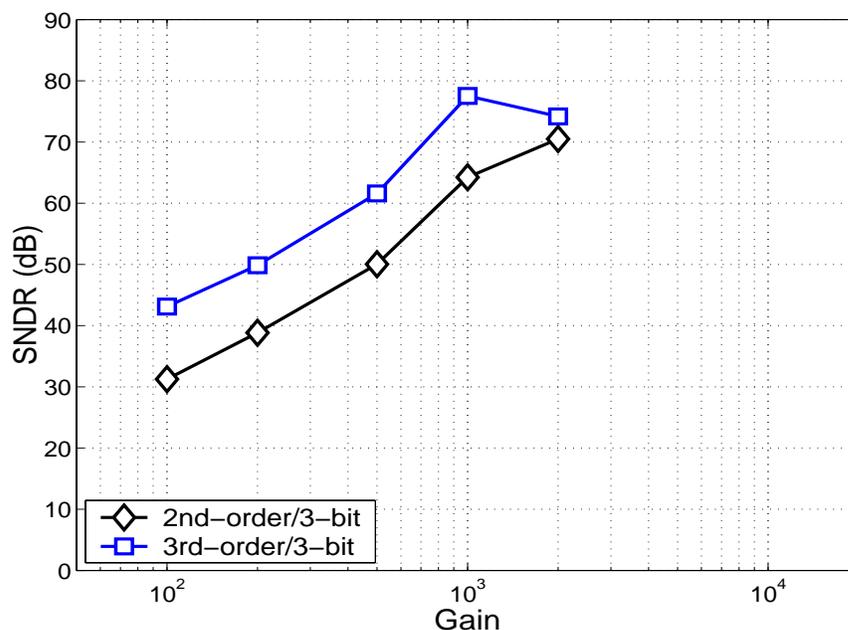
Figure 6-10: SNDR versus loop gain for 3-bit systems. The input is 5 g. The Q is 1000.

6.4.3 Effect of Transducer Resonant Frequency

The effect of the transducer resonant frequency is shown in Figure 6-11. The variations of transducer resonant frequency are caused by the variations of the proof-mass and the spring constant in the micromachined structure. Most thin-film MEMS accelerometer have resonant frequencies in the range of 1 - 10 KHz. In this test, it is found that all four types of systems are robust from 3 KHz to 9 KHz. Δ−Σ modulators with the same loop filter and the same compensation remain stable and experience no significant SNDR degradation in the entire range of resonant frequency. Thus, the same loop filter design can tolerate large variations of the proof-mass and spring constant, and can be used with different transducer designs. The quantization noise is lower at low resonant frequency. The total noise and distortion power is about 15 dB lower at 3 KHz than at 9 KHz. This shows that reducing the resonant frequency improves the noise shaping.
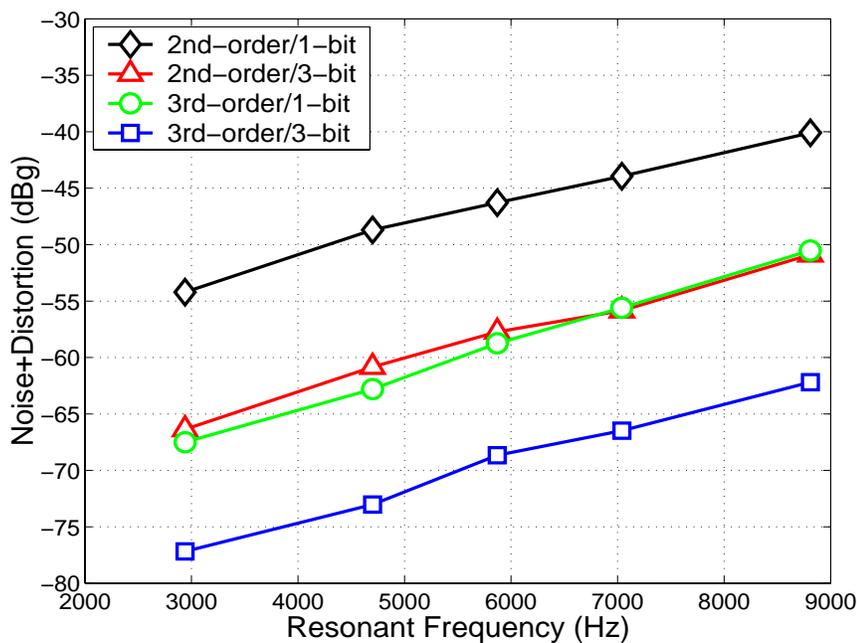
Figure 6-11: Power of noise and distortion versus transducer resonant frequency. The Q is 1000.

6.4.4 Effect of Anti-Aliasing Filter Bandwidth

If a continuous-time frond-end is employed to read out the signal, such as the circuit we describe in chapter 4, an anti-aliasing filter must be included in the loop to remove the out-of-band noise before sampling in order to prevent noise folding. The bandwidth and bandwidth variation of the continuous-time analog anti-aliasing filter complicate the compensation by introducing one or more poles. The effect of a first-order filter bandwidth on system stability and performance is shown in Figure 6-12. It is shown that for 1 MHz sampling frequency, the filter bandwidth must be greater than 400 KHz and 200 KHz, respectively for the 2nd-order and 3rd-order modulators to remain stable. The sensitivity of the 3rd-order system to the antialiasing filter bandwidth is reduced by the inclusion of the integrator. The phase lag caused by the anti-aliasing filter should not be neglected in systems employing continuous-time front-end, specially when the design space is limited..
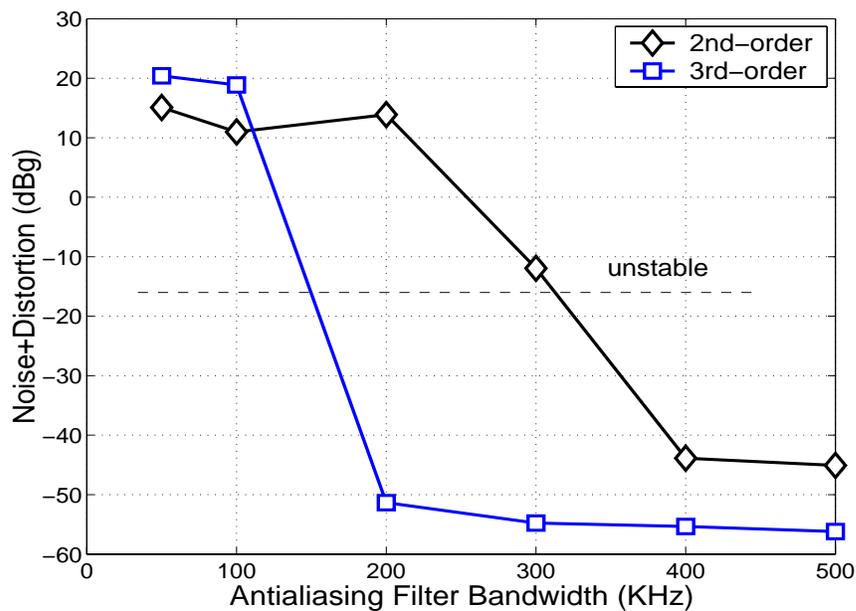
Figure 6-12: Power of noise and distortion versus anti-aliasing filter bandwidth. The Q is 1000.

However, the results show that the 3rd-order modulator is has quite large tolerance to anti-aliasing filter bandwidth variations.

6.5 Control Performance

In this work, one main objective of $\Delta-\Sigma$ feedback loop is controlling and stabilizing the high-Q MEMS structure to reduce closed-loop Q and achieve optimum damping in a vacuum environment. For sensors to function properly in vacuum, feedback control is necessary to suppress ringing and obtain fast settling upon sudden changes in acceleration, such as an impulse or a step input. The optimum settling is achieved by critical damping with closed-loop Q equaling 0.5. The control performance is characterized by the step response of the closed-loop system.

6.5.1 Settling Performance

The $\Delta-\Sigma$ loops are simulated with 5 g step input signal and the responses are shown in Figure 6-13. The open-loop Q of the transducer is 1000. Unlike in the previous studies, the bandwidth of the decimation filter is 8 KHz so that the effect of the transducer resonant frequency can be revealed. The first trace is the response of the open-loop sensor. It shows the ringing behavior and the settling time is well above 0.1 second. Such a settling time is far too slow to be used in practical sensing applications. The other four traces are the step responses of the four types of $\Delta-\Sigma$ modulators. These closed-loop step responses show only slight overshoots less than 5% and settle within 2 ms. At optimal compensation point where the modulator has the best quantization noise performance, their time-domain characteristics are closed to critical damping with Q < 1, thus, the systems having near opti-
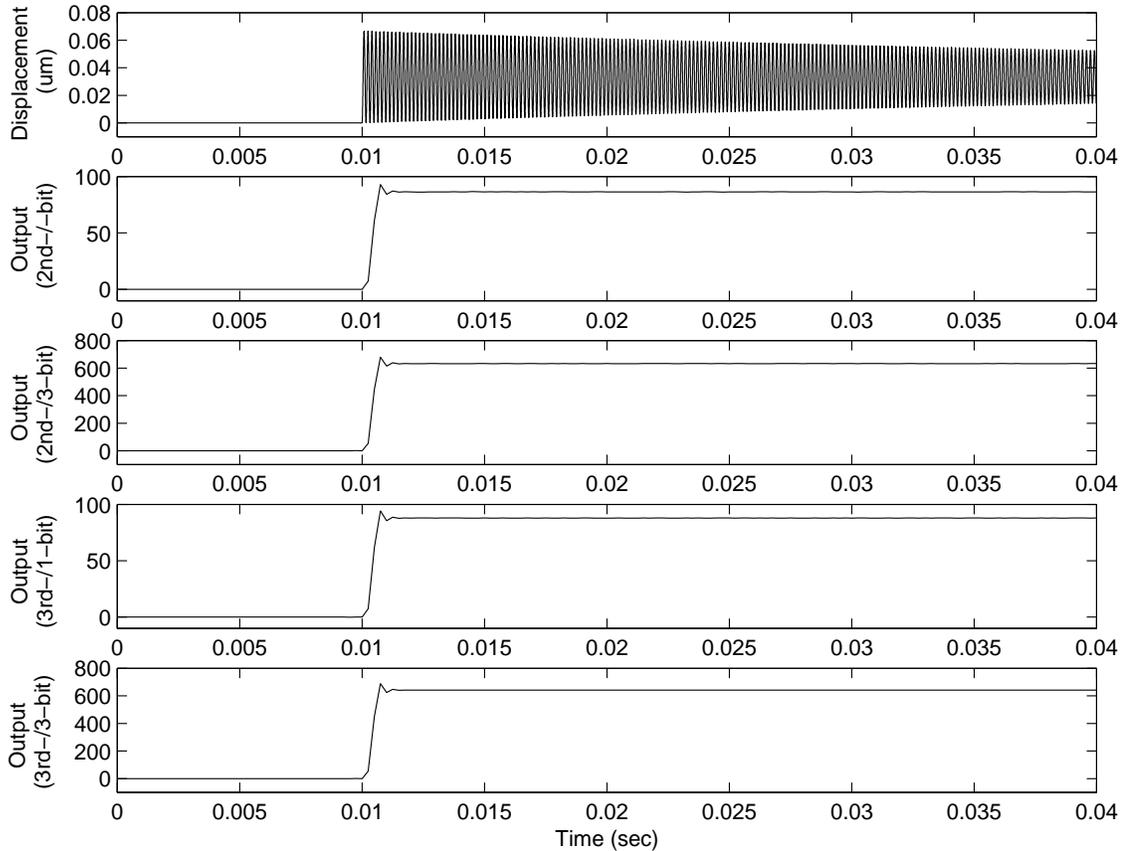
Figure 6-13: Output step response of open-loop transducer and the four delta-sigma feedback systems. The Q is 1000.

mum settling behavior. These simulations prove that the well compensated Δ–Σ modulation provides effective and robust feedback control to stabilize the high-Q MEMS structures.

6.5.2 Proof-mass Position Error

The further examine the control performance of Δ–Σ modulation, the displacements of proof-mass are plotted in Figure 6-14 for the four modulator types. In Figure 6-14, we can see the random motion of the proof-mass caused by the quantization noise. However, there is no fixed oscillation pattern, and the ringing caused by high-Q resonant mode of the transducer is completely removed. With 1-bit quantization and feedback, the scale of the

proof-mass random motion is about 1 nm. The scale of the random motion is reduced to

within 2 Angstrom by 3-bit quantization and feedback, a 300x reduction compared to the

open-loop displacement. In 3rd-order modulators, the steady-state displacement of the

proof-mass is orders of magnitude smaller than 1 Angstrom, as shown in Figure 6-15.

These results shown in Figure 6-14 match the power spectral density (PSD) of the

proof-mass displacement shown in Figure 6-15. In Figure 6-15, the only peak is the sin-

gle-frequency displacement induced by the input sinusoidal signal, besides that, there are
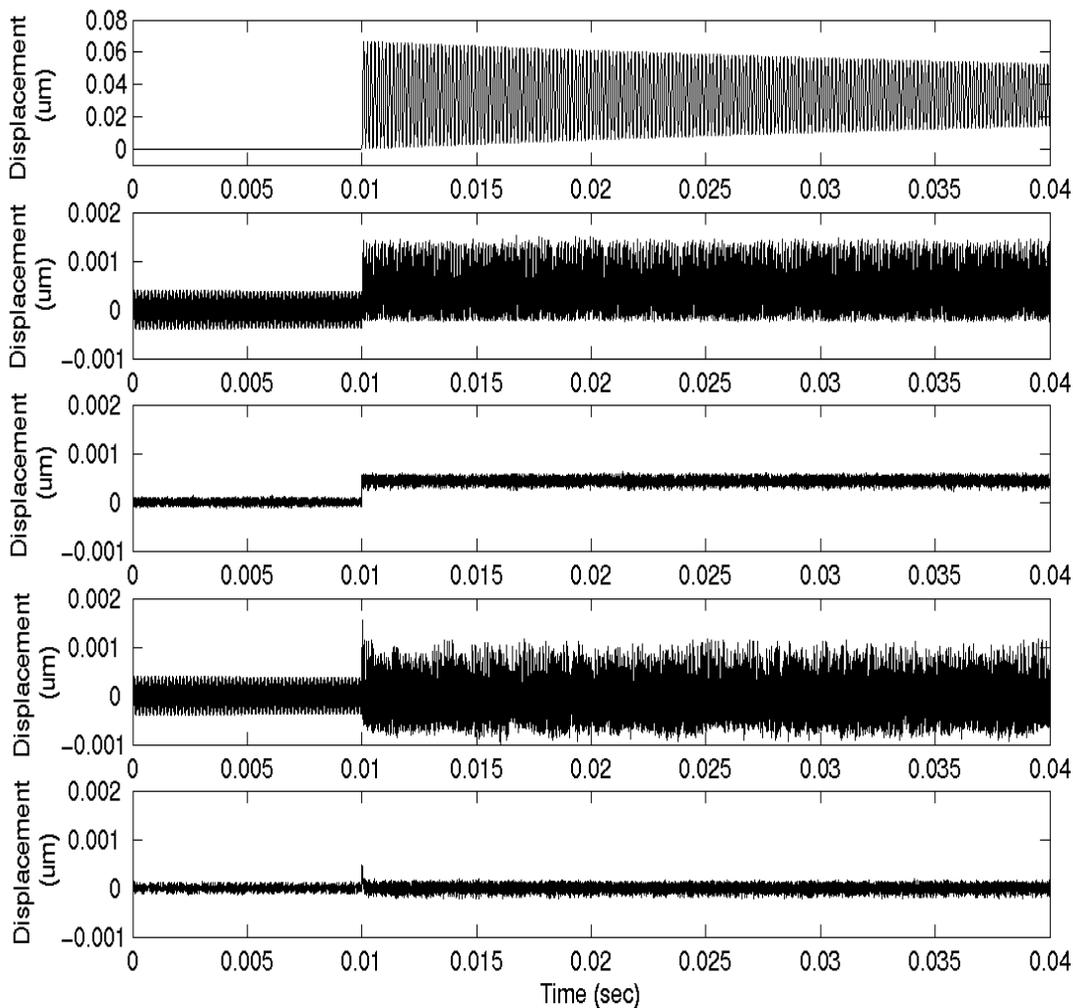
Figure 6-14: Step responses of proof-mass displacement in the open-loop transducer and the four delta-sigma feedback systems. The Q is 1000.

no frequency peakings in the PSD, meaning the high-Q resonant mode has been removed by the feedback.

As shown in Figure 6-15, the 3rd-order 3-bit Δ–Σ feedback control reduces the total proof-mass displacement caused by 5 g input acceleration and Δ–Σ quantization noise to within 2 Angstrom and achieves zero steady-state error. Therefore, multi-bit Δ–Σ modulation could be used as a position control method for micro structures to achieve sub-Angstrom total position error against external and internal disturbances. As we demonstrate in the previous discussions, the multi-bit Δ–Σ modulation has the advantages of simple hardware implementation and good robustness, compared to other control strategies.
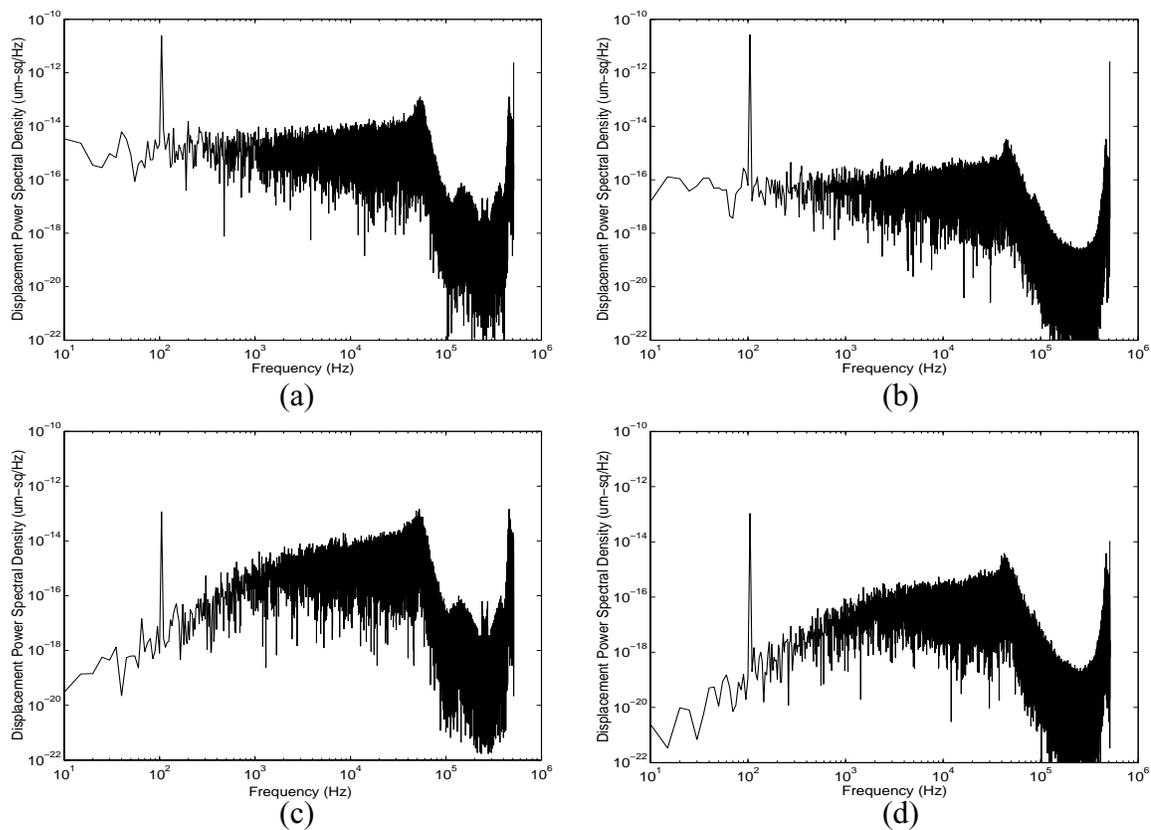
Figure 6-15: Power spectral density (PSD) of the proof-mass displacement of: (a) the 2nd-order 1-bit system; (b) the 2nd-order 3-bit system; (c) the 3rd-order 1-bit system; (d) the 3rd-order 3-bit system. The Q is 1000.

6.6 Vertical-Axis Vibration Mode

One major difficulty in vacuum packaging MEMS sensors is that the structure has modes of vibration other than the sensing mode. Low-damping operation in a vacuum raises the Q of all modes. While the closed-loop Q can be greatly reduced by feedback in the sensing axis, it is somtimes difficult to apply feedback control to all the other modes.

In lateral thin-film micro accelerometers, the mode in the vertical axis is the second most significant mode. In this study, the device is assumed to have Q = 1000 in both axes. To examine the effect of the high-Q z-axis mode, a step signal is applied in z axis to induce both a dc displacement and a resonant motion. Because the high-Q mode in vertical axis is not controlled, this vibration settles very slowly, as shown in Figure 6-16.
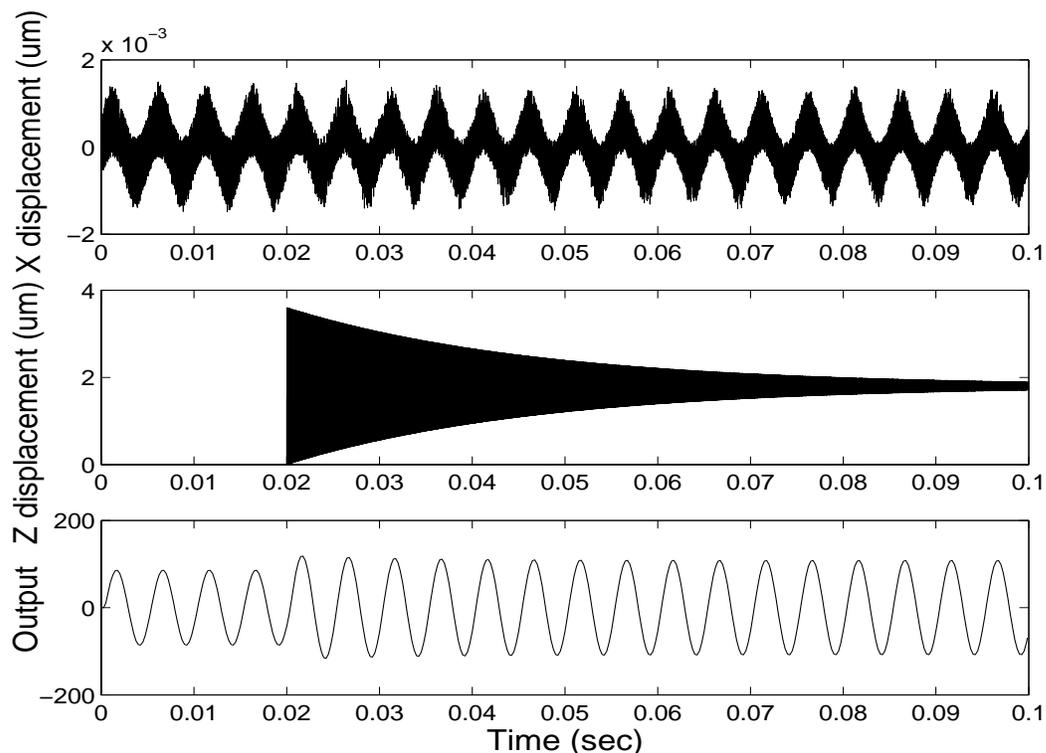
Figure 6-16: Proof-mass displacement in x and z axes and modulator output of the 2nd-order 1-bit modulator at 1000 g z-axis step input. The Q is 1000 in both axes.
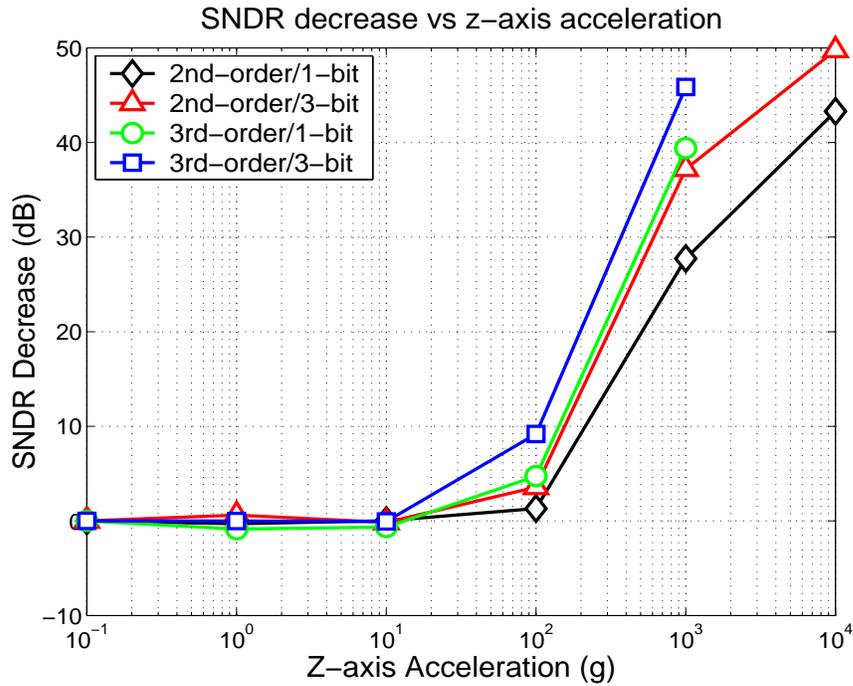
Figure 6-17: SNDR decrease versus z-axis step signal magnitude. The Q is 1000 in both axes.
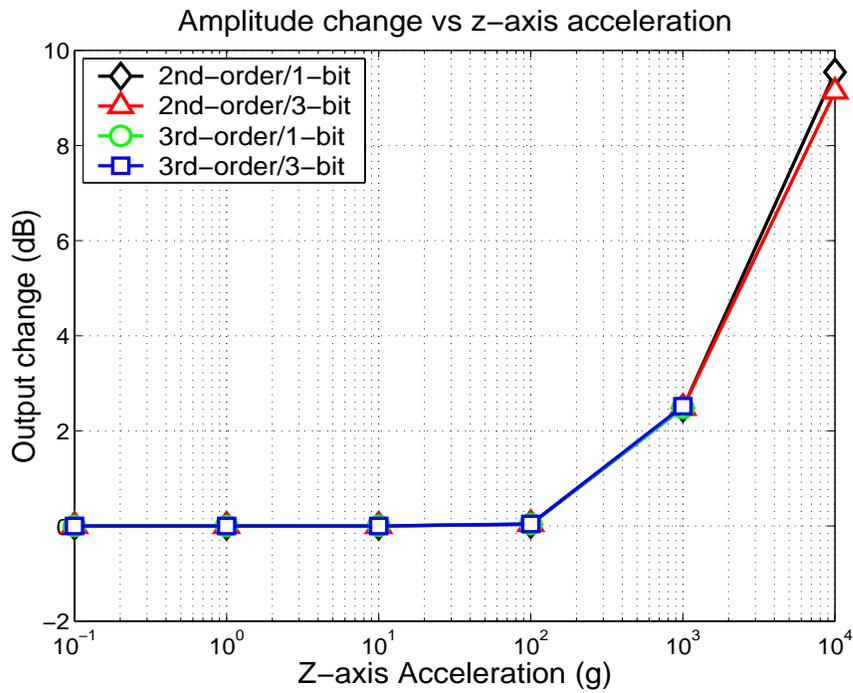
Figure 6-18: Output amplitude change versus z-axis step signal magnitude. The Q is 1000 in both axes.

Figure 6-16 shows the proof-mass displacements and modulator output of a 2nd-order 1-bit modulator under 1000 g z-axis step signal. Because the motion in x-axis is controlled while the motion in z-axis is not, the displacement in z axis is three orders of magnitude greater than in x axis. The displacement in z axis is a sum of a z-axis offset and a vibration at its resonant frequency of 11.8 KHz, both with amplitude of about 2 μm. As described in Chapter 2, the z-axis offset decreases the electrostatic actuation force, which causes the modulator output amplitude to increase due to smaller feedback factor. Meanwhile, the vibration introduces fluctuation in the feedback factor, which results in larger quantization noise and distortion.

Because the capacitive sensor, and more importantly, the feedback electrostatic actuator vary with z-axis displacement, there is a coupling between the x-axis mode and the z-axis mode. As a result, the loop performance in the x axis could be changed by the motion in z axis. The changes in modulator SNDR and output amplitude are plotted in Figure 6-17 and 6-18, respectively, with z-axis step signal ranging from 0.1 g to 10000 g. These changes are insignificant up to 100 g because both the capacitive sensor and the electrostatic actuator are relatively insensitive to z-axis motion. The coupling between the two modes increases rapidly between 100 g and 1000 g, or in terms of displacement, between 0.2 μm and 2 μm. At 1000 g, with z-axis motion increased to around 2 μm, SNDR degradation greater than 25 dB is observed due to fluctuation in the system. The 3rd-order modulators are more sensitive to z-axis motion than the 2nd-order systems. They become unstable at 10000 g z-axis step signal, while the 2nd-order systems remain stable but have very poor SNDR. This is easy to understand by considering the 3rd-order systems are con-

ditionally stable with stability dependent on input signal scale. In Figure 6-18, the increase of output amplitude is due to the dc displacement.

From Figure 6-17 and 6-18, we can conclude that even without z-axis control, the modulators could withstand low-g z-axis shocks quite well up to 100 g in a vacuum. One exception is that when the disturbance is at the resonant frequency of the z-axis mode, a small disturbance could result in a large motion. With Q of 1000, 1 g disturbance at 11.8 KHz is sufficient to generate 2 μm z-axis vibration in the proof-mass. As shown in Figure 6-16 and 6-17, 2 μm vibration in z-axis causes 25 - 45 dB SNDR degradation. And larger disturbances at the z-axis mode resonant frequency could destabilize the x-axis feedback loop. To prevent this from happening, it is very important to have feedback control on the z-axis mode and other significant modes, unless we can make sure there are no disturbances near their resonant frequencies. As we demonstrated in the previous section, a $\Delta-\Sigma$ feedback loop could lower the closed-loop Q to less than 1 and reduce the vibration by a factor of 300. Therefore, if sensing and actuation could be performed in all critical modes, a multi-mode control system could be built based on force-balanced $\Delta-\Sigma$ modulation. Since the cross-mode coupling is insignificant with small displacement, multiple $\Delta-\Sigma$ servo loops could be designed and operated independently without considering the coupling. Such a multi-loop system not only maintains the performance and stability in the main sensing axis, but could also be used to implement multi-axis sensors.

The CMU CMOS MEMS technology, however, lacks the capability of effective vertical sensing and actuation, because parallel plates could not be built in the vertical axis. Although vertical sensing and actuation have been investigated using side-wall capacitance [69], they are rather ineffective, specially when low voltage is required. Vacuum

packaging and operation of CMOS MEMS surface micromachined devices will be quite a challenge.

6.7 Summary

In this chapter, a simulation study on the stability, dynamic range, robustness and control performance of 2nd and 3rd-order force-balanced electromechanical $\Delta-\Sigma$ accelerometers with single and multi-bit feedback. The 3rd-order 3-bit $\Delta-\Sigma$ modulator operating at 1 MHz achieves 80 dB maximum SNDR, 100 dB dynamic range and 4.5 µg/rtHz quantization noise floor in a 2 KHz bandwidth. All systems show good robustness across variations in resonant frequency, Q factor and transducer gain. The CPDM digital feedback scheme achieves good robustness against sensor position offset. The $\Delta-\Sigma$ modulation also provides robust control to highly underdamped transducers with Q = 1000 to achieve near optimum settling performance with settling time less than 2 ms. In the 3rd-order 3-bit system, the proof-mass displacement, or its position error, is confined within 2 Angstrom by the force feedback. Although the design space shrinks for the 3rd-order systems, the hardware implementations of both 2nd and 3rd-order systems are well within the tolerance of analog integrated circuits.

Chapter 7

Conclusions and Future Work

In this work, circuit and system design techniques for sensing and controlling the motion of MEMS structures are investigated to realize low-noise integrated CMOS MEMS accelerometers. The accelerometer fabricated by CMOS MEMS surface micromachining is a low-sensitivity device with proof-mass on the order of 10^{-10} kg, total sensing capacitance smaller than 20 fF x 4, capacitance sensitivity less than 0.4 fF/g, and overall sensitivity about 1 mV/g. Despite all these limitations, the CMOS MEMS technology has an unique advantage of very close integration between MEMS and CMOS circuitry with low parasitics at low cost. Therefore, it is an ideal test vehicle for circuit and system techniques which utilize the integration capability of MEMS technology to obtain high system performance.

7.1 Summary of Results

There are three sources of noises in MEMS accelerometers: electronic noise from the sensor interface circuit; Brownian noise due to damping-related thermal-mechanical energy dissipation; and quantization noise if analog-to-digital conversion is included.

In the area of capacitive sensing circuit design, we introduce the following circuit techniques to minimize the electronic noise and suppress other nonidealities: a low noise

architecture based on chopper stabilized continuous-time voltage sensing; input-referred noise minimization based on capacitance matching at the sensor/circuit interface; a robust sensing node dc biasing scheme using periodic reset for charging suppression; and active offset cancellation using a differential difference amplifier. An integrated CMOS MEMS accelerometer prototype using these techniques achieves 50 μg/rtHz noise floor which is close to the Brownian noise floor, and > 40 dB of sensor offset reduction. We present a circuit noise model that is validated by experiments and provides insights on design trade-offs. We also conclude that the chopper-stabilized continuous-time voltage sensing fundamentally has better noise performance than the switched-capacitor charge sensing.

At system level, force-balanced electromechanical delta-sigma modulation with high-Q micromechanical transducers is investigated to reduce Brownian noise and quantization noise. A single loop architecture is introduced along with the switched-capacitor circuit implementation of the loop filter. A digital force feedback method called complementary pulse density modulation (CPDM), is proposed to realize highly linear offset-insensitive feedback using nonlinear actuators. Simulations show such systems realize high-resolution A/D conversion with 100 dB dynamic range and μg/rtHz quantization while simultaneously providing robust control to the high-Q micro structure to obtain near optimum closed-loop settling and < 2 Angstrom proof-mass position error.

7.2 Suggestions for Future Work

Following the work presented in this dissertation, the next step would be to implement the multi-bit 3rd-order Δ–Σ modulator, integrate it with the low-noise continuous-time

front-end, and experimentally characterize its performance in a vacuum environment. In such a fully integrated digital accelerometer system, on-chip trimming or calibration of offset and scale factor variations could also be implemented. With both quantization noise and Brownian noise down to the μg/rtHz level, the noise performance will once again be dominated by circuit noise. It is then necessary to operate the circuit in the thermal noise dominated region. As shown in 3.1.4, due to various short channel effects that cause higher thermal noise level, the noise floor of the capacitive accelerometers is fundamentally limited to about 10 μg/rtHz by the available sensing capacitance and the interconnect parasitic capacitance. To further improve the noise, better technologies with larger sensing capacitance sensitivity and lower interconnect capacitance are necessary.

The circuit and system design techniques introduced in this work could be applied to both thin-film and bulk MEMS technologies with larger sensing capacitance to further lower the circuit noise floor and the total noise floor. Larger capacitance can be obtained by either thicker or larger structures, or smaller gap width. If low-parasitic integration between sensor and circuit can be achieved in these processes, by using the noise minimization techniques, it is possible to obtain 1 μg/rtHz noise floor in thin-film accelerometers and sub-μg/rtHz noise floor in bulk micromachined accelerometers. Thus, combining good structural properties and integration capability is very important for building low noise capacitive sensing systems in MEMS.

The low noise capacitive sensing techniques could be used in many other capacitive sensing applications, such as pressure sensors and gyroscopes. For example, MEMS vibratory rate gyroscopes [70] require very sensitive accelerometers to sense the Coriolis motion, hence, noise minimization is more critical in gyroscopes.

We have demonstrated that multi-bit Δ–Σ modulation is a very robust and effective control strategy that also gives digital position readout. While the quantization noise of the 1-bit feedback causes high-frequency vibration of the proof-mass, it is easy to reduce such vibration down below 1 Angstrom with multi-bit feedback. Although undesirable vibration modes may cause problems for low-damping operation, multi-mode multi-bit Δ–Σ feedback control with independent loops without concerning the mode coupling could be implemented if the multi-axis sensing and actuation capability is available. Therefore, multi-mode multi-bit Δ–Σ force-balanced control is an attractive approach for motion control of micro structures, specially in low-g and low-damping environment. Potential applications include the sensing and servo in vibratory rate gyroscopes [70], MEMS-based data storage systems [71], and MEMS-based optical mirrors, where devices are often packaged in vacuum.

7.3 Technology Directions

We have seen that in MEMS capacitive sensors, both the minimum achievable noise floor and the power consumption of the circuit are constrained by the available sensing capacitance of the MEMS fabrication technology. With the scaling of VLSI technology, modern photolithography is able to make structures on the scale of 0.1 μm. If the MEMS micromachining could catch up with the technology scaling, both noise floor and power consumption of micro capacitive sensing systems would be greatly improved. According to the basic equation of capacitive sensing:

$$V_{out}(\Delta x) \propto \frac{C_s}{C_s + C_p} \cdot \frac{\Delta x}{x_0}, \qquad\qquad (7\text{-}1)$$

the technology scaling reduces the gap width (x_0), increases the sensing capacitance (C_s), and reduces the interconnect capacitance (C_p). As the result, the sensitivity increases at a rate greater than the technology scaling factor, even when the total sensing capacitance is reduced by decreasing device size. Meanwhile, based on our noise model, large input transistors with lower noise and lower 1/f corner would be used to match the larger sensing capacitance. Therefore, the noise floor could be lowered by a ratio larger than the scaling factor while the circuit operates at lower frequency and consumes less power. This is a key advantage of capacitive sensing.

Unlike capacitive sensing, the Brownian noise goes against the technology scaling because smaller mass increases the Brownian noise as:

$$\overline{a_n^2}(f) = \frac{4kT\omega_n}{mQ}. \tag{7-2}$$

This situation requires a two-way solution. On one hand is the low-cost fabrication of high-aspect-ratio structures to obtain larger mass even when the device size shrinks. Examples of such technologies include DRIE [72] and various processes to deposit thick-film structures on top of the CMOS die. On the other hand is the low-cost vacuum packaging techniques that allow devices to operate at high Q. As a consequence, closed-loop sensors will become more common, at least for low-g applications.

From the above analyses, it is clear that the two key techniques introduced in this work, noise minimization based on capacitance matching and multi-mode multi-bit force-balanced Δ–Σ feedback, will become increasingly important with the technology scaling in the future.

Chapter 8

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