

Executive Summary

This is the final technical quarterly summary for the KGS Phase II program. It is part of the contract extension where consideration was given by NRL to allow additional subcontractor work on CVD modeling and time for analysis of epitaxy experiments designed to improve the epitaxy doping uniformity.

Technical Progress

The following table documents the key program end metric goals.

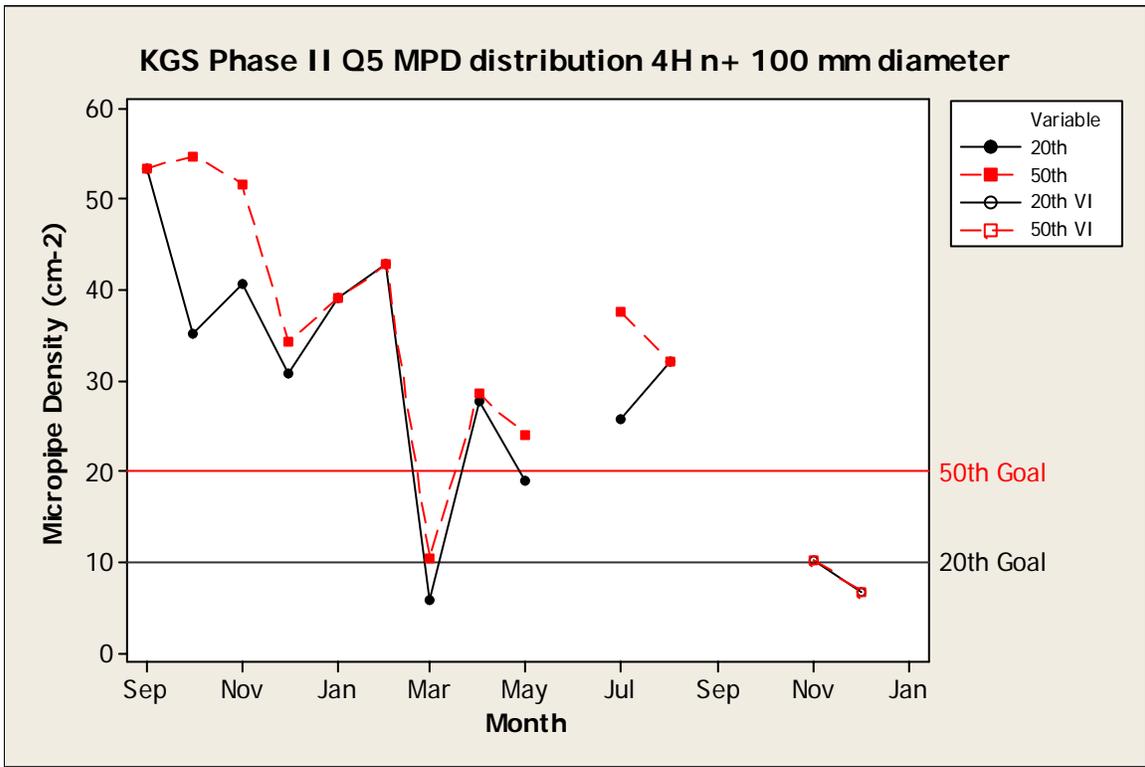
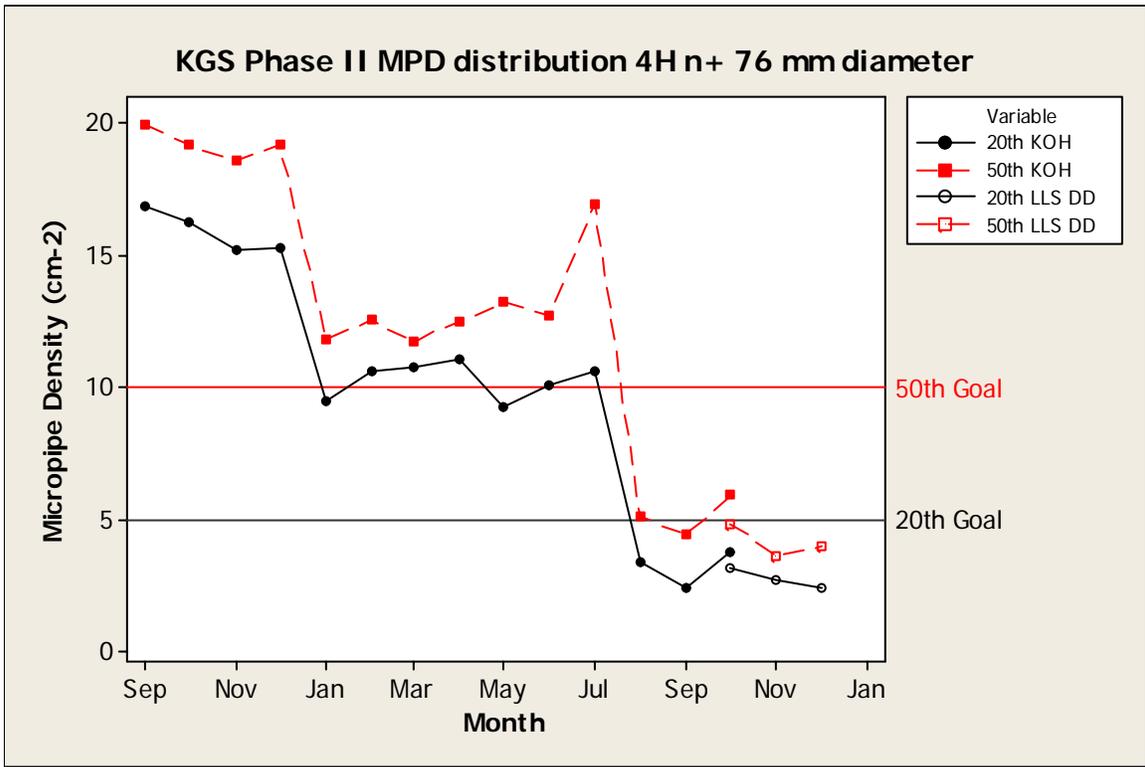
Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm-2)	10	5
MPD distribution 4H n+ 100 mm diameter (cm-2)	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm-2)	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/- 10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

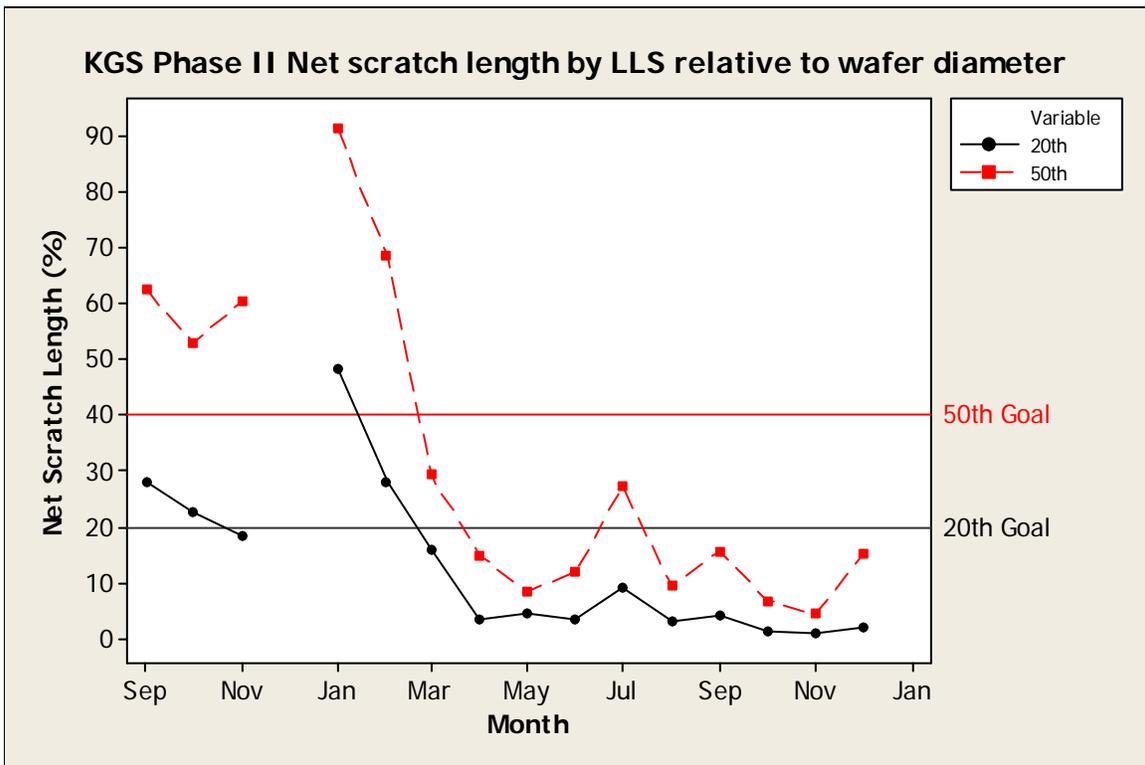
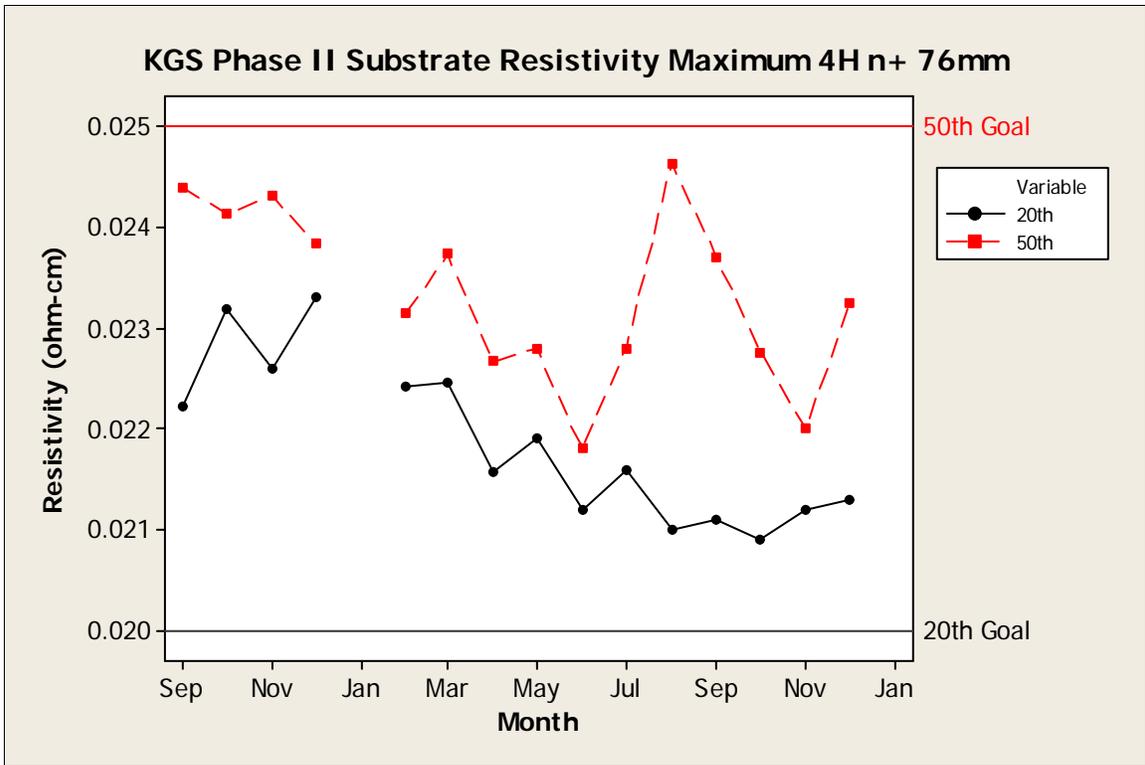
The table is now color coded to reflect the status of the program. Green=met goal; yellow=nearly met; red=not met. Details and data pertinent to the specific goals are provided in the next section of the report.

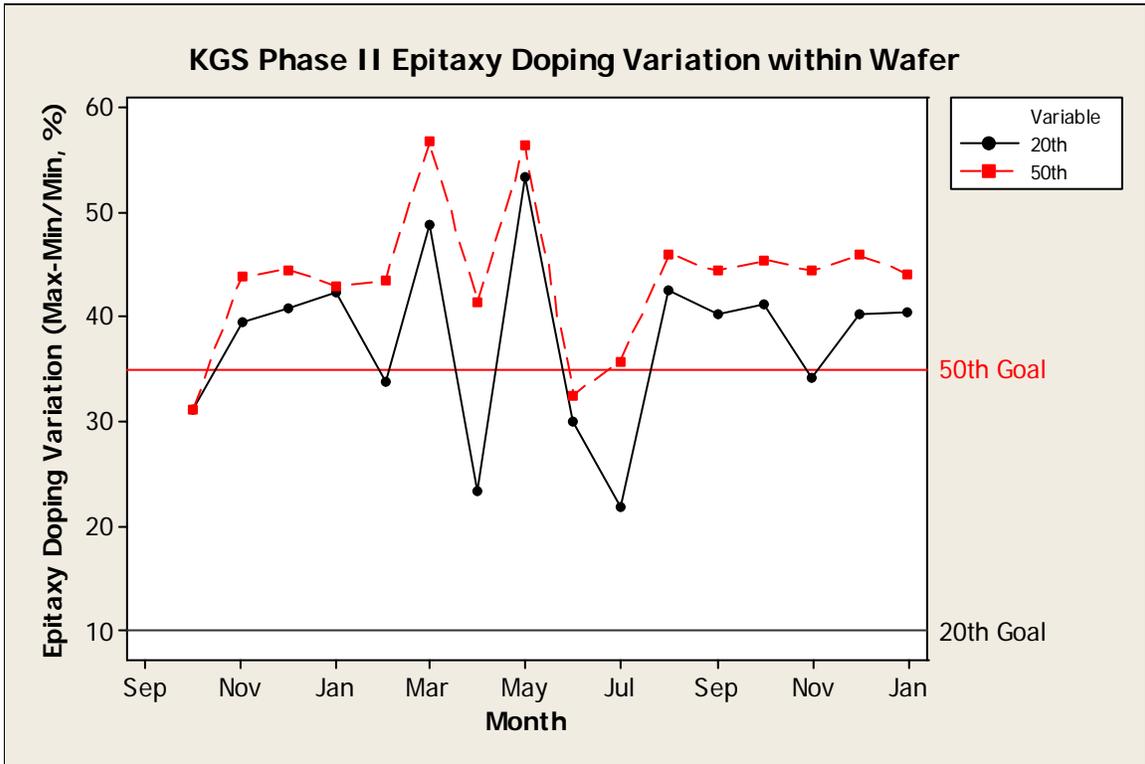
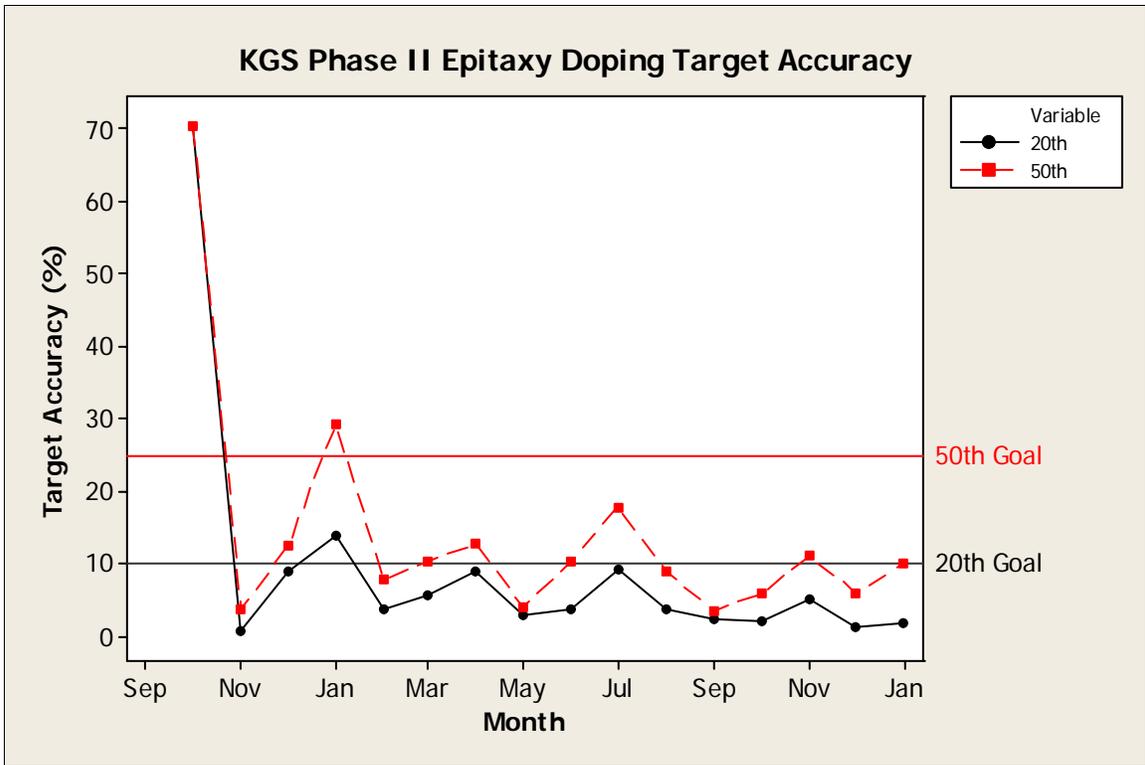
Progress against Metrics

The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears. As the KGS III program started in December 2008, KGS final data for Phase II will include December 2008 and January 2009. For continuity, Phase III will include January 2009 as well.

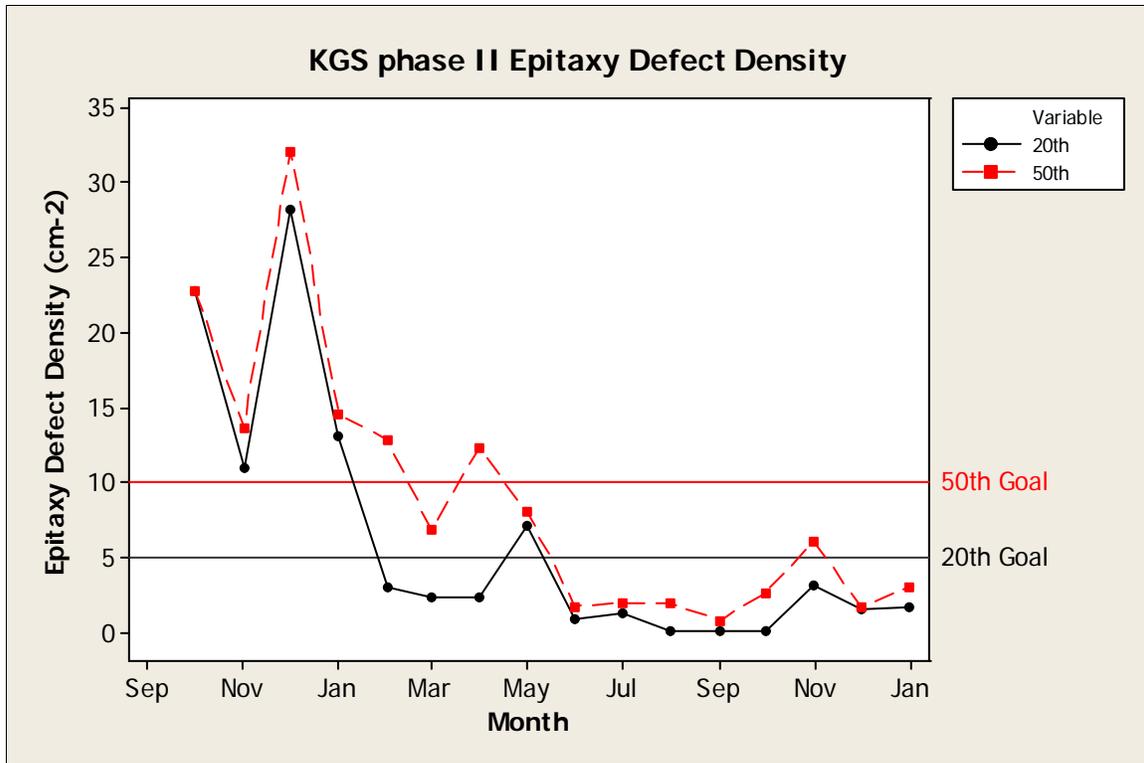
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14. ABSTRACT The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Subcontractor work on CVD modeling and analysis of epitaxy experiments have been the main focus of efforts in Q6. This technical report summarizes the progress by all team members against the tasks and milestones.				
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The above chart does not reflect improvements to the CVD epitaxy process. These are discussed later in the report.



Project Milestones

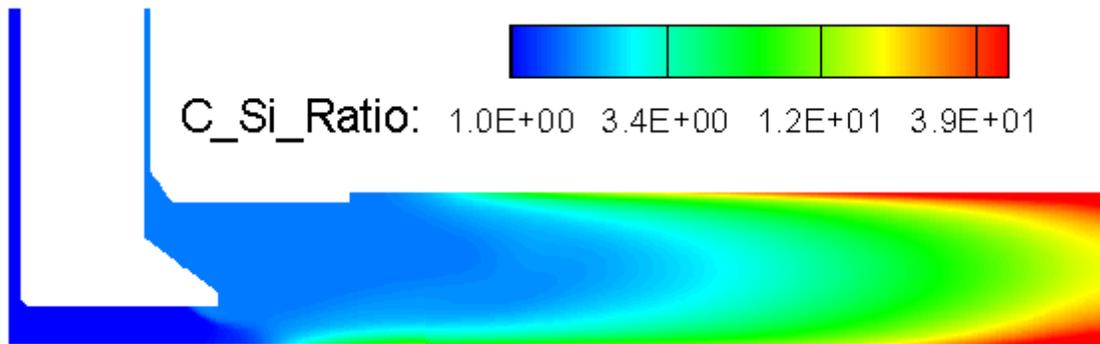
Task 1: SiC Wafers Products

Highlights:

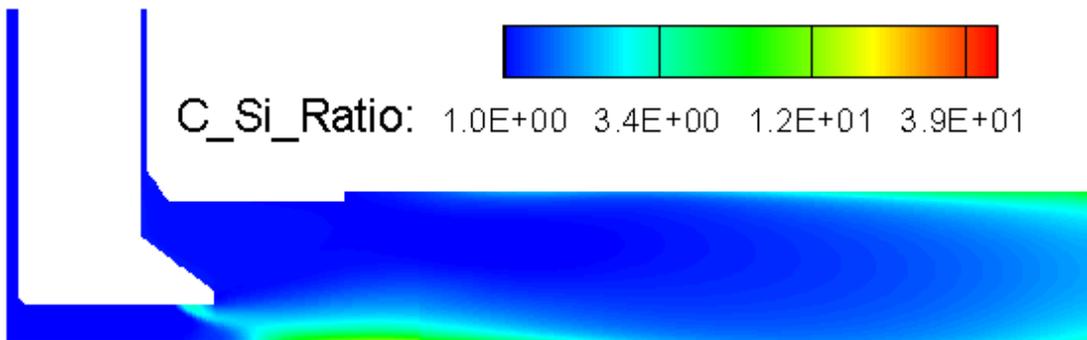
- Advances made in PVT growth in phase II of the program has allowed for a large reduction in 76mm 4H n+ MPD. The 20th percentile of performance is <2 cm⁻² while the 50th has moved to <5 cm⁻².
- 100mm MPD has also improved since the beginning of phase II however the reduction has been slower due to the speed of adoption of the new PVT technology. Currently the DCCSS program is expanding seed crystals beyond 90 mm diameter.
- New laser light scattering measurement techniques for MPD now allow for non-destructive measurements on all polished wafers.
- Wafer resistivity maximum has shown improvement in Phase II with a steady decline in the 20th percentile and a reduction in the 50th percentile without sacrificing crystal quality or yield.
- Wafer polishing has exceeded the 50th and 20th percentile goals of the program since the 2nd quarter of the program with typical LLS scratch lengths <10% of the wafer diameter.
- Epitaxial doping accuracy has continued to improve and has exceeded 50th and 20th percentile goals of the program since the 1st quarter of the program.
- Improvements in the Epitaxy process have resulted in a reduction in the Epi defect density to meet goal levels.
- New epitaxy process tested in the end of the program has delivered step change improvement in doping uniformity. In the first generation CVD process, the doping

was bowl shaped, i.e. high at the edges and low in the center. Concepts around the methods to alter the chemistry and distribution of reactants were developed and fed into the modeling effort to assess the concentrations of the carbon and silicon gas species above the wafer. The model data shown below confirmed the hypothesis behind the new CVD method. Plotted below are the distributions of C/Si concentration ratios for the original (Gen I) and new (Gen II) CVD processes. For the Gen II process, the chemistry allows for lower C/Si ratio at the wafer center compared to the wafer edge, which should help to flatten the bowled doping distribution in the wafer associated with the legacy method.

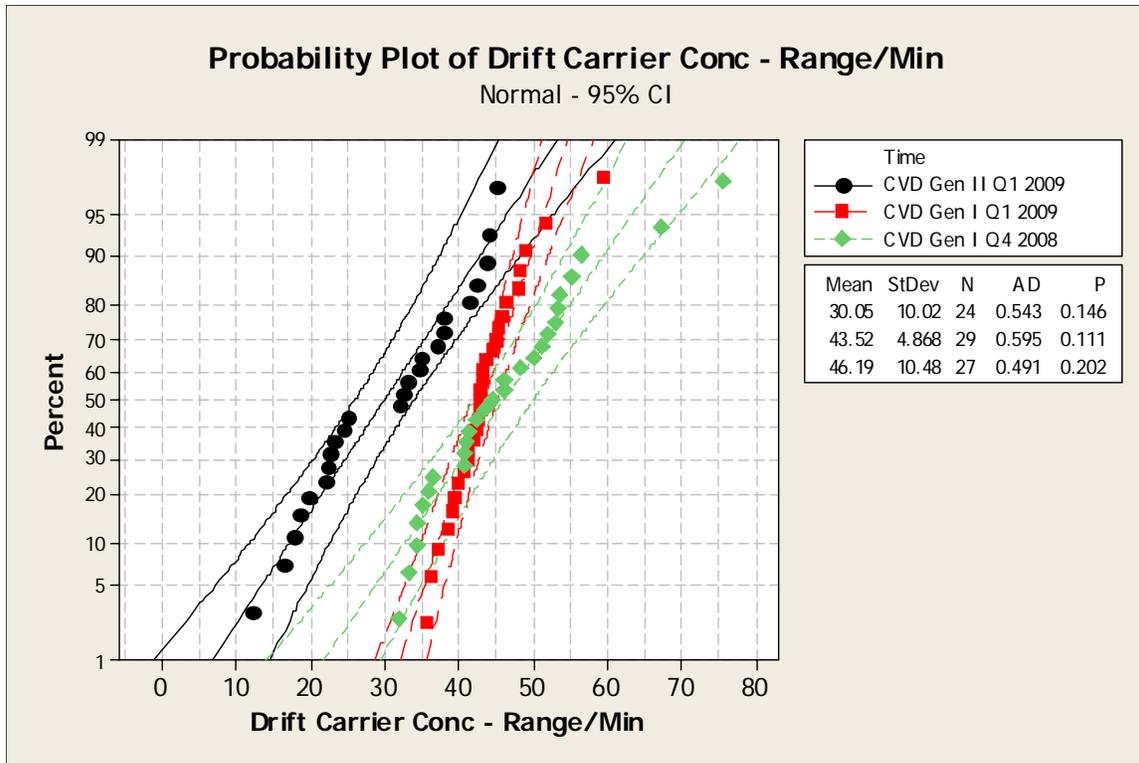
Gen 1 CVD



Gen 2 CVD



Several epitaxy experiments were conducted in calendar Q1 of 2009 on the Gen I CVD epitaxy process. The within wafer doping range was substantially reduced compared to the legacy process. This is shown statistically in the probability plot below. The mean of the wafer doping range distribution was reduced from ~45% for Gen I to ~30% for Gen II. The Gen II process was used to prepare deliverables for KGS III.



Roadblocks:

- Key roadblock for KGS II was the delay to develop 100mm diameter 4H-SiC wafer technology. In the first half of KGS II, it was apparent that 100mm wafers could be produced, but only with a undesirable amount of grain boundaries. With the advent of the learning that substantially improved DCCSS 76 mm diameter 4H-SiC crystal technology, DCCSS made a late program change and started a program of crystal expansion to develop a new set of 76-100 seed stock which would be free of grain boundary defects. The expansion effort did not reach 100mm by the end of the KGS II program, it did reach >85 mm diameter, and work will continue in 2009.

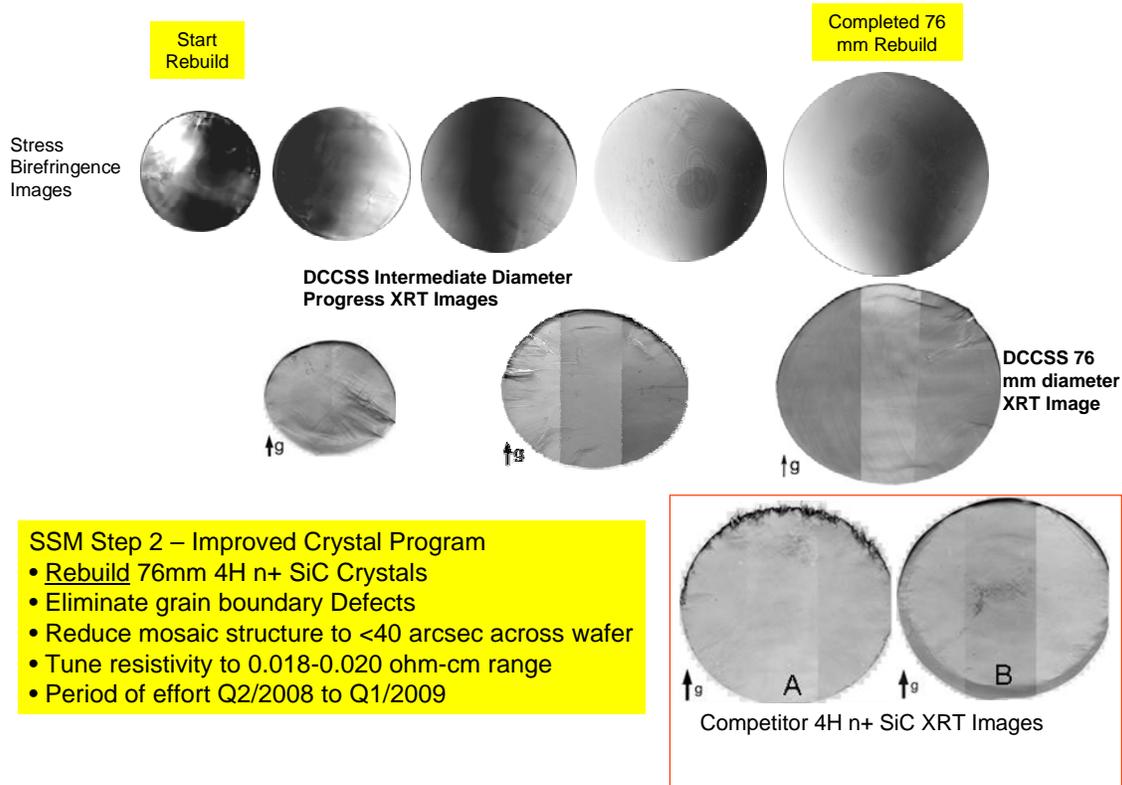
Project Milestones

Task 2: Continuous Improvements in SiC Substrates

Highlights

- Full implementation of the improved PVT growth process in Phase II has resulted in impressive material quality improvements in terms of lattice curvature and XRD full width at half maximum which have shown a 5X improvement. Crystal mosaicity has also decreased greatly as measured by XRT.

A montage showing the efforts of DCCSS to implement its new PVT growth technology to eliminate defects in 4H SiC crystals through crystal diameter expansion in the second half of 2008 and January 2009 is shown below:



Stress birefringence and x-ray topography evidence significant improvements in crystal quality. 76 mm diameter crystals from this new process show comparable quality with competitor wafers tested in 2008. Assessment of DCCSS and competitor wafers at SUNY show equivalent defect densities for micropipes and screw dislocations.

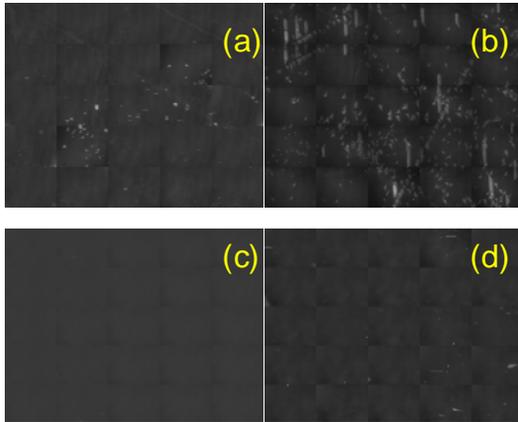
- Re-expansion of high quality crystal seeds using the improved PVT process is yielding the best 4H SiC crystal quality measured at DCCSS ever as seen by XRD FWHM averages <40 arcsec. This is representative of material shown in the above figure.
- The improved growth furnace RF heat source delivered in Q3 and installed in Q4 has been duplicated on several production crystal growth furnaces and continues to show the improvements in process consistency and crystal metrics such as defects and shape.

Task 3. Metrology for wafer specifications

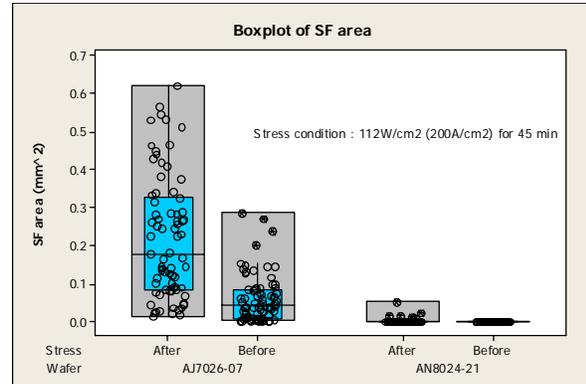
Highlights

- Using data from LLS defect testing and maps of high voltage breakdown a new effort has started to correlate the LLS data to the high voltage breakdown yield. Using an experimental design the LLS image analysis has been optimized and can now predict high voltage reverse yields to within +/- 10% (one standard deviation).

- Progress of SLIOS (Scanned laser-induced optical stress) involved imaging stacking fault (SF) growth propagation under optical stress in Schottky (n^-n^+) wafers lacking a p^+ contact layer. This approach doesn't require p^+ layer and complexity of metal grid formation. Recent SF propagation measurements on epiwafers prepared with wafers extracted from DCCSS's new crystal growth process (SSM) show extremely low stacking fault generation (data in figure below). Samples were stressed with an extremely high injection prior to SF measurement and the SSM sample still exhibited stable performance.



PL images from AJ7026-07(a,b) and new SSM wafer AN 8024-21(c,d), (a) and (c): before stress, (b) and (d): after stress



Boxplot of SF area before and after stressing on each 1mm² image

Task 4. Device Technology Maturation

Highlights:

- JBS diode from MicroSemi – Full forward I-V sweep curves show that Ni based Schottky contacts have more inconsistent data (larger SBH variation) than the Ti/W based one. Schottky contact formation and annealing for JBS are not fully optimized yet. Hot spot testing is also performed on selected JBS wafers to image the highest leakage current spots in the active device area. Ti/W based Schottky contact devices show no strong correlation between hot spots and scratch lines in epitaxy layer while the Ni based one shows strong correlation. Inconsistent Schottky behavior with Ni based contacts can be attributed to more failures with scratch lines. Several diode have been transferred to NRL for accelerated stress testing. Data will be reported by NRL in KGS III.
- Characteristic defect density (D_0) of JBS wafers is calculated from various device sizes with Poisson and Moore models to assess device killer defect density. Calculated D_0 is much higher than MPD of the wafers and this can be related with more device failures from process variations than material defects.
- SBD diode from NRL– Reverse leakage current increase rate of SBD from NRL is much higher than DCCSS SBD. This suggests either edge termination or Schottky contact interface formation at NRL are not fully optimized.

Progress toward Milestones for End of Program (Sub-bullets are progress this quarter)

- Correlation Maps of PiN forward IV characteristics and recombination lifetime (Complete)
- Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking (testing now at SUNY)
- Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)
 - Electrical reverse leakage current measurements at 300C suggest that Al dopants in p⁺ layer act as lifetime recombination centers and reduce effective recombination lifetimes of the p-n⁺ structure with addition of p⁺ layer as compared to the n⁻n⁺ structure.
- SiC materials parameter assessed as most important for SIT performance improvements based on wafer probe data (Roadmap input - NGES)
- SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)
- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis (Completed)
- Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime.
 - Non-nitride samples show much lower generation lifetime than nitride samples (NO passivation).

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Still waiting for device results.
Microsemi	SBD fabrication and testing	SBD are fabricated and tested. Wafer level testing data are analyzed. DCCSS wafers show good forward characteristics. High yield degradation rate with increasing bias is observed. More FA is underway.
GeneSiC Semiconductors	PiN diode fabrication and testing	Final report in progress. Record forward and reverse performance demonstrated.
SUNY – Stony Brook	Crystal Structure of SiC	XRT testing shows continuous improvement of

		the crystal quality with SSM materials
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	Stitched PL images show better correlation between SF and substrate scratch lines. New SSM crystals show virtually no SF propagation in epiwafer testing.
Fluxtrol	Modeling and design of high uniformity induction heating systems	Project completed, new heaters have demonstrated better crystal quality and process consistency.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	SBD diode are fabricated and tested. Large diodes show more SBH inhomogeneity. PiN fabrication is started.
STR	Modeling of CVD and PVT SiC Growth Processes	Modeling of CVD Epitaxy processes has provided key insights to understanding the sources of doping variations observed in the batch epitaxy reactor.