

TEACHING RATE CONVERSION USING HARDWARE-BASED DSP

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ABSTRACT

To enable us to affordably teach software defined radio at the undergraduate level, we developed a low cost system that allows realistic hardware projects and demonstrations. This new board connects a Texas Instruments C67x DSP starter kit (DSK) to an Analog Devices AD9857 quadrature modulator. This modulator is capable of operating at up to 200 million samples per second (MS/s), with a carrier (or intermediate frequency) of up to 80 MHz. Baseband 14-bit in-phase and quadrature (I/Q) data are presented to the modulator, which can be programmed to interpolate the data at rates from $4\times$ to $252\times$. The AD9857 is interfaced to the DSK using an Altera Cyclone FPGA which provides queuing of the I/Q data and the logic for control/programming of the modulator.

This paper describes the associated hardware and software issues and briefly describes recommended classroom use.

Index Terms— Communications engineering education, signal processing

1. INTRODUCTION

The convergence of digital communications and digital signal processing is gaining emphasis in many engineering colleges. The implementation of these communication systems using high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) is nothing new. In general, these concepts and techniques can be discussed under the umbrella term of software defined radio (SDR). To understand a SDR, one needs to understand rate conversion. While the basics of the rate conversion theory have been well established for decades, the inclusion of these topics at the undergraduate level can be fraught with teaching dangers. If realistic hardware projects and hardware-based demonstrations are to be included as part of a course, the cost can escalate rapidly. With most commercially available boards costing more than \$10,000 apiece, buying multiple units to support such a course is prohibitively expensive. To support our desire to teach these topics at the undergraduate level, we felt it was necessary to develop a low cost DSP board that would allow us to implement the realistic hardware projects and hardware-based demonstrations previously mentioned.

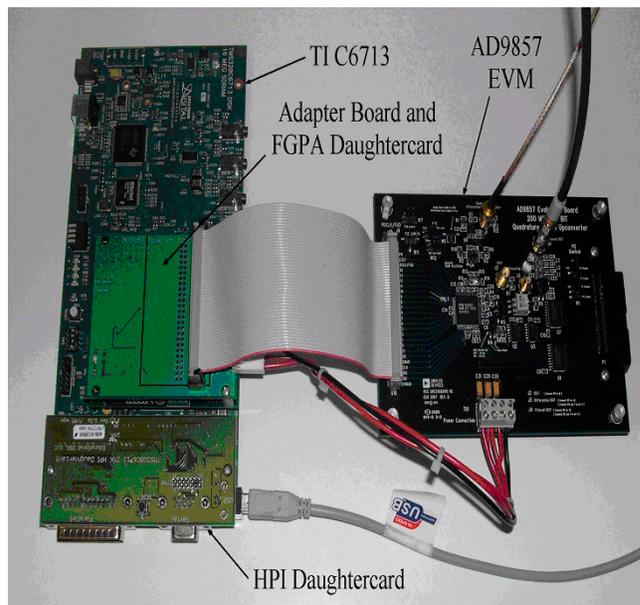


Fig. 1. The complete TI C6713 and AD9857 based rate conversion system.

2. DESCRIPTION OF THE HARDWARE

As shown in Figure 1, this new board interconnects a Texas Instruments (TI) C6711 or C6713 DSP starter kit (DSK) to an Analog Devices (AD) quadrature modulator (AD9857).

This modulator is capable of operating at up to 200 million samples per second (MS/s), with a resulting carrier or intermediate frequency of up to 80 MHz (i.e., 40% of the system's sample frequency). An onboard 32-bit direct digital synthesizer (DDS) is used to generate the carrier waveform values. Baseband 14-bit in-phase and quadrature (I/Q) data are presented to the modulator, which can be programmed to interpolate the data at rates from $4\times$ to $252\times$. The block diagram of the modulator is shown in Figure 2.

The AD9857 is interfaced to the DSK using an Altera Cyclone FPGA. The FPGA provides queuing of the I/Q data, and the logic for control/programming of the modulator. The FPGA daughtercard and the required adapter board are shown in Figure 3.

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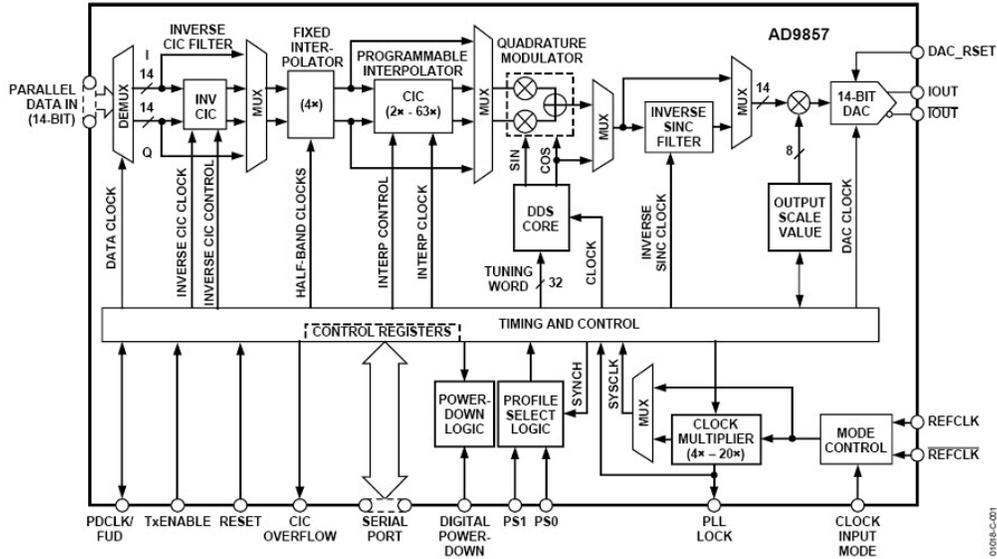


Fig. 2. The block diagram of the AD9857 (courtesy of Analog Devices).



Fig. 3. Adapter board and FPGA daughtercard stacked on top of a TI C6713 DSK. The HPI daughtercard in the foreground is required to operate this system from winDSK6.

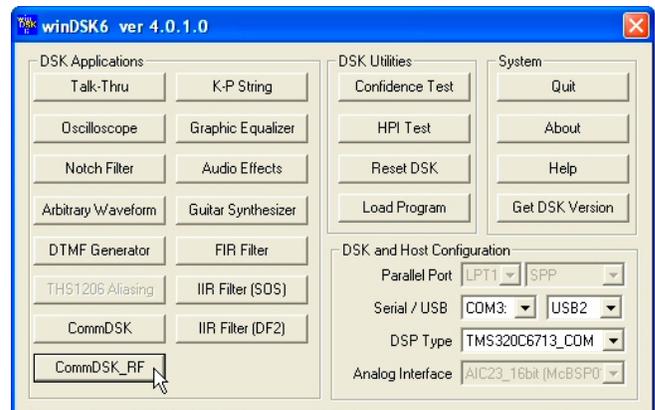


Fig. 4. The modified winDSK6 graphical user interface.

3. THE INTERFACE AND CONTROL SOFTWARE

To allow for both rapid experimentation and demonstration, the winDSK6 program (see Figure 4) was modified to allow for direct control of the hundreds of options and register settings that control the AD9857 EVM (evaluation module). In particular, a new button called CommDSK_RF was added to the graphical user interface (GUI) of winDSK6. The standard release of winDSK6 does not include the CommDSK_RF button, but this special version is available upon request.

In Figure 4, notice that the cursor arrow is resting on the CommDSK_RF button. Clicking on this button opens a window similar to that shown in Figure 5.

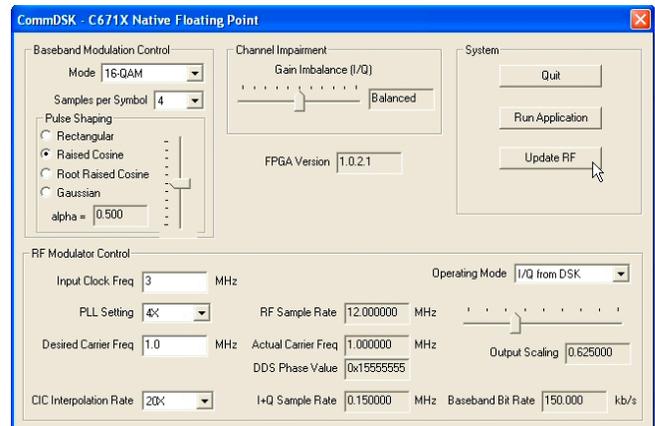


Fig. 5. Controls for the AD9857 modulator and the TI C6713 baseband data generator.

4. SYSTEM OPERATION

The AD9857 quadrature digital up-converter device has three distinct operating modes: quadrature modulation, single-tone generation, or interpolating DAC mode. The hardware we designed is capable of operating the AD9857 in all three modes. However, this paper focuses on the quadrature modulator mode. To reduce the design risk and complexity associated with designing a complete AD9857 board, we chose to utilize the evaluation board supplied by Analog Devices. (One important note for anyone attempting to reproduce this work is that the AD9857 evaluation board will not operate correctly from its signal headers unless a pull-up resistor is attached to “U2 pin 5” on the development board.)

The AD9857 requires a data source that provides 14-bit interleaved in-phase and quadrature (I/Q) data. Direct connection to the DSK external memory interface is not practical given the data rates desired, so an adapter board based on the Altera Cyclone FPGA was developed. In order to make the FPGA daughtercard design usable for other projects, it was designed with a generic interface exposing as many available FPGA input/output pins as possible. This interface is not directly compatible with the connectors on the AD9857 evaluation board. A simple adapter board was designed to provide the necessary signals and connectors to interface to the AD9857 evaluation board. The block diagram of the complete system is shown in Figure 6.

The FPGA daughtercard provides the direct control of the AD9857. Three modulation data sources are supported: baseband pulse shaped data from the DSP, ramps on the I or Q data channels, or pseudorandom (PN) data. The functional block diagram of the FPGA logic is shown in Figure 7. If the ramp or PN data source is selected, the board operates autonomously without DSP data. If baseband data from the DSP is used, a 64-word FIFO is used to reduce the interrupt overhead incurred in sending the data. Depending on the baseband modulation scheme and pulse shaping used, baseband sample rates in excess of 500kS/s can be achieved. The AD9857 de-

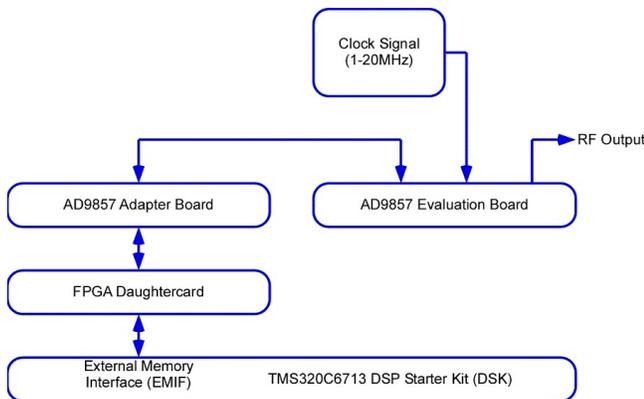


Fig. 6. Complete system block diagram.

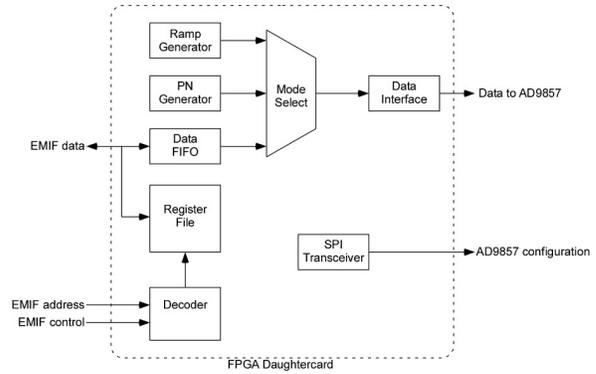


Fig. 7. The functional block diagram of the FPGA logic.

vice has an SPI-compatible serial interface for configuration and programming. The FPGA implements an SPI transceiver to send and read configuration data stored in the AD9857 registers.

The software application that was developed provides complete control over the AD9857 data path. This application is an extension of our previous work that provided a complete quadrature modulator at carrier frequencies in the audio band [1–6]. With digital up-conversion, the carrier frequency may now be as high as 80MHz. The DSP supplies baseband data in a number of modulation schemes with variable pulse shaping features. That data is then sent to the AD9857. The AD9857 provides additional interpolation, and then modulates the signal onto the desired carrier frequency.

5. SYSTEM PERFORMANCE

With the complete system shown in Figure 1 connected to a host PC running winDSK6 (upgraded for commDSK_RF functionality) and an external clock attached to the AD9857 EVM, proper operation can be verified by measuring the output of the system. A typical system output as displayed on a spectrum analyzer (SA) or vector signal analyzer (VSA) is shown in Figure 9.

In Figure 9, a slight amount of carrier leakage is clearly present. The central portion of the signal is the desired signal’s spectral content, with the remaining skirting effect due to the rate conversion process. The rapid roll-off of the signal’s power near the edges of the display is due to on-board analog filtering. Finally, the horizontal portions of the display indicate the system’s noise floor. The constellation diagram associated with this signal is shown in Figure 8.

6. CLASSROOM USE

Previous offerings of our DSP course have discussed rate conversion but have reinforced student knowledge by using the ubiquitous homework problem set and its associated MATLAB

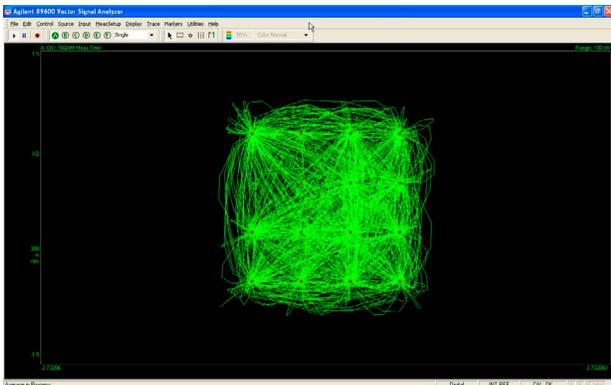


Fig. 8. Constellation diagram for the example signal.

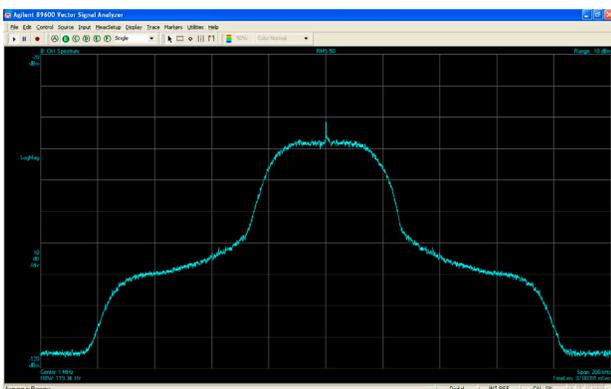


Fig. 9. Typical spectral display. Carrier frequency: 1 MHz, modulation scheme: 16-QAM, raised-cosine pulse shaping (roll-off factor = 0.5), and a baseband data rate of 150 kbps.

exercise. The extension to a real-time rate conversion system is not a trivial step. If student involvement in parameter selection and signal monitoring (for proper operation) is desired, significant time must be devoted to both the theory of the rate conversion process (as implemented in Figure 2) and the inherent limitations associated with this, and any, real-time system. This transition from a theoretical result to an actual signal output can be very frustrating if not handled properly. We prefer to handle these issues with added classroom time devoted to the rate conversion topic.

7. CONCLUSIONS

If you wish to educate your students about the implementation of communication systems using both high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) without spending tens of thousands of dollars for an individual board, consider this approach to solving the problem. This approach was very well received by our students and has also reinforced RF and communication system test and measurement skills.

The winDSK6 and other software packages we have developed are freely available for educational, non-profit use, and we invite user suggestions for improvement (see [7]). Interested parties are also invited to contact the authors via e-mail. The HPI daughtercard is available for purchase from Educational DSP, LLC as a fully assembled unit [8].

8. REFERENCES

- [1] T. B. Welch, C. H. G. Wright, and M. G. Morrow, "Caller ID: An opportunity to teach DSP-based demodulation," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. V, pp. 569–572, Mar. 2005. Paper 2887.
- [2] T. B. Welch, R. W. Ives, M. G. Morrow, and C. H. G. Wright, "Using DSP hardware to teach modem design and analysis techniques," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. III, pp. 769–772, Apr. 2003.
- [3] C. H. G. Wright, T. B. Welch, D. M. Etter, and M. G. Morrow, "Teaching hardware-based DSP: Theory to practice," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. IV, pp. 4148–4151, May 2002. Paper 4024 (invited).
- [4] M. G. Morrow, T. B. Welch, C. H. G. Wright, and G. W. P. York, "Demonstration platform for real-time beamforming," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, May 2001. Paper 1146.
- [5] M. G. Morrow and T. B. Welch, "winDSK: A windows-based DSP demonstration and debugging program," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. 6, pp. 3510–3513, June 2000. (invited).
- [6] M. G. Morrow, T. B. Welch, and C. H. G. Wright, "An introduction to hardware-based DSP using winDSK6," in *Proceedings of the 2001 ASEE Annual Conference*, June 2001. Session 1320.
- [7] M. G. Morrow, "University of Wisconsin at Madison," 2005. <http://eceserv0.ece.wisc.edu/~morrow/software/>.
- [8] Educational DSP (eDSP), L.L.C., "DSP resources for TI DSKs," 2005. <http://www.educationaldsp.com/>.