Trapping Effects in GaN and SiC Microwave FETs

STEVEN C. BINARI, MEMBER, IEEE, P. B. KLEIN, AND THOMAS E. KAZIOR, MEMBER, IEEE

Invited Paper

It is well known that trapping effects can limit the output power performance of microwave field-effect transistors (FETs). This is particularly true for the wide bandgap devices. In this paper, we review the various trapping phenomena observed in SiC- and GaN-based FETs that contribute to compromised power performance. For both of these material systems, trapping effects associated with both the surface and with the layers underlying the active channel have been identified. The measurement techniques utilized to identify these traps and some of the steps taken to minimize their effects, such as modified buffer layer designs and surface passivation, are described. Since similar defect-related phenomena were addressed during the development of the GaAs technology, relevant GaAs work is briefly summarized.

Keywords*—*GaN, heterojunction, high electron mobility transistor (HEMT), metal–semiconductor field-effect transistor (MESFET), microwave transistor, SiC, trapping.

I. INTRODUCTION

In recent years, both SiC and GaN-based field-effect transistors (FETs) have demonstrated impressive microwave performance, with SiC metal–semiconductor field-effect transistors (MESFETs) producing 4.6 W/mm at 3.5 GHz [1] and AlGaN/GaN high electron mobility transistors (HEMTs) exhibiting 9.8 W/mm at 8 GHz [2]. The material properties underpinning these results and the prospective application areas for these devices have been previously reviewed [3]. Although these results have set the state of the art for microwave power density, it is generally recognized that significant developmental work remains for these technologies to become viable. An area of particular concern is the limiting effect of electronic traps on microwave power performance [4]–[8]. Traps influence power performance through the formation of quasi-static charge distributions, most notably on the wafer surface or in the buffer layers underlying the active channel. This parasitic charge acts to restrict the drain-current and voltage excursions, thereby limiting the high-frequency power output.

In this paper, the current issues associated with trapping in AlGaN/GaN HEMTs and GaN MESFETs and, to a lesser extent, SiC MESFETs will be addressed. A variety of trapping effects have been observed, including transconductance frequency dispersion, current collapse of the direct current (dc) drain characteristics, gate- and drain-lag transients, and restricted microwave power output. Significant research activity has been directed toward understanding and eliminating these effects. This activity in many ways parallels that conducted during the development of the GaAs-based technology. Much of the knowledge obtained and techniques utilized for the GaAs case can be applied to the wide bandgap materials as well. Consequently, in Section II, we introduce some of the main concepts associated with trapping in microwave FETs by summarizing some of the related work carried out in support of the GaAs technology. A more detailed account of trapping effects in the wide bandgap devices will follow, with GaN and SiC covered in Sections III and IV, respectively.

II. TRAPPING IN GaAs FETs—AN OVERVIEW

GaAs is now a well-established commercial technology for both microwave and digital applications. It has reached this level of maturity after years of development in the 1980s and 1990s. During the course of this development, trapping effects were recognized as a serious issue. Deep levels, in both the GaAs substrate and buffer layers, and GaAs surface states or mobile surface charge were identified as the primary causes of deleterious trapping effects in GaAs MESFETs [9]–[13]. A variety of measurement techniques were utilized to characterize trapping in actual device structures. Drain-current transient measurements were frequently used because they are sensitive to the entire channel between the source and drain, unlike capacitance

Manuscript received September 13, 2001; revised December 27, 2001. This work was supported by the Office of Naval Research.

S. C. Binari and P. B. Klein are with the Naval Research Laboratory, Washington, DC 20375 USA (e-mail: binari@nrl.navy.mil).

T. E. Kazior is with Raytheon RF Components, Andover, MA 07870 USA.

Publisher Item Identifier S 0018-9219(02)05580-9.

0018-9219/02$17.00 © 2002 IEEE

Report Documentation Page

Form Approved
OMB No. 0704-0188

Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
DEC 2001		**00-00-2001 to 00-00-2001**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Trapping Effects in GaN and SiC Microwave FETs	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Naval Research Laboratory,4555 Overlook Avenue SW,Washington,DC,20375**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**11**	

techniques that primarily probe the area under the gate [14]. The measurement of drain-current transients in response to gate and drain voltage pulses, referred to as gate lag and drain lag, respectively, was commonly employed. For GaAs MESFETs, it was demonstrated that drain lag was associated with buffer layer and substrate traps [11] and that gate lag was associated with surface effects [12]. Frequency dispersion measurements of the small-signal output conductance and transconductance were also employed to study trapping behavior. Transconductance dispersion was attributed to trapping at or near the surface and output conductance dispersion attributed to trapping in the material underlying the active channel [15].

As a result of trapping effects, the drain characteristics of GaAs MESFETs, measured using low-frequency curve tracers or parameter analyzers, did not accurately reflect the high-frequency drain characteristics. This prevented device and circuit designers from obtaining accurate device information to use in small- and large-signal models. The use of pulsed current–voltage (I–V) test systems [16], which pulsed both gate and drain voltage with submicrosecond pulsewidths, yielded the drain characteristics that more accurately represented the device characteristics under high-frequency conditions, especially for those systems for which an arbitrary quiescent bias could be set [17]. It was demonstrated that device performance could be accurately predicted by using the pulsed I–V characteristics in small- and large-signal models [17]. The provision for setting a quiescent bias is an important feature in that the bias establishes steady-state trap populations, which generally could not follow the short pulses or high-frequency signals. As a result, varying the quiescent bias in a pulsed I–V measurement provided useful insight into trapping behavior. It was demonstrated that the drain current measured under pulsed conditions could be considerably less than that measured for dc conditions. This difference between the static and pulsed drain characteristics is directly related to the limitation in the large signal performance of these devices. Devices fabricated with silicon nitride passivation were shown to exhibit better agreement between the dc and pulsed I–V drain characteristics, as well as improved microwave power performance, suggesting the role of surface trapping in these effects [17].

The effect of surface trapping in GaAs MESFETs was reduced to manageable levels through the control of the gate recess geometry, proper surface preparation, modifications to the epitaxial layer doping profile [18], and dielectric passivation. Modifications to the layer structure underlying the active channel (e.g., the incorporation of buried p-layers) led to reductions in drain lag and output conductance dispersion.

AlGaAs/InGaAs pseudomorphic HEMTs (PHEMTs) displayed similar surface trapping effects, which were possibly exacerbated due to the closer proximity of the surface to the active channel [19]. Analogous to the GaAs MESFET, compressed pulsed I–V characteristics and poor microwave power performance were obtained for devices plagued by surface trapping. Parasitic gating due to surface charge between the gate and the drain was thought responsible for the poor performance. This parasitic gate was believed to be formed as the result of electrons tunneling from the gate metal to nearby surface states, with the associated trapped charge resulting in a reduction of the maximum alternating current (ac) drain current. Similar to the GaAs MESFET, improvements in the material quality and optimization of the epitaxial layer structures, gate recess structure (particularly the double recess), surface pretreatment, and surface passivation were collectively responsible for the attainment of optimal power performance. As a result, GaAs PHEMTs have become one of the leading devices for a wide range of commercial and military applications, including cellular phone power amplifiers (800–1900 MHz), radar (X band), satellite communications (Ka band), and automotive applications (V band).

During the evolution of GaAs-based HEMTs, a phenomenon known as “current collapse” was observed in AlGaAs/GaAs device structures. In recent years, the term “current collapse” has been used as a generic description of any observed reduction in the drain current of GaN-based FETs. Historically, it is associated with a very specific phenomenon: the persistent (yet recoverable) reduction of the dc drain current that results from the application of a high drain-source bias. We will continue to use this terminology in reference to nitride-based devices. A detailed study of this effect was first carried out in AlGaAs/GaAs HEMTs (where collapse is observed only at low temperature) by Drummond *et al.* [20] and by Fischer *et al.* [21]. These authors concluded that current collapse resulted from the trapping of hot channel carriers (accelerated by the high drain-source bias) that were injected into the AlGaAs layer, predominantly on the drain side of the gate (where the electric field is highest). This model was based, in part, on the similarity of the AlGaAs/GaAs results with earlier studies of Si MOSFETs [22], [73] and CdSe thin-film transistors [23], where it was concluded that hot channel carriers were being injected into the oxide layer. As the trapped carriers constitute a nonequilibrium charge distribution in the AlGaAs, any stimulus, such as light or heat, that assists the trapped carriers in overcoming the emission barrier of the traps, will tend to return the carriers to the channel and to restore the equilibrium drain current. It was suggested [20], [21] that the deep trap responsible for collapse in the AlGaAs/GaAs HEMT was the same center that was associated with persistent photoconductivity (PPC) in the AlGaAs layer (i.e., the DX center). This was verified in a very detailed investigation by Kastalsky and Kiehl [24], where both current collapse and shifts in the threshold voltage were shown to be associated with the presence of DX centers.

In addition to the effects described above, the lack of stability of microwave power output over time, for both GaAs MESFETs and PHEMTs, has been associated with charge trapping [25], [26]. In the discussion thus far, all of the trapping effects have been transitory in nature. However, power output stability is classified according to the permanence of the change in power output. A *recoverable* reduction in power output over time is referred to as power

drift and a *permanent* degradation in power output is referred to as power *slump* [26]. Both effects have been correlated with changes in the degree of gate lag and are attributed to electron trapping in the silicon nitride passivation layer [26] or to the creation of interface traps due to hot-electron effects [27]. In PHEMTs, power slump has been accompanied by a permanent reduction in drain current, but this was not necessarily the case for MESFETs. Slump and drift were reduced by material improvements, passivation, surface pretreatment optimization (mostly proprietary), and channel geometry/doping optimization, which resulted in reducing the peak fields in the gate-drain region of the device channel in order to minimize hot electron effects.

III. Trapping Effects in GaN-Based MESFETs and HEMTs

In this section we will review trapping effects in nitride-based FETs. In principle, trapping centers can reside at the surface, in the AlGaN barrier layer, at the two-dimensional electron gas (2DEG) interface, or in the GaN buffer layer. While it is known that defects exist in the AlGaN layer [28], [29], a correlation with compromised microwave performance has not been established. This holds true for states at the AlGaN/GaN interface as well, although their presence is expected to limit the 2DEG channel mobility. Although there are a variety of conflicting explanations for the observed trapping effects, the picture that seems to be emerging is that trapping at the surface and in the underlying buffer layers are primarily responsible for compromised microwave power performance. Consequently, the discussion that follows will be divided between trapping phenomena associated with these two regions.

It should also be noted that the nitrides are characterized by a high concentration (typically 10^8 to 10^{10} cm^{-2}) of dislocations. A number of studies have shown that electrically active trapping centers can exist in the vicinity of these extended defects [30], [31]. However, there is little information to directly link specific traps and trap-related phenomena with dislocations. Consequently, while some of the trapping phenomena discussed below may eventually be shown to result from defects localized at dislocations, we are currently unable to distinguish these from traps located elsewhere in the material.

A. Terminology

In reviewing the literature cited below, it is important to bear in mind that the terminology being used has sometimes been inconsistent. The use of the terms gate lag, drain lag, pulsed I–V, transconductance and output resistance dispersion, power drift, and power slump have been reviewed above and are generally used with little ambiguity in the literature. We have already defined current collapse, based on its origins in the GaAs technology. However, it is not uncommon to find the term "current collapse" applied to any measured reduction in drain current when, in fact, one of the other trap-related phenomena is being observed. Furthermore, the differences between the pulsed and dc drain characteristics and the differences between the expected microwave power output (based on the dc characteristics) and the actual power output are referred to as various types of "dispersion" or "slump." In this paper, will we restrict the terminology to the terms already defined above.

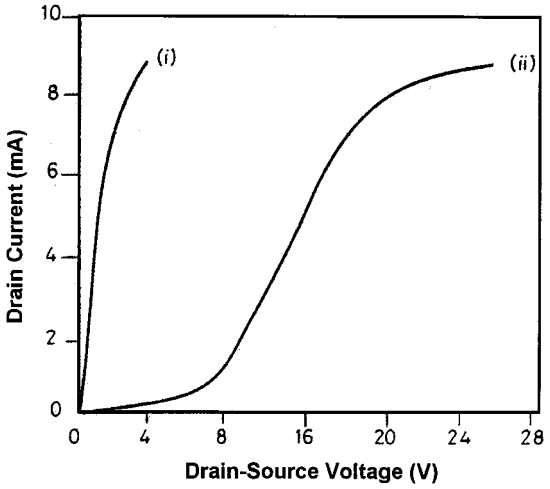
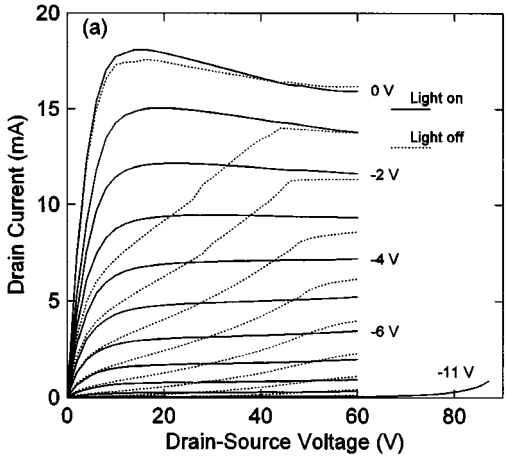


Fig. 1. Current collapse in an AlGaN/GaN HEMT [32]. Drain current as a function of drain–source voltage (with the gate floating) is shown i) before and ii) after the application of a 20-V drain–source bias.

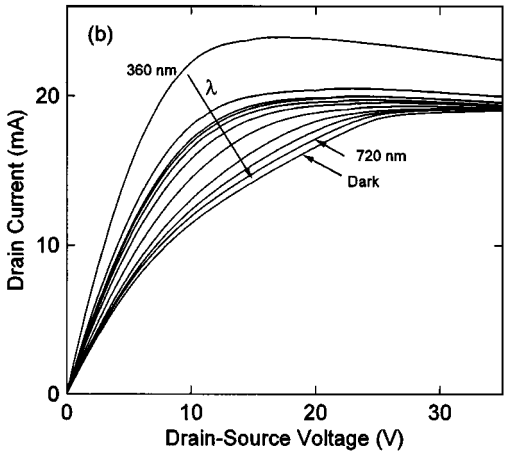
B. Buffer Trapping—Current Collapse

Current collapse in a nitride-based FET was first reported in an AlGaN/GaN HEMT by Khan *et al.* [32], shown in Fig. 1, for characteristics taken both before i) and after ii) the application of a large drain bias. The drain current could be recovered by illumination with light either corresponding to the GaN bandgap or near 600 nm, the latter being associated with an unknown trap. Following earlier work done in the AlGaAs/GaAs system, the collapse was assigned to hot carrier trapping in the AlGaN.

Trapping effects in GaN MESFETs were reported by Binari *et al.* [33]. Current collapse is evident in comparing the I–V characteristics shown in Fig. 2(a), with (solid line) and without (dotted line) light illumination. At elevated temperature (up to 155 °C), the drain current exhibited little or no collapse, consistent with thermal emission from the deep traps, while the time dependence of the drain-current recovery reflected a multicomponent response, suggesting the involvement of multiple traps in the collapse. Under illumination, the qualitative wavelength dependence of the drain-current recovery, shown in Fig. 2(b), suggested a broad, trap-related absorption below the GaN bandgap. These results were interpreted in terms of deep traps in the high-resistivity (HR) organometallic vapor phase epitaxy (OMVPE) GaN buffer layer, which is grown under conditions that enhance trap formation in order to compensate the shallow donors and produce HR material. Further studies [6], [34] confirmed the location of the traps in the HR GaN buffer layer, as collapse was not observed in devices grown on conducting substrates: the traps in the structure were already filled by compensating shallow donors.



(a)



(b)

Fig. 2. (a) Current collapse in a GaN MESFET, with (solid) and without (dotted) light illumination. (b) Dependence of drain-current recovery on illumination wavelength [33].

By studying the wavelength dependence of the drain-current recovery in detail, Klein *et al.* [35] were able to develop a method to provide spectroscopic signatures of the traps responsible for current collapse and to estimate the trap depth relative to the band edges. This was accomplished by measuring the fractional drain-current increase, above the collapsed level, induced by illumination with a measured amount of light. The wavelength dependence of this increase, normalized by the total number of incident photons, was shown [36] to be proportional to the absorption spectrum associated with the photoionization process that released the carriers from the traps. This *photoionization* spectrum is a characteristic of a given trap and may be employed for defect identification. The spectrum obtained from a GaN MESFET at 300 K is shown in Fig. 3. Two broad absorptions were observed below the GaN bandgap, corresponding to the photoionization of carriers from two distinct traps, labeled Trap1 and Trap2. The fitted photoionization thresholds located these defects approximately 1.8 and 2.85 eV below the conduction band, respectively. It is interesting that each of these absorptions was also found to match published spectra (see Fig. 3) of PPC centers in GaN [37], [38], indicating that these traps can induce both PPC and current

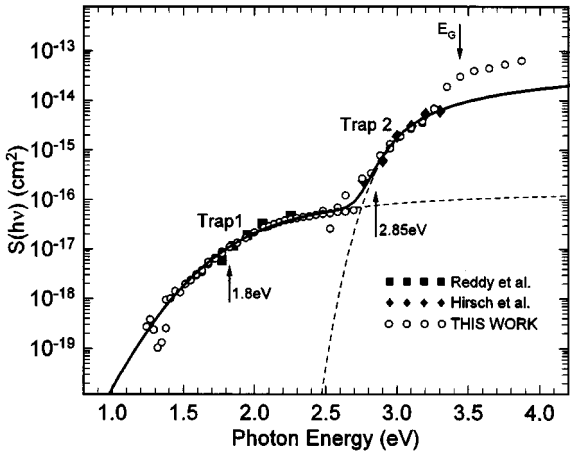


Fig. 3. Photoionization spectrum of a GaN MESFET. Two traps responsible for current collapse are observed. Spectra are similar to those observed in recent studies of PPC [35].

collapse. The DX center in AlGaAs is also known to play this dual role. In the nitrides, a DX-like center associated with oxygen in AlGaN has recently been observed [39]. This trap, like DX in AlGaAs, is effective only at low temperatures. However, in the nitrides, current collapse is observed at room temperature. It is, therefore, unlikely that collapse in nitride-based FETs is due to a DX-like defect. This is supported by spectral measurements in the nitrides, analogous to those of Kastalsky and Kiehl [24], which exhibit no increase in response at the AlGaN bandgap [40]. Using a simple modeling approach [36], measurements of the dependence of the light-induced drain-current increase upon the total amount of incident light were fitted to enable the determination of areal densities and photoionization cross-sections for each of the traps. In the GaN MESFET, the densities for both traps were found to be $\sim$mid-10^{11}/cm^2.

Several other investigators have assigned current collapse effects observed in GaN MESFETs to traps in the buffer layer. Zhang *et al.* [41] suggested that the significant reduction in dc drain current that they observed in GaN junction FETs (FETs) after application of high drain bias was a result of high field injection and subsequent trapping of electrons in the HR GaN buffer layer. Kuliev *et al.* [42] observed a significant collapse in the dc drain current of a GaN MESFET subjected to reverse gate diode bias stress and UV illumination was found to recover the current collapse. They suggested the presence (but not the location) of electron traps. Meneghesso *et al.* [43] studied current collapse in GaN MESFETs and found a correlation between the decrease in drain current and a shift in threshold voltage. Using phototransient measurements, they attribute this collapse to trapping under the gate and in the gate-drain access region. Using photoionization spectroscopy measurements, they also identified traps in the undoped buffer or at the buffer/channel interface.

Photoionization measurements have also been carried out in AlGaN/GaN HEMT structures [40]. The photoionization spectra were found to be similar to those of the GaN MESFET, exhibiting the two broad trap-related absorptions and a rapid increase at the GaN bandgap. No enhancement

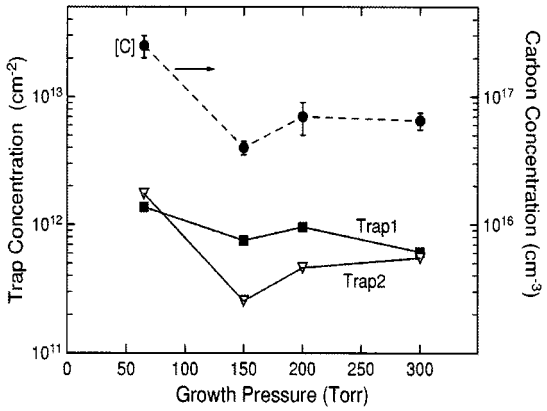


Fig. 4. Dependence of the areal concentrations of traps associated with current collapse on the OMVPE growth pressure [44].

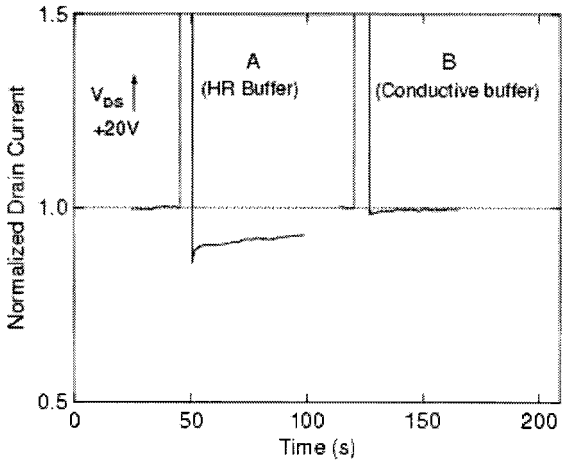


Fig. 5. Drain lag measurements. Drain current is normalized to the low-field value (V_{DS} = 10–100 mV). "A": Representative response for a device on a HR buffer. "B": Device on a conductive buffer layer [6].

of the optically induced drain-current recovery was observed for photon energies at or above the AlGaN bandgap. This suggested that the same traps in the HR GaN buffer layer, which were responsible for current collapse in the MESFET, produced collapse in the HEMT as well. Subsequent studies were carried out [44] on wafers with HR GaN layers grown at differing OMVPE growth pressures in order to vary the deep trap incorporation. Lower pressures have been observed to correlate with more severe current collapse as well as a greater incorporation of carbon impurities into the layers [45]–[47]. Photoionization spectra of these devices indicated [44] a clear enhancement of Trap2 absorption at the lowest growth pressures. Fitting the measured dependence of the drain-current increase on total light illumination, using a model similar to that employed for the GaN MESFET [36], the concentration of each of the traps could be determined as a function of OMVPE growth pressure. This is shown in Fig. 4, along with the carbon concentration in the HR GaN layer as determined by secondary ion mass spectrometry. Both trap concentrations were found to increase at low growth pressures and the Trap2 concentration was seen to *track* the carbon concentration. The two were shown to be proportional, thus, suggesting that Trap2 is a carbon-related deep defect in the HR GaN layer, similar to that suggested two decades ago by Ogino and Aoki [48]. While the concentration of Trap1 did not track the carbon in the same way, the increase in trap concentration at low growth pressures, where dislocations and grain boundary effects are expected to be greatest, suggested that Trap1 may be related to these defects. The current evidence would suggest that current collapse in nitride-based FETs grown by OMVPE is associated with traps in the HR GaN buffer layer related to carbon incorporation and to structural defects.

C. Buffer Trapping—Drain Lag

Recovery from current collapse by thermal emission of the trapped carriers has a characteristic time dependence and the temporal response of the current collapse (i.e., reduced drain current) can be investigated with drain lag measurements. In addition to establishing this time dependence, drain lag measurements are also useful for quantifying this effect, since devices that exhibit minimal current collapse also exhibit minimal drain lag. Drain lag measurements for two devices are shown in Fig. 5. For these measurements, the device is pulsed from an equilibrium condition at a low V_{DS} value (10–100 mV) to a high V_{DS} value (15–20 V) and then returned to the low V_{DS} value. V_{GS} is maintained at 0 V. Exposure to the high V_{DS} induces current collapse and the return of the drain current to its starting value is monitored as a function of time. The plotted drain current is normalized to the low-field value. A typical long-term drain lag characteristic is given by curve A. The recovery time is on the order of minutes. Devices A and B were fabricated on the same wafer, which had a spatially varying conductivity (HR for device A, conductive for device B). The degree of drain lag is apparently related to the conductivity of the buffer layer. The deep levels responsible for producing the HR material are likely to be responsible for this trapping effect. The reduction in drain lag for device B is consistent with fewer traps in the conductive buffer regions or with the filling of these traps by shallow donors.

Dang *et al.* [49] also used drain lag measurements to study traps in GaN HFETs. Although drain lag is usually associated with buffer layer trapping, it was demonstrated that modifying the surface through the use of KOH exposure can result in changes to both gate and drain lag. Three traps were identified: 1) intermediate time constant traps ($\sim$10 s), which were attributed to deep levels in the AlGaN; 2) fast traps ($\sim$1 s), attributed to the surface; and 3) slow traps ($>$100 s), which were associated with the channel. Further work is needed to clarify the effect that surface treatment has on drain lag.

D. Surface Trapping in GaN FETs

It is widely acknowledged that surface states or surface charge can have a pronounced effect on the microwave performance of HEMTs. As in the GaAs case, surface trapping can generally be identified through gate lag measurements. A number of groups have used this approach to study the effect of trapping on GaN devices [6], [49]–[51]. The association between gate lag and surface trapping is generally estab-

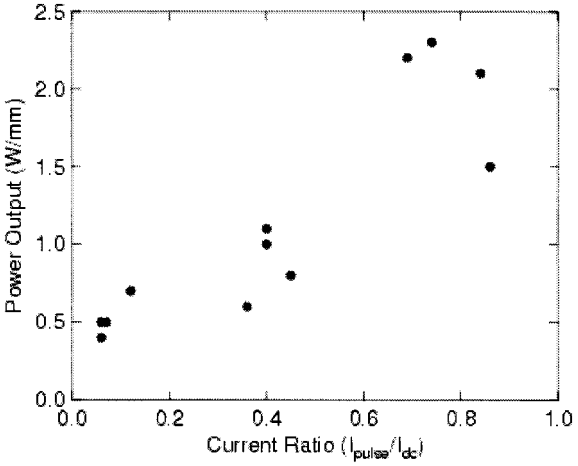


Fig. 6. Correlation with power output with gate lag for AlGaN/GaN HEMTs. The maximum microwave power output at 2 GHz is plotted against the ratio of the pulsed drain current to the dc drain current [54].

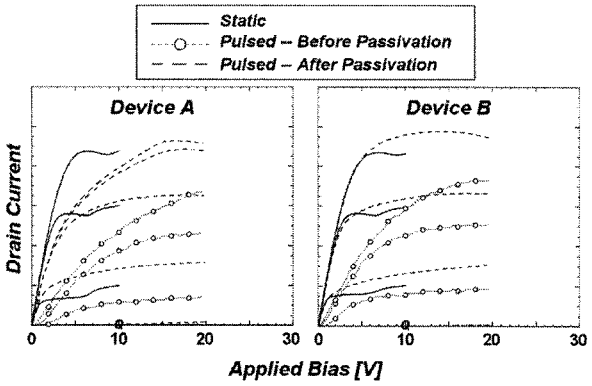


Fig. 7. DC and pulsed I–V drain characteristics for AlGaN/GaN HEMT wafers fabricated with different passivation processes. Pulsed I–V characteristics are shown both before and after passivation.

lished by correlating gate lag with changes made to the device surface through techniques such as chemical treatment or dielectric passivation. Binari *et al.* [52]–[54] associated gate lag with the presence of surface trapping in the access region between gate and drain. They found that annealing unpassivated AlGaN/GaN HEMTS at 300 °C reduced or eliminated gate lag and g_m dispersion, possibly due to the passivation of surface traps during the annealing process. Similar to GaAs FETs, they observed a direct correlation between gate lag and output power in unpassivated GaN HEMTs, as shown in Fig. 6. By adding a silicon nitride passivation layer, a dramatic improvement in drain-current response was observed [34], [50]. As mentioned above, Dang *et al.* [49] also used drain-current transient measurements to study traps in GaN HFETs. While surface modifications usually affect gate lag, these authors demonstrated that treating the surface with KOH can result in changes to both gate lag and drain lag.

Trassaert *et al.* [55] observed a significant difference between the dc and pulsed I–V characteristics of unpassivated GaN MESFETs. Since they observed no shift in threshold voltage, they concluded that the traps responsible for the difference between the dc and pulsed characteristics are associated with surface states. Others have utilized pulsed I–V measurements to provide information on trapping effects and have correlated these measurements with microwave power performance [56], [57]. Kazior *et al.* [56] found that unpassivated devices tended to exhibit significantly compressed pulsed I–V characteristics and this was correlated with poor microwave power performance. Passivation was found to reduce the pulsed I–V compression with a concomitant improvement in RF power. Passivation presumably establishes a near-optimal dielectric/semiconductor interface that best neutralizes the net surface charge arising from the combination of a polarized AlGaN barrier and surface states associated with surface defects, dangling bonds and adsorbed ions, or charged residuals. Several other groups [6], [50], [58] have reported on the effect of silicon nitride passivation on microwave power performance. Due to the reduction of surface trapping, increases in output power from 20% to a factor of two have been observed relative to the unpassivated case. However, devices passivated with nominally the same passivation process and surface pretreatment exhibit varying degrees of pulsed I–V current compression (see Fig. 7), suggesting that the reduction in pulsed I–V current compression is a strong function of surface and material quality.

While the pulsed measurements referred to above can be thought of as approximating large-signal conditions, it is possible to directly measure the drain current under large-signal gate voltage drive. This has been done as a function of frequency [59]–[61] and transition frequencies varying over a very large range (10^{-3} Hz to 10 GHz) were observed. Large reductions in the current amplitude were observed over this frequency range, which translates directly into lower power outputs. This dispersion was attributed to piezo-related charge states at the surface, which create a parasitic gate between the gate and drain. This parasitic gating concept is analogous to that described for GaAs devices [19]. In related large-signal measurements, Nguyen *et al.* [5] observed changes in the dc drain current of GaN HEMTs as a function of the input radio frequency (RF) drive. To identify the location of the responsible traps, they performed RF measurements as a function of gate bias. It was concluded that the drain-current compression under RF drive is due to traps located either in the AlGaN barrier or at the surface and not due to trapping of hot electrons in the buffer layer (i.e., current collapse).

In contrast to the large-signal studies referred to above, small-signal frequency dispersion measurements have been employed to determine the activation energies of traps causing g_m and output resistance (R_{ds}) dispersion in AlGaN/GaN HEMTs. Kruppa *et al.* [62] measured the g_m and R_{ds} dispersion as a function of temperature of AlN/GaN HFETs. Two energy levels were identified to be associated with traps responsible for the observed frequency dispersion and suggested that they were located in the GaN channel. Umana-Membreno *et al.* [63] used the frequency dispersion of the output admittance characteristics to characterize traps in AlGaN/GaN HEMTs. Two trap levels were identified—one attributed to the Si donor in AlGaN and the

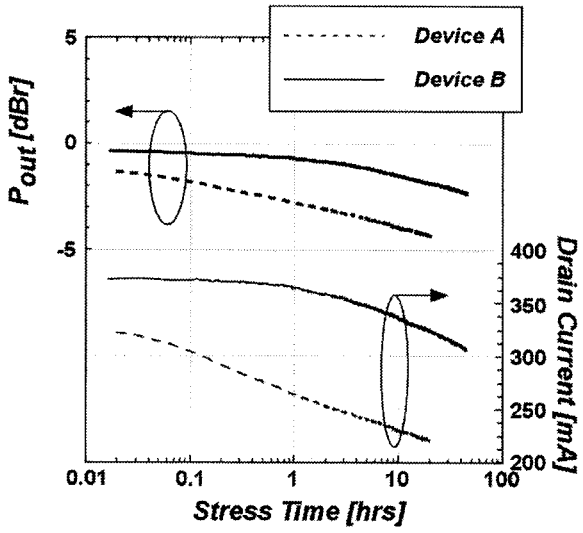


Fig. 8. Measured drain-current and power output at 10 GHz as a function of time for two 1.2-mm-wide AlGaN/GaN HEMT devices. Devices were continuously biased at a V_{DS} of 20 V and driven at the 3-dB compression point.

other to either surface states on the drain side of the gate or to traps at the AlGaN/GaN interface. The location of the traps could not be identified without ambiguity.

In addition to the measurement techniques discussed above, capacitance spectroscopy has also been shown to be sensitive to surface properties. Schaadt *et al.* [64] used this technique to confirm the existence of a high density of traps and identified these as electron traps at or near the AlGaN surface.

The stability of the microwave power output of GaN HEMTs has recently received a fair amount of discussion [65], though little has been published on this topic. It is generally recognized that GaN HEMTs can display an appreciable power drift and power slump. Power slump is typically accompanied by concomitant changes in the dc drain characteristics. An example of this permanent degradation in drain-current and power output is shown in Fig. 8 for 1.2-mm-wide devices biased at a V_{DS} of 20 V and driven at the 3-dB compression point. The power output levels are referenced to the starting value. While the magnitude of these deleterious effects is observed in varying degrees, it is recognized that their existence is a significant issue. In the GaAs PHEMT, electron trapping in the silicon nitride passivation layer [26] and the creation of traps due to hot-electron effects [27] were thought to be the mechanisms that contributed to power slump. With the higher fields present in GaN devices, these hot-electron effects can be expected to be more pronounced compared to GaAs devices. However, at this time it is unclear whether the power slump present in the GaN HEMTs is due to this mechanism or whether other trapping effects or nontrapping related mechanisms, such as contact degradation, are responsible.

E. Traps in GaN-Based Devices—Summary

It is clear that trapping effects play a significant role in the widely variable performance observed in GaN-based FETs. However, while many similar trends and trapping effects are observed, there is not yet a consensus on the nature of the traps responsible for the observed performance variations. This arises from the relative immaturity of the GaN-based FET material system. Variations between laboratories in material quality, layer structure, growth technique, and device processing complicate this picture. At this point in time, there is a preponderance of evidence to suggest that current collapse of the dc device characteristics is related to the presence of traps in the GaN buffer, whereas, gate lag and the related pulsed I–V characteristics are associated with surface effects. Both sources of trapping lead to a compromised microwave power performance.

IV. Trapping Effects in SiC MESFETs

Similar to GaN, SiC exhibits a high breakdown field and a high saturated electron velocity. Silicon carbide also offers a high thermal conductivity, making it a natural choice for high-power electronics. However, without a viable heterostructure technology to support the fabrication of HEMT structures, SiC microwave devices are at a distinct disadvantage for high-frequency applications, relative to the GaN-based structures. While vertical devices such as the SiC static induction transistor (SIT) have been developed for high-power lower frequency applications, the SiC MESFET has been advanced as the SiC device for use at higher frequency. Although nitride-based HEMT structures can attain considerably higher frequency response, the frequency-power-bandwidth design tradeoffs between SiC MESFETs and GaN HEMTs are not well established and the SiC MESFET may offer advantages for total power output due to its lower input capacitance [66]. The SiC technology is certainly more mature than that of GaN. However, SiC MESFETs are not without trapping problems associated with both the surface and with the layers underlying the active channel. Over the past few years, there has been a significant effort to overcome the trapping problems that have compromised the microwave power output in these devices.

With the realization of large-area semi-insulating (SI) SiC substrate material, larger FET structures could be fabricated for higher output powers without suffering the large parasitic capacitive losses of previous devices grown on n^+ substrates. However, it was observed by Noblanc *et al.* [67], [68] that the drain current of these devices decayed with time, with a time constant on the order of seconds. The current could be restored by removing the drain bias for several seconds. As a result of this effect, the RF power output of these devices was observed to be inferior to that of devices grown on n^+ substrates. As shown in Fig. 9, the drain-current decay was found to be much less severe for devices grown on n^+ substrates [see Fig. 9(b)] than on SI substrates [see Fig. 9(a)]. In addition, with increasing negative gate bias, the effect became more severe. It was, thus, concluded that the traps responsible for this effect were probably associated with the SI substrate or the substrate/p-buffer layer interface. Further work by these authors [69] probed the sensitivity of this trapping

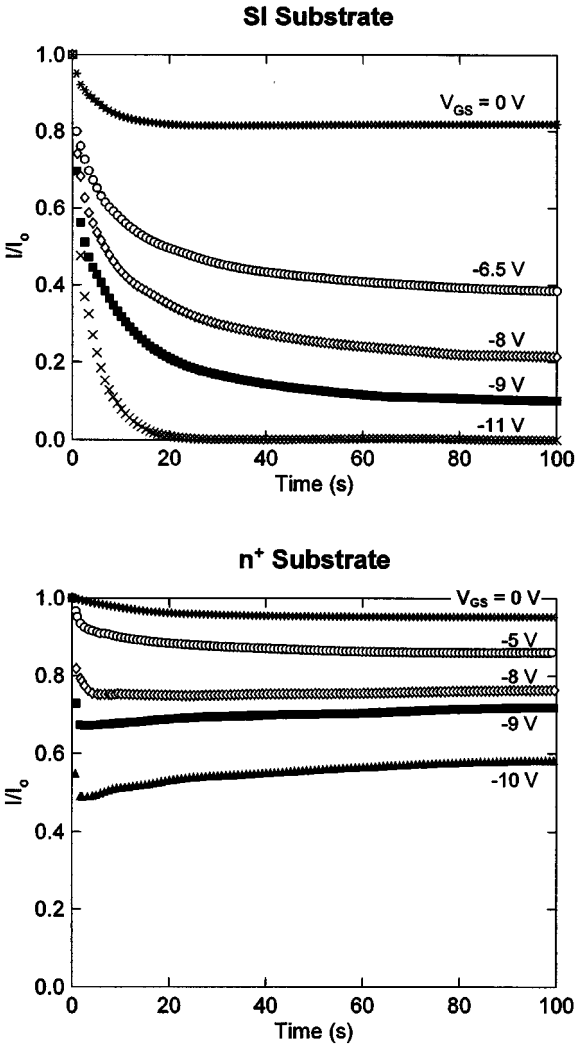


Fig. 9. Relative drain-current decay for SiC MESFETs grown on SI and n^+ substrates following the application of $V_{DS} = 30$ V for several values of V_{GS} [67].

effect to variations in the thickness and doping level of the p-type buffer. While the dc drift could be almost eliminated by using a thicker buffer, a rapid (μs) decay of the drain current persisted if an RF signal was applied to the gate, leading to a reduction in the RF output power. It was concluded that the trapping effect was caused by the injection of carriers from the channel into the p-buffer, similar to the mechanism of current collapse discussed above, and that the effect was dependent upon the depletion state of the buffer layer. In fact, the dc I–V characteristics before and after high voltage biasing clearly indicated a collapse of the drain current.

In addition to the substrate/buffer layer trapping discussed above, drain-current transients related to surface trapping have also been observed in SiC MESFETs [70], [71]. This can be seen in Fig. 10, where the drift in the drain current for three values of drain bias is compared for devices with etch damage (etched) and with etch damage removed by an oxidation and strip procedure (SacOx). It was observed [70] that if the recess etch damage was removed from the ungated surface regions between the gate and the source and drain, the drain current decay was decreased substantially.

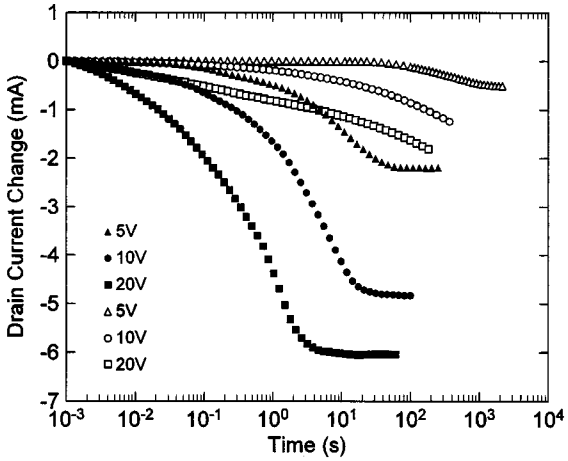


Fig. 10. Relative drain-current decay for SiC MESFETs grown on an SI substrate following the indicated drain voltage step. Devices with recess damage removed with a sacrificial oxidation/strip process (SacOx, open symbols) and recess etch damage not removed (etched closed symbols). $V_{GS} = 0$ V [70].

After passivating the channel recess and placing the gate in a second channel recess cut through the passivation [71], the dc drain-current transient was essentially eliminated.

Siriex *et al.* [72] advanced work on substrate trapping by carrying out pulsed I–V and S-parameter measurements (with varying gate and drain quiescent levels) on MESFETs grown on SI substrates. The observed trapping effects were analyzed using a nonlinear modeling procedure that was able to account for the experimental observations, including a substantial drop in the average drain current with increasing input power. This behavior was associated with an increase in trap-filling as the drain voltage swing was increased. The nonlinear model was applied [7] to optimize the buffer layer between the SI substrate and the active layer, such that carrier injection at high bias was minimized or eliminated. Measurements were carried out on several devices grown with varying buffer layer thickness and doping. It was reported [7] that channel carrier injection was successfully reduced or eliminated by this procedure, although no information about the optimized device was provided, for proprietary reasons. Additionally, the conductance dispersion was studied as a function of temperature in order to extract trap parameters. It was concluded that a trap with activation energy of 1.07 eV was involved, which was tentatively identified as due to vanadium defects.

V. Conclusion

Although outstanding microwave power performance has been demonstrated with both SiC and GaN-based FETs, significant issues remain regarding the further development of these technologies. One prominent issue is the limiting effect of electronic traps on the device microwave power performance. Similar trapping problems were faced during the development of the GaAs technology and it is apparent that much of the knowledge obtained and techniques utilized for the GaAs case can be applied to the present situation in the wide bandgap devices.

Although the SiC technology is more mature than that of GaN, SiC MESFETs still suffer from trapping-related issues. Trapping associated with the SiC substrate is apparent, but buffer layer solutions to the substrate trapping problem have yielded promising results. Surface-related trapping has been shown to affect device performance and passivation and gate-recess schemes have been utilized to minimize this effect.

Considerably more work has been published on trapping in GaN FETs than on SiC devices. While it is clear that trapping effects play a significant role in the performance observed in GaN-based FETs, the relative immaturity of the GaN-based material system and the variations between laboratories in device design, material quality, and device processing complicate the understanding of trapping in these devices. At this point in time, there is considerable evidence to show that current collapse of the dc device characteristics is related to the presence of traps in the GaN buffer layer. Surface trapping has been shown to be minimized through the use of dielectric passivation, though with variable degrees of success. Both sources of trapping result in compromised microwave power performance.

The results of these investigations provide direction regarding the optimization of material quality, process technologies, and epitaxial material and device design. We anticipate that device performance will be improved and trapping phenomena will continue to be minimized through further improvements in the materials growth and process technology for these two materials systems.

ACKNOWLEDGMENT

The authors would like to thank their colleagues at the Naval Research Laboratory and at Raytheon for many fruitful discussions on this topic.

REFERENCES

[1] S. T. Allen, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring, and J. W. Palmour, "Progress in high power SiC Microwave MESFETs," in *Proc. IEEE MTT-S*, 1999, pp. 321–324.

[2] Y.-F. Wu, D. Kapolnek, J. Ibbetson, N.-Q. Zhang, P. Parikh, B. P. Keller, and U. K. Mishra, "High Al-content AlGaN/GaN HEMT on SiC substrates with very-high power performance," in *Proc. Int. Electron Device Meeting*, 1999, pp. 925–927.

[3] J. C. Zolper, "Wide bandgap semiconductor microwave technologies: From promise to practice," in *Proc. Int. Electron Device Meeting Digest*, 1999, pp. 389–392.

[4] ——, "Progress toward ultra-wideband AlGaN/GaN MMICs," *Solid-State Electron.*, vol. 43, no. 8, pp. 1479–1482, Aug. 1999.

[5] C. Nguyen, N. X. Nguyen, and D. E. Grider, "Drain current compression in GaN MODFETs under large-signal modulation at microwave frequencies," *Electron. Lett.*, vol. 35, no. 16, pp. 1380–1382, Aug. 1999.

[6] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 465–471, Mar. 2001.

[7] N. Sghaier, A. K. Souifi, J.-M. Bluet, M. Berenguer, G. Guillot, O. Noblanc, and C. Brylinski, "Influence of interface states on output conductance on 4H-SiC MESFETs on semi-insulating substrate," in *Proc. Mater. Res. Soc. Symp.*, vol. 640, 2001, pp. H4.4.–H4.4.6.

[8] E. Morvan, O. Noblanc, C. Dua, and C. Brylinski, "SiC microwave power devices," *Mater. Sci. Forum*, vol. 353–356, pp. 669–674, 2001.

[9] M. Rocci, "Status of the surface and bulk parasitic effects limiting the performances of GaAs ICs," *Physica*, vol. 129B, pp. 119–138, 1985.

[10] P. C. Canfield and D. J. Allstot, "The potential of p-well GaAs MESFET technology for precision integrated circuits," in *Proc. IEEE Int. Symp. Circuits and Systems*, 1990, pp. 3065–3068.

[11] W. Mickanin, P. Canfield, E. Finchem, and B. Odekirk, "Frequency-dependent transients in GaAs MESFETs: Process, geometry, and material effects," in *Proc. IEEE GaAs IC Symp.*, 1989, pp. 211–214.

[12] R. Yeats, D. C. D'Avanzo, K. Chan, N. Fernandez, T. W. Taylor, and C. Vogel, "Gate slow transients in GaAs MESFETs-causes, cures, and impact on circuits," in *Proc. Int. Electron Device Meeting*, 1988, pp. 842–845.

[13] B. Van Rees, B. Liles, B. Hewitt, and W. Schaff, "The effect of deep levels on the large-signal performance on GaAs FETs," in *Proc. 1982 Int. Symp. GaAs and Related Compounds*, 1983, pp. 355–362.

[14] R. Magno, R. Shelby, and W. T. Anderson, "A deep-level transient spectroscopy study of high electron mobility transistors subjected to lifetime stress tests," *J. Appl. Phys.*, vol. 66, no. 11, pp. 5613–5617, Dec. 1989.

[15] P. C. Canfield, D. J. Allstot, J. Medinger, and L. Forbes, "Buried-channel GaAs MESFETs with improved small-signal characteristics," in *Proc. IEEE GaAs IC Symp.*, 1987, pp. 163–166.

[16] T. M. Barton, C. M. Snowden, J. R. Richardson, and P. H. Ladbrooke, "Narrow pulse measurement of drain characteristics of GaAs MESFETs," *Electron. Lett.*, vol. 23, no. 13, pp. 686–687, June 1987.

[17] A. Platzker, A. Palevsky, S. Nash, W. Struble, and Y. Tajima, "Characterization of GaAs devices by a versatile pulsed I–V measurement system," in *Proc. IEEE MTT-S*, 1990, pp. 1137–1140.

[18] H. Takahashi, K. Asano, K. Matsunaga, N. Iwata, A. Mochizuki, and H. Hirayama, "Step-recessed gate structure with an undoped surface layer for microwave and millimeter-wave high power, high efficiency GaAs MESFETs," *IEICE Trans. E-74*, pp. 4141–4146, 1991.

[19] J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with improved breakdown voltage for X- and Ku-band power applications," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 752–759, May 1993.

[20] T. J. Drummond, R. J. Fischer, W. F. Kopp, H. Morkoc, K. Lee, and M. S. Shur, "Bias dependence and light sensitivity of (Al,Ga)As/GaAs MODFETs at 77K," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1806–1811, Dec. 1983.

[21] R. Fisher, T. J. Drummond, J. Klem, W. Kopp, T. S. Henderson, D. Perrachione, and H. Morkoç, "On the collapse of drain I–V characteristics in modulation-doped FETs at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1028–1031, 1984.

[22] T. H. Ning, C. M. Osburn, and N. H. Yu, "Effect of electron trapping on IGFET characteristics," *J. Electron. Mater.*, vol. 6, pp. 65–76, 1977.

[23] J. J. Wysocki, "Drain-current distortion in CdSe thin-film transistors," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1798–1805, Nov. 1982.

[24] A. Kastalsky and R. A. Kiehl, "On the low-temperature degradation of (AlGa)As/GaAs modulation-doped field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 414–423, 1986.

[25] J.-M. Dumas, F. Garat, and D. Lecrosnier, "Development of gate-lag effect on GaAs power MESFETs during aging," *Electron. Lett.*, vol. 23, no. 4, pp. 137–141, Feb. 1987.

[26] J. C. M. Hwang, "Relationship between gate lag, power drift, and power slump of pseudomorphic high electron mobility transistors," *Solid-State Electron.*, vol. 32, no. 8, pp. 1325–1331, Aug. 1999.

[27] G. Meneghesso, A. Paccagnella, Y. Haddab, C. Canali, and E. Zanoni, "Evidence of interface trap creation by hot-electrons in AlGaAs/GaAs high electron mobility transistors," *Appl. Phys. Lett.*, vol. 9, no. 10, pp. 1411–1413, Sept. 1996.

[28] S. T. Bradley, A. P. Young, L. J. Brillson, M. J. Murphy, W. J. Schaff, and L. F. Eastman, "Influence of AlGaN deep level defects on AlGaN/GaN 2DEG carrier confinement," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 412–415, Mar. 2001.

[29] A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, and J. M. Redwing, "Deep traps in high resistivity AlGaN films," *Solid-State Electron.*, vol. 42, no. 5, pp. 831–888, May 1998.

[30] P. J. Hansen, Y. E. Strausser, A. N. Erickson, E. J. Tarsa, P. Kozodoy, E. G. Brazel, J. P. Ibbetson, U. Mishra, V. Narayanamurti, S. P. DenBaars, and J. S. Speck, "Scanning capacitance microscopy imaging of threading dislocations in GaN films grown on (0001) sapphire by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 72, no. 18, pp. 2247–2249, May 1998.

[31] A. F. Wright and U. Grossner, "The effect of doping and growth stoichiometry on the core structure of a threading edge dislocation in GaN," *Appl. Phys. Lett.*, vol. 73, no. 19, pp. 2751–2753, Nov. 1998.
[32] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "Current/voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias," *Electron. Lett.*, vol. 30, no. 25, pp. 2175–2176, Dec. 1994.
[33] S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden, and J. A. Freitas, Jr., "Fabrication and characterization of GaN FETs," *Solid-State Electron.*, vol. 41, no. 10, pp. 1549–1554, Oct. 1997.
[34] S. C. Binari, K. Ikossi-Anastasiou, J. A. Roussos, D. Park, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "GaN electronic devices for microwave power applications," in *Proc. Int. Conf. GaAs Manufacturing Technology*, 2000, pp. 201–204.
[35] P. B. Klein, J. A. Freitas, Jr., S. C. Binari, and A. E. Wickenden, "Observation of deep traps responsible for current collapse in GaN metal semiconductor field effect transistors," *Appl. Phys. Lett.*, vol. 75, no. 25, pp. 4016–4018, Dec. 1999.
[36] P. B. Klein, S. C. Binari, J. A. Freitas, Jr., and A. E. Wickenden, "Photoionization spectroscopy of traps in GaN metal semiconductor field effect transistors," *J. Appl. Phys.*, vol. 88, no. 5, pp. 2843–2852, Sept. 2000.
[37] C. V. Reddy, K. Balakrishnan, H. Okumura, and S. Yoshida, "The origin of persistent photoconductivity and its relationship with yellow luminescence in molecular beam epitaxy grown undoped GaN," *Appl. Phys. Lett.*, vol. 73, no. 2, pp. 244–246, July 1998.
[38] M. T. Hirsch, J. A. Wolk, W. Walukiewicz, and E. E. Haller, "Persistent photoconductivity in n-type GaN," *Appl. Phys. Lett.*, vol. 71, no. 8, pp. 1098–1100, Aug. 1997.
[39] M. D. McCluskey, N. M. Johnson, C. G. Van de Walle, D. P. Bour, and M. Kneissl, "Metastability of oxygen donors in AlGaN," *Phys. Rev. Lett.*, vol. 80, no. 18, pp. 4008–4011, May 1998.
[40] P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors," *Electron. Lett.*, vol. 37, no. 10, pp. 661–662, May 2001.
[41] L. Zhang, L. F. Lester, A. G. Baca, R. J. Shul, P. C. Chang, C. G. Willison, U. K. Mishra, S. P. Denbaars, and J. C. Zolper, "Epitaxially-grown GaN junction field effect transistors," *IEEE Trans. Electron Devices*, vol. 47, pp. 507–511, Mar. 2000.
[42] A. Kuliev, C. Lee, W. Lu, E. Piner, S. R. Bahl, and I. Adesida, "A study of on-state and off-state breakdown voltages in GaN MESFETs," in *Proc. IEEE/Cornell Conf.*, 2000, pp. 110–114.
[43] G. Meneghesso, A. Chini, E. Zanoni, M. Manfredi, M. Pavesi, B. Boudart, and C. Gaquiere, "Diagnosis of trapping phenomena in GaN MESFETs," in *Proc. Int. Electron Device Meeting*, 2000, pp. 389–392.
[44] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, "Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy," *Appl. Phys. Lett.*, vol. 79, no. 21, pp. 3527–3529, Nov. 2001.
[45] M. E. Twigg, D. D. Koleske, A. E. Wickenden, R. L. Henry, and M. Fatemi, presented at the 42nd Electronic Materials Conf., Denver, CO, 2000.
[46] A. E. Wickenden, D. D. Koleske, R. L. Henry, R. J. Gorman, M. E. Twigg, M. Fatemi, J. A. Freitas, Jr., and W. J. Moore, "The influence of OMVPE growth pressure on morphology, compensation, and doping of GaN and related alloys," *J. Electron. Mater.*, vol. 29, no. 1, pp. 21–26, Jan. 2000.
[47] G. Parish, S. Keller, S. P. Denbaars, and U. K. Mishra, "SIMS investigations into the effect of growth conditions on residual impurity and silicon incorporation in GaN and $Al_xGa_{1-x}N$," *J. Electron. Mater.*, vol. 29, no. 1, pp. 15–20, Jan. 2000.
[48] T. Ogino and M. Aoki, "Mechanisms of yellow luminescence in GaN," *Jpn. J. Appl. Phys.*, vol. 19, no. 12, pp. 2395–2405, Dec. 1980.
[49] X. Dang, P. M. Asbeck, E. T. Yu, K. S. Boutros, and J. M. Redwing, "Long time-constant trap effects in nitride heterostructure field-effect transistors," in *Proc. Mater. Res. Soc. Symp.*, vol. 622, 2000, pp. T6.28.1–T6.28.6.
[50] E. M. Chumbes, J. A. Smart, T. Prunty, and J. R. Shealy, "Microwave performance of AlGaN/GaN metal insulator semiconductor field effect transistors," in *Proc. Int. Electron Device Meeting*, 2000, pp. 385–388.
[51] A. Tarakji, G. Simin, N. Ilinskaya, X. Hu, A. Kumar, A. Koudymov, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "Mechanism of radio-frequency current collapse in GaN-AlGaN field-effect transistors," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2169–2171, Apr. 2001.
[52] S. C. Binari, J. M. Redwing, G. Kelner, and W. Kruppa, "AlGaN/GaN HEMTs grown on SiC substrates," *Electron. Lett.*, vol. 33, no. 3, pp. 242–243, Jan. 1997.
[53] S. C. Binari, H. B. Dietrich, W. Kruppa, G. Kelner, N. S. Saks, A. Edwards, J. M. Redwing, A. E. Wickenden, and D. D. Koleske, "GaN-based electronic devices for high-power, high-speed, and high-temperature applications," in *Proc. Int. Conf. Nitride Semiconductors*, 1997, pp. 476–478.
[54] S. C. Binari, K. Ikossi-Anastasiou, W. Kruppa, H. B. Dietrich, G. Kelner, R. L. Henry, D. D. Koleske, and A. E. Wickenden, "Correlation of drain current pulsed response with microwave power output in AlGaN/GaN HEMTs," in *Proc. Mater. Res. Soc. Symp.*, vol. 572, 1999, pp. 541–545.
[55] S. Trassaert, B. Boudart, C. Gaquière, D. Théron, Y. Crosnier, F. Huet, and M. A. Poisson, "Trap effects studies in GaN MESFETs by pulsed measurements," *Electron. Lett.*, vol. 34, no. 16, pp. 1386–1388, Aug. 1999.
[56] T. E. Kazior *et al.*, presented at the Proc. Second Workshop GaN Electronics, 2001.
[57] Y.-F. Wu, B. P. Keller, S. Keller, J. J. Xu, B. J. Thibeault, S. P. Denbassrs, and U. K. Mishra, "GaN-based FETs for microwave power amplification," *IEICE Trans. Electron.*, vol. E82-C, pp. 1895–1905, 1999.
[58] B. M. Green, K. K. Chu, E. M. Chumbers, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, pp. 268–270, June 2000.
[59] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, and C. N. Nguyen, "Large signal frequency dispersion of AlGaN/GaN heterostructure field effect transistors," *Electron. Lett.*, vol. 35, no. 12, pp. 1022–1023, June 1999.
[60] I. Daumiller, D. Theron, C. Gaquiere, A. Vescan, R. Dietrich, A. Wieszt, H. Leier, R. Vetury, U. K. Mishra, I. P. Smorchkova, S. Keller, N. X. Nguyen, C. Nguyen, and E. Kohn, "Current instabilities in GaN-based devices," *IEEE Electron Device Lett.*, vol. 22, pp. 62–64, Feb. 2001.
[61] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, " The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, pp. 560–566, Mar. 2001.
[62] W. Kruppa, S. C. Binari, and K. Doverspike, "Low-frequency dispersion characteristics of GaN HFETs," *Electron. Lett.*, vol. 31, no. 22, pp. 1951–1952, Oct. 1995.
[63] G. A. Umana-Membreno, J. M. Dell, B. D. Nener, L. Faraone, G. Parish, Y.-F. Wu, and U. K. Mishra, "Low-temperature shallow-trap related output-admittance frequency dispersion in AlGaN/GaN MODFETs," in *Proc. Optoelectronic and Microelectronic Materials Devices*, 1999, pp. 252–255.
[64] D. M. Schaadt and E. T. Yu, "Frequency response of trap states in an AlGaN/GaN heterostructure field-effect transistor measured at the nanoscale by dC/dV spectroscopy," in *Proc. Mater. Res. Soc. Symp.*, vol. 680E, 2001, pp. E5.1.1–E5.1.6.
[65] *Nitride Electronics Workshop on Degradation Issues*, Wright-Patterson AFB, May 9, 2001.
[66] J. W. Palmour, S. T. Allen, S. T. Sheppard, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring, and C. H. Carter, Jr., "Progress in SiC and GaN microwave devices fabricated on semi-insulating 4H-SiC substrates," in *Proc. Device Research Conf.*, 1999, pp. 38–41.
[67] O. Noblanc, C. Arnodo, E. Chartier, and C. Brylinski, "Characterization of power MESFETs on 4H-SiC conductive and semi-insulating wafers," *Mater. Sci. Forum*, vol. 264–268, pp. 949–952, 1998.
[68] O. Noblanc, C. Arnodo, C. Dua, E. Chartier, and C. Brylinski, "Power density comparison between microwave power MESFETs processed on conductive and semi-insulating wafer," *Mater. Sci. Forum*, vol. 338–342, pp. 1247–1250, 2000.
[69] ——, "Progress in the use of 4H-SiC semi-insulating wafers for microwave power MESFETs," *Mater. Sci. Eng. B*, vol. 61–62, pp. 339–344, 1999.
[70] K. P. Hilton, M. J. Uren, D. G. Hayes, P. J. Wilding, H. K. Johnson, J. J. Guest, and B. H. Smith, "Surface-induced instabilities in 4H-SiC microwave MESFETs," *Mater. Sci. Forum*, vol. 338–342, pp. 1251–1254, 2000.

[71] K. P. Hilton, M. J. Uren, D. G. Hayes, P. J. Wilding, and B. H. Smith, "Suppression of instabilities in 4H-SiC microwave MESFETs," in *High Performance Electron Devices for Microwave and Optoelectronic Applications*. Piscataway, NJ: IEEE Press, 2000, pp. 67–70.
[72] D. Siriex, D. Barataud, R. Sommet, O. Noblanc, Z. Ouarch, and C. Brylinski, "Characterization and modeling of nonlinear trapping effects in power SiC MESFETs," in *Proc. IEEE MTT-S*, vol. 2, 2000, pp. 765–768.
[73] L. Forbes, E. Sun, R. Alders, and J. Moll, "Field-induced reemission of electrons trapped in SiO2," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 1816–1818, 1979.

Steven C. Binari received the B.S. degree in physics from the College of William and Mary, Williamsburg, VA, in 1979 and the Master of Engineering Physics degree from the University of Virginia, Charlottesville, in 1980.

In 1981, he joined the Naval Research Laboratory, Washington, DC. He has worked on a wide range of semiconductor materials and devices, focusing on GaN-based electronic devices for the last few years.

P. B. Klein received the Ph.D. degree in engineering and applied science from Yale University, New Haven, CT, in 1975.

After two years as a National Research Council Postdoctoral Associate tenured at the Naval Research Laboratory, Washington, DC, he became a Member of the Semiconductors Branch. His previous research interests include a range of optical investigations of defects and impurities in semiconductor materials and structures, with a particular emphasis on deep defect centers. His current research interests include investigating defects that lead to the degradation in performance of nitride-based microwave devices.

Thomas E. Kazior received the B.S.E.E. degree from Tufts University, Medford, MA, in 1978 and the Ph.D. degree in material science and engineering from the Massachusetts Institute of Technology, Cambridge, in 1982.

Upon completing his studies, he joined Raytheon's Research Division and is currently a Senior Principal Scientist and Leader of the Advanced Technology Development Team at Raytheon RF Components, Andover, MA. His current research interests include the development of next generation device and process technologies for microwave and millimeter wave applications, including GaAs- and InP-based HEMTs and HBTs, metamorphic device technology, GaN HEMTs, novel millimeter wave components, three-dimensional integrated circuits, and advanced packaging concepts.