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## **Thermal Simulation of Four Die-Attach Materials**

**by Gregory K. Ovrebo**

**ARL-MR-0686**

**January 2008**

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**REPORT DOCUMENTATION PAGE**

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<b>14. ABSTRACT</b> We performed a time-dependent simulation of thermal transfer in a circuit board, comparing the effects of using four different die-attach materials with high-power silicon carbide diodes. This simulation attempted to reproduce the results of a laboratory experiment in which thermal measurements were made of circuit boards under a time-varying load.					
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## **1. Introduction**

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Investigators in ARL's Power Components Branch have performed experiments which compare the thermal performance under load of four different die-attach materials used in high power circuit boards. Silicon carbide (SiC) diodes were subjected to time-varying loads and their maximum temperatures were observed with a thermal imaging camera. This report describes efforts to reproduce the results of those experiments in a thermal transfer simulation.

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## **2. Thermal Transfer Simulation Preparation**

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The simulation process begins by creating a solid model of the circuit boards used in the experiment, reproducing the dimensions and materials of parts used in the boards. The model was prepared with SolidWorks<sup>®</sup> modeling software, and is shown in figure 1. The circuit board substrate material is aluminum nitride, with direct bonded copper lands on the AlN. The silicon carbide diodes are shown in blue, and are attached to the direct bonded copper with the die-attach materials we are evaluating. The bottom of the circuit board is attached to a water-cooled coldplate which is maintained at a constant temperature of 17 °C.

Three of the four die-attach materials being evaluated are metallic, with good heat transfer characteristics as well as good electrical conductivity. The fourth die-attach material is an epoxy which, although having good electrical properties, has much lower thermal conductivity than the other materials. These materials will be described in more detail later in this section.

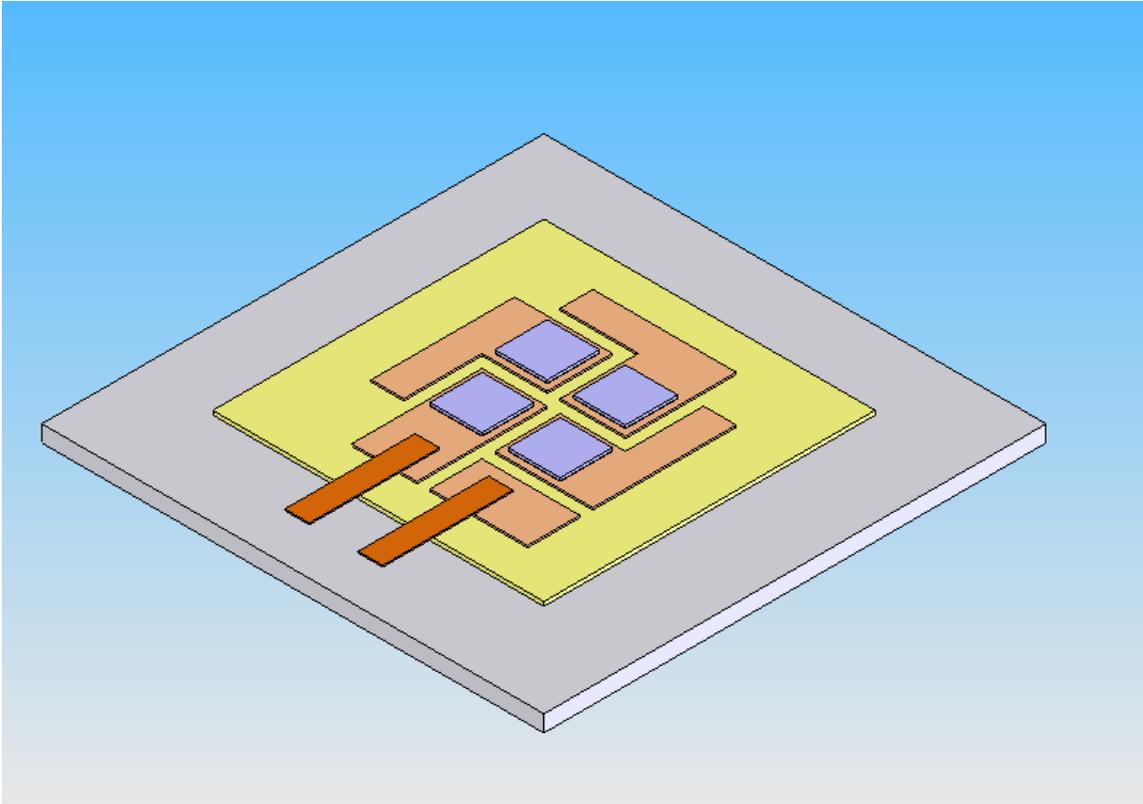


Figure 1. Model of the diode circuit board, produced in SolidWorks. The SiC diodes are shown in blue, on copper lands.

## 2.1 Laboratory Test Conditions

During the laboratory test, each diode had 20 A of current pass through it, with a 3.7 V drop across the diode, for a power dissipation of 74 W per diode and total power dissipation across the board of 296 W. Power was applied for five seconds, just long enough for the devices to reach temperature equilibrium. Power was then cut off for five seconds, during which time the device temperature returned to ambient. This cycle was repeated continuously for extended periods to observe any changes in diode performance due to changes in the die-attach layer. The time history of the power load is shown in figure 2. This history was used as a time-dependent heat input for each diode. It was assumed, for purposes of the simulation, that power dissipation was spread evenly throughout the diode's volume.

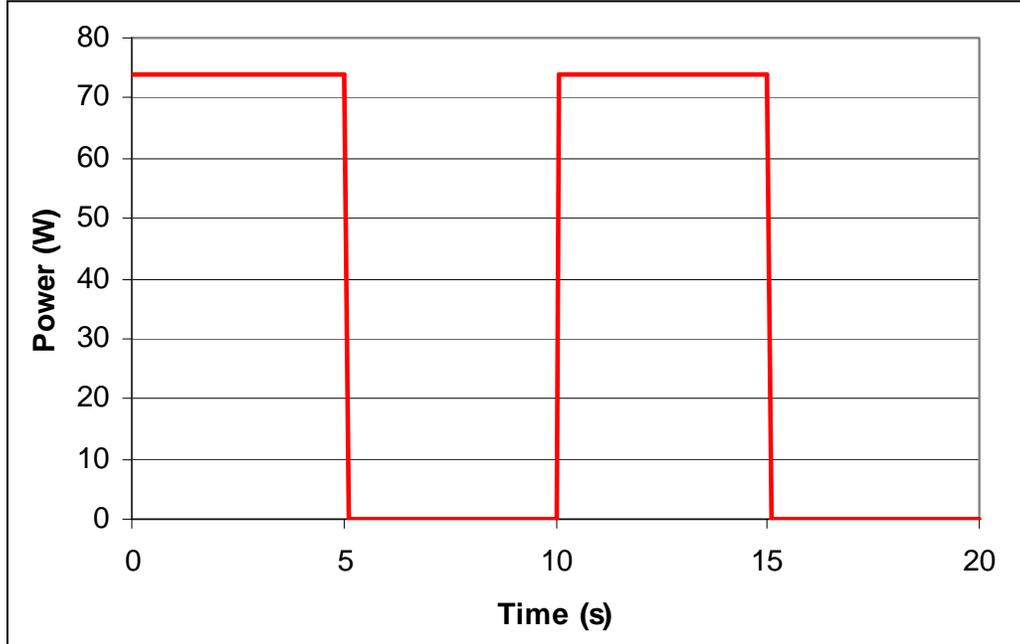


Figure 2. Time-varying power load applied to each SiC diode during thermal simulation.

A thermal imaging camera was used to measure temperatures on the exterior of the die and the circuit board during the heating cycle. After applying power for 5 seconds, the dies with metallic die-attach materials had a maximum measured temperature of approximately 90-110 °C. The dies with the epoxy attachment reached a maximum temperature of 140 °C. After power was cycled off, the temperature of the board returned to the temperature of the coldplate, 17 °C.

## 2.2. Die-Attach Materials

Of the four die-attach materials being investigated, three were metallic, with good thermal conductivity. These materials were a Au/Sn braze, in an 80%/20% mixture; a CPES nanoscale silver powder; and Kester R520A solder paste, an alloy which is 96.5% Sn, 3.0% Ag, and 0.5% Cu, commonly called SAC. The fourth die-attach material was Epo-Tek P-1011 single-element polyimide epoxy. Because the epoxy has much lower thermal conductivity than the metallic die-attach materials, using epoxy results in higher temperatures on the SiC diodes than using metallic die-attach materials. The physical properties of the materials required in the time-dependent thermal transfer calculation are listed in table 1. These properties are required to solve the heat diffusion equation,

$$\frac{\partial}{\partial x} \left( k \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( k \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( k \frac{\partial T}{\partial z} \right) + \dot{q} = \rho c_p \frac{\partial T}{\partial t},$$

where T is temperature, k is thermal conductivity,  $\rho$  is density, and  $c_p$  is specific heat.

Table 1. Physical properties of die-attach materials in thermal transfer simulation.

<b>Die-attach Material</b>	<b>Density (kg/m<sup>3</sup>)</b>	<b>Specific Heat (J/kg-K)</b>	<b>Thermal Conductivity (W/m-K)</b>
Au/Sn (80/20) braze	14510	150	57
Nanoscale silver	8580	233	200
SAC alloy solder paste	7400	220	57.26
Epo-Tek P1011 epoxy	3190	628	1.29

### 3. Simulation and Results

The time-dependent thermal simulation of the circuit board was performed with CosmosWorks, an analysis software package associated with SolidWorks. This finite element code breaks up the model into a mesh of nodes and elements, and solves the heat diffusion equation across the circuit board. After defining heat sources, boundary conditions, and material physical properties, we can calculate temperature distributions across our board as a function of time.

I began by defining the materials composing the circuit boards, along with their pertinent physical properties—thermal conductivity, specific heat, and density. The circuit boards were aluminum nitride, the lands on the circuit boards were copper, and the devices were silicon carbide. The die-attach properties have already been discussed. Each of the four SiC dies was designated as a volume heat source, each with the time dependent function shown in figure 2. The coldplate attached to the bottom of the board was modeled as a constant surface temperature of 17 °C on the bottom of the AlN circuit board.

The first attempt at simulation established a baseline result. Using the model described above, I obtained a maximum temperature of 37.3 °C to 38.3 °C on the SiC dies with metallic die-attach materials, and a maximum temperature of 90.3 °C on the die with the epoxy die-attach. The temperature spread among the die corresponds fairly well with the 30-50 °C spread observed in the lab, but the absolute temperatures are too low. Figure 3 shows a surface plot of calculated surface temperatures on the board after 5 seconds of heating, with all four die-attach materials used simultaneously.

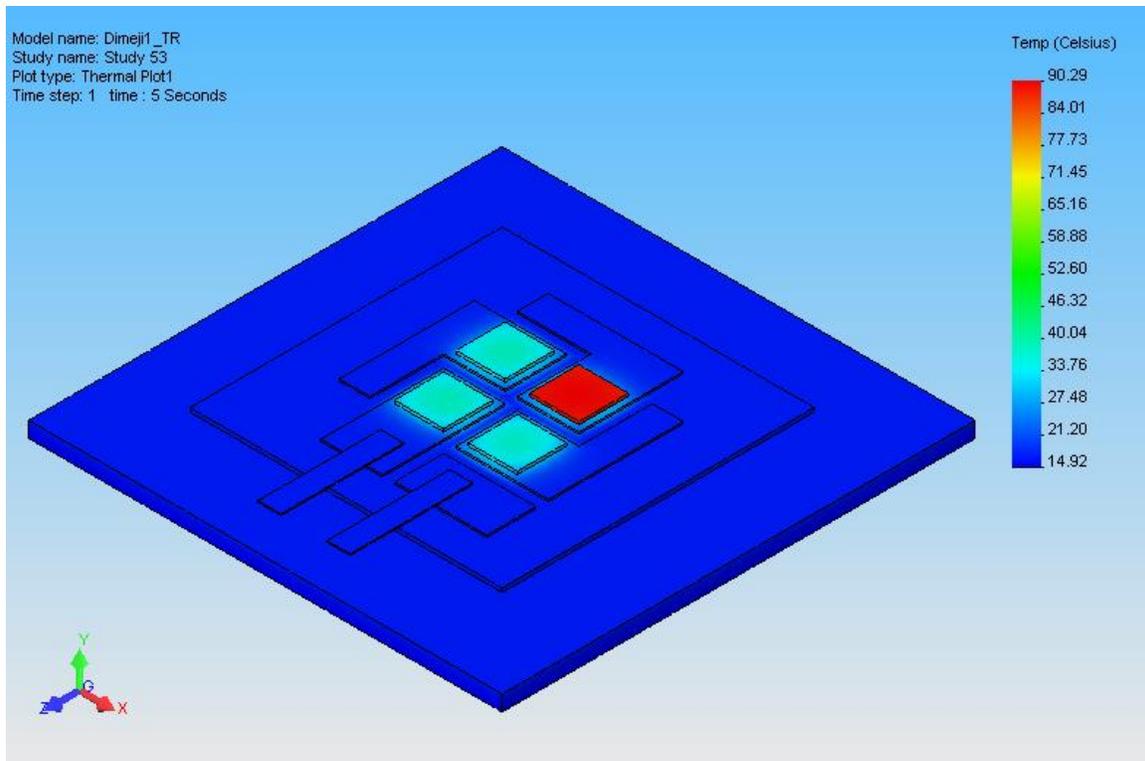


Figure 3. Simulation results using four die-attach materials simultaneously. Simulation assumes perfect contact between circuit board layers.

I next investigated several mechanisms which might account for the temperature difference between our simulation and the laboratory observations.

### 3.1 Modeling of Die-Attach Voids

I considered the effect voids might have on the thermal conductivity of the die-attach layers. Because the thermal conductivity of air is much lower than that of the die-attach materials, I approximated 50% voids in the die-attach layers by reducing the thermal conductivity of the material by 50%. To expedite the simulation process, I set up the models with all four die-attach materials simultaneously, one per die, rather than perform a separate simulation for each material.

Reducing thermal conductivities by 50% raised the maximum temperature on the P-1011 die to 139 °C, but raised the maximum temperature on the three metallic attach dies to only 35-40 °C. Reducing thermal conductivities of the SAC, nanosilver, and Au/Sn attaches to 25% of original values (and thus increasing voiding in the model to 75%) raised temperatures on the dies by another 5 °C. These temperatures are much lower than those observed in the lab; obtaining

calculated temperatures of 90-110 °C in dies with metallic attaches would require unrealistic levels of voiding.

### 3.2 Thermal Resistance Modeling

The next step in the simulation was to increase the temperatures, while maintaining the temperature spread among the die, by introducing thermal resistances between material layers in the model. This is more than mere expedience; the lower-than-expected temperatures calculated indicate that I have not accounted for all of the thermal resistance in the material stack and so overestimated the capacity of the system to carry away heat generated in the SiC die.

I considered the possibility of thermal resistance between the AlN circuit board and the copper lands. However, this particular board uses direct bonded copper (DBC), in which the aluminum nitride and copper are bonded at the molecular level. The bonding between these layers makes the notion of contact resistance unphysical, and I discarded this approach.

I next attempted to reproduce experimental results in this simulation by introducing thermal contact resistances between the die-attach layers and the copper lands, and between the die-attach layers and the SiC dies. After a trial-and-error process, I obtained the best results with a distributed thermal resistance of  $3 \times 10^{-5}$  K-m<sup>2</sup>/W at all 8 interfaces. However, the best I could manage was a temperature difference of about 70 °C between dies with epoxy die-attach and dies with metallic die-attach, greater than the 30-50 °C difference observed in the lab.

In the end, the modeling approach which produced the best simulation results involved adding a thermal resistance between the bottom of the circuit board and the coldplate. Up to this point, I had accounted for the coldplate in the simulation by fixing the temperature of the bottom of the circuit board at a constant 17 °C. For this phase of the simulation, I introduced an aluminum plate of arbitrary size to the bottom of the model stack, representing the water-cooled coldplate; for the thermal simulation, the top of the plate was set to a constant temperature of 17 °C.

Thermal resistances of varying values were added between the aluminum plate and the AlN board; no other thermal resistances were used elsewhere in the model. I again used all four die-attach materials in the initial simulations. With a total thermal resistance of 0.04 K/W in the model, CosmosWorks calculated a maximum temperature of 139.4 °C on the die with epoxy die-attach, and a maximum temperature of approximately 88 °C on the other dies. This result was promising, closer to the temperature spread seen in the lab than our other simulations.

The next step was to conduct the simulations with one die-attach material on all four dies. Figure 4 shows a plot of surface temperatures at  $t = 5$  seconds on a board using Au/Sn (80/20) braze; CosmosWorks calculated a maximum surface temperature of 90 °C. Simulations with nanoscale silver and SAC die-attaches yielded maximum temperatures of 88.7 °C and 90 °C, respectively. Plots of calculated surface temperatures for all of the metallic die-attach materials were very similar.

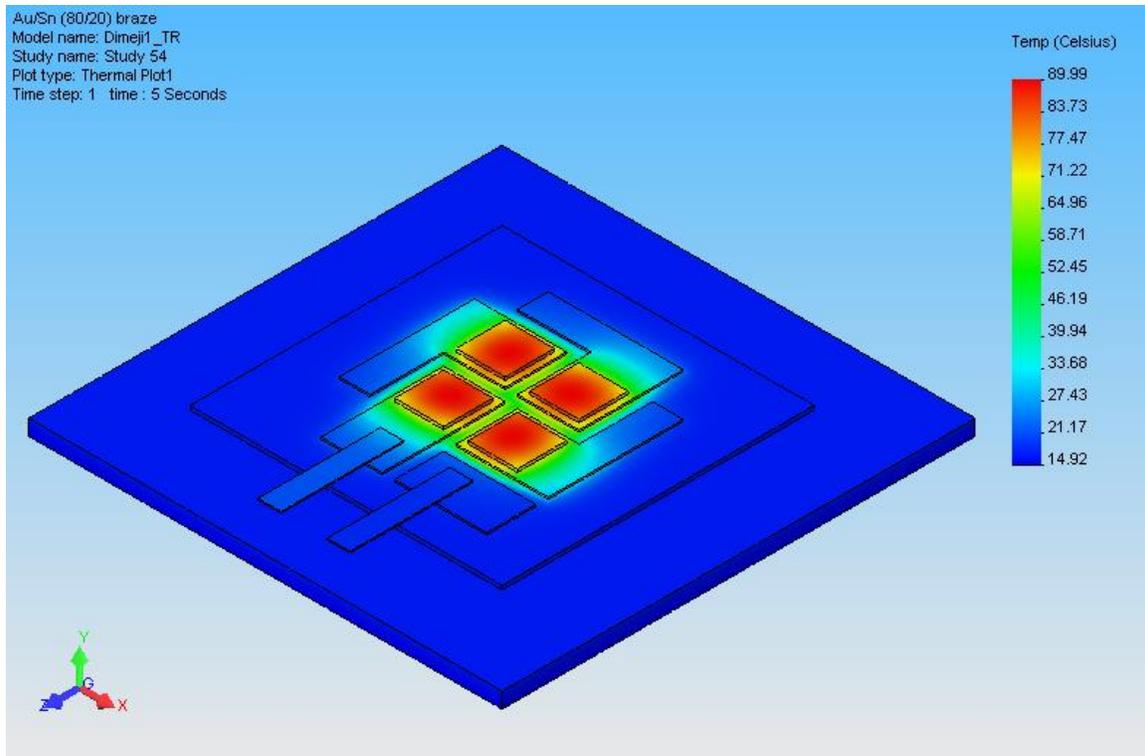


Figure 4. Simulation results with AuSn braze on all diodes at  $t = 5$  seconds.

Figure 5 shows the results of a CosmosWorks simulation with the Epo-Tek P1011 die-attach and the same  $0.04 \text{ K/W}$  thermal resistance between coldplate and circuit board as before, plotting surface temperature at  $t = 5$  seconds. Note that the maximum temperature on this board is almost exactly that of the board with all 4 die-attach materials. We infer that there is little heat spreading across the face of the circuit board. If significant heat spreading had occurred, each diode would have influenced its neighbors and increased the maximum temperatures on the diodes.

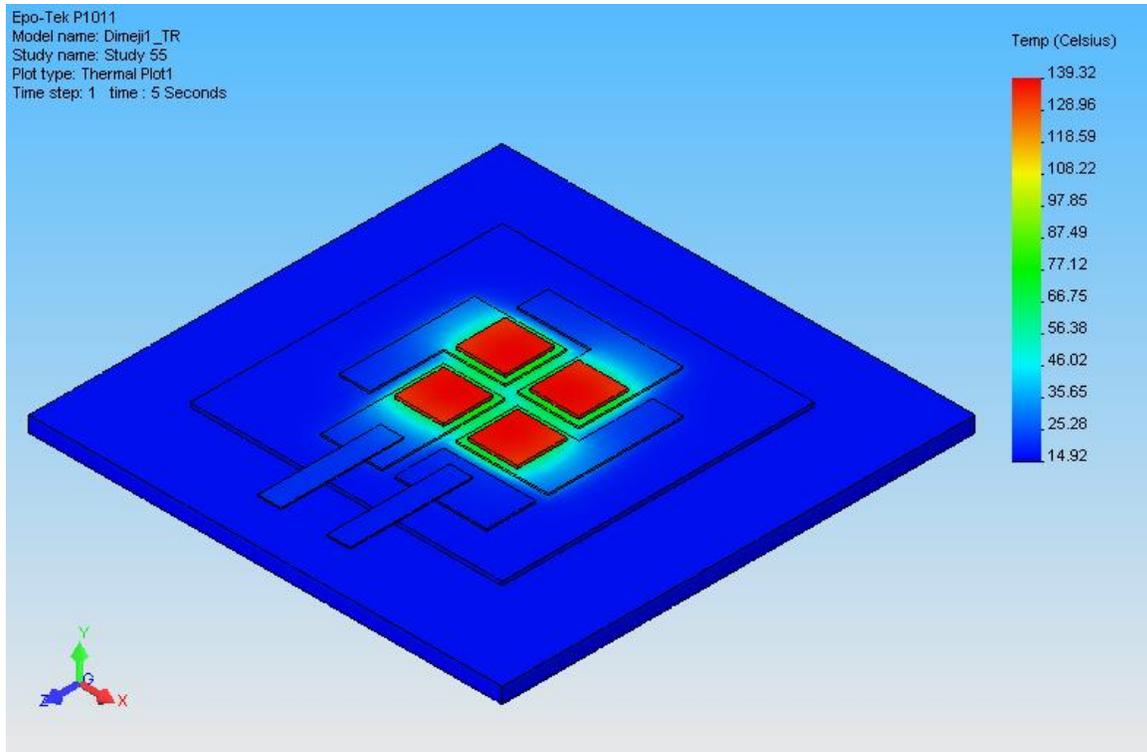


Figure 5. Simulation results with epoxy die-attach at  $t = 5$  seconds.

Figure 6 shows calculated surface temperatures on the diode board with P-1011 epoxy die-attach at  $t = 10$  seconds, when power has been off for 5 seconds and temperatures on the board have returned to near initial temperature.

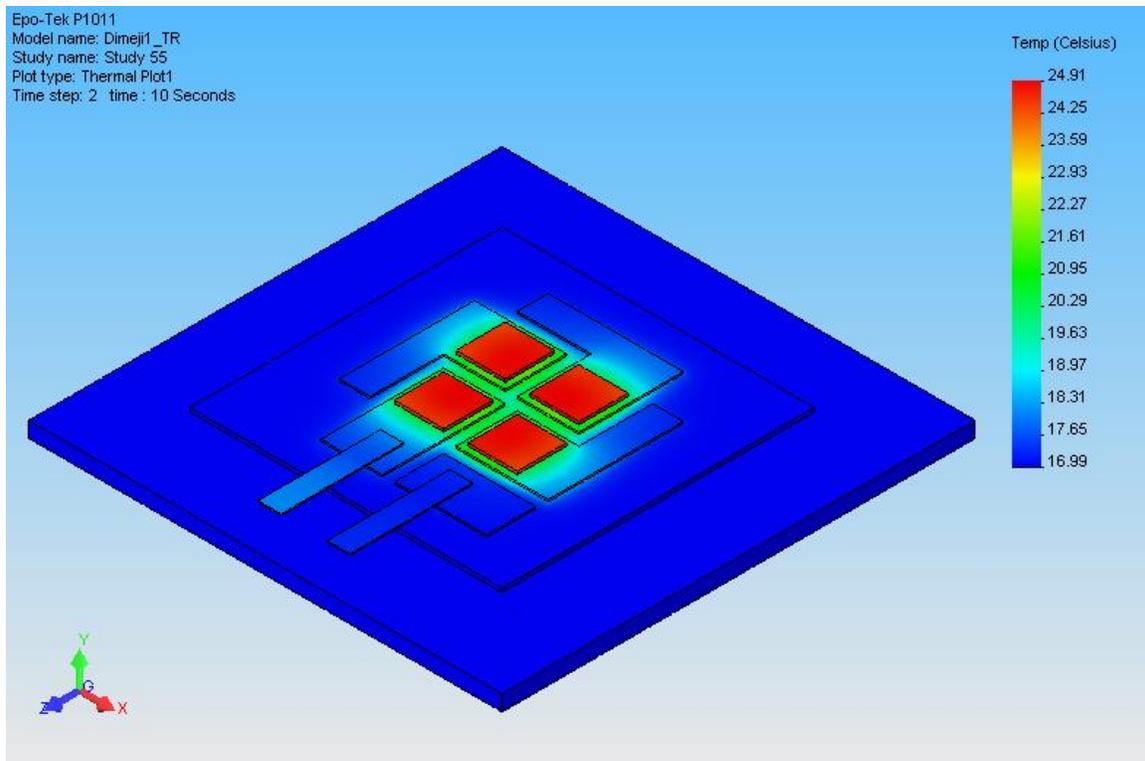


Figure 6. Simulation results with epoxy die-attach at  $t = 10$  seconds.

Finally, I performed a time dependent simulation with a fine time resolution. Previous simulations had recorded results at five second intervals:  $t = 0$  seconds,  $t = 5$  seconds,  $t = 10$  seconds, etc. In this simulation, CosmosWorks recorded temperatures at 0.1 second intervals over a 10-second period. All other simulation conditions remained unchanged from the earlier P-1011 epoxy simulation. Figure 7 is a graph of changes in maximum temperature on the surface of the diode board, using the diode power function shown in figure 2. Although the resulting peak temperature is slightly higher in this simulation than in the previous case, the result agrees qualitatively with the observation in the lab, where temperatures rose to a stable maximum about a second after power was applied, and then dropped quickly to the coldplate temperature after power was cut off.

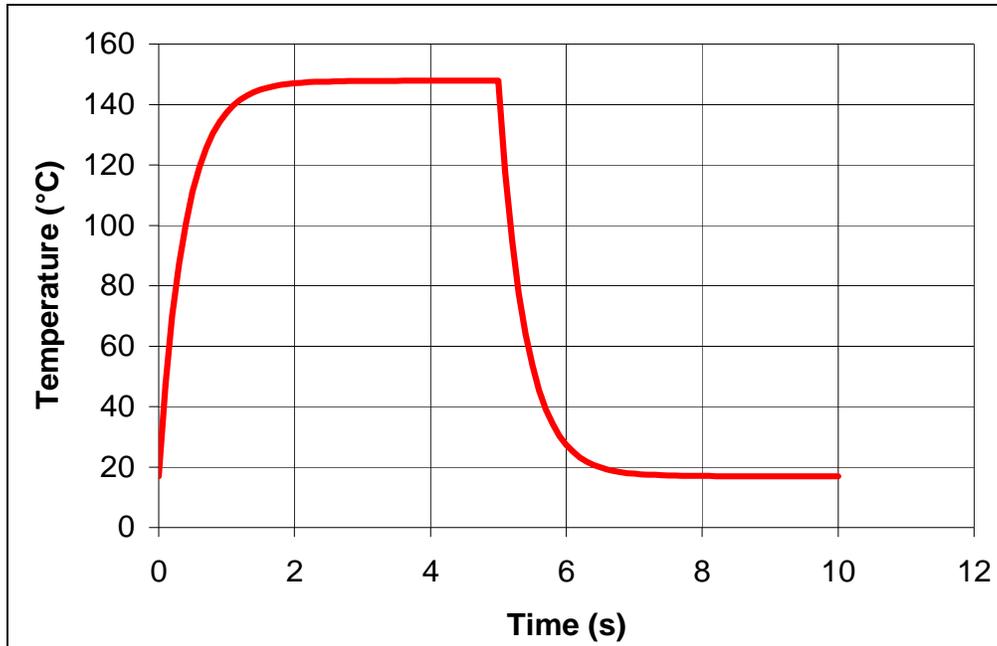


Figure 7. Maximum calculated diode temperature, through one cycle of heating and cooling.

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## 4. Conclusions

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Although I was able to reproduce the maximum temperature readings observed in experiments on circuit boards populated with SiC diodes, getting temperature predictions is not the only goal. The results of this simulation may change somewhat depending on the fineness of the mesh in the finite element analysis, how often we record results during the time-dependent calculations, and other details of the simulation unrelated to the circuit boards, their constituent materials, and the power loading of the devices. Instead, these results may be viewed as a baseline for analyses to come, where the geometry of the board might change, the materials in that board, or the power dissipated in the devices, and I want to know the magnitude of the possible changes in the thermal performance of the system. With that information, I can evaluate proposed design modifications and calculate the effect of new system requirements before the hardware is built, and have some confidence in what will be discovered when that hardware is tested.

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