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TECHNOLOGY FOR AIR AND
SPACE-SCIENTIFIC RESEARCH
PROGRAM**

**Delivery Order 0003: Electrical Technology
Component Development**



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ABSTRACT

AlNi and Ni₂Si based ohmic contacts to p-type 4H-SiC have been produced using low energy ion implantation, a Ti contact layer, and sequential anneals. Low resistivities were promoted by degenerately ($>10^{20}$ cm⁻³) doping the surface region of 4H-SiC epilayers via low energy Al⁺ implantation. High acceptor activation and improved surface morphology was achieved by capping the samples with pyrolyzed photoresist prior to a two-step anneal sequence in argon. Ti/AlNi/W and Ti/Ni₂Si/W stacks of varying Ti and/or binary layer thickness were compared at different anneal temperatures. For this set of AlNi based samples, specific contact resistivities as low as 5.5×10^{-5} ohm-cm² were reliably and repeatedly achieved after annealing at temperatures of 700-1000°C for 2 minutes in a high purity argon atmosphere. For the Ni₂Si samples, resistivities as low as 4.5×10^{-4} ohm-cm² were reached after annealing between 750 and 1100°C. Similarly, a set of Ti/AlNi/Au samples, with or without Ge as an additional contact layer, were prepared via the same procedure as those above. In this case specific contact resistivities as low as 5.0×10^{-4} ohm-cm² were achieved after annealing the Ti/AlNi/Au samples between 600 and 700°C for 30 minutes in a dynamic argon atmosphere or under high vacuum. Additional sets of Ti/AlNi/Au or W samples were later produced in order to confirm previous results and to demonstrate the effects of thermal aging. In all cases, the lowest resistivities were realized using thicker (~ 40 nm) Ti layers. I-V analysis revealed superior linear characteristics for the AlNi system, which also exhibited a more stable microstructure after anneal. AFM analysis demonstrated the superiority of photoresist capping over alternatives in minimizing surface roughness. SEM and optical microscopy illustrated microstructure evolution with temperature. SIMS and RBS were used to analyze the stability of the stacks subsequent to thermal treatment. Linear ohmic behavior after significantly reduced anneal temperature is the main observation of the present study. Also, 2D and 3D thermal and mechanical models of multilayer electronic packages have been developed using finite element analysis. The temperature and stress distributions from this work generally agree with theoretical predictions.

TABLE OF CONTENTS

SECTION	TITLE	PAGE
	LIST OF FIGURES.....	iv
	LIST OF TABLES	vi
	FOREWORD	vii
	PREFACE	viii
1	SUMMARY	1
2	INTRODUCTION.....	2
3	EXPERIMENTAL PROCEDURES	5
4	RESULTS AND DISCUSSION	11
5	CONCLUSION	29
6	RECOMMENDATIONS	31
7	REFERENCES.....	32
	APPENDIX A: Facility Capabilities for Power Semiconductor lab and Advanced Capacitor Research & Development Center	A-1
	APPENDIX B: Conferences and Abstracts for Submitted Papers	B-1

LIST OF FIGURES

FIGURE	TITLE	PAGE
1	Code profile using multiple energy level ion implantation	6
2	Ohmic contact measurement with the mesa structure	7
3	Ohmic contact measurement without the mesa structure.	8
4	AFM image of sample with (a)photoresist cap, (b)no cap, (c)SiC cap, (d)graphite cap.....	12
5	AES data verifying the desired stoichiometry of the AlNi intermetallic.....	13
6	RBS results of an as-deposited contact of Ti/AlNi/W.....	14
7	RBS data of post-annealed Ti/AlNi/W.....	14
8	Comparison of post 925°C anneal SEM image of W contact surfaces (a) before and (b) after thickness optimization and anneal purge gas purification.	15
9	The effect of anneal temperatures on the Ti/AlNi/W contact I-V curves	16
10	The effect of anneal temperatures on the specific contact resistivity of Ti/AlNi/W.....	17
11	Effect of the thickness of titanium on the specific contact resistivity of Ti/AlNi/W.....	17
12	The effect of anneal temperatures on the specific contact resistivity of Ti/AlNi/Au for samples annealed under vacuum or in an Ar atmosphere...	19
13	Comparison of post anneal (a) AFM image of Ti/AlNi/W (b) AFM image of Ti/AlNi/Au.....	20
14	Comparison of post anneal (a) (5kx) SEM image of Ti/AlNi/W (b) (5kx) SEM image of Ti/AlNi/Au.....	20
15	X-ray diffraction spectra of the control SiC/Ti/AlNi/Au sample	21
16	X-ray diffraction spectra of the post-anneal SiC/Ti/AlNi/Au sample	22
17	RBS results (a) of control SiC/Ti/AlNi/Au sample (b) after annealing at 650°C for 30 minutes.....	22

18	Typical I-V curves of Ti-AlNi-Au or W samples annealed at 650 C	23
19	The effect of anneal temperatures on the specific contact resistivity	23
20	The thermal aging effect on the specific contact resistivity of Ti/AlNi/Au	24
21	The full view 3D model of the IGBT	25
22	2D temperature distribution of the SiC stacking configuration	25
23	2D stress distribution of the SiC stacking configuration	26
24	3D temperature distribution of the SiC stacking configuration	26
25	The effect of the heat generation on the temperature distribution of the 3D thermal model	27
26	The effect of the heat generation on the stress distribution of the 3D mechanical model	28

LIST OF TABLES

TABLE	TITLE	PAGE
1	Calculated ion implantation conditions	6
2	Package model material properties	10
3	Al+ implantation effects on contact resistivity ($\Omega\text{-cm}^2$) when using SiC or graphite proximity caps during activation anneal.....	11

FOREWORD

The work documented in this report was performed by the University of Dayton Research Institute (UDRI) between March 2004 and December 2006 for the Propulsion Directorate of the Air Force Research Laboratory, Wright-Patterson Air Force Base, Ohio. The effort was performed as Delivery Order 0003 on Contract No. FA8650-04-D-2403, Power and Thermal Technologies for Air and Space -- Scientific Research Program.

Technical support and direction for this delivery order was provided by Dr. James Scofield. Dr. Bang-Hung Tsao was the delivery order Principal Investigator. He was assisted by Mr. Victor McNier and Mr. Jacob Lawson. Mr. McNier is the author of the appendix of this report and is responsible for the operation, maintenance, and improvements to the listed equipment.

The author also wishes to acknowledge the assistance of Ms. Sheila Liskany and Mr. Jeffrey Fox of UDRI, who provided the administrative support. Mr. Fox is the SRP Program Manager.

PREFACE

The objective of this program is to provide responsive support to assist the Propulsion Directorate, Power Division in meeting the goals of its in-house research and development program of advanced components for energy storage, power management, and control at the Air Force Research Laboratory (AFRL), Wright-Patterson Air Force Base, Ohio.

Air Force (AF) missions require electronic devices and circuits that are capable of operating in extreme temperatures both in air and space environments. Devices, which are fundamental to the establishment of advanced electronics technology, such as capacitors, resistors, and switches are needed in circuits that are capable of operating in temperatures between -50 to 250°C.

1. SUMMARY

Improved AlNi-based ohmic contacts to p-type 4H-SiC have been achieved using low energy ion (Al^+) implantation, the addition of a thin Ti layer, and a novel two-step implant activation anneal process. Resistivities of $5 \times 10^{-5} \text{ ohm-cm}^2$ were reached by doping the surface region of 4H-SiC epilayers via low energy Al^+ implantation. Acceptor activation was achieved by annealing the samples with a $1400+1700^\circ\text{C}$ two-step sequence in an Ar atmosphere, which also yielded improved surface morphology when implanted samples were capped with photo resist during the anneals. AFM average roughness values improved by over 5X compared to samples without capping. The metallurgical morphology and contact resistivity remained intact even after annealing at 1100°C , indicating good thermal stability. The Ti/AlNi/W contacts on implanted layers were compared to Ni_2Si intermetallics and were found to be comparable to or superior in terms of specific contact resistivity, uniformity, and thermal stability. Ni_2Si contacts exhibited significant potential for further work. Ti/AlNi/Au contacts were also studied which resulted in contact resistivities in the $5 \times 10^{-4} \text{ ohm-cm}^2$ range. Even though these values are an order of magnitude higher than those of the Ti/AlNi/W system, the reduced anneal temperature (650°C) implies that Ti/AlNi/Au is a promising stacking configuration. Furthermore, the metallurgical morphology and contact resistivity of the Ti/AlNi/Au contacts remained intact even after thermal aging up to 350°C and back down to room temperature. The benefits of using Ge to reduce the anneal temperature necessary for ohmic behaviors of the Ti/AlNi/Au stacks was not observed in this investigation. On the other hand, benefits of a longer 30 minute anneal time at $600 - 700^\circ\text{C}$, in either vacuum or atmospheric pressure Ar ambients, was observed. Further investigations are underway to identify the acting metallurgical mechanism(s) and the compounds formed under these conditions. Research was later redirected toward packaging and the development of 2D and 3D thermal and mechanical models of multilayer electronic packages using finite element analysis. The temperature and stress distributions from this work generally agree with theoretical predictions.

2. INTRODUCTION

Discrete devices are continuing to grow at a double-digit rate; the industry shipped 715 billion discrete surface mount technology (SMT) capacitors and resistors in 1998. Yet it is estimated that 160 billion discrete devices have been replaced with some form of integrated passive device from 1998 to 2000. In addition, the wide acceptance of chip scale packages (CSPs) will increase the use of integrated passive devices (IPD). These small array packages could cost-effectively contain networks of integrated passives. The use of integral passives is expected to be cost driven, although there are performance and reliability advantages as well. The cost advantage will be at the product or system level through savings in conversion cost, board size, weight, and finished product size. These benefits are predicted to impact both the commercial and military markets. The military market, however, is quite different from the commercial sector due to the restriction of the requirements and specifications. For the commercial applications, the voltage requirement is usually in the range of 5 to 10 volts; the military applications usually require a few hundred volts. The temperature requirement for commercial applications is room temperature. An operating temperature ranging from -50 to 250°C is a specification for military applications. Understanding the difference in commercial and military market specifications and providing for the technological needs of the AF are the driving forces for this research.

Research efforts are focused on investigating materials and fabrication techniques for high-performance capacitors and components for energy storage, power management, and controls capable of operating in extreme environments in air and space. Some devices that are fundamental to the establishment of advanced electronics technology include: (a) capacitors, (b) resistors, and (c) switches. As mentioned, these capacitors, resistors, transistors, and other components needed to build circuits have to be capable of operating at temperatures between -50°C to 250°C. Hence, the development of materials for fabricating active and passive components is a definite future need for the Air Force.

New technologies based on wide-bandgap semiconductors are required to overcome the limitations of conventional Si power devices and achieve semiconductor devices operating above 300°C. Implementation of a semiconductor production technology based on a new material is challenging, however, since complete production infrastructure and device technologies are

required. Elements of a viable semiconductor technology include the availability of high quality bulk materials for device substrates, controlled doping methods, stable electrical contacts, appropriate activation and passivation procedures, methods for incorporating high quality insulating layers, device design, processing methods with an emphasis on plasmas, associated software tools, and the requisite materials properties data. In addition to improved semiconductor devices, advanced power electronic building blocks require insulators and passive devices such as capacitors. Thermal stress and dielectric breakdown limit the performance, lifetime, and reliability of many power system components. Furthermore, some potential materials solutions are cost prohibitive. Thus, research directed towards the development of improved dielectric and insulating materials will provide significantly enhanced performance and cost savings for Air Force systems. The specific needs are for affordable materials that maintain their properties in adverse environments.

Semiconductor integrated circuits (ICs) and devices made from conventional Si often cannot function in high temperature, high power density, or adverse operating environment applications without sophisticated heat sinking and packaging which adds to the cost of the device and unwanted weight. New wide-bandgap semiconductor materials such as SiC, and III-V's such as GaN, are becoming increasingly important in the development of next generation electronic devices for adverse environments. Based on its material and electronic properties and its relative maturity comparable to that of GaAs 20 years ago, SiC is the primary candidate for these applications. For example, high frequency and high power devices are being fabricated, and the first blue light emitting diode (LED) was fabricated from SiC. The high breakdown voltage and high thermal conductivity of SiC can lead to the fabrication of devices with enhanced performance, but the unanswered question is whether or not the performance benefits of SiC devices can be obtained at a cost that will allow them to compete against Si and GaAs devices.

Continued improvements in crystal growth and device fabrication processes are needed before SiC-based devices and circuits can be scaled-up and incorporated into electronic systems. However, recent achievements include the realization of SiC integrated circuit operational amplifiers and digital logic circuits, as well as significant improvements to epitaxial and bulk crystal growth processes that impact the viability of this rapidly emerging technology. SiC-based semiconductor electronic devices and circuits are presently being developed for use in

high-temperature, high-power, and/or high-radiation conditions under which conventional semiconductors cannot adequately perform. The ability of SiC to function under such extreme conditions is expected to enable significant improvements to a far ranging variety of applications and systems. These range from greatly improved high-voltage switching in electric power distribution and electric vehicles to more powerful microwave electronics for radar and communications to sensors and controls for cleaner-burning and more fuel-efficient jet aircraft and automobile engines. In the area of power devices, SiC power MOSFET's and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, yet have die sizes nearly 20 times smaller than correspondingly rated Si-based devices. SiC's exceptionally high breakdown field (>5 times that of Si), wide-bandgap energy (>2 times that of Si), carrier saturation velocity (>2 times that of Si), high thermal conductivity (>3 times that of Si), chemical inertness, and low dopant diffusivity, lead to substantial performance gains in many device applications, in spite of its low carrier mobility disadvantages [1]. The combination of these properties shows promise for applications in high power semiconductor devices, in high frequency electronic devices, in devices to be used in high temperature (400 to 700°C), and/or in chemically harsh and high radiation flux environments. The extreme thermal and electronic properties of SiC, diamond, and the direct bandgap of GaN provide combinations of properties that lead to the highest figures of merit for selecting semiconductor materials for high power, high speed, high temperature, and high frequency applications.

3. EXPERIMENTAL PROCEDURES

Sample Preparation

8° off-axis <0001> 4H SiC wafers with a $N_a=1 \times 10^{17} \text{ cm}^{-3}$, 3- μm -thick epilayer, were purchased from CREE, Inc. Samples were cleaned using the following steps:

Step (1) organic solvents degrease:

- (a) TCE (5 min @ 50°C)
- (b) Acetone (5 min @ 50°C)
- (c) Methanol (5 min @ 50°C)
- (d) Propanol (5 min @ 50°C)
- (e) DI water rinse and Nitrogen dry

Step (2) acid etch

- (a) $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ (1:1, 5 min @ 50°C)
- (b) DI water rinse
- (c) $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ (1:1, 5 min @ 50°C)
- (d) DI water rinse
- (e) HF (2 min @ room temperature)
- (f) DI water rinse and Nitrogen dry

Ion Implantation

Degenerate doping of a thin surface region contact layer was accomplished using multiple energy/dose (80, 45, 24 keV / $5\text{E}15$, $2\text{E}15$, $1.2\text{E}15 \text{ cm}^{-2}$, respectively) Al^+ implantation at 650°C. SIMS analysis of the $\sim 0.3 \mu\text{m}$ implanted layer was accomplished to verify the profile and desired atomic concentration of $>10^{20} \text{ cm}^{-3}$. The simulated code profile using multiple energy/dose levels is shown in Figure 1.

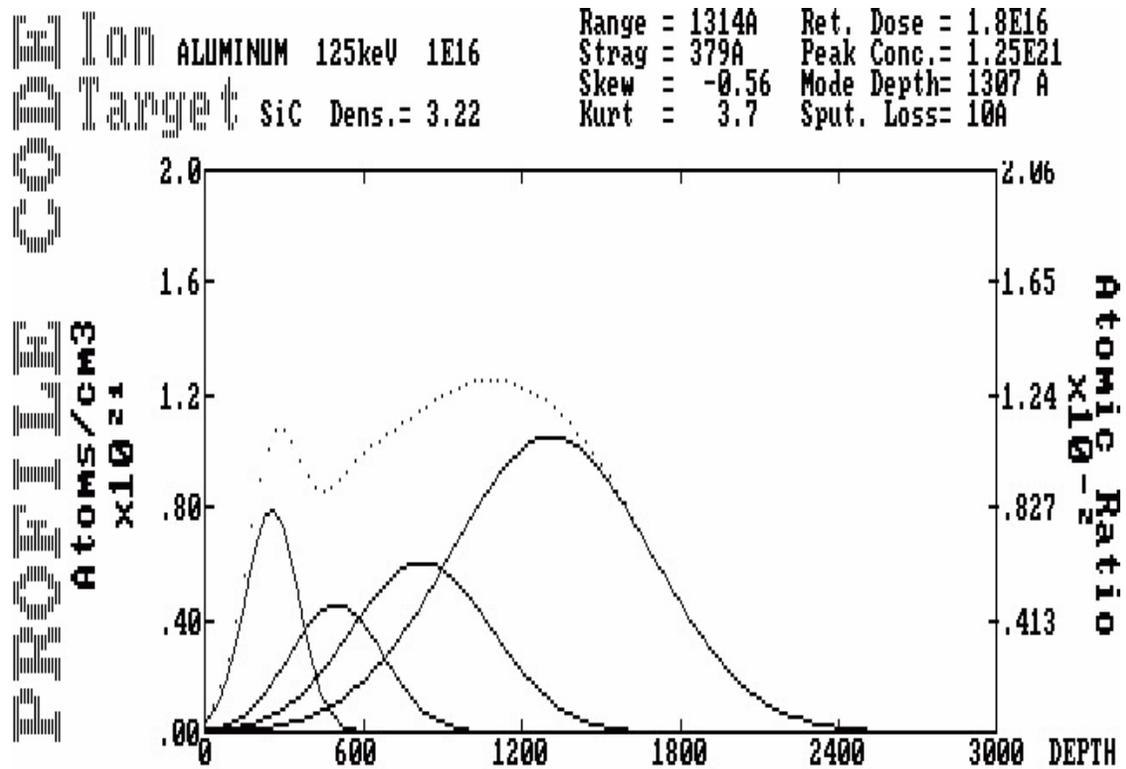


Figure 1: Code profile using multiple energy level ion implantation.

The ion implantation conditions calculated by using the profile code were performed using Al⁺ at 500°C with the parameters in the following table:

Table 1

Wafer	Energy (keV) (Two levels)	Dose (For both energies)	Peak concentration	Range (μ)
CB0454-01	10 + 20	3.8 E13/cm ²	4.09E19	215
CB0454-02	10 + 20	1E14/ cm ²	1.08E20	215
XU0960-03	10 + 20	4E14/ cm ²	4.3E20	215
BN0506-04	10 + 20	1E15/ cm ²	1.07E21	215

Table 1: Calculated ion implantation conditions.

Implantation was followed by a two-step activation anneal at 1400°C and 1700°C for 15 minutes at each temperature. During the anneal process, the implanted surfaces were proximity capped with 1813 photo resist to protect the surface.

Photolithography

TLM patterns on the mesa structures were prepared by the same cleaning procedures describe above. Positive resist photolithography and subsequent metal etching were employed to define the mesa and contact metal patterns. The improved undercut of two layers of the photo resistor was used for the lithography and lift off process. The latest process uses LOR5a and 1805 photo resistor. The recipe is shown as the following:

Spin LOR 5a @ 4000 rpm for 30 seconds

Bake at 150°C for 2 minutes

Spin 1805 photo resistor @ 4000 rpm for 30 seconds

Bake at 120°C for 5 minutes

Exposure @ 4.5 seconds

Develop using CD-26 for 75 seconds

Aluminum deposition

Lift off using two baths of 1165 micro-deposit remover at 80°C.

The patterns of the structure are shown in Figures 2 and 3. Prior to loading into the high vacuum chamber for TLM metal deposition, the samples were oxygen plasma cleaned, dipped into a HF: H₂O (1: 9) solution for 60 seconds and dried with N₂ gas.

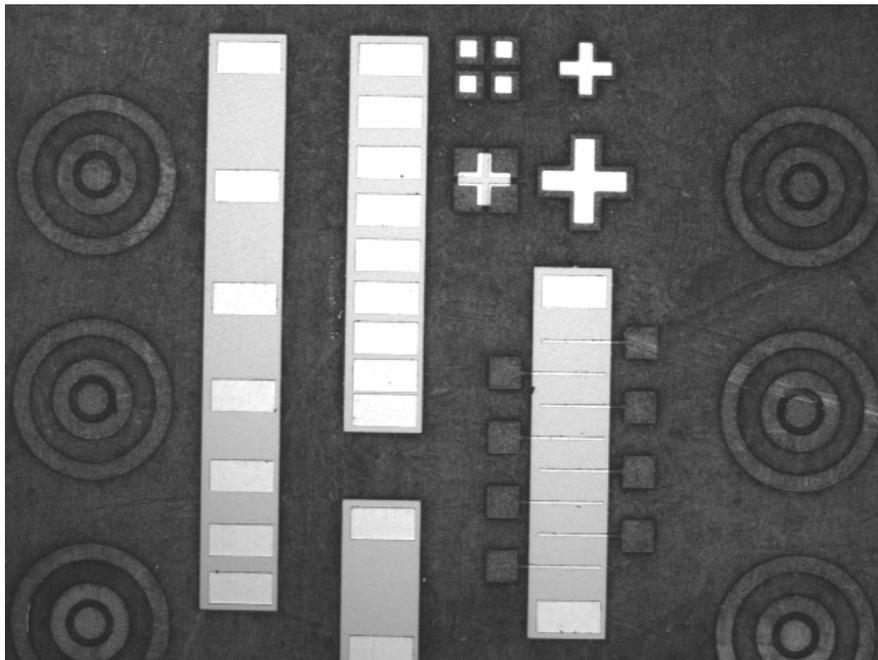


Figure 2: Ohmic contact measurement with the mesa structure.

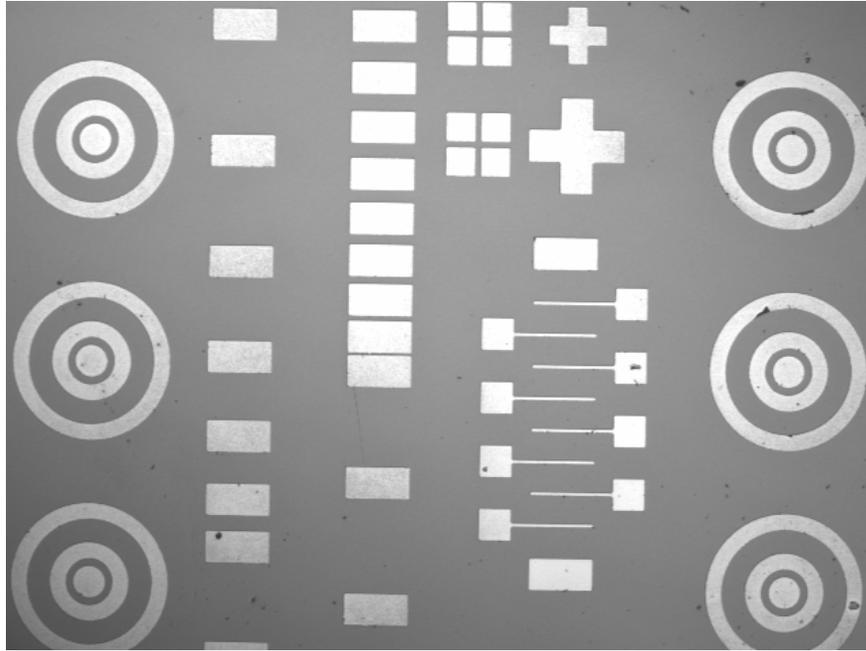


Figure 3: Ohmic contact measurement without the mesa structure.

Metallization, Annealing, and Testing Procedures

The metal stacks were prepared by rf sputtering deposition resulting in the following composite metallizations: 10, 20, 30, or 40 nm Ti as the first layer, followed by either 100 or 200 nm AlNi or 100 or 200 nm Ni₂Si as the second, and a third layer consisting of 100 nm W. Post deposition annealing was carried out in the temperature range of 700°C to 1100°C for 2 minutes in a high purity Ar atmosphere with an upstream gas purification system. An additional sample set was then prepared with or without 24 nm Ge as a first layer, with 32 nm Ti as the next, followed by 144 nm of AlNi and 100 nm Au. These samples were annealed between 600 and 700°C for 30 minutes in argon or under high vacuum. Current-voltage (I-V) measurements on all TLM patterns were performed at room temperature between heating cycles. Additional sets of Ti/AlNi/Au or W samples were later produced in order to confirm previous results and to demonstrate the effects of thermal aging. After annealing at their respective optimum anneal temperature, these later samples were heated on hot plate in 50 degree increments from room temperature to 350°C and back down to room temperature; I-V measurements were performed at each temperature level.

Wire Bonding and Potting Gel Optimization

Some effort was directed toward examining die attachment to various packages including multiple wire bonds. Commercial silicon diodes were attached to modified packages via high temperature brazes. Several wire bonds were made from the dies to the packages in order to study bond stability with different potting gel mixtures. All gel combinations were carefully mixed and then out gassed in a desiccator with a small mechanical pump. Once applied, gels were cured on a hot plate as per the manufacturer's recommend time and temperature. At first, two part silicon encapsulating gel 8100, available from NuSil Technology, was explored. This gel is stable from -65 to 200 C, but only has a viscosity of 500 Cps. Various ratios of the two parts were explored in order to enhance the properties, but a gel with the proper consistency and flow characteristics was never achieved. As a result NuSil 8155 was ordered which has the same operating temperature range as the 8100, but much higher viscosity of 15000 Cps. At a 1:1 ratio, 8155 yielded somewhat desirable results.

Modeling Parameters

Multilayer electronic packaging configurations were simulated using finite element analysis (FEA). That is, ANSYS was used to model the thermal and mechanical behaviors of generic electronic package geometries comprised of multiple materials. The representative geometry of a Si isolated gated bipolar transistor (IGBT) was chosen for the initial simulation. The chosen parameters were the thickness, the materials layout, and heat generation. The layer configurations were SiC/AuGe/Au/Ni/Cu/AlN/Cu as seen in the following table:

Table 2

1. SiC	E (e3 MPa) =(420) 430-466	Pr=0.16-0.17	Alpx (e-6 m/m/K) =2.2-3.7	Thermal Conductivity e6 pW/(mm)(K) = 63-94	Source: (www.matweb.com , silicon Carbide,CVD)
2. AuGe Eutectic	72.739	0.42	20C, 14.4, 250C, 14.6, 500C,15.2, 1000C,16.7	440	www.indium.com , www.matweb.com , gold, Au
3. Au	77.2	0.42	20C, 14.4, 250C, 14.6, 500C,15.2, 1000C,16.7	301	www.matweb.com , gold, Au
4. Ni	207	0.31	20C, 13.1	60.7	www.matweb.com , nickel, Ni; annealed
5. Cu	110	0.343	20C, 16.4, 250C, 18.5, 500C, 20.2 1000C,24.8	385	www.matweb.com , Copper, Cu, Annealed
6. AlN	320-350	0.25	3.5-5.7	170-250	AN 180 Aluminum Nitride Ceramic Substrate, 99% Purity
7. Cu	See #5				

Table 2: Package model material properties.

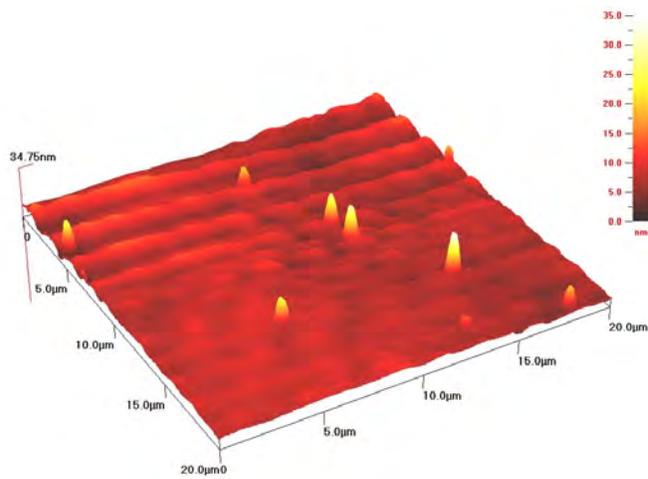
4. RESULTS AND DISCUSSION

Using low energy ion (Al^+) implantation and the two-step $1400^\circ\text{C} + 1700^\circ\text{C}$ implant activation anneal process, resistivities were consistently achieved in the mid- $10^{-5} \Omega\text{-cm}^2$ range. This improvement is attributed in part to the addition of a thin Ti layer to improve adhesion and mitigate Al spiking into the SiC [3]. Additionally, improved surface morphology and uniform implant activation of low-energy Al^+ implanted contact layers has been a crucial component of the improvements realized during this effort. Namely, implicit in the presented data is that consistently low contact resistivities were accomplished only after efforts to minimize implanted and annealed SiC surface roughness were successfully realized. Routine processing, involving the use of SiC proximity capping during activation anneals, was found to be only marginally successful at curtailing excessive step bunching and surface roughness. An alternative graphite wafer proximity cap was used on several wafers with improved results. Capping with pyrolyzed photoresist, however, was found to be a significantly superior, likely owing to the more intimate contact with the SiC surface compared to the graphite wafer proximity cap. Table 3 shows the effect of Al^+ implantation effects on contact resistivity ($\Omega\text{-cm}^2$) when using SiC or graphite proximity caps during activation anneal. Fig. 4 shows post-activation anneal AFM scan data for samples which differed only in their surface cap. The SiC capped AFM representation shows excessive step bunching, with its concomitant average roughness value of over 5.39 nm. By comparison, the sample which resulted from the polished graphite-disk cap possesses a relatively smooth, slowly undulated surface which had a measured average roughness value of only 3.06 nm. As can be seen in the figure, the average surface roughness for the photo resist capped sample is over 5X lower than that achieved without using a cap. The exact physical mechanism for this phenomenon is unknown, although it appears that an effective near-surface overpressure of carbon is significantly more proficient at preventing the sublimation loss of Si and aggressive step bunch formation.

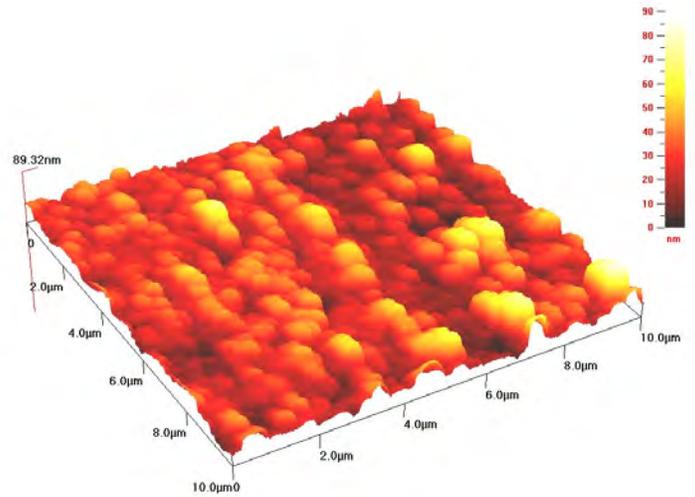
Table 3

Cap	$\text{Al}_3\text{Ti}/\text{W}$	$\text{Ti}/\text{AlNi}/\text{W}$	$\text{Ti}/\text{Ni}_2\text{Si}/\text{W}$
SiC	3.2×10^{-2}	1.1×10^{-3}	2.8×10^{-2}
Graphite	1.1×10^{-2}	5.1×10^{-5}	2.7×10^{-5}

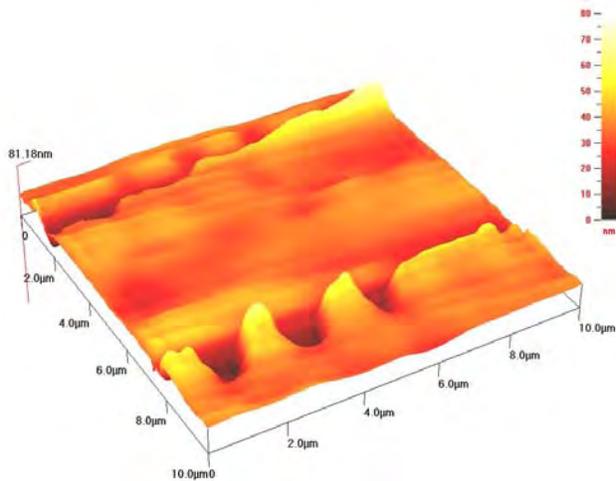
TABLE 3: Al^+ implantation effects on contact resistivity ($\Omega\text{-cm}^2$) when using SiC or graphite proximity caps during activation anneal.



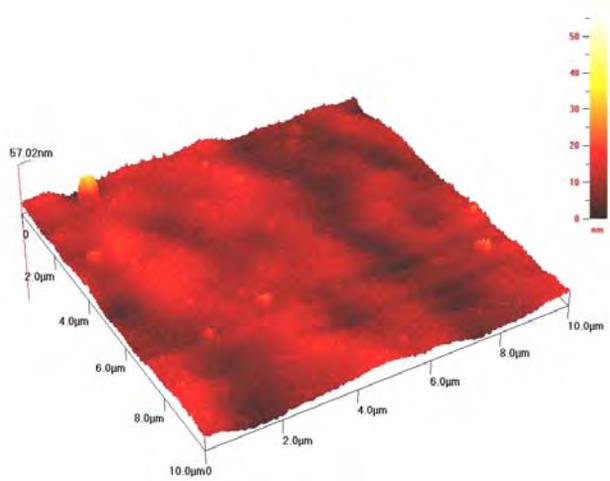
(a) Photo resist cap
Mean Dev: 1.40 nm



(b) No cap
Mean Dev: 8.76 nm



(c) SiC cap
Mean dev: 5.39 nm



(d) Graphite cap
Mean dev: 3.06 nm

Figure 4: AFM image of sample with (a) photo resist cap (b) no cap (c) SiC cap, and (d) graphite cap.

This ohmic contact study began with a focus on the Ti/AlNi/W stacking configuration. Initially, Auger Electron Spectroscopy (AES) was performed on control samples to verify the chemical composition of the rf sputtered AlNi intermetallic. AES results, presented as Fig. 5 showed that the desired compound stoichiometry was obtained. As shown in Fig. 6, Rutherford Backscattering Spectrometry (RBS) was subsequently used to validate the AES results and

analyze the composition and thicknesses of each layer in the entire stack. In addition, RBS was employed to investigate constituent metal intermixing and undesirable oxygen incorporation occurring during contact formation anneals (Fig. 7). The data clearly shows that the target layer thicknesses and compositional structure were achieved, in agreement with the AES results. The data also illustrates a minimal amount of component intermixing after annealing, with primary reactions apparently being the formation of desirable Ti and Al intermetallics with the Si-C. Also indicated is the incorporation of oxygen into the structure via the formation of a thin aluminum oxide layer on the surface of the W. The source of this contamination is probably due to the unavoidable partial pressure of background water vapor in the anneal system. While W appears to have prevented the diffusion of oxygen into the reactive Al and Ti layers, it was ineffective in preventing the out-diffusion of Al to the surface, enabling the formation of the thin oxide layer. This result emphasizes the need for development of effective diffusion barriers or elimination of reducing metals in contact structures to obtain optimal high temperature stability. Hence, Au was also chosen which can effectively act as a protective cap and a compatible layer for wire bonding.

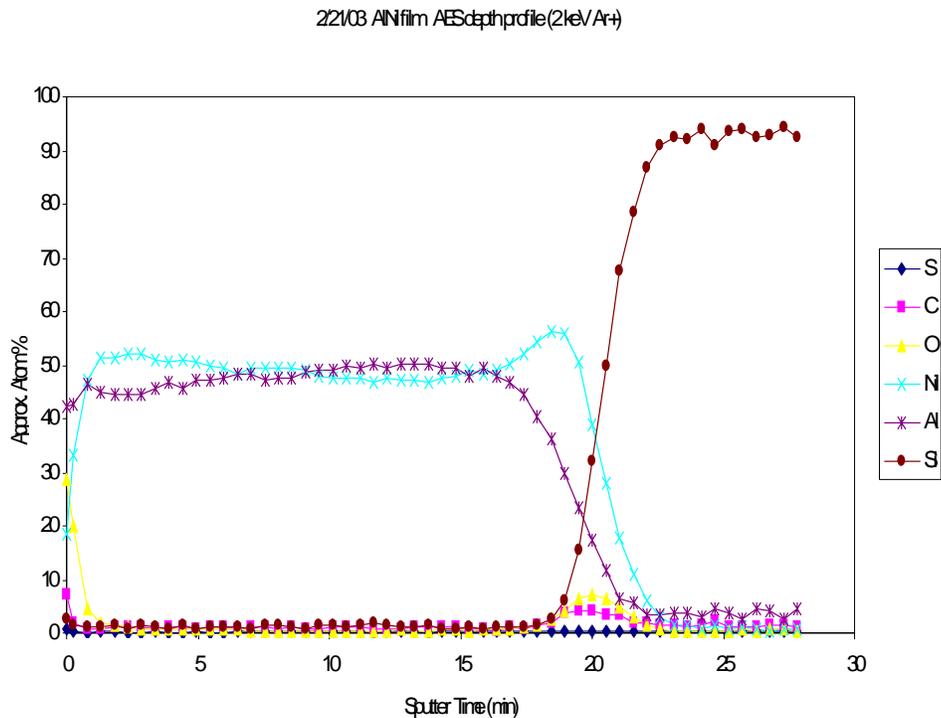


Figure 5: AES data verifying the desired stoichiometry of the AlNi intermetallic.

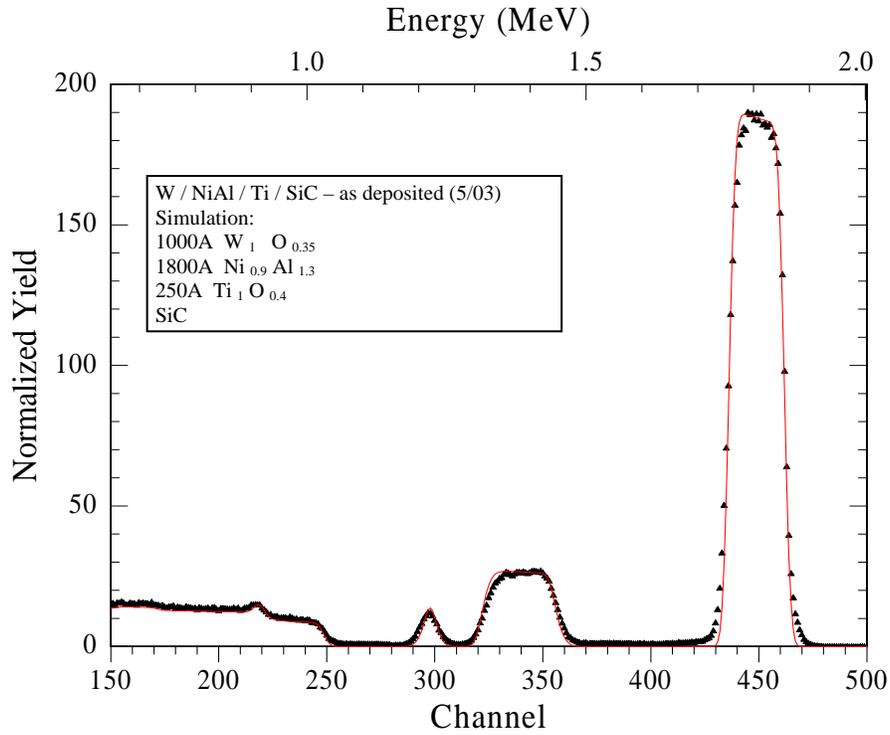


Figure 6: RBS results of an as-deposited contact of Ti/AlNi/W.

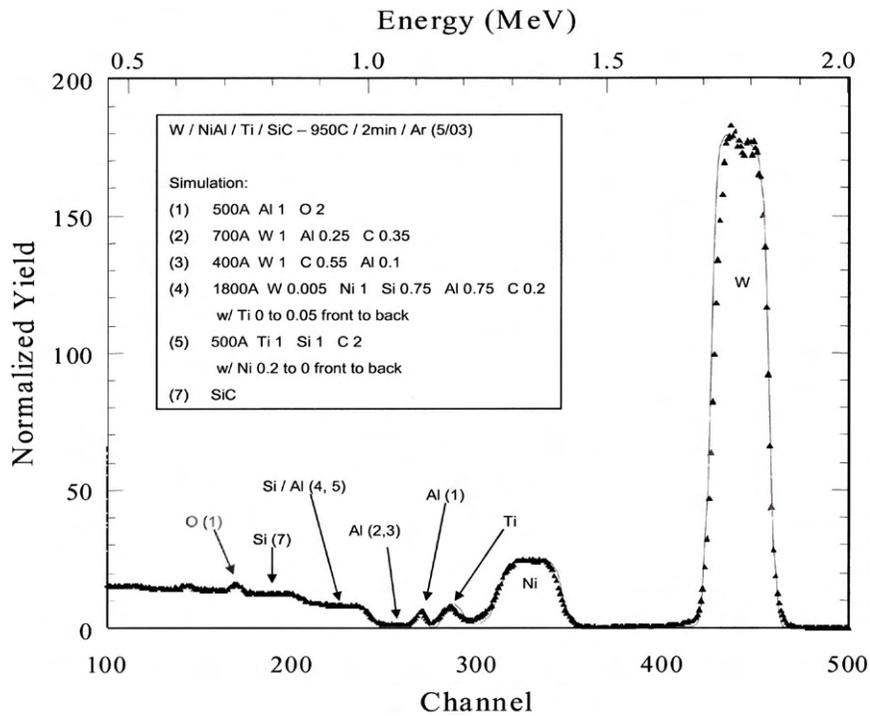
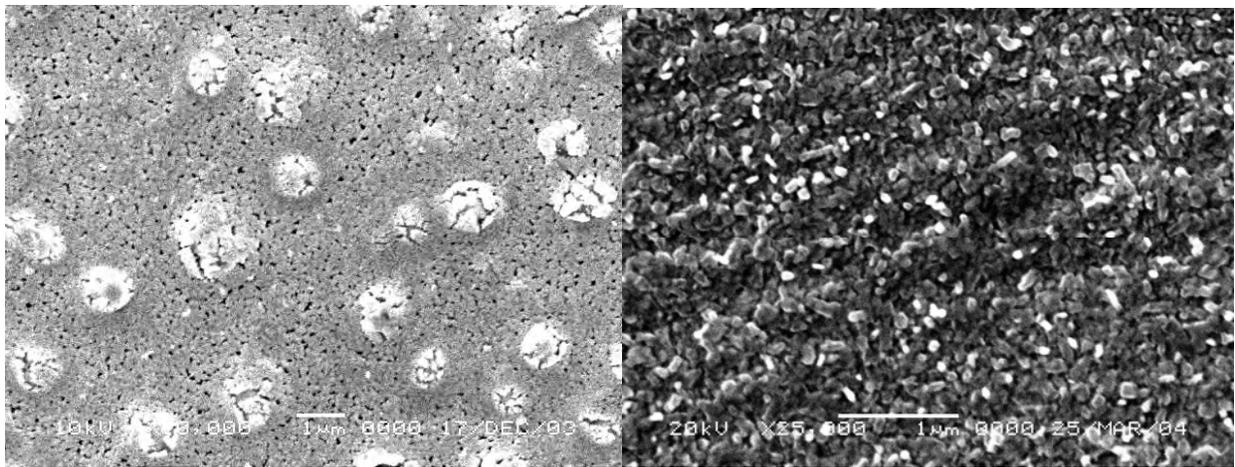


Figure 7: RBS data of post-annealed of Ti/AlNi/W.

Fig. 8 represents SEM images of the Ti/AlNi/W contacts after annealing which show the results of careful Ar purge line purification and W layer thickness optimization. Prior to insertion of an oxygen gettering tube into the anneal purge line and determination of the optimal W cap-layer thickness; post-anneal contact morphologies were characterized by high levels of oxygen incorporation, delamination bubbles, and excessive film stress resulting in marginal contact performance. Post-anneal morphology was improved significantly by these efforts and contact resistivity, consistency, and thermal stability were enhanced commensurately.



(a)

(b)

Figure 8: Comparison of post 925°C anneal SEM image of W contact surfaces (a) before and (b) after thickness optimization and anneal purge gas purification.

Fig. 9 illustrates the effect of anneal temperature on the I-V characteristics of optimized Ti/AlNi/W samples annealed at various temperatures. At 875°C the I-V curves are not quite ohmic, but above 950°C they become linear. Minimum resistivities are obtained after anneal at 975°C.

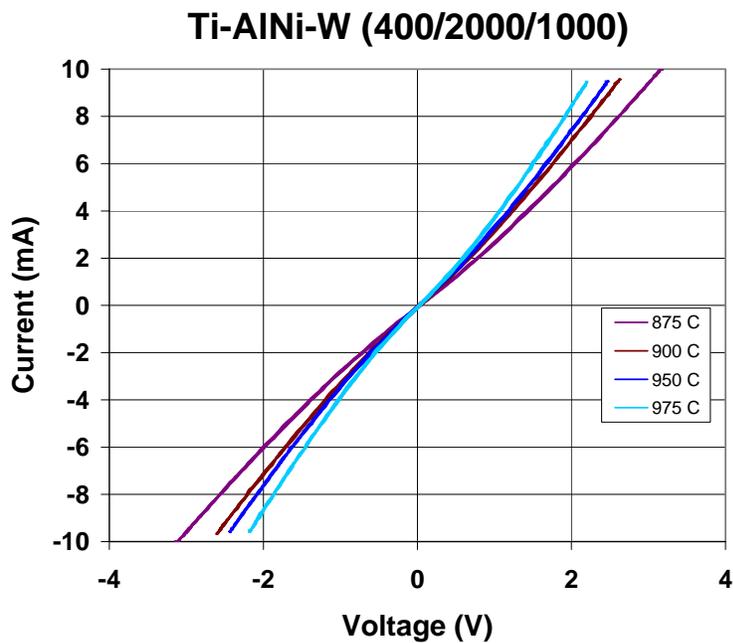


Figure 9: The effect of anneal temperatures on the Ti/AlNi/W contact I-V curves.

Fig. 10 shows the effect of anneal temperatures, parameterized by Ti and AlNi layer thicknesses, on the specific contact resistivity of Ti/AlNi/W. The data shown in this figure is representative for contacts formed on Al⁺ implanted materials under the conditions described in the previous section. As seen in Fig. 10, measurable differences occur between different Ti and AlNi layer thicknesses in terms of contact resistivity. A distinct preference is observed for the 400 Å Ti/2000 Å AlNi layered structure. The bar chart of Fig. 11 summarizes this effect by highlighting the specific contact resistivity minima for each of the layer thickness combinations.

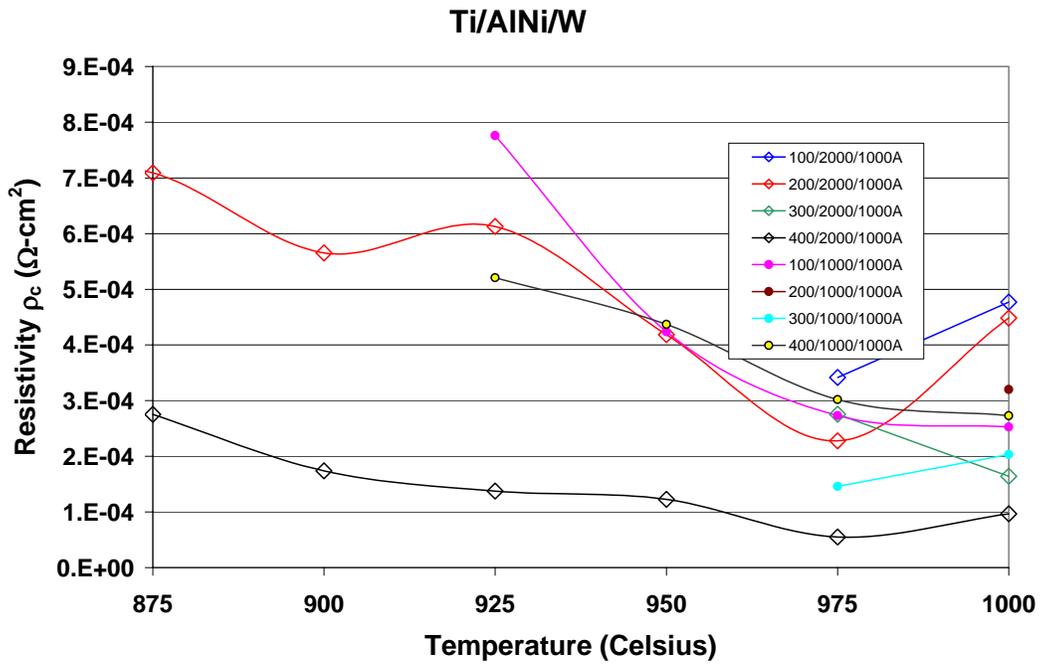


Figure 10: The effect of anneal temperatures on the specific contact resistivity of Ti/AlNi/W.

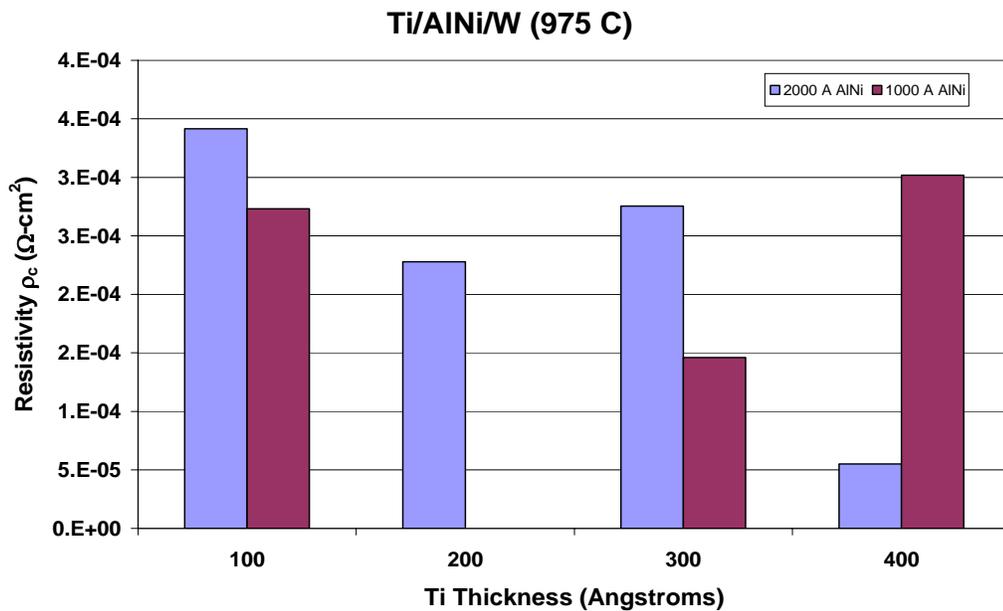


Figure 11: Effect of the thickness of titanium on the specific contact resistivity of Ti/AlNi/W.

Also studied was a comparison of Ti/AlNi/W contact performance to Ti/Ni₂Si/W on the same Al⁺ implanted material. Ni₂Si has been used successfully in recent work, although it suffered from similar repeatability problems as observed with the base-AlNi contact system. The data clearly illustrates the benefits obtained when contacts are formed on the smooth photoresist capped surfaces. Again, it is possible that some of the previous difficulty obtaining consistent results was directly related to the large average roughness occurring during activation anneals. As before, all of the data reflect the inclusion of purge gas purification during anneals and optimized W thickness layers. Also apparent from the data is that the Ni₂Si based contact system yielded comparable ρ_c values to those obtained using an AlNi binary layer. A second motivating factor for the continued investigation of this system is the possibility for it to serve as an ohmic contact for both n- and p-type material. However, surface morphologies were found to be inferior to the AlNi based contacts, and if exposed to temperatures above that required for ohmic formation, resistivity degraded rapidly.

Eventually Au was considered as a possible capping layer in place of the W. Fig. 12 shows the effect of anneal temperatures on the specific contact resistivity of Ti/AlNi/Au with or without Ge. It was reported that the addition of Ge would significantly reduce the anneal temperature and resulting resistivity [5], but this was not observed in this study. The Ti/AlNi/Au samples annealed at 650°C for 30 minutes in either the tube furnace with an oxygen gettering system or in the vacuum chamber, represented the superior stacking configuration. This sample set exhibited linear, slightly higher resistivities, at a much lower anneal temperature than that of the conventional Ti/AlNi/W stacks.

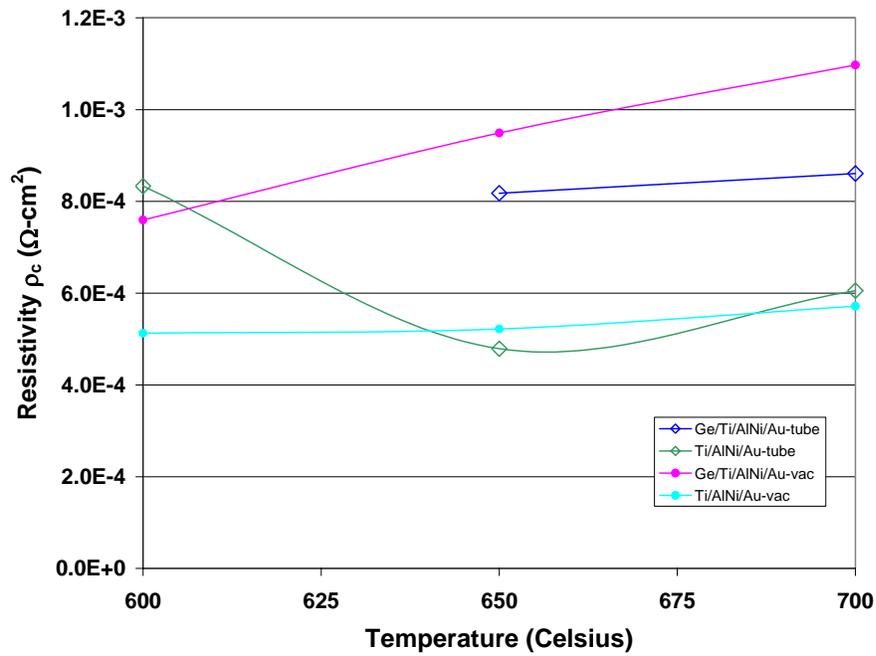


Figure 12: The effect of anneal temperatures on the specific contact resistivity of Ti/AlNi/Au for samples annealed under vacuum or in an Ar atmosphere.

Fig. 13 shows the post anneal AFM scan data of both Ti/AlNi/W and Ti/AlNi/Au samples. Fig. 13 (a) represents the surface of a Ti/AlNi/W sample, which exhibited a roughness mean deviation of 3.40nm. Fig. 13 (b) shows the Ti/AlNi/Au surface, which exhibited a roughness mean deviation of 18.5nm. The mean deviations of the Ti/AlNi/W and Ti/AlNi/Au control samples of were 2.86nm and 2.70nm respectively. This increase in surface roughness indicates a strong chemical reaction between the interlayers of the contact, especially for the case of the Ti/AlNi/Au metallization profile.

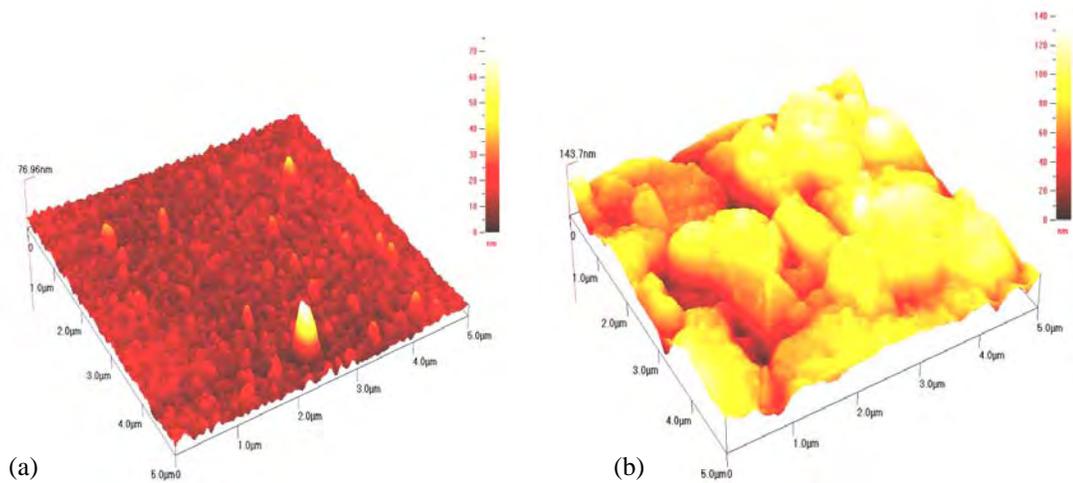


Figure 13: Comparison of post anneal (a) AFM image of Ti/AlNi/W (b) AFM image of Ti/AlNi/Au.

Similar results were observed using scanning electron microscopy. Fig. 14 (a) shows a SEM image of a Ti/AlNi/W stack after annealing at 950°C, and Fig. 14 (b) shows a Ti/AlNi/Au surface image after anneal at 650°C. As expected, the apparent surface morphologies of the samples indicate that the post-anneal Ti/AlNi/W is much smoother than that of the Ti/AlNi/Au.

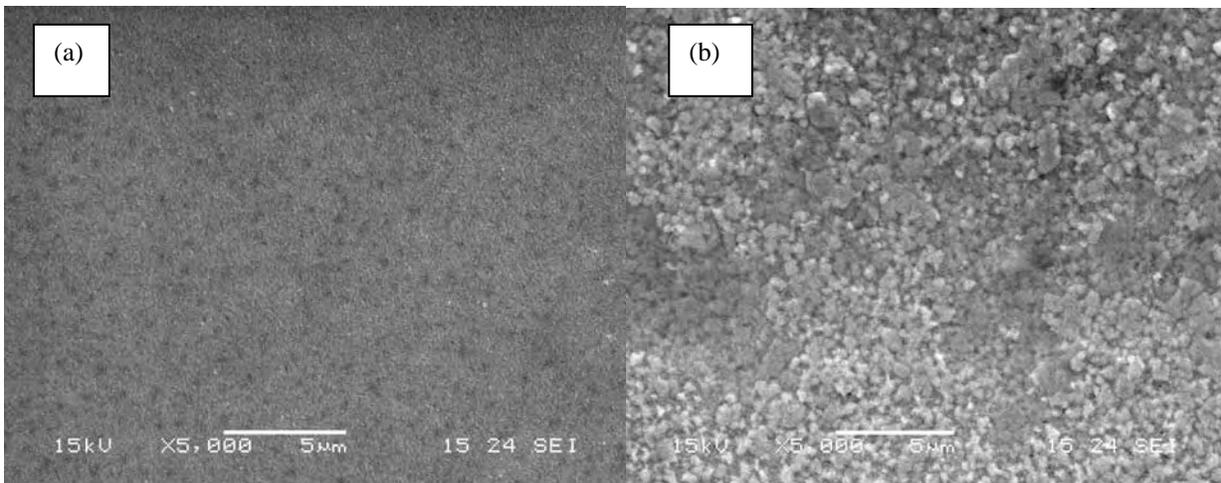


Figure 14: Comparison of post anneal (a) (5kx) SEM image of Ti/AlNi/W (b) (5kx) SEM image of Ti/AlNi/Au.

X-ray diffraction was used to identify component mixtures of Ti/AlNi/Au samples of interest. For example, both control and post anneal SiC/Ti/AlNi/Au samples were examined. The results are shown in Figures 15 and 16. The XRD results below indicate the formation of

TiC, TiSi₂ and certain Au-Al compounds. RBS data, represented by Fig. 17, also showed significant component intermixing between the Au and AlNi after annealing, with primary reactions apparently being the formation of desirable Ti and AlNi intermetallics with the SiC. The roles these compounds play need to be further investigated to better understand their contribution to improved contact resistivity and lowered anneal temperature.

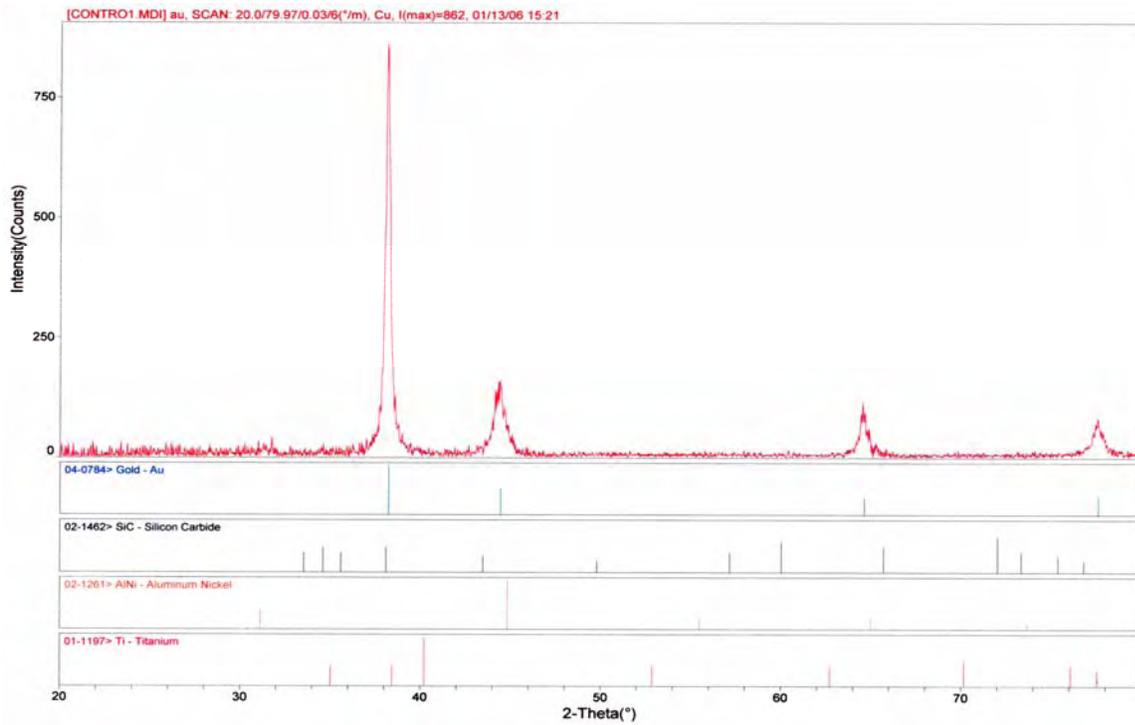


Figure 15: X-ray diffraction spectra of the control SiC/Ti/AlNi/Au sample.

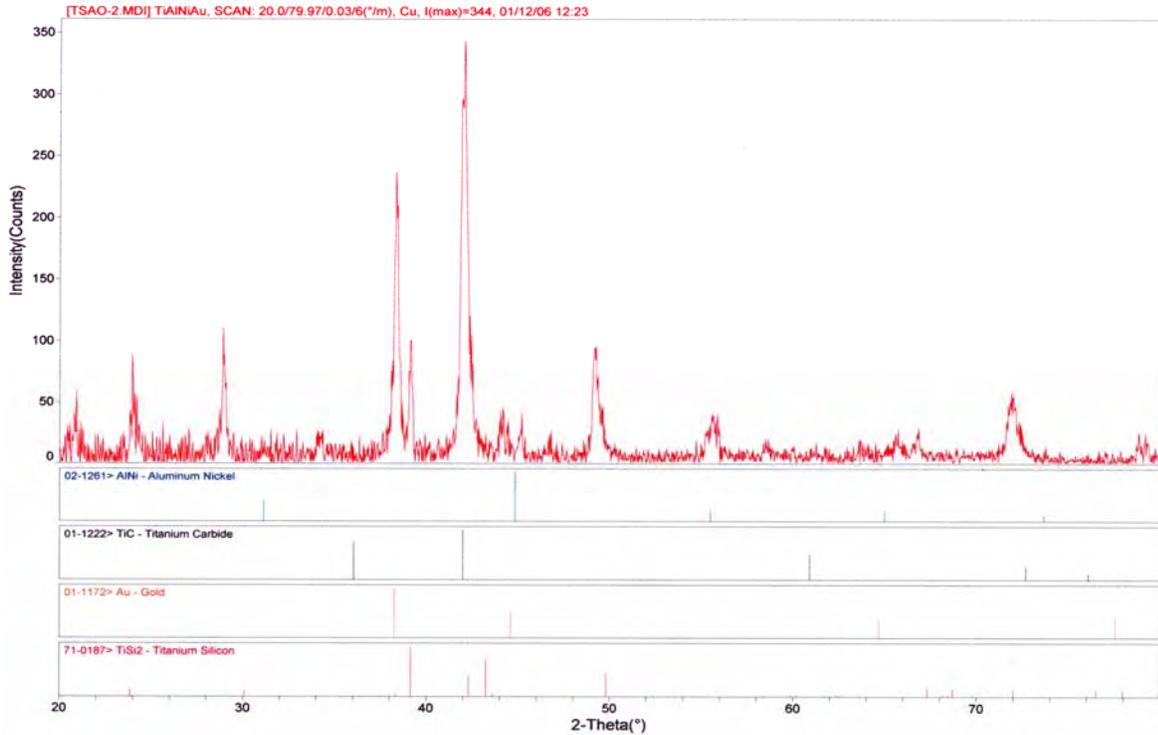


Figure 16: X-ray diffraction spectra of the post-anneal SiC/Ti/AlNi/Au sample.

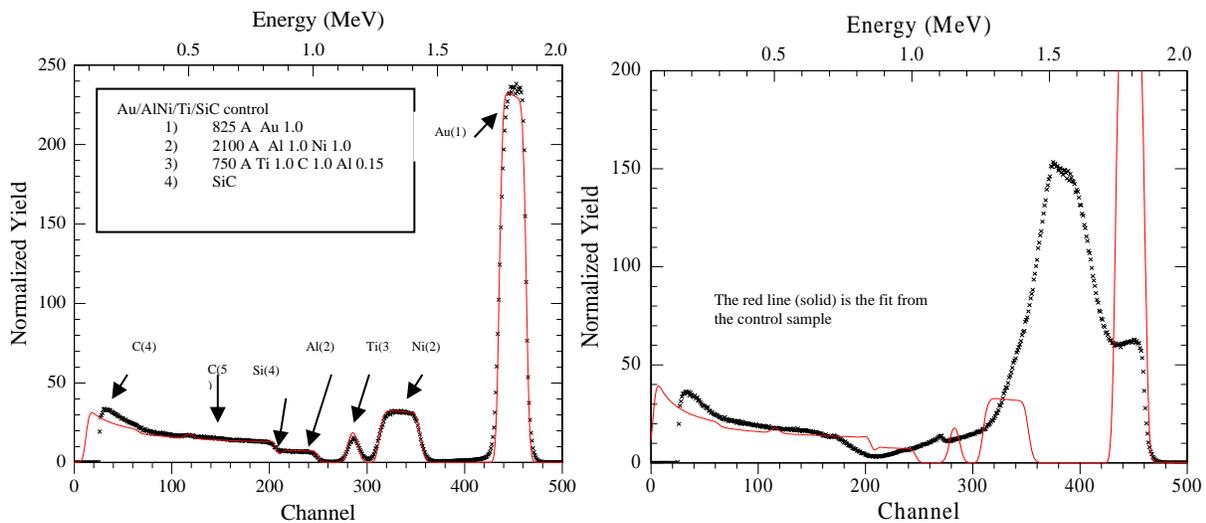


Figure 17: RBS results (a) of control SiC/Ti/AlNi/Au sample (b) after annealing at 650°C for 30 minutes.

Fig. 18 illustrates the I-V characteristics of optimized Ti/AlNi/Au and Ti/AlNi/W samples annealed at 650°C. At this temperature only the I-V curve of the Ti-320-AlNi-1440-Au

sample is linear, but above 950°C all of the Ti/AlNi/W I-V curves also become classically ohmic. Minimum resistivities of Ti-320-AlNi-1440-Au are obtained after anneal at 650°C for 30 minutes.

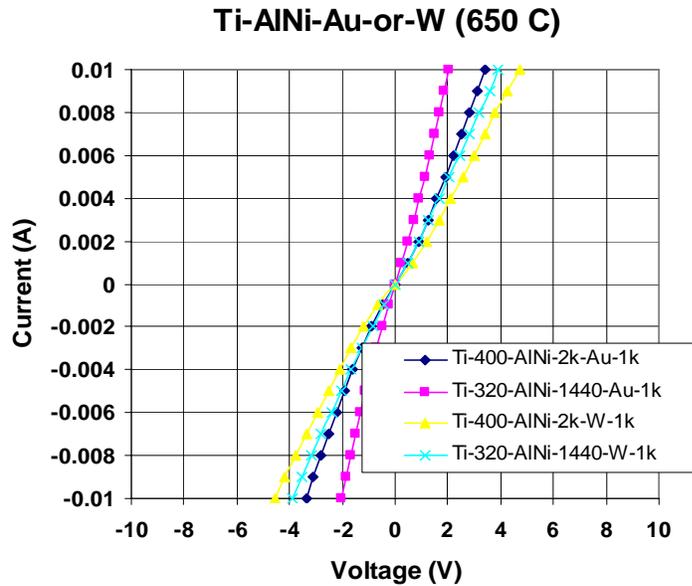


Figure 18: Typical I-V curves of Ti-AlNi-Au or W samples annealed at 650 C.

Fig. 19 summarizes the effect of anneal temperature on the specific contact resistivity of both Ti/AlNi/Au and Ti/AlNi/W metallization schemes. This confirms that an annealing temperature of 650°C for 30 minutes is sufficient to obtain ohmic characteristics for the gold capped samples, and is significantly lower when compared to the annealing temperature required for resistivity optimization of Ti/AlNi/W contacts.

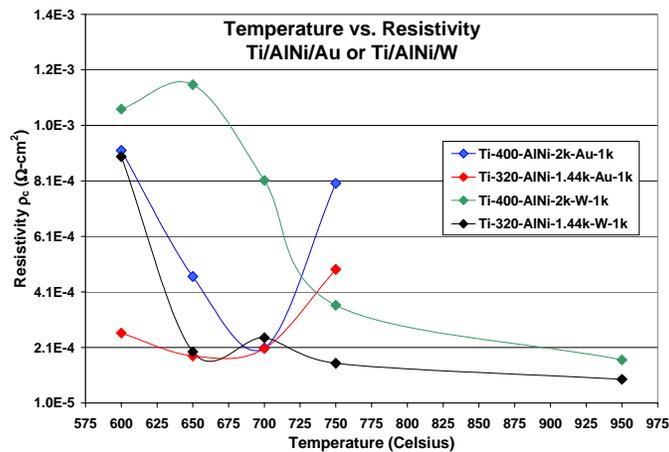


Figure 19: The effect of anneal temperatures on the specific contact resistivity.

Fig. 20 shows the thermal aging effect on the specific contact resistivity of a separately prepared set of Ti/AlNi/Au contacts annealed at the optimum temperature of 650°C. Again, the resistivity is well in the low 10^{-4} range at room temperature; this value is further reduced when tested at increasing aging temperature. The overall trend was relatively steady whether heating up to or cooling down from 350° C.

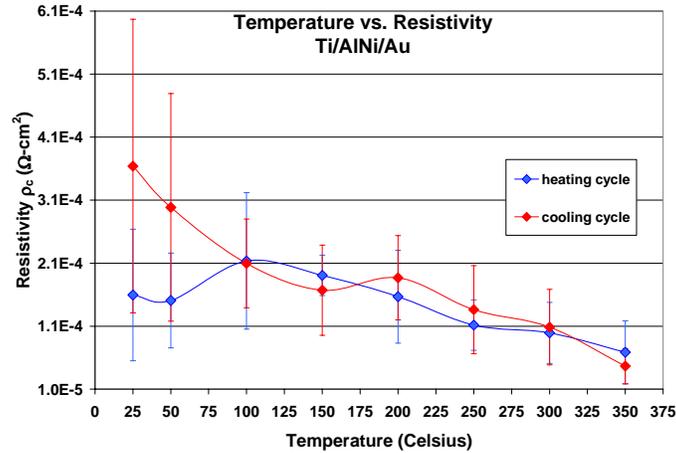


Figure 20: The thermal aging effect on the specific contact resistivity of Ti/AlNi/Au.

As mentioned, multilayer electronic packaging configurations were simulated using ANSYS. Significant progress was made on the IGBT model as shown in Fig. 21. Due to the inherent difficulties of 3D modeling, a 2D model for the SiC stacking was pursued first. The results are shown in Figures 22 and 23. The boundary conditions were set 250°C for the top line, and the remainder was set for the free-convection to the air at 20°C.

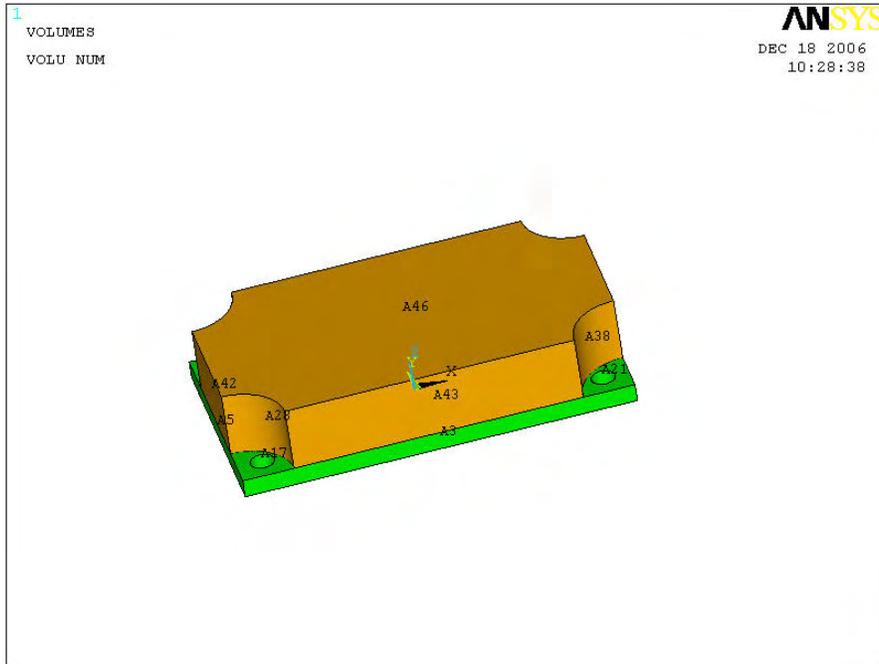


Figure 21: The full view 3D model of the IGBT.

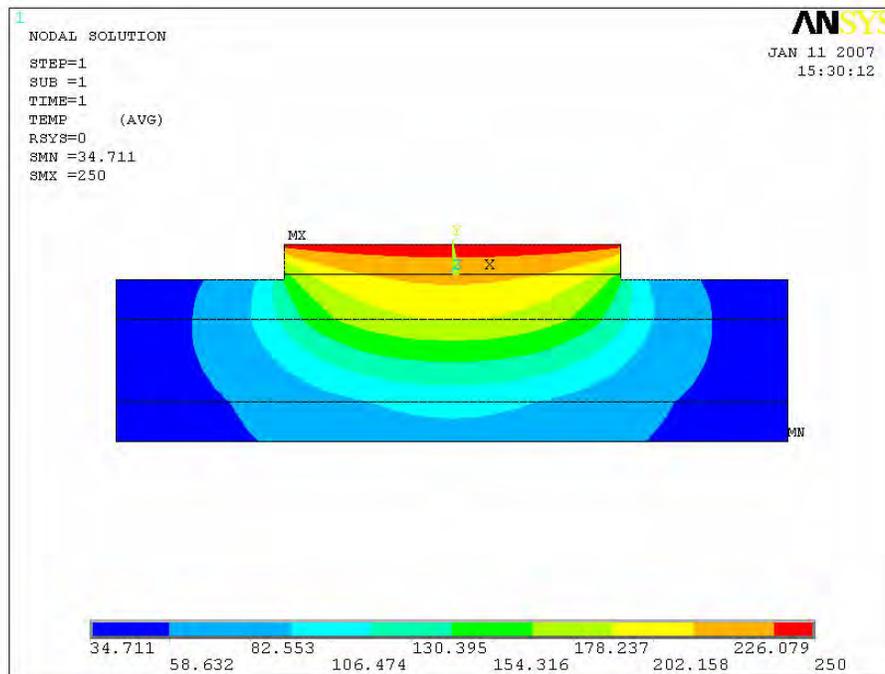


Figure 22: 2D temperature distribution of the SiC stacking configuration.

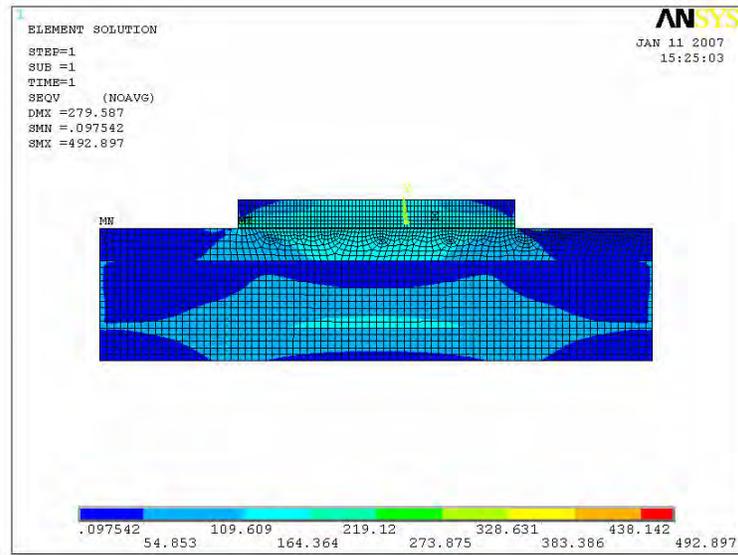


Figure 23: 2D stress distribution of the SiC stacking configuration.

As skill and insight increased, ANSYS modeling and simulation continued with the simplified SiC stacking configuration. The 2D model was refined, and some preliminary 3D models have been generated and examined. Figure 24 is an example of the 3D thermal modeling.

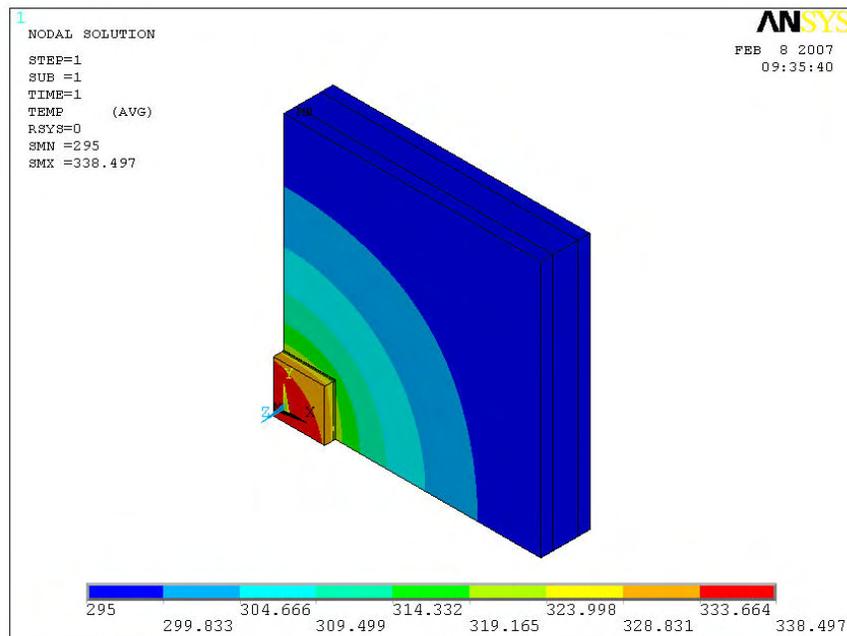


Figure 24: 3D temperature distribution of the SiC stacking configuration.

Heat generations from 24 watts to 96 watts were simulated in the 3D thermal model. The output temperature distributions are shown in Figure 25. The output chip temperatures range from 367 to 585 K. The output stress distributions are shown in Figure 26. The output Von Mises Stresses, maximum stress criterion, range from 427 to 1839 MPa.

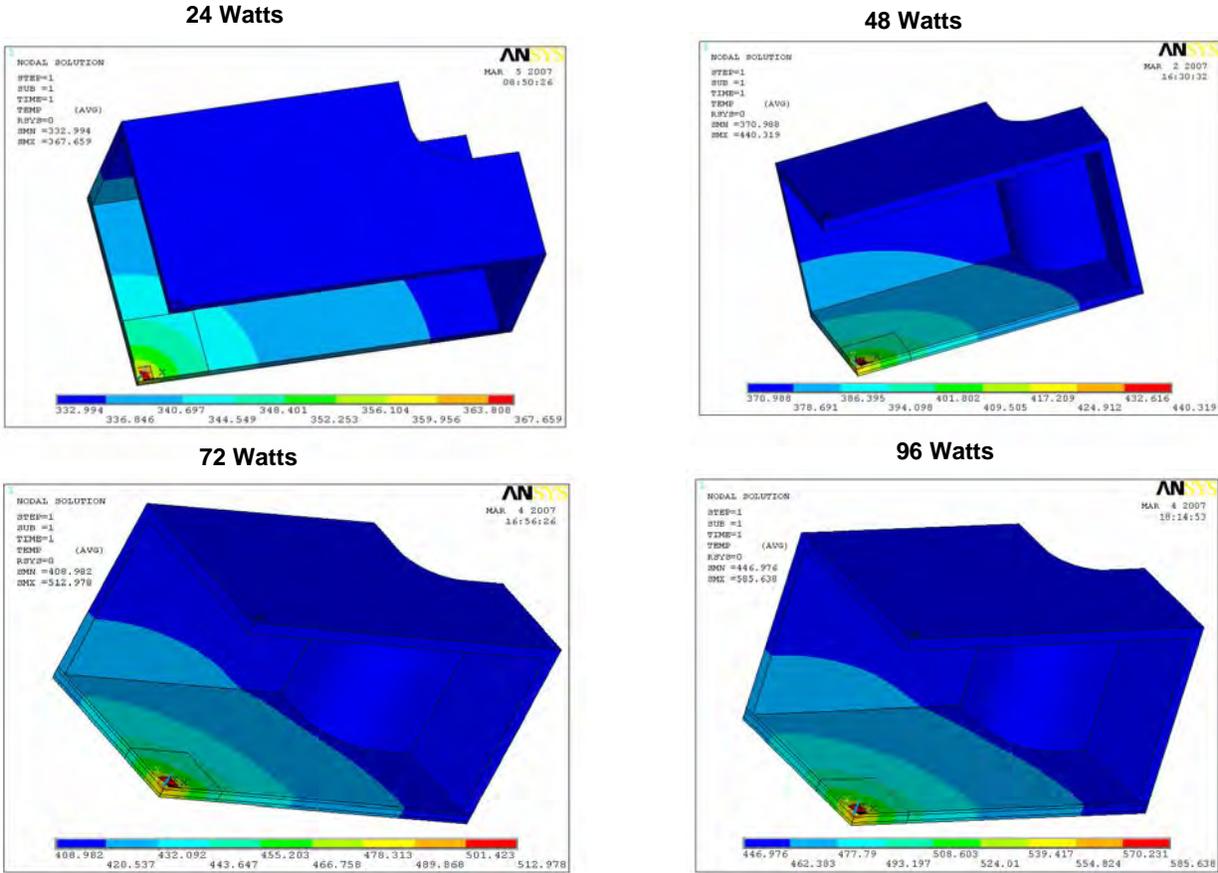
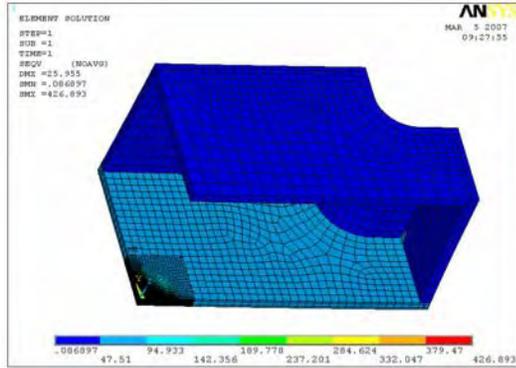
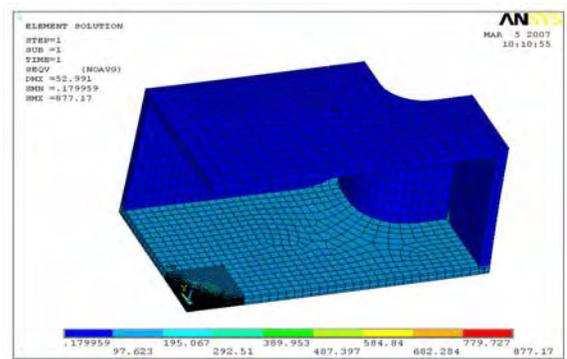


Figure 25: The effect of the heat generation on the temperature distribution of the 3D thermal model.

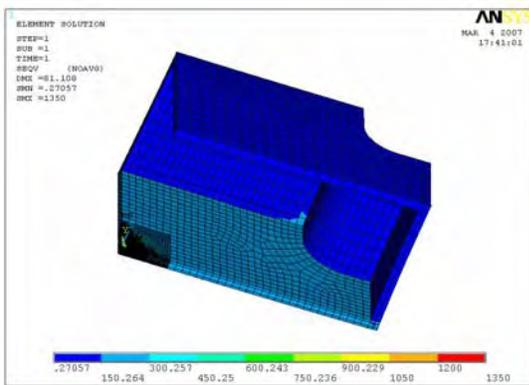
24 Watts



48 Watts



72 Watts



96 Watts

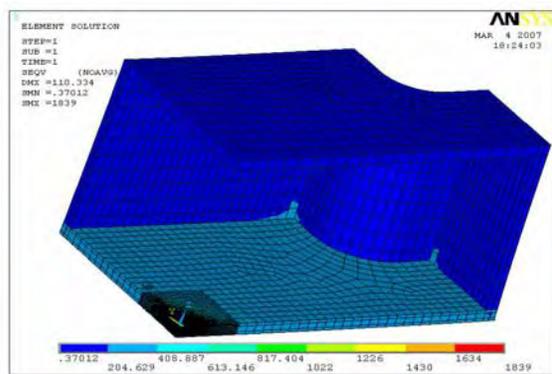


Figure 26: The effect of the heat generation on the stress distribution of the 3D mechanical model.

5. CONCLUSION

Improved AlNi-based ohmic contacts to p-type 4H-SiC have been achieved using low energy ion (Al^+) implantation, the addition of a thin Ti layer, and a novel two-step implant activation anneal process. Resistivities of $5 \times 10^{-5} \Omega\text{-cm}^2$ were reached by doping the surface region of lightly p-doped 4H-SiC epilayers via low energy Al^+ implantation. Acceptor activation was achieved by annealing the samples with a 1400+1700°C two-step sequence in an Ar atmosphere, which also yielded improved surface morphology when implanted samples were capped with photo resist during the anneals. AFM average roughness values improved by over 5X compared to samples without capping. The metallurgical morphology and contact resistivity remained intact even after annealing at 1100°C, indicating good thermal stability. The Ti/AlNi/W contacts on implanted layers were compared to Ni_2Si intermetallics and were found to be comparable to or superior in terms of specific contact resistivity, uniformity, and thermal stability. Ni_2Si contacts exhibited significant potential for further work. Ti/AlNi/Au contacts were also studied which resulted in contact resistivities in the $5 \times 10^{-4} \Omega\text{-cm}^2$ range. Even though these values are an order of magnitude higher than those of the Ti/AlNi/W system, the reduced anneal temperature (650 °C) implies that Ti/AlNi/Au is a promising stacking configuration. Using Au as the top layer contact not only reduced the annealing temperature required for linear performance, but will also serve as the bonding layer of the device package; whereas wire bonding requires additional layers if W is used as the cap layer. Furthermore, the metallurgical morphology and contact resistivity of the Ti/AlNi/Au contacts remained intact even after thermal aging up to 350°C and back down to room temperature. The benefits of using Ge to reduce the anneal temperature necessary for ohmic behaviors of the Ti/AlNi/Au stacks was not observed in this investigation. On the other hand, benefits of a longer 30 minute anneal time at 600 – 700°C, in either vacuum or atmospheric pressure Ar ambients was observed. Namely, the 2 minute annealing cycle used for the Ti/AlNi/W and Ti/ Ni_2Si /W study resulted in higher anneal temperatures before ohmic characteristics were seen. This same anneal time was not sufficient for the Ti/AlNi/Au samples, whereas increasing the cycle time to 30 minutes resulted in ohmic behavior at a much lower temperature. Increasing the anneal time however, had little or no impact on reducing the required anneal temperature of the Ti/AlNi/W and Ti/ Ni_2Si /W samples

when the experiments were repeated. Also, 2D and 3D thermal and mechanical models of multilayer electronic packages have been developed using finite element analysis (FEA). The temperature and stress distributions from this work generally agree with theoretical predictions.

6. RECOMMENDATIONS

The research conducted in this program revealed the importance of specific contact resistivity and surface roughness for SiC devices. These characteristics rely heavily on the activation anneal procedures, particular temperatures and surface protections. With the newly constructed high vacuum annealing station (capable of annealing a sample up to 1800°C under vacuum or in an argon atmosphere) and the quartz tube furnace (capable of annealing up to 1200°C); it is now much more efficient to continue this type of research. The exact chemical composition at the interface of the ohmic contact still needs to be identified and the new configurations optimized to achieve the minimum contact resistivity.

Packaging is another aspect that needs to be addressed more fully. Even though the SiC exhibited superior electrical properties, it needs to be packaged for practical applications. A preliminary study of packaging should be conducted. 3D models should be refined with greater understanding and control of the boundary and initial conditions. More complicated multi-chip configurations need be simulated. Since the material layout plays such an important role in improving the overall performance of the power module, material selection, compatibility and placement needs to be explored. Also, issues involving electrochemical deposition for the dies to enhance bonding ability need to be addressed. A filling gel or encapsulant of appropriate composition and properties must be established and further wire bonding between dies and the packages needs to be conducted. Prototype SiC devices need to be packaged to verify the modeling results and to ensure the power devices for high temperature applications. Due to increased in-house capability, such as a larger diameter wire bonder and a reactive plasma etcher, it is much easier to perform deposition and lithography as well as packaging procedures. With the increased performance of SiC power devices, optimized packaging of these power devices may be demonstrated in the very near future.

7. REFERENCES

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APPENDIX A

**FACILITY CAPABILITIES
FOR
POWER SEMICONDUCTOR LAB
AND
ADVANCED CAPACITOR RESEARCH & DEVELOPMENT CENTER**

APPENDIX A

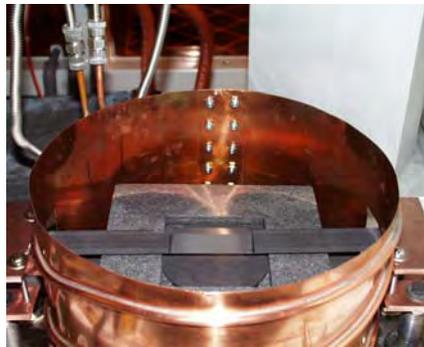
POWER SEMICONDUCTOR LAB

3000°C HIGH TEMPERATURE ANNEALING STATION

The 3000°C / 2KW annealing furnace contains a cooling stage that surrounds a graphite heating section. An Omega PID temperature controller and thermocouples with a range of 0°C to 3000°C control the heating process. Two controllers are installed for measuring the temperature of the one graphite rod and the ambient temperature between the two graphite rods where the sample is placed. The pressure is measured by MKS type 286 and type 290 ion gauge controllers with a roughing pump / Helix Cryo-Torr system for pressures < 1microtorr.



Annealing System



Graphite Electrodes and Cooling Shield

BOC EDWARDS AUTO 306 ELECTRON BEAM

The Boc Edwards electron beam setup is used primarily for depositing a variety of materials at an ultimate pressure of < 1 microtorr. It contains four thermal resistive heating sources, source shutters and a quartz crystal film deposition controller. The pressure is controlled by a roughing / cyrodrive pumping system.



Electron Beam



Control System and Vacuum Chamber

APPENDIX A

JEOL JSM6060 SCANNING ELECTRON MICROSCOPE

The Jeol scanning electron microscope has a magnification range of 5 to 300,000x with accelerating voltage levels of 0.5 to 30 kV in a high vacuum environment with a roughing pump. The maximum specimen size is 32 mm, and the system employs an 18.1 inch high resolution FPD. The system also possesses a Thermo Lab x-ray system that combines elemental and spatial data to create true representation of a material. The system is capable of spectral analysis; quantitative x-ray mapping or line scans with compass and X phase.



Scanning Electron Microscope



Scanning Electron Microscope

QUESANT Q-SCOPE 350 ATOMIC FORCE MICROSCOPE

The Quesant atomic force microscope has an AFM scan head choice of 20, 40 or 80 μ m. The system is equipped with an isotopic focal system, a loop feedback, a color video subsystem, electronic and stage interface units. The system was also upgraded with a new PC and Scan Atomic software package.



Atomic Force Microscope



Microscope with New PC & Software

APPENDIX A

DEKTAK 3ST SURFACE PROFILER

The Dektak surface profiler possesses a color video camera with: 60-420x zoom, scan length range from 50 μ – 50mm, vertical range of 131 μ m, 8000 data points per scan, and accommodates a 6.5” diameter sample. The unit received periodic maintenance with the acquisition of all previous installed and updated software.



Surface Profiler

ZEISS AXIOSKOP 451485 MICROSCOPE

The Zeiss Axioskop Microscope is an optical characterization unit with a selectable optical zoom of 5-100x. The unit is controlled by PC using Scion Image software.



Microscope

APPENDIX A

SOUTH BAY TECHNOLOGIES RIE 2000 REACTIVE ION ETCHER

The reactive ion etcher is designed for anisotropic etching of microelectronic devices. The turbo molecular pump system enables vacuums of < 1microtorr. The system can handle wafers up to six inches diameter in the 200mm diameter vacuum chamber. The system is equipped with two channel gas delivery and possesses a 200W, manual tuning 13.56 MHz RF power supply. The system is also equipped with all digital readouts and a process timer.



Reactive Ion Etcher

KARL SUSS MJB3 MASK ALIGNMENT SYSTEM

The alignment system possesses HP 200W exposure optics with a CIC 500W power supply using optical feedback control selectable to either 365 or 405nm. It also possesses a selectable contact mode between either high precision - vacuum contact, or standard - hard contact using nitrogen.



Mask Alignment

APPENDIX A

WIRE BONDERS 4524A & M20B

The Kulicke & Soffa wire bonder is a multi-process ball bonder for gold wire. It possesses semi-auto, automatic and manual modes, individual bond parameter control and can be used with a wide range of wire diameters. The digital operation enables programming of unique bonding schedules, with up to 200 different programs stored in memory.

The Orthodyne Electronics M20B wire bonder ultrasonically bonds 4 to 20 mil aluminum wire and 3 to 25 mil gold wire to semiconductor devices.



Kulicke & Soffa 4524A



Orthodyne Electronics M20B

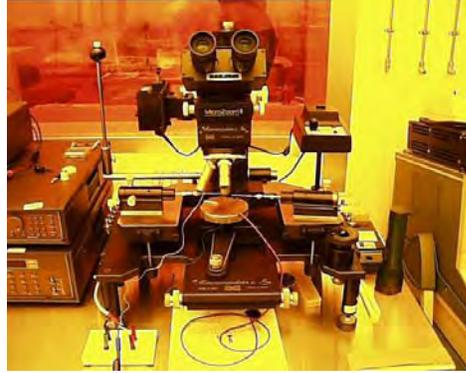
KEITHLEY CV TEST SYSTEM

The CV test system contains a Keithley Model 590 C-V Analyzer, Model 236 source measurement unit and Model 617 electrometer. The source measurement unit is currently PC controlled using National Instruments CVI with voltage and current measurements. The unit has 10fA, 10 μ V measurement sensitivity with custom sweep and pulse capability. The Model 590 C-V analyzer possesses 100 kHz/ 1MHz test frequencies, measures capacitances of 10fF-20nF and conductance 0.1nS-1 μ S. It displays capacitance versus voltage and capacitance versus time characteristics of semiconductor devices. The Model 617 electrometer possesses a +/-102V power supply and measures voltage, current, resistance and charge. The system uses a Micromanipulator MM 6000 with 2.25 to 25x magnifications for probing samples.

APPENDIX A



CV Test System



Probing Station

TEKTRONIX 370A & 371A CURVE TRACERS

The 371A Curve Tracer features up to 3KV, 400A, 3kW, high power parametric characterization of semiconductor devices. It also features waveform comparison, envelope display, waveform averaging and Kelvin sense measurements. The unit features interactive program control, automated cursor measurements and sweep measurement mode.



Curve Tracer

APPENDIX A

THERMOLYNE 79400 TUBE FURNANCE

The Thermolyne 79400 3" Tube Furnace is primarily used for material annealing with step temperatures up to 1200°C.



Tube Furnace

ADVANCED CAPACITOR RESEARCH & DEVELOPMENT CENTER

1000°C HIGH TEMPERATURE TEST SYSTEM

The 1000°C high temperature test station contains the Kepco JQE 100V / 10A power supply, an Omega PID temperature controller and a Granville Phillips 340 vacuum controller. The system also contains a safety interlock system to monitor vacuum, cabinet access, system cooling, AC power disconnect and emergency stop conditions. To achieve <1 microtorr, a turbo pump combined / scroll pump system is installed. The sample probing is accomplished with 3-axis molybdenum probing rod test fixture. The system was modified with a 2nd thermocouple to monitor the sample temperature independent of the hot stage temperature.



High Temperature Test Station



Control Rack

APPENDIX A

ASTEX 1.5 KW POLYCRYSTALLINE DIAMOND DEPOSITION SYSTEM

The control rack contains a safety interlock system which monitors all critical subsystem operation has complete control over the gases and microwave control to allow unattended operation. The system also contains a Granville Philips 340 vacuum controller for high vacuum using a Hull mechanical pump, Astex stage heater 1.5KW, 2.45 GHz microwave system and stage height controller. The gas flow is controlled via unit flow controllers by PC control per safety interlock permission. It is capable of controlling four gases, H₂, CH₄, N₂, and O₂. The system is equipped with three H₂ detectors for added safety which are also controlled by the safety interlock system.



1.5 KW Diamond Deposition System



Safety Interlock System

ASTEX 5 KW PCD DEPOSITION SYSTEM

The system is controlled by a safety interlock system which monitors all critical subsystem operations, has complete control over the four gases H₂, CH₄, N₂, O₂ and microwave power control. Four hydrogen sensors, along with the safety interlock system, allow complete unattended operation. The system contains an Astex 5KW, 2.45 GHz microwave system, a stage height controller, a Granville Phillips 318 vacuum controller under high vacuum using a Hull mechanical pump and a MKS 647B gas flow system.



5 KW Diamond Deposition System



Safety Interlock System

APPENDIX A

MRC M862 RF SPUTTERING SYSTEM

The system is operational at 1000V / 500W power. It contains a 1.5KW, 13.56 MHz RF generator. The pressure is measured by a Granville Phillips 340 pressure controller with a Varian Scroll / Turbo-V 300 pump combination and LN₂ cold trap for pressures <1microtorr. The entire system is controlled by a safety interlock system which monitors cooling, cabinet and RF head access and controls RF power.



Modified MRC Sputtering System



Original MRC Sputtering System

DENTON DV-502A RF SPUTTERING SYSTEM

The original system contained only a single RF gun control. The addition of a Kepco JQE 100VDC / 10A power supply for a 1000°C hot stage, RF power generator and automatic RF network tuner, allowed the operation of the second RF gun. The system has the capability of pressures of <1microtorr and a power maximum power output of 350W.



New RF Supply Rack



RF Sputtering Machine

APPENDIX A

VEECO VE400 THERMAL EVAPORATOR SYSTEM

With an attempt to prolong use of the system, interior control & power cables were replaced. The analog vacuum meter was replaced with a Varian 880 vacuum ionization gauge. Pressures of <1 microtorr is achieved by a Duo Seal mechanical / diffusion pump combination. The unit is capable of producing 400W.



Modified Evaporator System



Original Evaporator System

LESKER PVD 75 THERMAL EVAPORATOR SYSTEM

The Lesker PVD 75 thermal evaporator is the primary electrical contact deposition system in the laboratory. It posses a Sigma SQC-122c thin film deposition controller and a scroll / turbo pump combination for pressures <1 microtorr.



Thermal Evaporator



Internal Components

APPENDIX A

HIGH TEMPERATURE PCD DEPOSITION SYSTEM

The high temperature PCD deposition system which contains a safety interlock system that monitors critical subsystem components as well as 4 hydrogen sensors has total control over the H₂, CH₄ and O₂ and the hot stage power supply to allow unattended operation. The system also contains Sorenson DCS 60-50 50V / 50A, Xantrex XFS 150V / 10A power supplies, a Varian 880 vacuum ionization gauge, a MKS 647C multi gas controller, a Granville Phillips 375 convection gauge, and a Eurotherm 2416 pressure controller in a high vacuum using a Hull mechanical pump. The system operates at a temperature of 500°C.



High Temperature PCD Deposition System



Hot Filament

RUSSELL'S RB-32-LN₂ ENVIRONMENTAL CHAMBER

With the loss of lab LN₂, the Russell environmental chamber RB-32 was modified to accept a small portable LN₂ doer. The chamber originally had a temperature capability of -200C to +200C and is controlled by a JC Systems Model 600 temperature controller.



Environmental Chamber



Portable LN₂ Doer

APPENDIX A

THERMCO MINI BRUTE HIGH TEMPERATURE TUBE FURNACE

The Thermco Mini Brute 5" tube furnace is a 3 stage furnace capable of heating up to 1200°C.



Tube Furnace

LINDBERG 51828 HIGH TEMPERATURE OVEN

The Lindberg 51828 oven is capable of heating up to 1100°C.



Oven

GRIEVE HIGH TEMPERATURE AA-350 OVENS

The Grieve AA-350 ovens are capable of heating up to 850°F.



Ovens

A-13

APPENDIX A

OLYMPUS BX51 MICROSCOPE

The Olympus BX51 microscope is an optical characterization unit which has a selectable optical zoom of 10-100x. It possesses a 12V/100W halogen light source, neutral density filters, a 22mm field of view, and UIS2 optics.



Microscope

ALUMINUM NITRIDE RF SPUTTERING SYSTEM

The RF Sputtering System is used for the growth of aluminum nitride. The safety interlock system monitors various subsystem components and has complete control over the gas flow and RF power supply. The system contains 2 Advanced Energy Pinnacle Plus 5KW 13.56Mhz RF power supplies, 4 Varian Turbo-V 1000HT turbo pumps and controllers, 2 Varian scroll pumps for pressures <1microtorr, a Granville Phillips 358 micro-ion controller, a Danielson Phototron scanner controller and unit flow controllers controlling Ar, O₂, and N₂, with National Instruments Lab View. The system has been recently retrofitted from a rolling scanner to a multi-layer stackable system.



Aluminum Nitride Deposition System



Control Panel

APPENDIX A

HIGH SPEED DRIVESTAND

The conversion of the drive stands from Vax to PC control using National Instruments CVI continues with support in the electronic interfaces supplied. The drive stand possesses 3 stands that are rated from 1150 to 1920 RPM at 350HP.



Drive Stand Control Console



Status and Control Racks

TRANSFORMER TEST STATION

The transformer test station was created to test SiC components at 200°C. The system consists of a 270VDC input to 28VDC output using in-house transformers, silicon carbide diodes and supporting components. The system contains 2 HP 6030A 170V / 17A power supplies, a Wavetek 2Mhz sweep generator, a Tektronix PS280 DC power supply, a Lecroy LC574AM 1 GHz and Tektronix TPS 3054 500MHz O-Scopes.



Power & Control Components



Environmental Chamber

APPENDIX A

CAPACITOR DATA ACQUISITION SYSTEM (CAPDAS)

LABORATORY PC MAINTENANCE

The database was maintained with all current data and system backups. All PC's received mandatory and periodic maintenance for continued consistent operation including antivirus updates.

HP4284A CHARACTERIZATION SYSTEM

The HP4284A LCR characterization system, which collects data such as capacitance, dissipation factor, and ESR, was used to measure DLC, aluminum nitride, ML films, carbon nitride, and other experimental materials. The system performs frequency, voltage and current scans from 20Hz to 1 MHz with 40V DC Bias and 40A current available. The Janis Research cryogenic test system possesses a CTI 8300 compressor with a 5400 controller, a MKS 286 pressure controller and a Lakeshore 330 auto tuning temperature controller. The vacuum is generated by an Alcatel 2020A scroll / CTI Cryogenics model 22 refrigerator. The system has a temperature capability of -150°C and is PC controlled by National Instruments Lab Windows CVI.



Characterization Test System



Cryogenic Test System



Probing Station



Probing Station

APPENDIX A

HP 4192A LF IMPEDANCE ANALYZER

The HP4192A LCR characterization system, which collects data such as capacitance, dissipation factor, and ESR, was used to measure DLC, aluminum nitride, ML films, carbon nitride, and other experimental materials. It performs frequency and voltage scans from 5 Hz to 13 MHz, \pm 35VDC bias. The system is PC controlled by National Instruments Lab Windows CVI.



Characterization Test System



Impedance Analyzer

INSULATION RESISTANCE / IV & HV BREAKDOWN TEST SYSTEM

The IR / IV test system & HV breakdown test system collected data on a wide variety of materials such as DLC, aluminum nitride, ML films, carbon nitride and other experimental materials. The Keithley 6517A electrometer measures current from 10pA to 21mA, resistances up to $10e17$ ohms and contains a \pm 1000VDC power supply. The system is PC controlled by National Instruments Lab Windows CVI. The safety interlock system has complete control over the entire operation. A second 6517A electrometer was setup to provide additional testing capabilities.



IR / IV / HV Test System



Safety Interlock System

APPENDIX A

HIGH VOLTAGE BREAKDOWN TEST SYSTEM

The high voltage breakdown system has a Bertan 210-05R, 5KV / 40mA and a Spellman SR6, 30KV / 200mA power supply. The sample measurements are made by a HP 3457A multimeter and a HP 4349A 4-channel high resistance meter which measures from 1pA to 100pA. The system is PC controlled by National Instruments Lab Windows CVI. The safety interlock system has complete control over the entire operation.



High Voltage Breakdown System



HV Power Supplies

CAPACITOR REPETITION RATE TEST SYSTEM

The capacitor repetition rate test system is manually operated with a beta version of data collection software by National Instruments Lab Windows CVI. The system has been modified and is being used as a rep-rate and pulse collection unit to evaluate charge/discharge characteristics of capacitors. It contains a Kepco 150-7M 150V / 7A power supply, a Kepco SN 488-032 IEEE488 controller, and a HP 54503A 500 MHz O-Scope. A new low voltage system was fabricated with the use of experimental capacitors as a charge capacitor in a 555 timer circuit using 5V and 15V.



High Repetition Rate Test System



Rep-Rate Control Console

APPENDIX A

GENERAL LABORATORY IMPROVEMENTS

POWER SEMICONDUCTOR LAB

The power semiconductor lab saw many facility improvements, as well as, routine maintenance. All Windows 98 PC`s were converted to Windows 2000. Due to the increased PC automation and number of researchers using the systems, a local area network was installed to allow the sharing of peripherals and the creation of a database which is routinely backed up for data protection. This database was then transferred daily to a network based PC to allow researchers to access the data from personal office PC`s. All research equipment was maintained and repaired as needed. All lab PC`s were upgraded as needed with antivirus definitions on LAN based machines. A Millipore Super-Q high resistance water system installation was finished in the clean room, allowing access to water with resistances of 19 M-ohm. General facility care was provided by the replacement of light bulbs in the lab and UV blocking amber sleeves in the clean room. The floors were mopped and waxed, and rubber matting placed in high traffic areas for ease of work conditions. Old paint was scrapped from windows and replaced with aluminum foil as needed. General housekeeping was continually performed to allow the passage of fire and safety inspections. With the onset of the new UCI compliance regulations, the entire facility was reorganized to the new standards. This included inventory and control of all test equipment, stock material and hand tools. All test and deposition systems were repaired as needed to allow continued operation.

ADVANCED CAPACITOR RESEARCH & DEVELOPMENT CENTER

The advanced capacitor research & development center saw improvements during the past year. Software packages on lab PC`s were upgraded to enhance operational capabilities, along with antivirus updates on LAN based machines. All Windows 98 PC`s were converted to Windows 2000. A local area networked based database was created to compliment the existing networked based database. With the onset of the new UCI compliance regulations, the entire facility was reorganized to the new standards. This included inventory and control of all test equipment, stock material and hand tools. All test and deposition systems were repaired as needed to allow continued operation

OTHER SUPPORT PROVIDED

The laboratory has tested DLC, PCD, aluminum nitride, ML films, carbon nitride, and many generic samples from various sources outside the lab in support of Air Force SBIR`s, etc. Technical and engineering support was continually supplied to the research efforts of DLC, PCD, aluminum nitride, carbon nitrite, and polymers. Delivery of compressed gas cylinders & LN₂ was provided to the branch. Support was also provided to the High Power Lab in Bldg. 450 for high current pulse injection testing. Forklift and crane support was provided for the branch as requested. On an existing 1.25kW microwave system, an induction stage heater was replaced with a resistive type heater. An existing power supply was modified to provide proper power requirements. A new resistive load bank was built for the testing of the DC-DC converter. The load bank

APPENDIX A

consisted of (10) 80ohm resistors that are switched in various parallel configurations with MOSFET's. The system also contains a fan cooling system and is mounted with casters for ease of maneuvering.



DC-DC Converter Load Bank

APPENDIX B

CONFERENCES AND ABSTRACTS FOR SUBMITTED PAPERS

Conference: 3rd international Energy Conversion Engineering Conference, 13-18 August 2005, San Francisco, California.

Title: "Temperature and Thickness Dependence of Ti/AlNi/W and Ti/Ni₂Si/W Ohmic Contacts to P-Type SiC"

Authors: Bang-Hung Tsao and Jacob Lawson (UDRI)
James Scofield (AFRL/PRPE)

Abstract: AlNi and Ni₂Si based ohmic contacts to p-type 4H-SiC have been produced using low energy ion implantation, the addition of a thin Ti layer, and a novel two-step implant activation anneal process. Resistivities in the reported range were achieved by degenerately ($>10^{20} \text{ cm}^{-3}$) doping the surface region of p-type 4H-SiC epilayers via low energy Al⁺ implantation. A high acceptor activation was promoted by annealing the samples with a two-step sequence in an Ar atmosphere, first at 1400°C and then at 1700°C for 15 minutes at each temperature level. It was also discovered that SiC surface morphologies could be significantly improved by capping implanted samples with pyrolyzed graphite during the activation anneals. AFM results indicated the average surface roughness was significantly reduced, by up to 5X, with these caps compared to samples without the protective layer. For the AlNi based samples, specific contact resistivities as low as $5.5 \times 10^{-5} \text{ ohm-cm}^2$ were reliably and repeatedly achieved after annealing at temperatures of 700-1000°C for 2 minutes in a high purity argon atmosphere. For the Ni₂Si samples, resistivities as low $4.5 \times 10^{-4} \text{ ohm-cm}^2$ were reached after annealing between 750 and 1100°C. I-V curves collected between heating cycles confirm these results and show a more linear ohmic profile with increasing anneal temperature. Additionally, SEM and optical microscopy show microstructure evolution with anneal temperature. The effect of Ti thickness and anneal temperature of Ti/AlNi/W and Ti/Ni₂Si/W stacks on implanted layers were compared and are reported. The specific resistivities and annealing temperatures of AlNi based ohmic contacts were found to be consistently lower than those of the Ni₂Si based system.

APPENDIX B

Conference: Intl Conference on Silicon Carbide and Related Materials 2005, September 18-23, 2005, Pittsburgh

Title: "Ti/AlNi/W and Ti/Ni₂Si/W Ohmic Contacts to P-Type SiC"

Authors: Bang-Hung Tsao and Jacob Lawson (UDRI)
James Scofield (AFRL/PRPE)

Abstract: AlNi and Ni₂Si based ohmic contacts to p-type 4H-SiC have been produced using low energy ion implantation, a Ti contact layer, and sequential anneals. Low resistivities were promoted by degenerately ($>10^{20}$ cm⁻³) doping the surface region of 4H-SiC epilayers via low energy Al⁺ implantation. High acceptor activation and improved surface morphology was achieved by capping the samples with pyrolyzed photoresist and a two-step anneal sequence in argon. Ti/AlNi/W and Ti/Ni₂Si/W stacks of varying Ti and/or binary layer thickness were compared at different anneal temperatures. For this set of AlNi based samples, specific contact resistivities as low as 5.5×10^{-5} ohm-cm² were reliably and repeatedly achieved after annealing at temperatures of 700-1000°C for 2 minutes in a high purity argon atmosphere. For the Ni₂Si samples, resistivities as low 4.5×10^{-4} ohm-cm² were reached after annealing between 750 and 1100°C. Similarly, a set of Ti/AlNi/Au samples, with or without Ge as an additional contact layer, were prepared via the same procedure as those above. In this case specific contact resistivities as low as 5.0×10^{-4} ohm-cm² were achieved after annealing the Ti/AlNi/Au samples between 600 and 700°C for 30 minutes in a dynamic argon atmosphere or under high vacuum. In all cases, the lowest resistivities were realized using thicker (~ 40 nm) Ti layers. I-V analysis revealed superior linear characteristics for the AlNi system, which also exhibited a more stable microstructure after anneal. SEM and optical microscopy illustrated microstructure evolution with temperature. SIMS and RBS were used to analyze the stability of the stacks subsequent to thermal treatment. AFM analysis demonstrated the superiority of photoresist capping over alternatives in minimizing surface roughness. Linear ohmic behavior after significantly reduced anneal temperature is the main observation of the present study.

APPENDIX B

Conference: Intl Conference on Silicon Carbide and Related Materials 2005, September 18-23, 2005, Pittsburgh, Pennsylvania.

Title: "Accurate SIMS Aluminum Dopant Profiling in SiC"

Authors: Howard E. Smith and Bang-Hung Tsao (UDRI)
James Scofield (AFRL/PRPE)

Abstract: The accuracy of Secondary Ion Mass Spectrometry (SIMS) depth profiles of aluminum (Al) dopant in silicon carbide (SiC) has been investigated. The Al SIMS profile differs in apparent shape depending on whether it was obtained using a cesium or oxygen primary ion SIMS beam, and depends in the former case on which secondary ion is followed. The cesium-beam "matrix signals" indicate that the secondary ion signal yields change over the course of the Cs⁺ depth profile, perhaps because of the work-function lowering due to the previously-implanted aluminum. These same matrix ion signals are used for a depth-dependent empirical correction to increase the accuracy of the Al concentration profile. The physics of these phenomena and the accuracy of the correction are discussed.

APPENDIX B

Conference: *IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2006)*

Title: “Thermal Aging of Ti/AlNi/Au Ohmic Contacts to P-Type SiC”

Authors: Bang-Hung Tsao and Jacob Lawson (UDRI)
James Scofield (AFRL/PRPE)

Abstract: *Improved AlNi-based ohmic contacts to p-type 4H-SiC have been achieved using low energy ion (Al^+) implantation, the addition of a thin Ti layer, and a novel two-step implant activation anneal process. Resistivities of $5 \times 10^{-5} \Omega\text{-cm}^2$ were reached by doping the surface region of p-doped 4H-SiC epilayers via low energy Al^+ implantation. Acceptor activation was achieved by annealing the samples with a 1400+1700 °C two-step sequence in an Ar atmosphere, which also yielded improved surface morphology when implanted samples were capped with pyrolyzed photoresist during the anneals. AFM average roughness values improved by over 5X compared to samples without capping. The metallurgical morphology and contact resistivity remained intact even after annealing at 1100 °C, indicating good thermal stability. The Ti/AlNi/W contacts on implanted layers were compared to Ni_2Si intermetallics and were found to be comparable to or superior in terms of specific contact resistivity, uniformity, and thermal stability. Ti/AlNi/Au contacts were studied which resulted in contact resistivities in the $1.8 \times 10^{-4} \Omega\text{-cm}^2$ range. Even though these values are 5X higher than those of the Ti/AlNi/W system, the reduced anneal temperature (650 °C) implies that Ti/AlNi/Au is a promising stacking configuration. Benefits of a longer 30-minute anneal at 600–700 °C, in either vacuum or Ar ambient was observed. Namely, the 2 minute annealing cycle used for the Ti/AlNi/W and Ti/ Ni_2Si /W study resulted in higher anneal temperatures before ohmic characteristics were seen. This same anneal time was not sufficient for the Ti/AlNi/Au samples, whereas increasing the cycle time to 30 minutes resulted in ohmic behavior at a much lower temperature. Increasing the anneal time however, had little impact on reducing the required anneal temperature of the Ti/AlNi/W and Ti/ Ni_2Si /W samples when the experiments were repeated. The contact resistivities of Ti/AlNi/Au after thermal aging up to 350 °C were steady.*

APPENDIX B

Conference: *2006 MRS Spring Meeting, April 16-24, San Francisco*

Title: "Ti/AlNi/W Ohmic Contacts to P-Type SiC"

Authors: Bang-Hung Tsao and Jacob Lawson (UDRI)
James Scofield (AFRL/PRPE)

Abstract: Improved AlNi-based ohmic contacts to p-type 4H-SiC have been achieved using low energy ion (Al^+) implantation, the addition of a thin Ti layer, and a novel two-step implant activation anneal process. Resistivities sometimes as low as $5 \times 10^{-5} \Omega\text{-cm}^2$ were reached by doping the surface region of lightly p-doped 4H-SiC epilayers via low energy Al^+ implantation. Acceptor activation was achieved by annealing the samples with a 1400+1700°C two-step sequence in an Ar atmosphere, which also yielded improved surface morphology when implanted samples were capped with photo resist during the anneals. In this study, Ti/AlNi/W contacts on implanted layers were compared to Ti/AlNi/Au contacts. Even though the resistivities are higher than those of the Ti/AlNi/W system, the reduced anneal temperature, 650°C for Ti/AlNi/Au compared to 950°C for Ti/AlNi/W implies that Ti/AlNi/Au is a promising stacking configuration. Furthermore, the effects of a longer 30 minute anneal time at 600 – 700°C, in atmospheric pressure Ar ambients was observed. Namely, the 2 minute annealing cycle used for the Ti/AlNi/W study resulted in higher anneal temperatures before ohmic characteristics were seen. This same anneal time was not sufficient for the Ti/AlNi/Au samples, whereas increasing the cycle time to 30 minutes resulted in ohmic behavior at a much lower temperature. Increasing the anneal time however, had little or no impact on reducing the required anneal temperature of the Ti/AlNi/W.