DC and RF Characterization of Laser Annealed Metal-Gate SOI CMOS Field-Effect Transistors

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ADMINISTRATIVE INFORMATION

The work described in this report was performed for the Office of Naval Research Internal Applied Research (IAR) Program by the Electromagnetics & Advanced Technology Division (Code 2853) of SPAWAR Systems Center San Diego (SSC San Diego).

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S. D. Russell, Head
Electromagnetics & Advanced Technology Division

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DC and RF Characterization of Laser Annealed Metal-Gate SOI CMOS Field-Effect Transistors

Ryan P. Lu, Bruce W. Offord, Jeremy Popp, Ayax D. Ramirez, Jason Rowland, Stephen D. Russell

Space and Naval Warfare Systems Center
San Diego

American Physical Society
21–25 March 2005, Los Angeles, CA
Abstract

The conventional polysilicon gate in a MOSFET has been replaced by an aluminum metal gate which offers higher RF performance through the reduction of gate resistance. Pulsed excimer laser annealing of the source and drain was then used to avoid conventional furnace annealing that would melt the aluminum metal gate. CMOS field-effect transistors utilizing metal gates were fabricated in Silicon-on-Insulator (SOI) technology down to 0.25-micron gate lengths. The DC characteristics of devices with 10-micron gate lengths were consistently well-behaved. The 0.25-micron devices were found to be more sensitive to the laser energy that showed up in the DC measurements in threshold voltage variations and larger leakage currents in the subthreshold characteristics. At higher laser fluences, Technology Computer-Aided Design (TCAD) simulations show excessive lateral diffusion, explaining the observed effects. RF results of the drawn 0.25-micron metal-gate devices have an $F_t$ and $F_{\text{max}}$ of 25 GHz and 60 GHz, respectively. Similar devices with polysilicon gates were fabricated and characterized for comparison. RF results of the drawn 0.25-micron polysilicon-gate devices have an $F_t$ and $F_{\text{max}}$ of 34 GHz and 7 GHz, respectively. This device processing advance offers a deeply scalable technology for future “system-on-a-chip” applications.
Why use SOI?

As devices are scaled down in size, MOSFET performance suffers from short channel effects and the parasitic resistances and capacitances become more apparent in RF applications. These parasitics limits the potential to achieve a high cutoff frequency and power gain, $F_t$ and $F_{\text{max}}$, respectively. Silicon-on-insulator technology reduces the short channel effects as well as parasitic junction capacitances for improved microwave frequency figures of merit.
Using Al as the material for the metal gate creates a device that has at least an order of magnitude lower gate resistance than a silicide polygate. Reducing the gate resistance directly improves the RF performance of the device.
Why Use Laser Annealing?

Activation of source/drain impurities via excimer laser annealing is necessary because the high temperatures used in conventional thermal annealing will melt the Al gate. The main disadvantage of laser annealing is the low throughput of wafers, which is an important consideration for manufacturability.

\[ \lambda = 308 \text{ nm XeCl Excimer Laser} \]

Activation of dopants during melt regime, removal of damage caused by implantation, and formation of shallow junctions.
Threshold Voltage Calculation

Threshold Voltage Calculations for nMOS with Short Channel Effects

\[
VT = \Phi_{MS} \frac{Q_{SS}}{C_{OX}} + 2\Phi_r + \frac{qN_d \chi_{dmax}}{C_{OX}}
\]

- \( \Phi_{MS} = 4.33 \) eV
- \( \chi(Si) = 4.05 \) eV
- \( Q_{SS} = 7e11 \) cm\(^{-2}\)
- \( T_{Si} = 700 \) A
- \( T_{ox} = 75 \) A

Doping (cm\(^3\))

Threshold Voltage (V)
MOSFET Fabrication Process

Implant Si to set voltage threshold of MOSFET, grow gate oxide, deposit, etch aluminum gate

Implant arsenic ions to create the source/drain of the transistor
Laser Annealing Process

Expose wafer to Laser energy to activate implanted arsenic to define source/drain regions.

Deposit oxide, pattern, etch contacts and metal interconnect, end product.
Laser Annealing System

- Pressure Sensor
- CCD Camera
- Beam Homogenizer
- Diode Laser
- 6" Wafer Vacuum Chamber
- Height Adjust Stage
- To Turbo Pump
- 6 x 8mm
### Laser Parameters

<table>
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- Ion Implanted with As at a dose of $5 \times 10^{15}$/cm² @ 30 KeV
- SIMS Analysis Performed to determine carrier concentration
SIMS Analysis

Redistribution of dopants

Unaltered sample

Si (raw ion counts) ->

As

No Laser Anneal

Counts Per Second

Concentration (atoms/cm^3)

Depth (angstroms)

Laser Annealed 350 mJ/cm^2
SEM Images

- 0.25-micron drawn gate length.
- 0.40-micron actual gate length.

Lithography and PVD Gate metal etch process needs optimization.
### Summary of Device Transfer Characteristics

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<tr>
<th>Energy</th>
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Rapid Thermal Processing (RTP) simulation using integrated systems engineering (ISE) DIOS (a multidimensional process simulator for semiconductor devices) shows noticeable As dopant diffusion under the gate for a 0.1-sec RTP, which can explain shorting of submicron devices. However, laser pulse length are several magnitudes smaller (20 to 30 ns) where the source/drain profile is better represented by Figure (a).
Metal-Gate Device Transfer Characteristics

Vgs vs Ids

\[ \text{Current, Ids (Amps)} \]
\[ \text{Voltage, Vgs (Volts)} \]

- \( L_g = 0.25 \) microns
- \( W_g = 20 \) microns
- 7 fingers

(Vd=0.00)  
(Vd=0.50)  
(Vd=1.00)  
(Vd=1.50)  
(Vd=2.00)  
(Vd=2.50)
Polygate Device Transfer Characteristics

Vgs vs Ids

Current, Ids (Amps)
-0.5 0 0.5 1 1.5 2
Voltage, Vgs (Volts)
1.0E-01
1.0E-02
1.0E-03
1.0E-04
Lg = 0.25 microns
Wg = 20 microns
7 fingers

(Vd=0.00)
(Vd=0.50)
(Vd=1.00)
(Vd=1.50)
(Vd=2.00)
(Vd=2.50)
Metal-Gate Device Transconductance

Vgs vs gm

Transconductance, gm

Voltage, Vgs (Volts)
Polygate Device Transconductance

Vgs vs gm

Voltage, Vgs (Volts)

Transconductance, gm (Siemens)

(Vd=0.00)  
(Vd=0.50)  
(Vd=1.00)  
(Vd=1.50)  
(Vd=2.00)  
(Vd=2.50)
Metal-Gate Device Output Characteristics

Vds vs Ids

- Voltage, Vds (Amps)
- Current, Ids (Amps)

(Vg=0.00)
(Vg=0.20)
(Vg=0.40)
(Vg=0.60)
(Vg=0.80)
(Vg=1.00)
(Vg=1.20)
(Vg=1.40)
(Vg=1.60)
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(Vg=2.00)
Polygate Device Output Characteristics

Vds vs Ids

Voltage, Vds (Volts)

Current, Ids (Amps)

(Vg=0.00)
(Vg=0.20)
(Vg=0.40)
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(Vg=1.20)
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(Vg=1.60)
(Vg=1.80)
(Vg=2.00)
**RF Figures of Merit**

**Unity Current Gain Frequency**

\[ f_t = \frac{g_m}{2\pi \left( C_{gs} + C_{gd} + C_{gb} \right)} \]

**Unity Power Gain Frequency**

\[ f_{\text{max}} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd}} + g_{ds} \left[ R_g + R_s \right]} \]

**Minimum Noise**

\[ F_{\text{min}} = 1 + k \frac{f}{f_t} \sqrt{g_m \left[ R_s + R_g \right]} \]
RF Characterization of Metal-Gate Device

--- 10 dB/decade slope

h21

MAG/MSG

Frequency (Hz)

dB

1.0E+08 1.0E+09 1.0E+10 1.0E+11

1.0E+09 1.0E+10 1.0E+11

1.0E+08 1.0E+09 1.0E+10 1.0E+11
RF Characterization of Polysilicon Gate Device

- 20
- 10
0
10
20
30
40
50
60
1.E+08 1.E+09 1.E+10 1.E+11

Frequency (Hz)

- 10 dB/decade slope

h21
MAG/MSG
Conclusions

1. Performed DC and RF characterization of laser annealed MOS SOI devices with Ti/TiN/Al gate.
2. DC device characteristics were found to be relatively independent of laser fluence.
3. Device shorting occurs for 0.25-micron drawn gate length devices.
4. ISE DIOS Process simulation indicates laser-induced Source/Drain shorting is not possible for 0.25-micron devices due to nanosecond laser pulses. Further studies need to be conducted to explain the low yield of submicron devices.
5. nMOS devices exhibit $I_d$ values of over 50 mA, $F_t$ values of over 25 GHz, and $F_{max}$ values of 60 GHz.
DC AND RF CHARACTERIZATION OF LASER ANNEALED METAL-GATE SOI CMOS FIELD-EFFECT TRANSISTORS

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