

HPEC 2004

Title: Processing Challenges in Shrinking HPEC Systems into Small UAVs
First & Presenting Author: Dr. Stephen Pearce
Mercury Computer Systems, Inc.
199 Riverneck Road, Chelmsford, MA 01824
978-967-1384/ FAX 978-256-0588; spearce@mc.com
Citizenship: United Kingdom
Second Author: Richard Jaenicke
Mercury Computer Systems, Inc.
199 Riverneck Road, Chelmsford, MA 01824
978-967-1727 FAX 978-256-0852; rjaenicke@mc.com
Citizenship: USA
Format: Poster
Areas: Future Program Office Needs for Embedded Computing Technologies
Embedded Computing for Global Sensors and Information Dominance
Case Study Examples of High Performance Embedded Computing

The best-known unmanned aerial vehicles (UAVs), Predator and Global Hawk, are large, multi-million dollar aircraft managed as theater/national assets. With synthetic aperture radar (SAR), electro-optic/infrared (EO/IR), and signals intelligence (SIGINT) payloads, these UAVs have proven their worth in battlefields from Bosnia to Afghanistan and Iraq. This success has led to surge in proposed UAV missions and designs using a layered approach with multiple classes of UAVs to provide persistent narrow and wide ISR (intelligence, surveillance, reconnaissance) coverage. Programs such as the Future Combat System (FCS) include a large role for tactical UAVs, small UAVs, and unmanned ground vehicles (UGVs). The smaller, cheaper unmanned vehicles can be deployed at the brigade or company level to “see over the next hill.” With many vehicles and many sensors, network bandwidth becomes an issue. So future UAVs will include aided/automatic target recognition (AiTR/ATR) capabilities to reduce both communication bandwidth and latency.

Large UAVs such as Global Hawk and Predator have been successful using today’s HPEC solutions. Global Hawk currently uses a 9U VME system with PowerPC processors for SAR and EO/IR processing, while the Predator is a bit smaller, using a 6U VME system for TESAR processing. The challenge is to provide similar processing power for much smaller UAVs, many of which have less than ½ the payload weight and ¼ the volume of the Predator (see examples in Table 1). Note that only a small portion of the payload is allocated for signal and image processing. For example, the TESAR image processor on the Predator is just 55 pounds, less than 1/10 of the total payload weight.

Report Documentation Page

*Form Approved
OMB No. 0704-0188*

Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

1. REPORT DATE 01 FEB 2005	2. REPORT TYPE N/A	3. DATES COVERED -	
4. TITLE AND SUBTITLE Processing Challenges in Shrinking HPEC Systems into Small UAVs		5a. CONTRACT NUMBER	
		5b. GRANT NUMBER	
		5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)		5d. PROJECT NUMBER	
		5e. TASK NUMBER	
		5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Mercury Computer Systems, Inc. 199 Riverneck Road, Chelmsford, MA 01824		8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)	
		11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release, distribution unlimited			
13. SUPPLEMENTARY NOTES See also ADM001742, HPEC-7 Volume 1, Proceedings of the Eighth Annual High Performance Embedded Computing (HPEC) Workshops, 28-30 September 2004. , The original document contains color images.			
14. ABSTRACT			
15. SUBJECT TERMS			
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT
a. REPORT unclassified	b. ABSTRACT unclassified	c. THIS PAGE unclassified	UU
			18. NUMBER OF PAGES 23
			19a. NAME OF RESPONSIBLE PERSON

Table 1: UAV Payloads

UAV	Global Hawk	Predator B	Heron A	Hunter	Eagle Eye	Fire-scout	Sentry	Dragon Warrior	Dragon Eye
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

In the past, we have relied on Moore’s Law to help us out. We could wait a couple of years and the technology improvements in the electronics would have enabled significant shrinking of size. However, we’ve come to a point where Moore’s Law effects still increase absolute performance, but not performance per Watt, per pound, or per cubic foot. Although the number of transistors available is increasing, the power consumption is increasing at almost the same rate (see figure 1). The increased infrastructure to handle the power distribution and heat extraction incurs a penalty in size and weight. Alternative approaches are needed.

One approach is to leverage field-programmable gate arrays (FPGAs) as programmable processors. For some front-end signal and image processing functions, FPGAs have been shown to provide a 10-20 fold performance boost over a PowerPC G4 processor. However, some front-end tasks, like filter weight computation, and most back-end processing still performs much better on a PowerPC processor. Given the higher power consumption of an FPGA, there is a limit on the number of FPGAs that can be used in a system. In trying to fit the most processing power in the smallest space for a given application, the trick is not only trying to find the optimum balance between FPGAs and PowerPCs, but also exactly which model of each chip to choose.

PowerPC Performance/Watt

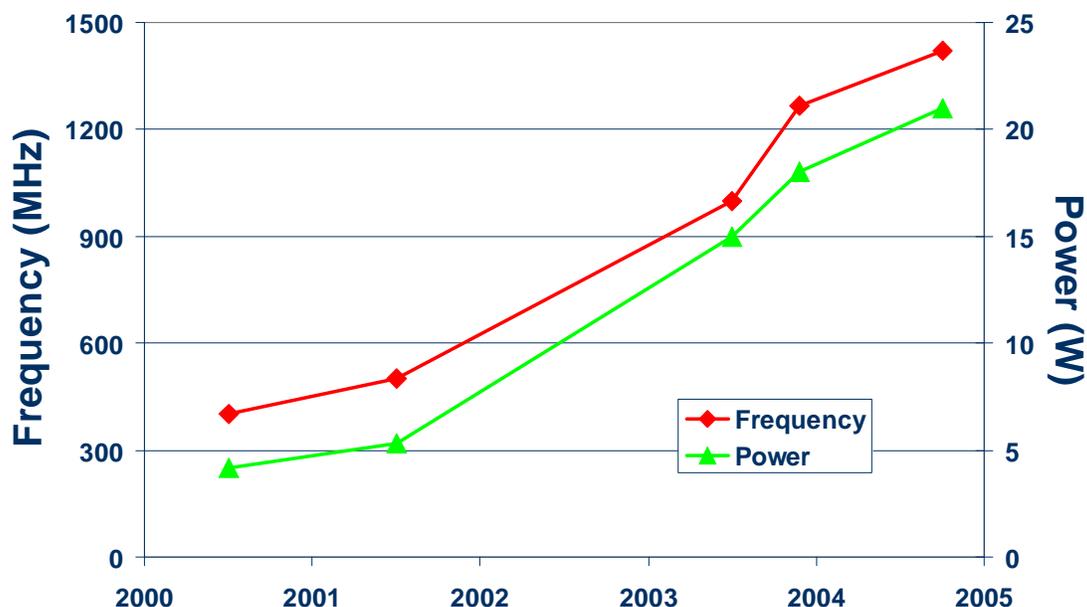


Figure 1: PowerPC frequency and power consumption.

Most evaluations of FPGA chips focus on the number of logic cells, slices, and processor blocks. An example comparison of Xilinx FPGAs is shown in Figure 2. For embedded signal and image processing applications, more critical elements tend to be the number of multiplier blocks and the size of the block RAM. This leads to different component selection, as shown in Figure 3.

The slot limitations on space-constrained systems also lend to integration of the analog-to-digital conversion and general I/O with the processing. This is especially important for multi-channel systems. That sensor I/O can be part of the base-board design along with processors or be a separate mezzanine card. A separate mezzanine card gains board real estate but restricts the power and cooling available to each card.

This presentation will provide a detailed set of trade-offs in computational capabilities, I/O capabilities, and memory capacities distributed between FPGAs and PowerPCs for sample applications of SAR image formation and SIGINT channelized receiver throughout.

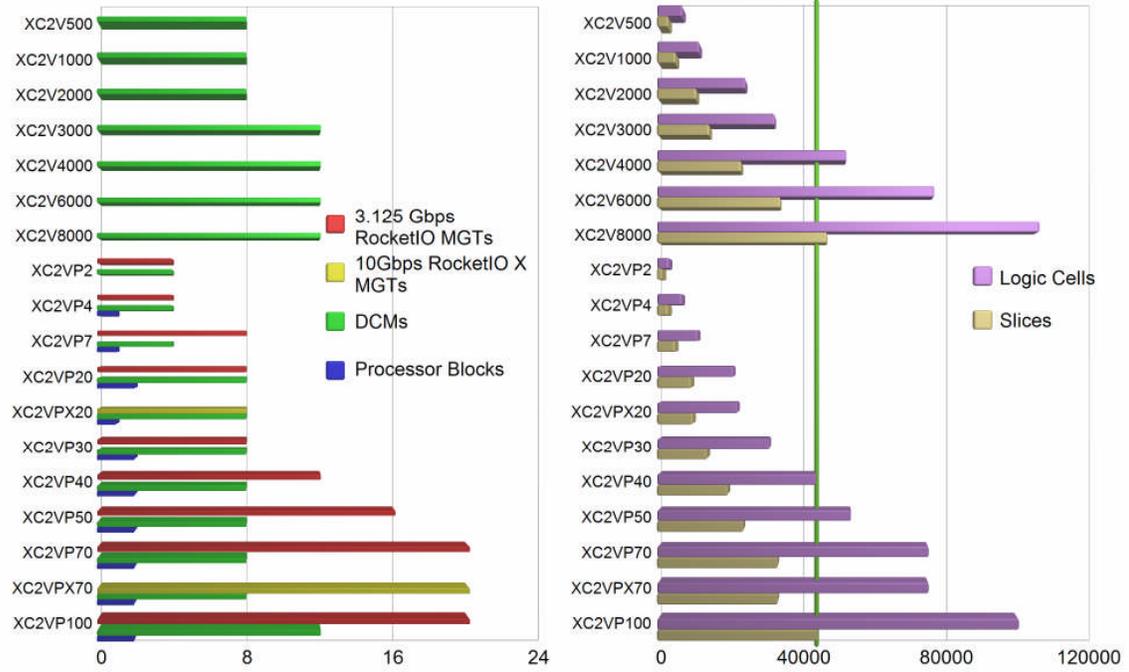


Figure 2: Typical comparison of FPGA attributes.

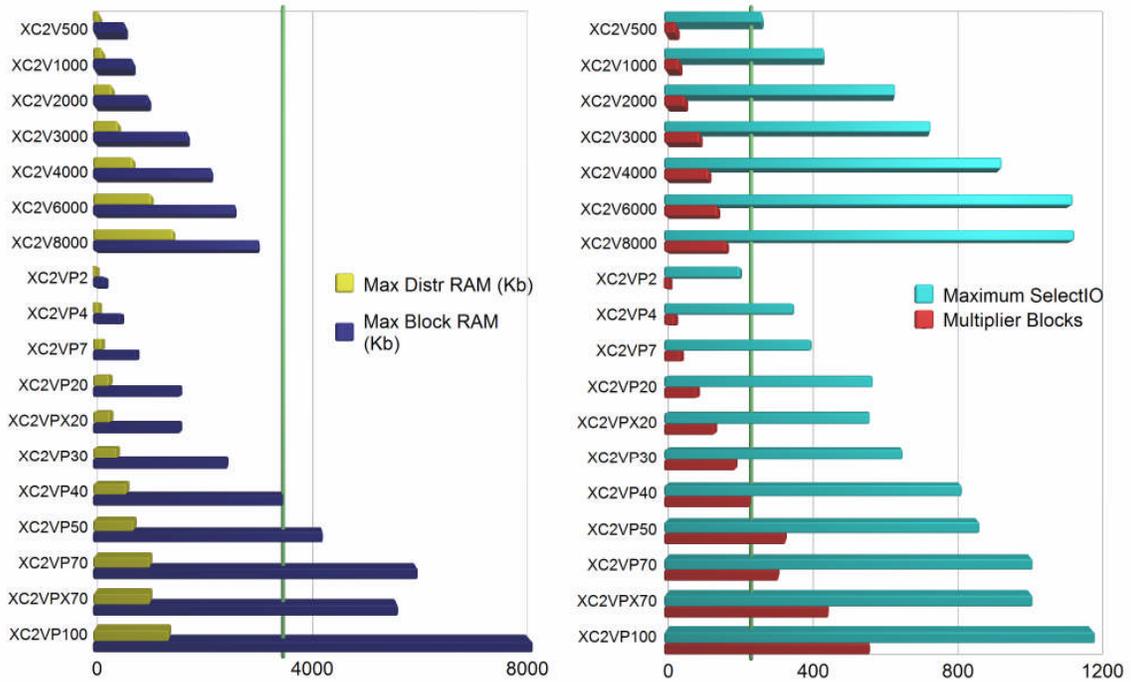


Figure 3: Focusing on RAM and multiplier blocks for FPGA computing.

Processing Challenges in Shrinking HPEC Systems into Small Platforms

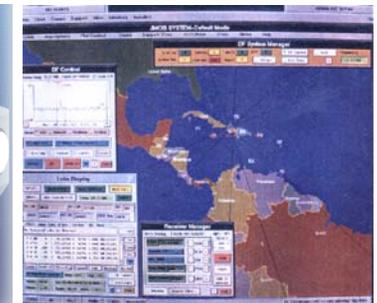
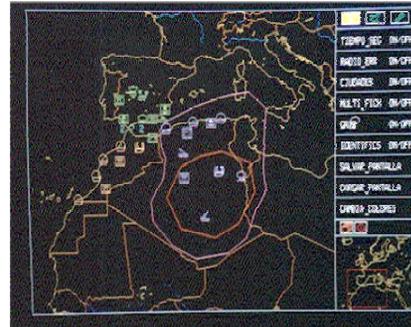
Stephen Pearce & Richard Jaenicke
Mercury Computer Systems, Inc.

High Performance Embedded Computing (HPEC) Conference
September 28, 2004

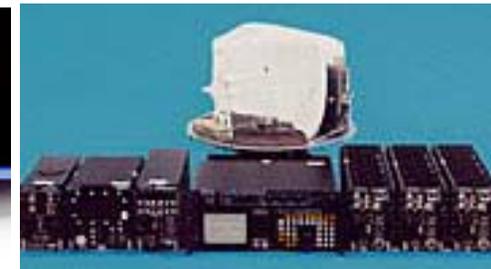
The Ultimate Performance Machine

Target Applications

- **COMINT/ESM**
- **Software Radio**
- **Radar**
- **ELINT/ESM/RWR**
- **EO/IR Imagery**



... and other HPEC challenges, such as ATR, to reduce sensor communication bandwidth/latency needs

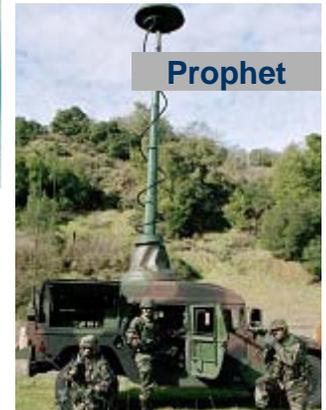


Target Platform Types

- UAVs
- Helicopters
- Man-pack/Briefcase
- Small Vehicle
 - ◆ e.g., Humvee
- Manned aircraft
 - ◆ e.g., ARC-210 radio
- Airborne Pods



SH60



Prophet



JSF



F-18 (POD)



F-16



RAPTOR



Gripen



Litening Pod

Platforms with SWAP Constraints - UAVs

UAV	Global Hawk	Predator B	Heron A	Hunter	Eagle Eye	Fire-Scout	Sentry	Dragon Warrior	Dragon Eye
Picture									
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

- UAVs height is very small; tends to lead to smaller system designs than 6U arrayed on base of fuselage/wings
- Payload weight is small, thus weight constrained solutions are demanded

- UAVs tend to fly fairly high. A consequence is that without life support environments (no man) at this altitude, conduction cooled becomes mandatory.
- All traditional HPEC applications are represented on all the platforms.

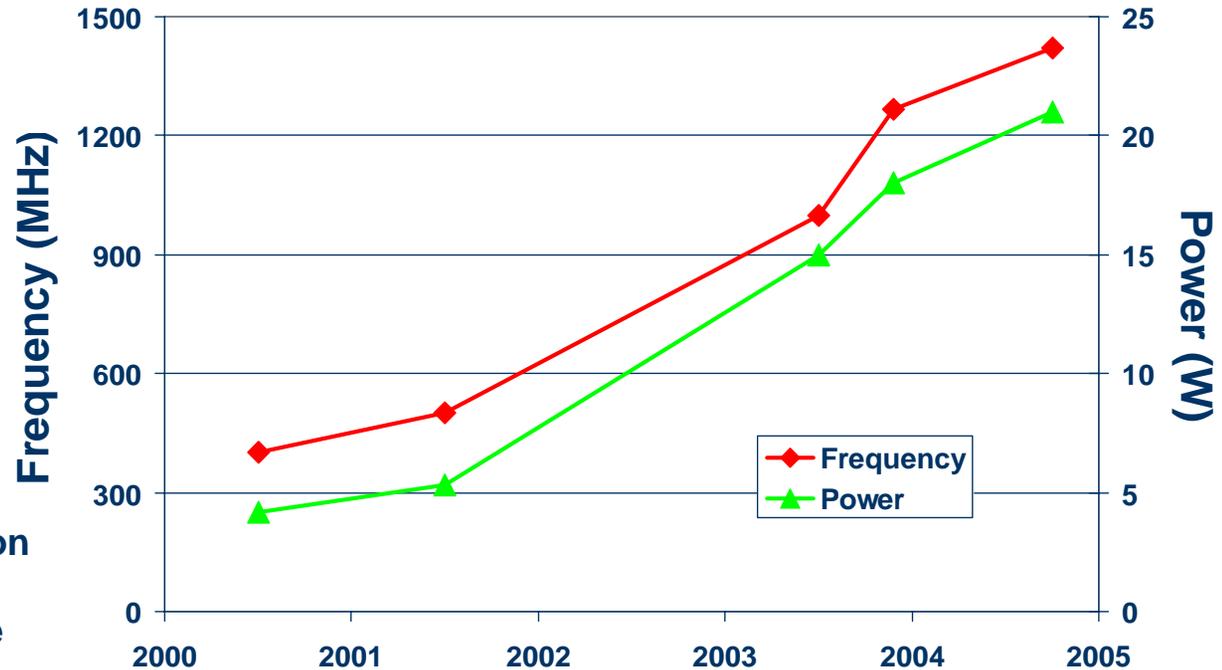
PowerPC Performance/Watt History

Historically, have relied on Moore's Law. Could wait and technology improvements would enable significant miniaturization. However, we observed increases in absolute performance are accompanied by increases in power, and by consequence weight and volume.

Number of transistors available is increasing, but power consumption is increasing at almost same rate. Increased infrastructure to handle power distribution and heat extraction incurs a penalty in size and weight. Alternative approaches are needed.

One approach: leverage field-programmable gate arrays (FPGAs) as programmable processors.

PowerPC Performance/Watt

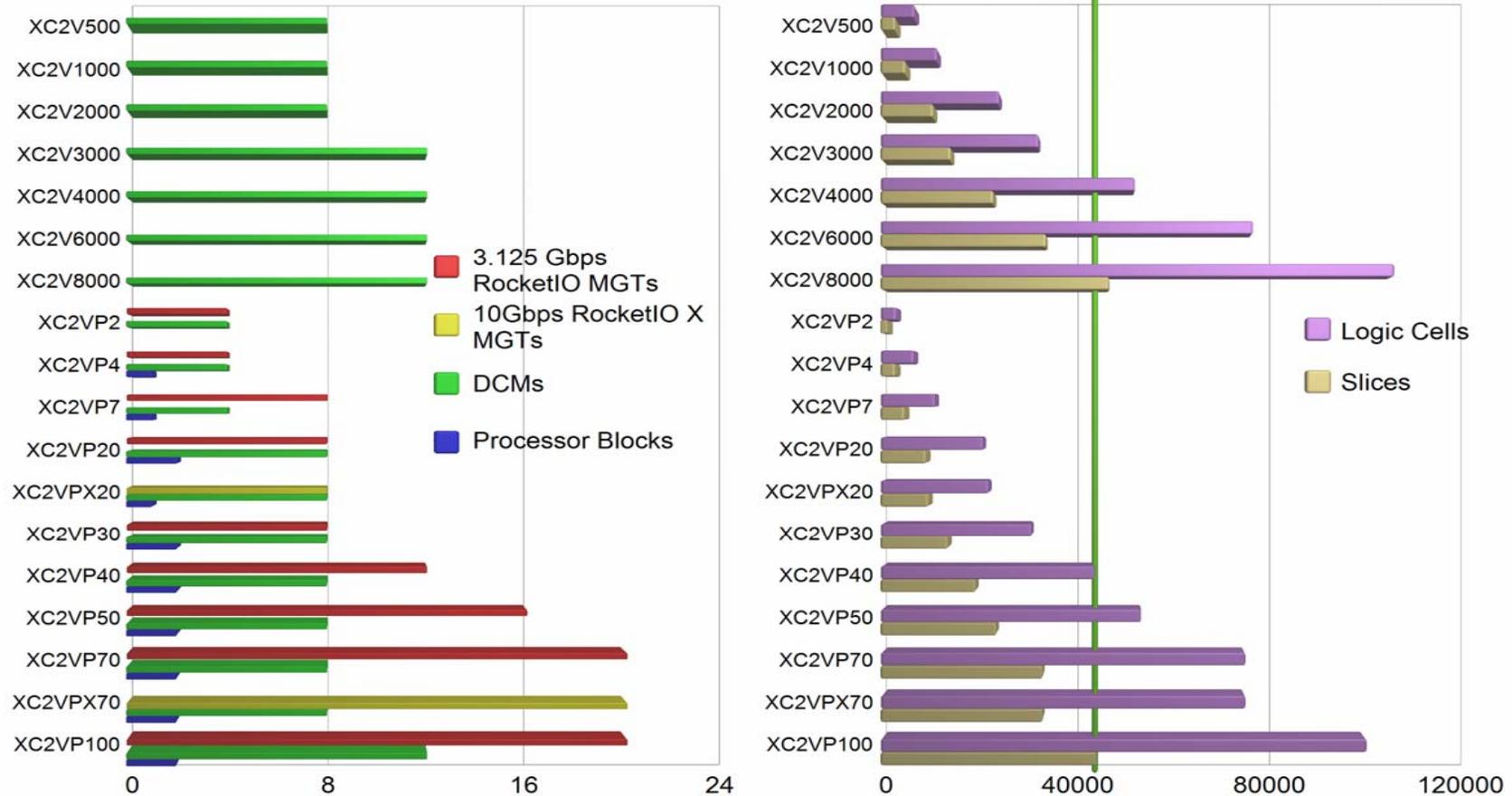


For some signal/image processing functions, FPGAs shown to provide a 10-20 fold performance boost over a PowerPC G4 processor. However, some tasks, e.g. filter weight computation, back-end processing, still perform better on a PowerPC.

In trying to maximize processing power in smallest space, trick is not only trying to find optimum balance between FPGAs and PowerPCs, but also exactly which model of each chip to choose.

FPGA Selection

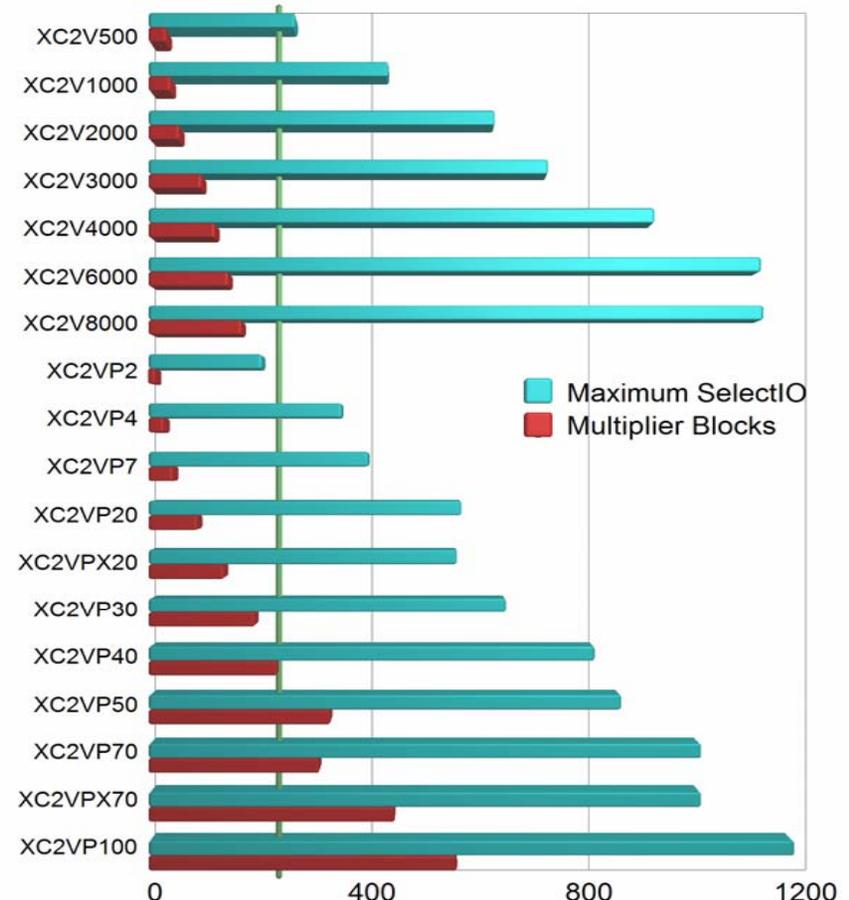
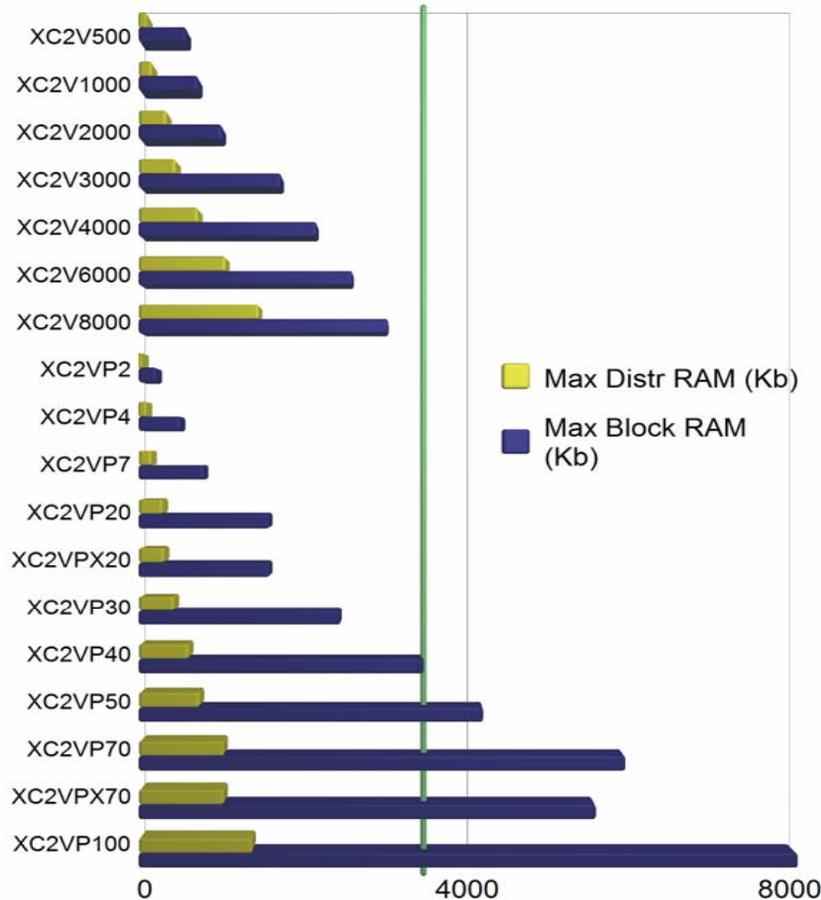
- The popular comparison....



- These are the resources most often receiving attention when people look at Xilinx parts

FPGA Selection

-But what really matters



- For embedded signal/image processing applications, more critical elements tend to be number of multiplier blocks and block RAM size
- Leads to different component selection favoring Pro range

Scaling the Processing

500 MHz class PPC x 4
 = 16 GFLOPS per slot =>

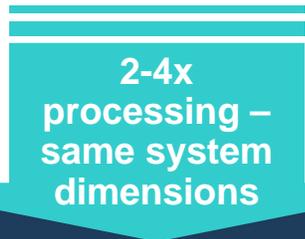
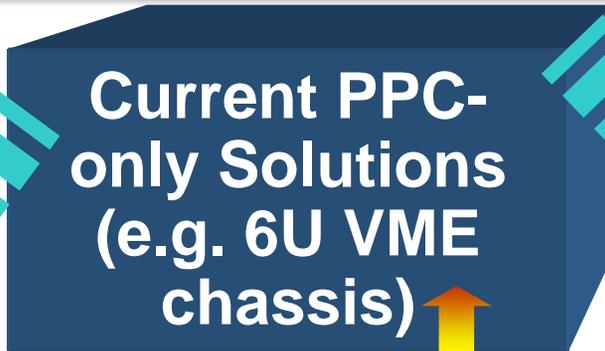
- ♦ 6 slot=96 GFLOPS
- ♦ 12 slot=192 GFLOPS
- ♦ 20 slot=320 GFLOPS

Assumptions

- ♦ FPGA= Equivalent 40-100 GFLOPS
- ♦ 500 MHz PPC=4 GFLOPS



Similar Processing –
 smaller system



2-10x processing – same system dimensions



- 2x 1GHz class PPC per board or 2 FPGA per board=>

- ♦ 2 slot=96-216 GFLOPS
- ♦ 4 slot=112-616 GFLOPS
- ♦ 8 slot=224-1232 GFLOPS

- => Future FPGA + PPC exploitation on 3U better than existing 6U

4x 1.5 GHz class PPC = 48 GFLOPS per slot =>

- ♦ 6 slot=288 GFLOPS
- ♦ 12 slot=576 GFLOPS
- ♦ 20 slot=960 GFLOPS

- => PPC exploitation of VITA 46

- 4x 1 GHz class PPC per board or 2 FPGA per board=>

- ♦ 6 slot=192-1032 GFLOPS
- ♦ 12 slot=384-2232 GFLOPS
- ♦ 20 slot=640-3832 GFLOPS

- =>FPGA + PPC exploitation on VME

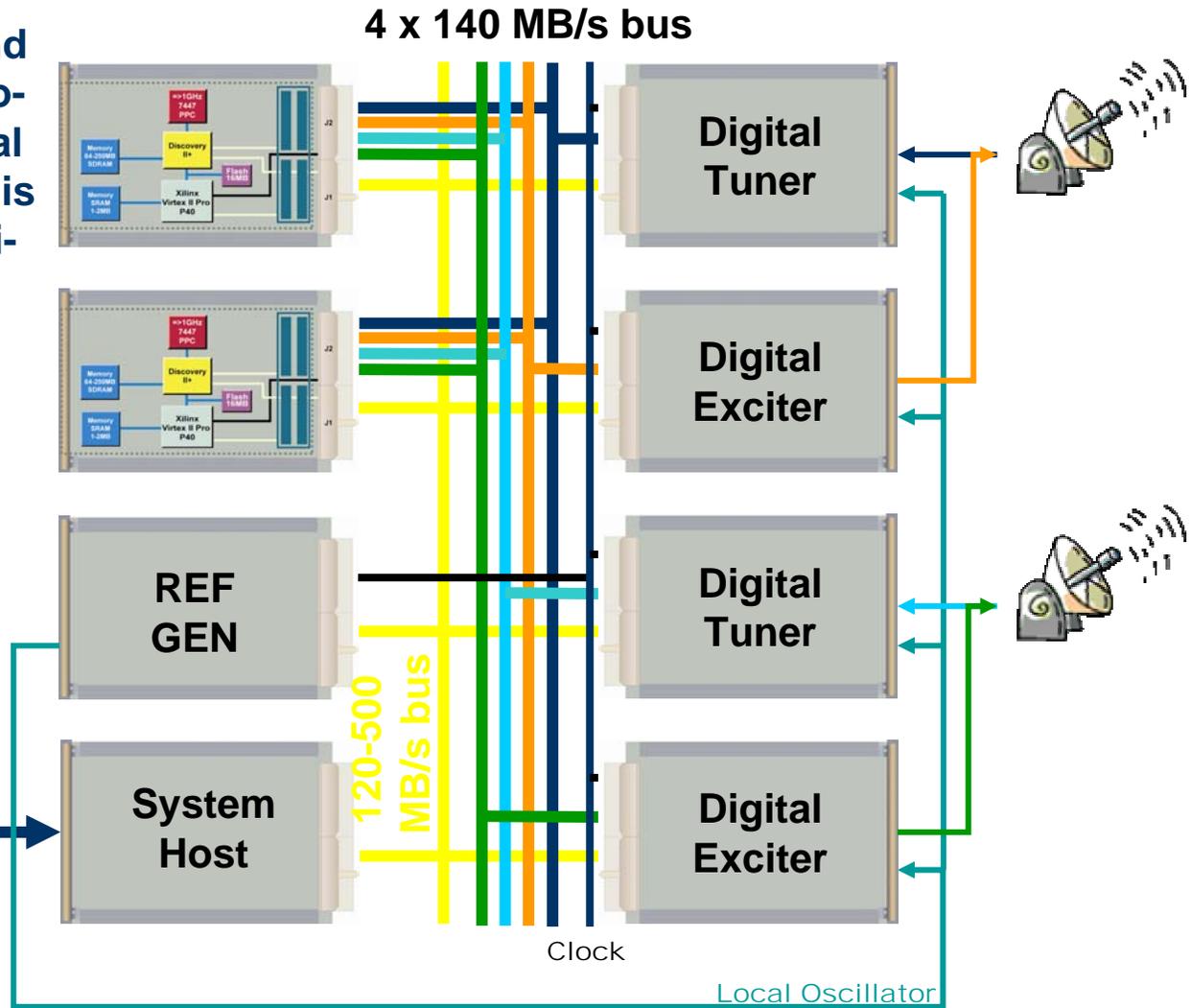
2-Channel Software Radio

Slot limitations on space-constrained systems also lend to integration of the analog-to-digital conversion and general I/O with the processing. This is especially important for multi-channel systems.

User Display

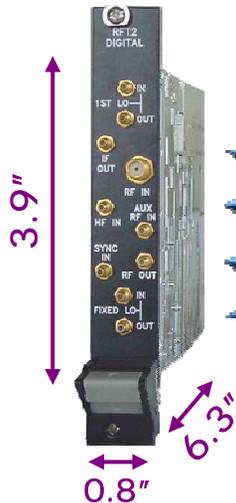
Sensor I/O can be part of base-board design, e.g. tuner/ADC or be a mezzanine card attached to processors.

Ethernet /VGA



SDR Example Mapped to Enclosure

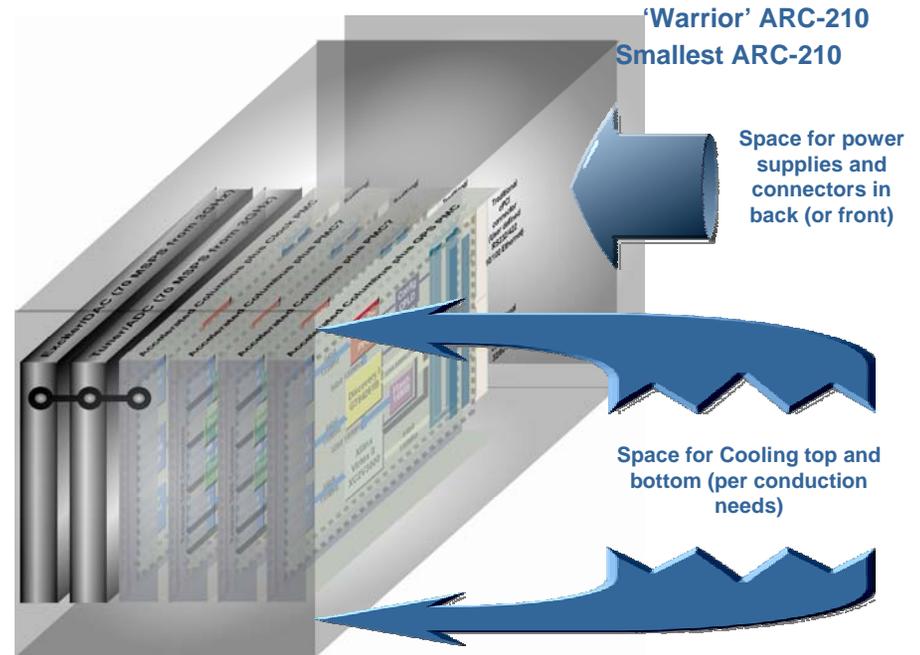
- Example ARC-210 Form



Fitting 6 x 3U cPCI slots leaves total remaining space of

- ◆ Width 1" (20%)
- ◆ Height 1.7" (>30%)
- ◆ Length 6.3" (>35%)

- MCP3 FCN + DRTi Analogue
 - ◆ dimensions to scale



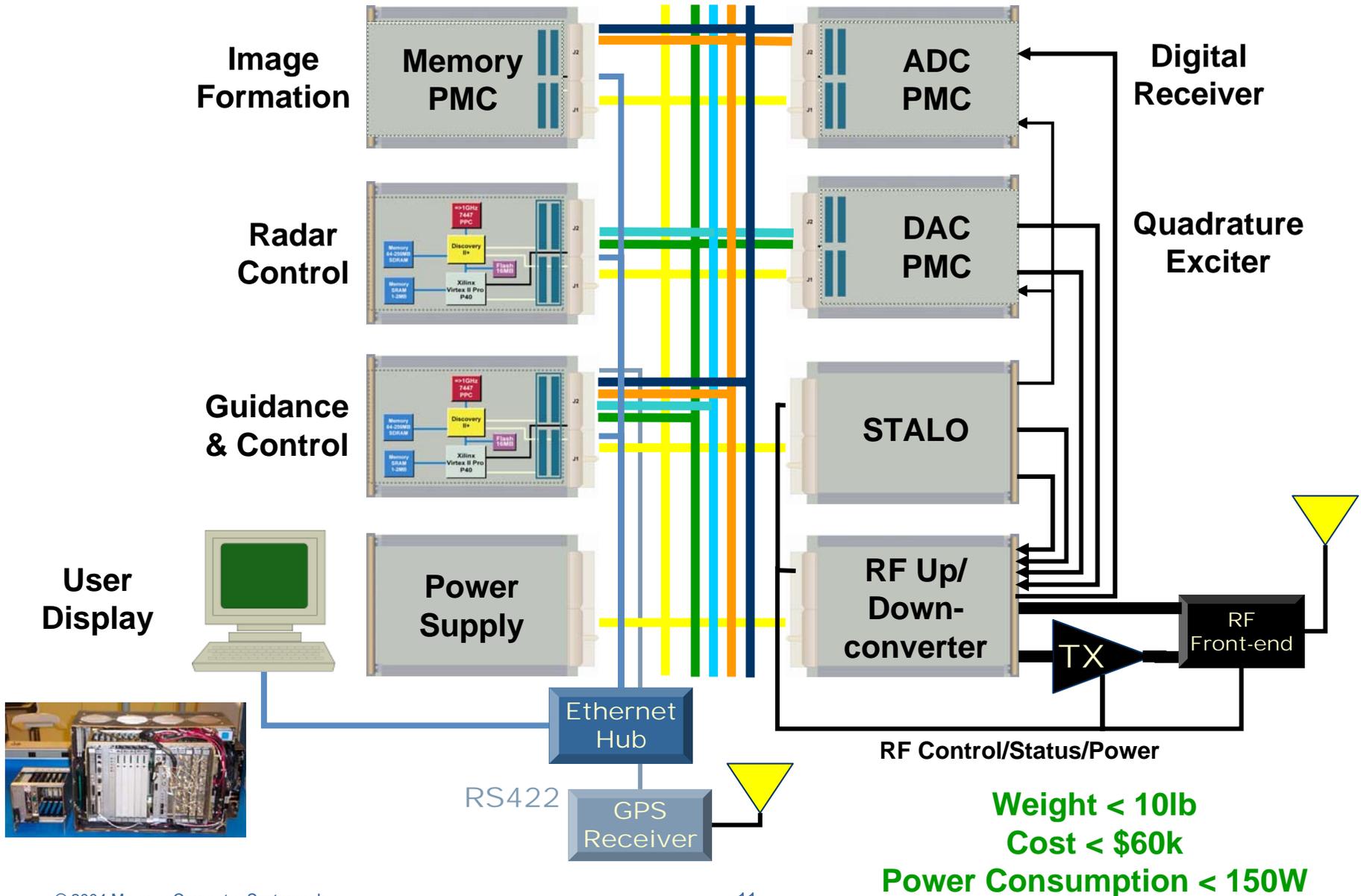
- RF

- ◆ 1 channel at 70 MSPS 14 bit input from 3GHz operating band
- ◆ 1 channel at 70 MSPS 14 bit output to 3 GHz operating band +20dBm

- Digital = ~80-240 GFLOPs

- ◆ 4 x 1 GHz PPCs
- ◆ =~ 40 GFLOPs
- ◆ 4 x Virtex II P40 FPGAs
- ◆ =~ 40-200 GFLOP equivalent

Small SAR

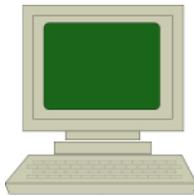


4-Channel Spatial Discrimination

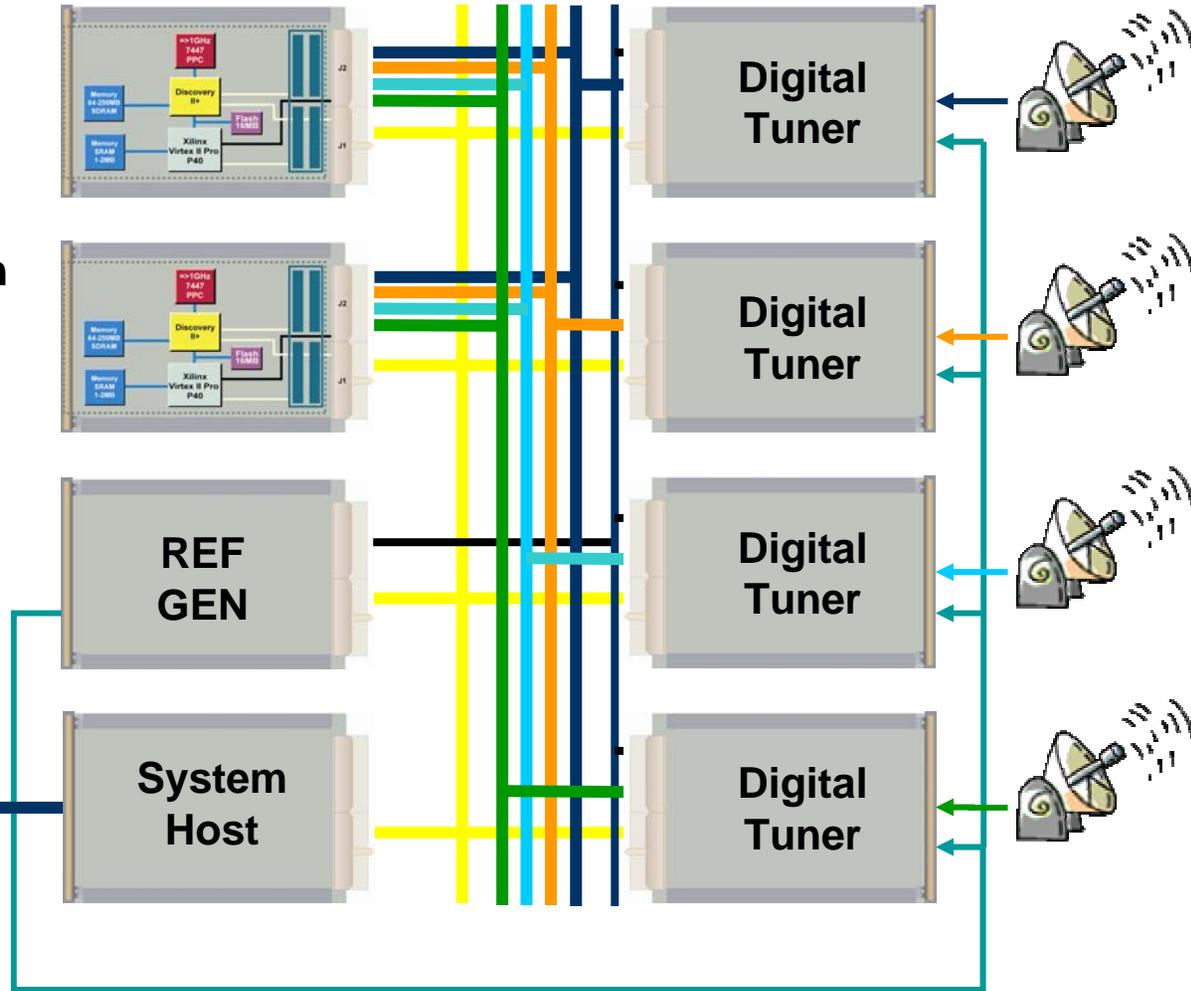
Beamformer/DF

- ◆ COMINT
- ◆ ESM
- ◆ ELINT
 - If down-conversion added

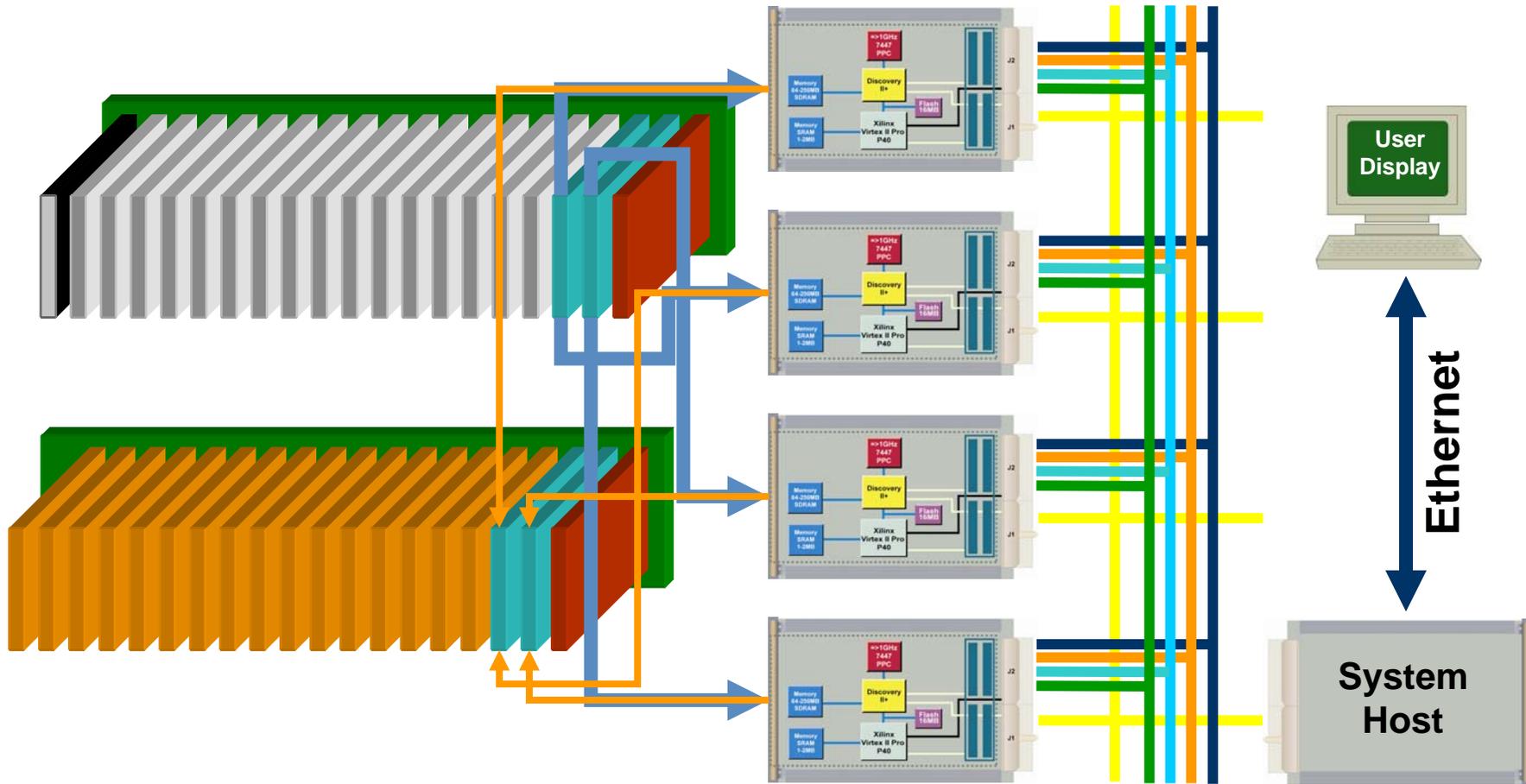
User Display



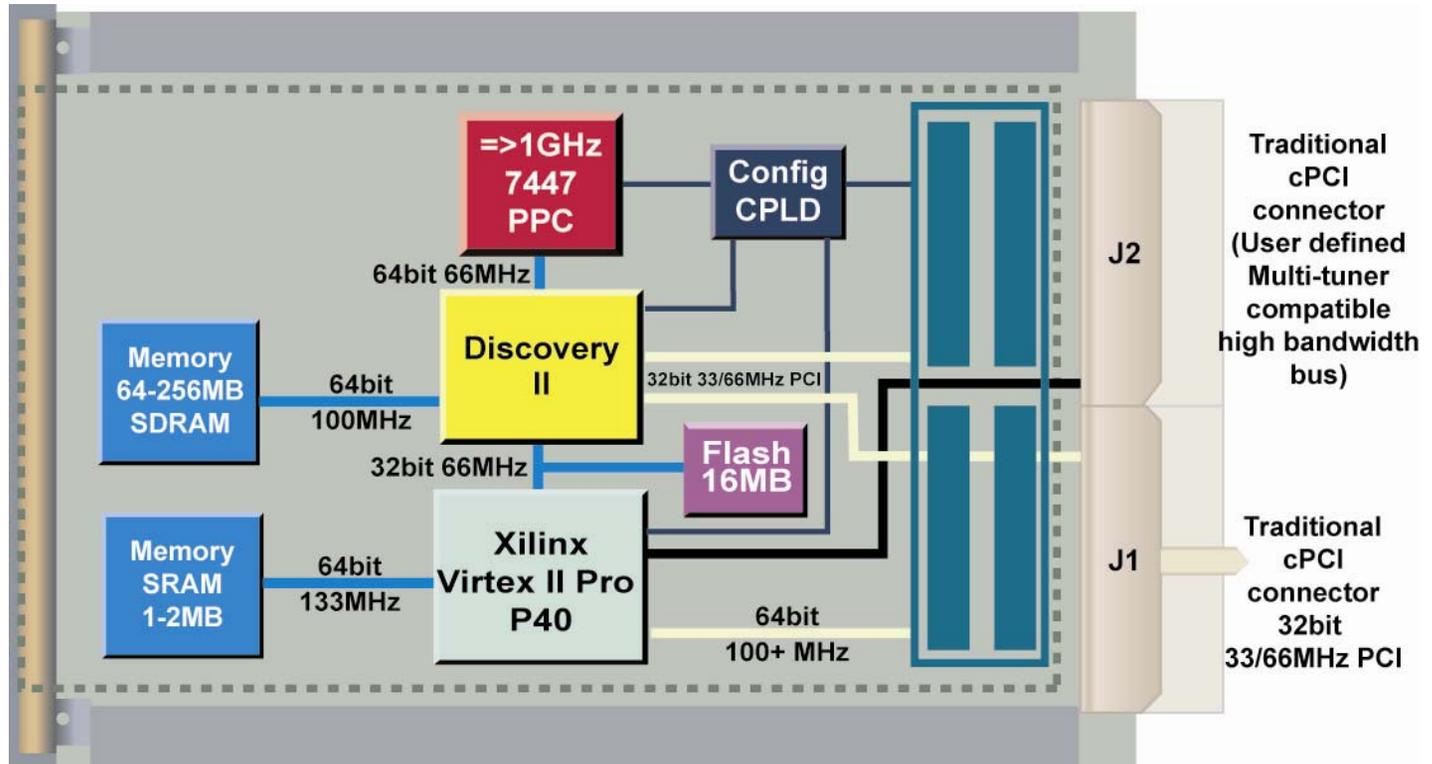
Ethernet
VGA



16-Channel Spatial Discrimination



3U Design for Signal Processing



- PowerPC 7447, 1 GHz
- 250 MB/s off-board via cPCI
- MCOE 6.2.x support
- WindRiver VxWorks + Tools

- FPGA Virtex II Pro
- 4x Direct high speed 'digital IF' interfaces
- PMC site for digital receiver or modem etc.
- FDK 2.0.x support

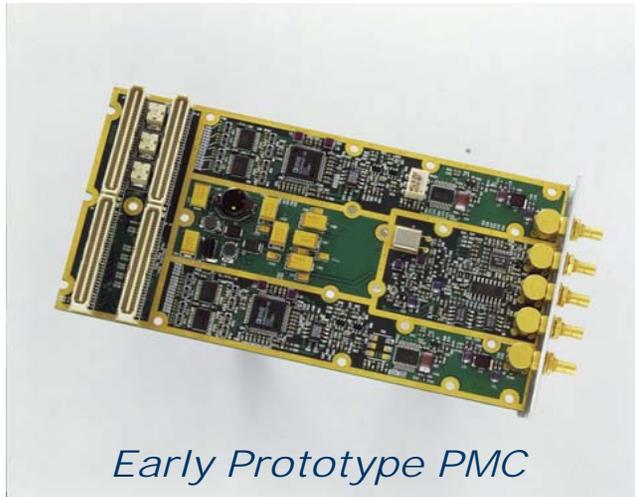
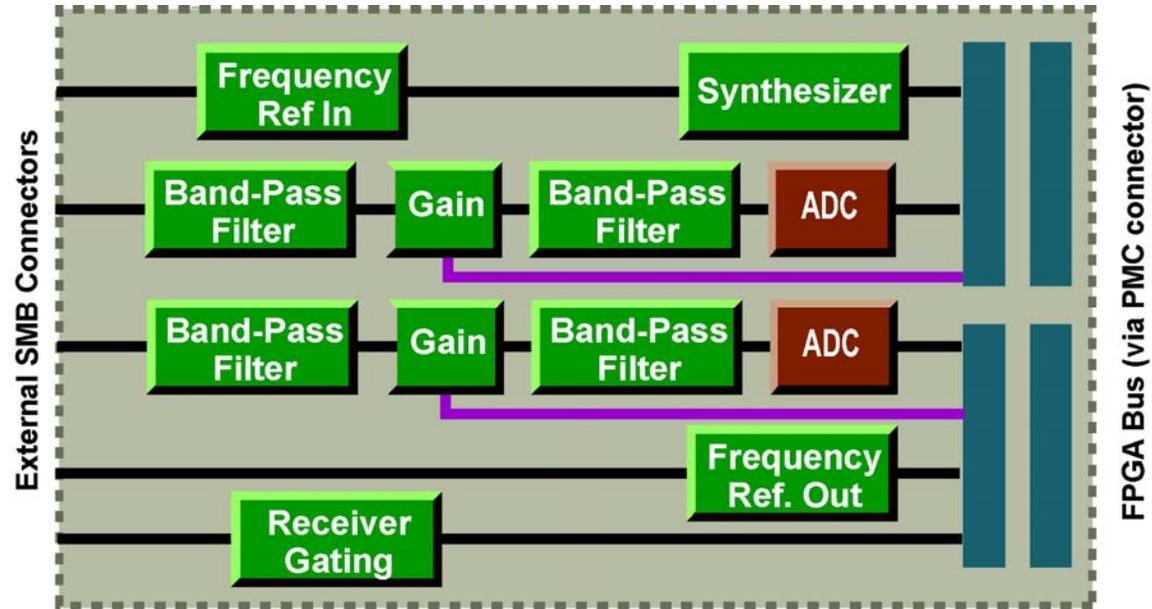
- **Combined PowerPC & FPGA**
 - ◆ Flexibility of RISC processing code
 - ◆ Density and bandwidth handling strengths of FPGAs
- **Deployable**
 - ◆ Ruggedized & conduction-cooled
- **Multiple I/Os direct to FPGA**
 - ◆ 4x high-speed bus via J2
 - ◆ Dual-channel analogue input digital receiver PMC option



Initial PMC Offering

Analog I/O receiver

- ◆ 2x 80 MSPS 14 bit ADC
- ◆ Factory configurable
 - IF up to 100 MHz



Early Prototype PMC

PMC general features

- ◆ Direct interface to FPGA
- ◆ Stepped attenuators
- ◆ RF screening
- ◆ Clocks (int./ext.)
- ◆ Power managed

Processing Challenges in Shrinking HPEC Systems into Small Platforms

Stephen Pearce & Richard Jaenicke
Mercury Computer Systems, Inc.

High Performance Embedded Computing (HPEC) Conference
September 28, 2004

The Ultimate Performance Machine

Platforms with SWAP Constraints - UAVs

UAV	Global Hawk	Predator B	Heron A	Hunter	Eagle Eye	Fire-Scout	Sentry	Dragon Warrior	Dragon Eye
Picture									
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

- UAVs height is very small; tends to lead to smaller system designs than 6U arrayed on base of fuselage/wings
- Payload weight is small, thus weight constrained solutions are demanded

- UAVs tend to fly fairly high. A consequence is that without life support environments (no man) at this altitude, conduction cooled becomes mandatory.
- All traditional HPEC applications are represented on all the platforms.

Scaling the Processing

500 MHz class PPC x 4
 = 16 GFLOPS per slot =>

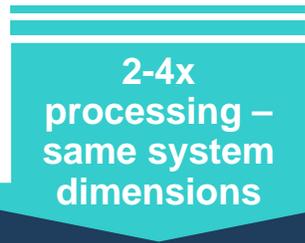
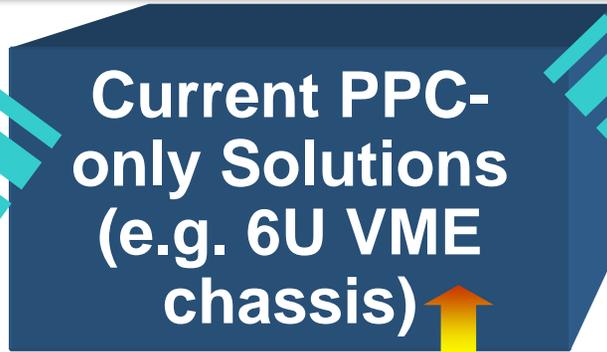
- ♦ 6 slot=96 GFLOPS
- ♦ 12 slot=192 GFLOPS
- ♦ 20 slot=320 GFLOPS

Assumptions

- ♦ FPGA= Equivalent 40-100 GFLOPS
- ♦ 500 MHz PPC=4 GFLOPS



Similar Processing –
 smaller system



2-10x processing – same system dimensions



- 2x 1GHz class PPC per board or 2 FPGA per board=>

- ♦ 2 slot=96-216 GFLOPS
- ♦ 4 slot=112-616 GFLOPS
- ♦ 8 slot=224-1232 GFLOPS

- => Future FPGA + PPC exploitation on 3U better than existing 6U

4x 1.5 GHz class PPC = 48 GFLOPS per slot =>

- ♦ 6 slot=288 GFLOPS
- ♦ 12 slot=576 GFLOPS
- ♦ 20 slot=960 GFLOPS

- => PPC exploitation of VITA 46

- 4x 1 GHz class PPC per board or 2 FPGA per board=>

- ♦ 6 slot=192-1032 GFLOPS
- ♦ 12 slot=384-2232 GFLOPS
- ♦ 20 slot=640-3832 GFLOPS

- =>FPGA + PPC exploitation on VME