VSIPPL++: Serial and Parallel Performance

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1 Introduction

The VSIPPL (the Vector, Signal, and Image Processing Library) specification defines a portable, C programming language interface to use in linear algebra and signal-processing applications. The VSIPPL standard has been implemented by a variety of vendors. VSIPPL’s portable interface provides developers the ability to write code once and reuse it in multiple environments.

At HPEC 2002, we presented an overview of VSIPPL++, a C++ specification designed to perform the same types of computations as VSIPPL. The primary goals for VSIPPL++ are improved serial performance relative to VSIPPL, support for multi-processor systems, extensibility, and simpler syntax.

The serial VSIPPL++ specification is virtually complete. By HPEC 2003, we expect to have a successful implementation of the specification. We anticipate that the performance of the VSIPPL++ reference implementation will be superior to that of VSIPPL for some applications. By HPEC 2003, the reference implementation of VSIPPL++ will contain preliminary support for parallel systems.

Our presentation will compare the performance of VSIPPL++ with VSIPPL, and demonstrate the VSIPPL++ support for parallel computation. We will also discuss VSIPPL++ implementation strategies, including the use of an existing VSIPPL implementation, a native C++ implementation using expression-templates, and a hybrid approach that allows an implementor to incrementally reimplement portions of VSIPPL++ to achieve higher performance.

2 Performance Comparisons

VSIPPL++ can be implemented on either uni-processor or multi-processor hardware. As a first step, we are implementing VSIPPL++ using an existing C VSIPPL library. While this implementation is straightforward, the performance is of course limited by the performance of the underlying VSIPPL implementation. We also have a preliminary implementation of some portions of VSIPPL++
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using a high-performance expression-template technique. By HPEC 2003, we plan to have a partial parallel implementation of VSIPL++.

We are using a simple FIR-filter and narrowband beamforming application as a benchmark. These computations are fundamental to many signal-processing applications. We plan to present performance comparisons between VSIPL, VSIPL++ built atop VSIPL, VSIPL++ using expression templates, and VSIPL++ using multiple processors.

3 Parallel Computation Model

VSIPL++ uses a Single Program Multiple Data (SPMD) model when performing parallel computations. The VSIPL++ model divides rectangular arrays of data (known as “blocks”) into sections using combinations of block and cyclic data distributions. We will explain the VSIPL++ model, and demonstrate how a very simple distribution model can accommodate systems ranging from small embedded systems to large systems with thousands of nodes. We will also explain how a wide variety of distribution policies can be implemented atop the simple distribution model provided by VSIPL++. Finally, we will explain how the VSIPL++ parallelism model provides support for fault-tolerance via dynamic reallocation of processors.
Serial and Parallel Performance

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Design Path

Performance
Portability
Productivity
Parallelism

VSIPL
Specification Status

• Serial Specification
  – 216-page draft.
  – Under review by VSIPL Forum.

• Parallel Specification
  – 24-page preliminary draft.
  – Initial conceptual review complete.
Serial Performance

• Uses VSIPL reference implementation.
  – Not the fastest implementation…
  – … but the relative performance is important.

• Environment:
  – 2GHz Pentium-M
  – 512KB cache, 512MB RAM
  – GNU/Linux, G++ 3.4
Matrix/Vector

\[ v += mv \]

Vector Length vs. Time graph showing performance comparison between VSIPL and VSIPL++.
Matrix/Matrix

result += tan(sin(m) + cos(m))
Checked Vector Access

![Graph showing checked vector access performance between VSIPL and VSIPL++]

- X-axis: Vector Length (10^4 to 10^7)
- Y-axis: Time (0 to 50)

Legend:
- Red line: VSIPL
- Yellow line: VSIPL++
Performance Conclusions

- VSIPL++ has approximately zero overhead.
  - Memory effects actually enable VSIPL++ to outperform VSIPL.
  - Expression-template techniques may also improve performance.
- Exceptions are expensive.
  - We are not sure if this overhead can be eliminated.
- Reference implementation will be directly useful.
  - Vendor-optimized versions will probably be better.
Parallelism

• Target systems:
  – Support 1-64K+ processors.
  – Support MPI, POSIX threads.

• Conceptual model:
  – Single-program multiple-data model.
  – Owner computes.
  – Parallelism requires changing only declarations, not expressions.
Parallel VSIPL++ Model

- view0
- view1
- view2
- view3

- block0
- block1
- block2

- data distribution
- grid function

- map

- processors

- user program

- hardware

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Using Parallelism

- **Declaration:**

  
  Vector<double,
  Dense<l, double,
  Map<Block> > >
  v (17, 1.0, Block(4));

- **Meaning:**
  - 17: Vector length.
  - 1.0: Initial value.
  - Block(4): Block distribution over 4 processors.
FYO4 Objectives

• Specification:
  – Finalize serial and parallel specifications.
  – Get approval from VSIPL Forum.

• Implementation:
  – Finish serial implementation.
  – Draft parallel implementation.

• Measurement:
  – Performance analysis.
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