MONARCH:
A Morphable Networked micro-ARCHitecture

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Outline

- MONARCH Team, Goals & Approach
- DIVA (Data Intensive Architecture) Leverage: The Chip
- Raytheon HPPS (High Performance Processor System)
- MONARCH Architecture & Applications
- Summary & Conclusions
The Team

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GOALS

♦ **To support multiple classes of military missions**
  with a single morphable architecture

♦ **To eliminate processing system redundancies**
  through rapid dynamic reconfiguration of front-end
  filtering and data-reduction processing

♦ **To reduce application development costs**
  by allowing the hardware to be mapped to the algorithms
  both statically and dynamically

♦ **To develop an architecture that can quickly and
  efficiently adapt to changing situations**
  - internal (fault tolerance, sensors configurations)
  - external (threats change, mission phasing, environment)
Key Ideas

Combines fine, medium and coarse grain processing resources on a single chip

Matches hardware to the algorithms and the control flow mechanisms

Configures memory structures for efficient front-end and back-end processing

Provides flexible gigabyte I/O channels for direct interface to sensors and inter-chip communication

Supports all systems processing requirements with a single MONARCH chip type
Approach

- Leverage DARPA-sponsored DIVA Project results, Raytheon IRAD-sponsored HPPS and Mercury Stream Co-processing Engine
- Use DoD missions to drive micro-architecture and morphing concepts and implementation
- Determine the “sweet spot” for mixing large, small-to-medium and fine-grained elements
- Through experiments and simulations demonstrate a “single chip” VLSI processing architecture based on DIVA and HPPS
DIVA Leverage: The Chip
Exploiting The Bandwidth in a System

Processor \leftrightarrow Memory

A Solution

DIVA Solutions:
- Move concurrent processing on-chip
- More bandwidth and less latency on chip
- Added bandwidth between memories
- Lower latencies throughout system
DIVA Software/Hardware

Tools & Applications
- Compiler
  Data Placement, Parallelism, Host-PIM Mapping, Parcels, Coherence
- OS (Linux)
  Page Placement, Paging for Host & PIMs, Scheduling, PIM Initialization
- PIM Backend Compiler
  Code generation for scalar and WideWord
- PIM Runtime Kernel
  Parcel Management, Address Translation Faults, PIM Context Switches, Synchronization

System Management
- Host Runtime Layer
  Synchronization, Flushing, Thread Management, Host Parcels
- Application

Runtime Coordination
- Host System
- Memory Controller
- PIM VLSI Devices
  Processor, Memory Array

Physical Hardware
- PIM Applications
- DARPA
- PCA
- MONARCH
WideWord ALU Data Flow

Source 1 (256 bits)  Source 2 (256 bits)

WideWord Register File

Arithmetic (8, 16, 32)
Logical (8, 16, 32, 256)
Multipliers (8 x 8, 16 x 16)
Permutation (8, 16, 32)

KISS: More compromises in architecture to enable early prototype
DIVA PIM Chip

♦ Current lab measurements
  – 640 MOPs (peak, 32-bit ops)
  – 0.8 Watts at 80MHz on cornerturn core loop

♦ Purpose
  – Demonstrate bandwidth advantages of PIM technology

♦ Key architectural components
  – High memory bandwidth
  – 256-bit WideWord processing
  – PIM routing component

♦ Chip statistics
  – 9.8mm X 9.8mm in TSMC 0.18µm
  – ~200K logic cells plus 8Mbit SRAM
  – 352 pins (241 signal pins)

♦Projected performance for 2nd prototype
  – 1.6 GOPs
  – 2.5 Watts at 200MHz
HPPS & FPCA ARCHITECTURES
♦ Multinode Processor
♦ One custom ASIC
♦ Innovative voting
♦ Inputs for high bandwidth A/D receiver channels or FPCA
**HPPS Node Architecture**

- **Fault-Tolerant Intf. Core**
  - I/O Capability
    - Intra-node
    - Inter-node
  - Distrib. Crossbar
  - Fault Detection
    - Memory EDAC
    - Processor voting
    - Node configuration controls

- **12 ea 4GByte I/O paths**

- **Point-To-Point Interconnect Fabric**

- **Field Programmable Computing Array**

- **Interface for COTS µP to Leverage Commercial Advances**
MONARCH: Node Architecture

Note: Not to Scale

- Fault-Tolerant Intf. Core
  - I/O Capability
    - Intra-node
    - Inter-node
  - Distrib. Crossbar
  - Fault Detection
    - Memory EDAC
    - Processor voting
    - Node configuration control

- 12 ea 4GByte I/O paths

- Virtual WideWord Unit/
  Data Flow Unit

- DFIM

- Interface for COTS μP
  For Legacy Systems
Virtual WideWord Unit/DFIM
♦ Multinode Processor
♦ One MONARCH chip
♦ Innovative voting
♦ Inputs for high bandwidth A/D receiver channels or direct chip-to-chip data transfer
MONARCH Chip Overview

- **Inter-Chip Communication Fabric**
- **Multichannel Sensor Input**
- **I/O Control & Data Integrity**
- **PARCEL BUFFER**
  - Data/Control Registers
- **COMPUTING RESOURCES**
  - ALUs/MACs
  - Memory Clusters
  - Register Files
- **INTERCONNECT**
  - Crossbars/DDEs
- **EDGEMEMORY**
- **DRAM MEMORY**
- **MEMORY CONTROL & ARBITER**
- **ICache**
- **Instruction Pipeline**
- **μCONTROLLER**
  - Datapath
- **Register Load/Store Requests**
- **GENERAL INTERFACE LOGIC**
  - (Fine-grain programmable)
Native Threaded Mode

- External Memory Interface
- High Speed I/O
- Parcel Logic
- I/O Adaptor ("FPGA")
- DRAM
- FPU
- ALU
- Reg File
- µController

MONARCH Application Processor

Stream Processing

Control

MC-SM

MC-SM

MC-SM

MC-TM

MC-TM

Inter-chip Memory Transfer

Inter-chip I/O (crossbar)

Parcel Interface

Threaded Processing
MONARCH Architecture Features

♦ Dual native mode, high throughput computing
  – Multiple wide word threaded (instruction flow) processors/chip
  – Highly parallel reconfigurable (data flow) processor
♦ Large on chip, multiport memories
  – High bandwidth access to memory
  – Extensible with off chip memory
♦ High speed, distributed cross bar I/O
  – Integrated with chip processing
  – Scalable I/O bandwidth - multiple topologies
  – Direct connect to high speed I/O devices, e.g., A/D’s
♦ Rich on chip interconnect
  – Supports on chip topology morphing and fault tolerance
  – Supports multiple computation models (SISD, SIMD, DF, SPMD,…)
♦ On chip Morph - Program bus and microcontrollers
<table>
<thead>
<tr>
<th>ISSUE</th>
<th>APPROACH</th>
<th>BENEFIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>256 bit wide word processing unit</td>
<td>Each Arithmetic Cluster has 8 32 bit units</td>
<td>1 AC provides same width as WW unit</td>
</tr>
<tr>
<td>Instruction Set Mapping</td>
<td>Basic functions same</td>
<td>Little impact</td>
</tr>
<tr>
<td></td>
<td>Need to add some insts</td>
<td></td>
</tr>
<tr>
<td>Large On-chip memory</td>
<td>Similar to Edge Memory</td>
<td>Performance boost</td>
</tr>
<tr>
<td></td>
<td>Now can have on chip</td>
<td></td>
</tr>
<tr>
<td>5 State pipeline, instruction flow decoder</td>
<td>Retain, and mux decoded signals with DF signals</td>
<td>Some hardware growth, but more control modes</td>
</tr>
<tr>
<td>Data flow control mode - streaming</td>
<td>Retain - switch mode bit</td>
<td>As above</td>
</tr>
<tr>
<td>High speed, multiple channel I/O</td>
<td>Incorporate dist. xbar and use for parcel com</td>
<td>Improved I/O performance</td>
</tr>
<tr>
<td>Parcel communications</td>
<td>Retain and map onto other physical protocol</td>
<td>Little impact</td>
</tr>
<tr>
<td>On-chip micro controllers</td>
<td>Retain</td>
<td>Performance boost</td>
</tr>
</tbody>
</table>

* Merger of features from DIVA and HPPS processors
## Architecture Merger Issues

<table>
<thead>
<tr>
<th>ISSUE</th>
<th>APPROACH</th>
<th>IMPACT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WideWord 8-bit math</td>
<td>Modify array carry-chain logic</td>
<td>Negligible delay</td>
</tr>
<tr>
<td>Thread control for array / WideWord</td>
<td>Switch RISC pipeline control into array</td>
<td>TBD</td>
</tr>
<tr>
<td>3-port WW register file implementation</td>
<td>Extend array arithmetic clusters</td>
<td>Small area increase</td>
</tr>
<tr>
<td>WideWord pipeline length / bypass</td>
<td>TBD / Simulation</td>
<td>Interconnect, Compiler</td>
</tr>
<tr>
<td>Minimum I Cache size</td>
<td>Simulation</td>
<td>Area</td>
</tr>
<tr>
<td>Data exchange: W→S / S→W</td>
<td>TBD</td>
<td>Area, Interconnect</td>
</tr>
<tr>
<td>I/O: Memory map or program?</td>
<td>Memory Map</td>
<td>None</td>
</tr>
<tr>
<td>WideWord shifter implementation</td>
<td>TBD (modify array)</td>
<td>Design complexity</td>
</tr>
<tr>
<td>Permute implementation</td>
<td>Enhance array x-bars for 8 bit data</td>
<td>Small area increase</td>
</tr>
</tbody>
</table>
FPCA Changes for WideWord

Multiplexor for dual mode instruction set control of elements

8 32-bit ALUs become 32 8-bit elements
32 word register file added

“Breakable” carry chains
(Actually still 32 bit processing elements, but condition codes and carries controllable at 8 bit boundaries)

---

OP
Data valid (default)
Consume (default)
Token (participation)
### MONARCH I/O Summary

<table>
<thead>
<tr>
<th>Port Type</th>
<th>Number of Ports</th>
<th>Wires per Port</th>
<th>Total Wires</th>
<th>Type</th>
<th>Clock Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>High speed ports</td>
<td>12</td>
<td>50</td>
<td>600</td>
<td>LVDS</td>
<td>1 GHz</td>
</tr>
<tr>
<td>Inter FPCA Links</td>
<td>4</td>
<td>52</td>
<td>208</td>
<td>LVDS</td>
<td>1-2 GHz</td>
</tr>
<tr>
<td>External memory</td>
<td>1</td>
<td>160</td>
<td>160</td>
<td>CMOS</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Standard I/O</td>
<td>2</td>
<td>60</td>
<td>120</td>
<td>variable</td>
<td>100+ MHz</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td><strong>1088</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Need to Select Preferred Parameters for 1st MONARCH Chip

Design choice will balance throughput, memory, and I/O needs for representative applications.

MONARCH Processor/Memory Trade Space

Could design chip for anywhere inside this space.
MONARCH Processing Card
- 6Ux160 double euro card form factor -

- 6 MONARCH chips + memory and power conditioning
- 75 GFLOPS
- 2.4 TOPS
- 192 MBytes on-chip DRAM
- 2 MBytes on-chip SRAM
- 1 GBytes on-board memory
Summary & Conclusions

♦ MONARCH features very attractive for multiple applications

♦ Merger of two existing architectures shows good fit
  – “Complementary” but compatible features
  – Rich experience base allows quick design trades

♦ “The devil is in the details” --- a lot more work
  – On-chip DRAM organization and access
  – Support for “morphing”
  – Simulation results at application-level
  – Trade offs for FPU capability