Short Vector SIMD Code Generation for DSP Algorithms

Franz Franchetti
Christoph Ueberhuber
Applied and Numerical Mathematics
Technical University of Vienna
Austria

Markus Püschel
José Moura
Electrical and Computer Engineering
Carnegie Mellon University

http://www.ece.cmu.edu/~spiral
http://www.math.tuwien.ac.at/~aurora
**Report Documentation Page**

<table>
<thead>
<tr>
<th>Field</th>
<th>Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. REPORT DATE</td>
<td>21 MAY 2003</td>
</tr>
<tr>
<td>2. REPORT TYPE</td>
<td>N/A</td>
</tr>
<tr>
<td>3. DATES COVERED</td>
<td>-</td>
</tr>
<tr>
<td>4. TITLE AND SUBTITLE</td>
<td>Short Vector SIMD Code Generation for DSP Algorithms</td>
</tr>
<tr>
<td>5a. CONTRACT NUMBER</td>
<td></td>
</tr>
<tr>
<td>5b. GRANT NUMBER</td>
<td></td>
</tr>
<tr>
<td>5c. PROGRAM ELEMENT NUMBER</td>
<td></td>
</tr>
<tr>
<td>5d. PROJECT NUMBER</td>
<td></td>
</tr>
<tr>
<td>5e. TASK NUMBER</td>
<td></td>
</tr>
<tr>
<td>5f. WORK UNIT NUMBER</td>
<td></td>
</tr>
<tr>
<td>6. AUTHOR(S)</td>
<td>Applied and Numerical Mathematics, Technical University of Vienna, Austria; and Electrical and Computer Engineering, Carnegie Mellon University</td>
</tr>
<tr>
<td>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</td>
<td>Applied and Numerical Mathematics, Technical University of Vienna, Austria; and Electrical and Computer Engineering, Carnegie Mellon University</td>
</tr>
<tr>
<td>8. PERFORMING ORGANIZATION REPORT NUMBER</td>
<td></td>
</tr>
<tr>
<td>9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)</td>
<td></td>
</tr>
<tr>
<td>10. SPONSOR/MONITOR’S ACRONYM(S)</td>
<td></td>
</tr>
<tr>
<td>11. SPONSOR/MONITOR’S REPORT NUMBER(S)</td>
<td></td>
</tr>
<tr>
<td>12. DISTRIBUTION/AVAILABILITY STATEMENT</td>
<td>Approved for public release, distribution unlimited</td>
</tr>
<tr>
<td>13. SUPPLEMENTARY NOTES</td>
<td>Also see ADM001473, The original document contains color images.</td>
</tr>
<tr>
<td>14. ABSTRACT</td>
<td></td>
</tr>
<tr>
<td>15. SUBJECT TERMS</td>
<td></td>
</tr>
<tr>
<td>16. SECURITY CLASSIFICATION OF:</td>
<td></td>
</tr>
<tr>
<td>a. REPORT</td>
<td>unclassified</td>
</tr>
<tr>
<td>b. ABSTRACT</td>
<td>unclassified</td>
</tr>
<tr>
<td>c. THIS PAGE</td>
<td>unclassified</td>
</tr>
<tr>
<td>17. LIMITATION OF ABSTRACT</td>
<td>UU</td>
</tr>
<tr>
<td>18. NUMBER OF PAGES</td>
<td>29</td>
</tr>
<tr>
<td>19a. NAME OF RESPONSIBLE PERSON</td>
<td></td>
</tr>
</tbody>
</table>

Standard Form 298 (Rev. 8-98)  
Prescribed by ANSI Std Z39-18
Work supported by DARPA (DSO), Applied & Computational Mathematics Program, OPAL, through grant managed by research grant DABT63-98-1-0004 administered by the Army Directorate of Contracting.
Outline

- Short vector extensions
- Digital signal processing (DSP) transforms
- SPIRAL
- Vectorization of SPL formulas
- Experimental results
**SIMD Short Vector Extensions**

- Extension to instruction set architecture
- Available on most current architectures
- Originally for multimedia (like MMX for integers)
- Requires fine grain parallelism
- **Large potential speed-up**

<table>
<thead>
<tr>
<th>Name</th>
<th>$n$-way</th>
<th>Precision</th>
<th>Processors</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSE</td>
<td>4-way</td>
<td>float</td>
<td>Intel Pentium III and 4, AMD AthlonXP</td>
</tr>
<tr>
<td>SSE2</td>
<td>2-way</td>
<td>double</td>
<td>Intel Pentium 4</td>
</tr>
<tr>
<td>3DNow!</td>
<td>2-way</td>
<td>float</td>
<td>AMD K6, K7, AthlonXP</td>
</tr>
<tr>
<td>AltiVec</td>
<td>4-way</td>
<td>float</td>
<td>Motorola G4</td>
</tr>
<tr>
<td>IPF</td>
<td>2-way</td>
<td>Float</td>
<td>Intel Itanium, Itanium 2</td>
</tr>
</tbody>
</table>
Problems

- SIMD instructions are architecture specific
- No common API (usually assembly hand coding)
- Performance very sensitive to memory access
- Automatic vectorization (by compilers) very limited

Requires expert programmers

Our Goal: Automation for digital signal processing (DSP) transforms
DSP (digital signal processing) transforms

Example: Discrete Fourier Transform (DFT) size 4

\[
DFT_4 = \left[ \begin{array}{cccc}
1 & 1 & 1 & 1 \\
1 & i & -1 & -i \\
1 & -1 & 1 & -1 \\
1 & -i & -1 & i \\
\end{array} \right] = \left[ \begin{array}{cccc}
1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 \\
1 & -1 & 1 & 1 \\
1 & 1 & i & 1 \\
\end{array} \right] \left[ \begin{array}{cccc}
1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 \\
1 & -1 & 1 & 1 \\
1 & 1 & i & 1 \\
\end{array} \right]
\]

\[
DFT_4 = (DFT_2 \otimes I_2)D(I_2 \otimes DFT_2)P
\]

- Fast algorithm = product of structured sparse matrices
- Represented as formula using few constructs (e.g., \( \otimes \)) and primitives (diagonal, permutation)
- Captures a large class of transforms (DFT, DCT, wavelets, …)
Tensor (Kronecker) Product of Matrices

\[ A \otimes B = [a_{kl}B]_{k,l} \]

for \( A = [a_{kl}]_{k,l} \)

Examples:

\[
\begin{bmatrix}
1 & 2 \\
3 & 4
\end{bmatrix} \otimes I_2 =
\begin{bmatrix}
1 & 2 \\
3 & 4
\end{bmatrix}
\]

\[
I_2 \otimes \begin{bmatrix}
1 & 2 \\
3 & 4
\end{bmatrix} =
\begin{bmatrix}
1 & 2 \\
3 & 4
\end{bmatrix}
\]

key construct in many DSP transform algorithms (DFT, WHT, all multidimensional)
SPIRAL: A Library Generator for Platform-Adapted DSP Transform

www.ece.cmu.edu/~spiral

Observation:

• For a given transform there are maaaany different algorithms (equal in arithmetic cost, differ in data flow)
• The best algorithm and its implementation is platform-dependent
• It is not clear what the best algorithm/implementation is

SPIRAL:

- Automatic algorithm generation
- + Automatic translation into code
- + Intelligent search for “best”

= generated platform-adapted implementation
SPIRAL’s Mathematical Framework

Transform

\[ DFT_n \]

parameterized matrix

Rule

\[ DFT_{nm} \rightarrow (DFT_n \otimes I_m) \cdot D \cdot (I_n \otimes DFT_m) \cdot P \]

- a breakdown strategy
- product of sparse matrices

Formula

\[ DFT_{16} = (DFT_4 \otimes I_4) \cdot T_4^{16} \cdot (I_4 \otimes DFT_4) \cdot L_4^{16} \]

- by recursive application of rules
- few constructs and primitives
- can be translated into code

Used as mathematical high-level representation of algorithms
(SPL = signal processing language)
Our Goal: extend SPL compiler to generate vector code
Generating SIMD Code from SPL Formulas

Example:

$$y := (A \otimes I_4)x$$

naturally represents vector operation

(vector length)

(Current) generic construct completely vectorizable:

$$\prod_{i=1}^{k} P_i D_i (A_i \otimes I_v) E_i Q_i$$

- Formulas contain all structural information for vectorization
- Construct above captures DFT, WHT, all multi-dimensional

permutations

diagonals

arbitrary formulas

SIMD vector length
The Approach

- Use macro layer as API to hide machine specifics
- Vector code generation in two steps
  1. Symbolic vectorization (formula manipulation)
  2. Code generation
Symbolic Vectorization

\[ DFT_{16} = (DFT_4 \otimes I_4) \cdot T_{4}^{16} \cdot (I_4 \otimes DFT_4) \cdot L_{4}^{16} \]

Formula manipulation (automatic using manipulation rules)

\[ \overline{DFT}_{16} = \left( (I_4 \otimes L_4^8) \cdot (DFT_4 \otimes I_4) \cdot T_{4}^{16} \right) \cdot \left( (I_4 \otimes L_2^8)(L_4^16 \otimes I_2)(I_4 \otimes L_4^8) \cdot (DFT_4 \otimes I_4) \cdot (I_4 \otimes L_2^8) \right) \]

Pattern matching

\[ \prod_{i=1}^{k} P_i D_i (A_i \otimes I_v) E_i Q_i \]

- Manipulate to match vectorizable construct
- Separate vectorizable parts and scalar parts
Normalizing formulas

\[(I_n \otimes L^{2^\nu}_v)(I_n \otimes L^{2^\nu}_n) = I_{2^n v}\]
\[A \otimes B = (A \otimes I_m)(I_n \otimes B)\]
\[I_v \otimes A = L^{n^\nu}_v (A \otimes I_v)L^{n^\nu}_n\]
\[I_{n^\nu + l} = I_{n^\nu} \oplus I_l\]
\[I_{mn} = I_m \otimes I_n\]
\[PD = D'P\]

Converting complex to real arithmetic

\[\bar{A} \cdot B = \bar{A} \cdot \bar{B}\]
\[\bar{A} = A \otimes I_2, \quad A \text{ real}\]
\[\bar{D} = (I_{n/\nu} \otimes L^{2^\nu}_v)\bar{D}'(I_{n/\nu} \otimes L^{2^\nu}_2), \quad \nu \mid n\]
\[A \otimes I_v = (I_n \otimes L^{2^\nu}_v)(\bar{A} \otimes I_v)(I_n \otimes L^{2^\nu}_2)\]
**Vector Code Generation**

\[
\prod_{i=1}^{k} P_i D_i (A_i \otimes I_v) E_i Q_i
\]

- arithmetic vector instructions
  - use standard SPL compiler on \( A_i \)
  - replace scalar with vector instructions

**easy part**

(due to existing SPL compiler)

**difficult part**

(easy to lose performance)

- fuse with load/store operations

\( P_i, Q_i \) permutations
\( D_i, E_i \) diagonals
\( A_i \) arbitrary formulas
\( i \) SIMD vector length
Challenge: Data Access

Example:

- highest performance code requires **properly aligned** data access
- permutation support differs between architectures
- performance differs between permutations (some are good, most very bad)

Solution:

- use formula manipulation to get “good” permutations
- macro layer API for efficient and machine transparent implementation
Portable High-level API

- restricted set of short vector operations
- requires C compiler with „intrinsics“-interface
- high-level operations
  - Vector arithmetic operations
  - Vector load/store operations
  - Special and arbitrary multi-vector permutations
  - Vector constant handling (declaration, usage)
  - Implemented by C macros

Example:

Unit-stride load of 4 complex numbers:

```c
LOAD_L_8_2(reg1, reg2, *mem)
```
Portable SIMD API: Details

All SIMD extensions supported:
- gcc 3.0, gcc-vec
- Intel C++ Compiler, MS VisualC++ with ProcessorPack
- Various PowerPC compilers (Motorola standard)

Examples:
Reverse load of 4 real numbers:
LOAD_J_4(reg, *mem)

Reverse load of 4 complex numbers:
LOAD_J_4_x_I_2(r1, r2, *mem)
- Vector parts: portable SIMD API
- Scalar parts: standard C
- \( P_i, Q_i, D_i, E_i \) handled by load/store operations
- \( A_i \) handled by vector arithmetics

```c
/* Example vector code: DFT_16 */
void DFT_16(vector_float *y,
            vector_float *x)
{
    vector_float x10, x11, x12;
    ...
    LOAD_VECT(x10, x + 0);
    LOAD_VECT(x14, x + 16);
    f0 = SIMD_SUB(x10, x14);
    LOAD_VECT(x11, x + 4);
    LOAD_VECT(x15, x + 20);
    f1 = SIMD_SUB(x11, x15);
    ...
    y17 = SIMD_SUB(f1, f4);
    STORE_L_8_4(y16, y17, y + 24);
    y12 = SIMD_SUB(f0, f5);
    y13 = SIMD_ADD(f1, f4);
    STORE_L_8_4(y12, y13, y + 8);
}

/* Intel SSE: portable SIMD API */
Intel C++ Compiler 5.0
typedef __m128 vector_float;
#define LOAD_VECT(a, b)    \( (a) = *(b) \)
#define SIMD_ADD(a, b)     \_mm_add_ps((a), (b))
#define SIMD_SUB(a, b)     \_mm_sub_ps((a), (b))
#define STORE_L_8_4(re, im, out) \{
    vector_float _sttmp1,_sttmp2; \_
    _sttmp1 = _mm_unpacklo_ps(re, im); \_
    _sttmp2 = _mm_unpackhi_ps(re, im); \_
    _mm_store_ps(out, _sttmp1); \_
    _mm_store_ps((out) + VLEN, _sttmp2); \_
\}
```
Experimental Results

- our code is generated, found by dynamic programming search
- different searches for different types of code (scalar, vector)
- results in (Pseudo) gigaflops (higher = better)
DFT Code: Pentium 4, SSE

DFT $2^n$ single precision, Pentium 4, 2.53 GHz, using Intel C compiler 6.0

Speedups (to C code) up to factor of 3.1
DFT $2^n$ double precision, Pentium 4, 2.53 GHz, using Intel C compiler 6.0

speedups (to C code) up to factor of 1.8
DFT Code: Pentium III, SSE

DFT $2^n$ single precision, Pentium III, 1 GHz, using Intel C compiler 6.0

speedups (to C code) up to factor of 2.1
DFT Code: Athlon XP, SSE

DFT $2^n$ single precision, Pentium III, 1 GHz, using Intel C compiler 6.0

speedups (to C code) up to factor of 1.6
Other transforms

- WHT has only additions
- very simple transform

speedups (to C code) up to factor of 3
Different search strategies

DFT $2^n$ single precision, Pentium 4, 2.53 GHz, using Intel C compiler 6.0

standard DP looses up to 25 % performance
### Best DFT Trees, size $2^{10} = 1024$

<table>
<thead>
<tr>
<th></th>
<th>Pentium 4 float</th>
<th>Pentium 4 double</th>
<th>Pentium III float</th>
<th>AthlonXP float</th>
</tr>
</thead>
<tbody>
<tr>
<td>scalar</td>
<td><img src="image1" alt="Tree" /></td>
<td><img src="image2" alt="Tree" /></td>
<td><img src="image3" alt="Tree" /></td>
<td><img src="image4" alt="Tree" /></td>
</tr>
<tr>
<td>C vect</td>
<td><img src="image5" alt="Tree" /></td>
<td><img src="image6" alt="Tree" /></td>
<td><img src="image7" alt="Tree" /></td>
<td><img src="image8" alt="Tree" /></td>
</tr>
<tr>
<td>SIMD</td>
<td><img src="image9" alt="Tree" /></td>
<td><img src="image10" alt="Tree" /></td>
<td><img src="image11" alt="Tree" /></td>
<td><img src="image12" alt="Tree" /></td>
</tr>
</tbody>
</table>

Trees are platform/datatype dependent.
Crosstiming of best trees on Pentium 4

DFT $2^n$ single precision, runtime of best found of other platforms

Software adaptation is necessary
Summary

- Automatically generated vectorized DSP code
- Code is platform-adapted (SPIRAL)
- We implement “constructs”, not transforms
  - tensor product, permutations, ...
  - DFT, WHT, arbitrary multi-dim supported
- Very competitive performance

Ongoing work:

- port to other SIMD architectures
- include filters and wavelets

http://www.ece.cmu.edu/~spiral
http://www.math.tuwien.ac.at/~aurora