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13. ABSTRACT (Maximum 200 words) The goal of this research program is to develop smart pixels and related technology for VLSI photonic systems. The native oxide and tunneling contact technology developed at the University of Illinois is the enabling technology for high performance vertical cavity surface emitting lasers (VCSELs) which will be used in future photonic systems and specifically in the smart pixels that are the focus of this research program. The smart pixel 8 x 8 (2.5 Gb/s) and 2 x 2 (20 Gb/s) arrays that will be studied will operate at 670 nm or 1330 nm and will utilize the native oxide defined VCSELs with tunnel junction contacts and heterogeneous materials integration through direct-wafer fusion, epitaxial lift-off, and bump-bonding techniques for integration and packaging. The University of Illinois and the University of Texas (20 GHz) and the Vitesse GaAs E/D MESFET/MSM technology utilizing the MOSIS foundry (2.5 GHz).				
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2 STATEMENT OF THE PROBLEMS STUDIED:

Task 1– VCSEL Development:

Design, growth, fabrication, and testing of M-V semiconductor VCSEL and RCPD optoelectronic devices. This work includes 670nm and 1330nm VCSELs employing the latest native oxide and tunnel injection techniques to achieve operation at low voltages and threshold currents.

Task 2–Smart Pixel Development

Design, fabrication, and testing of 8 x 8 smart pixels operating at 2.5 Gb/s using the Vitesse GaAs E/D MESFET/MSM MOSIS foundry. Design, fabrication, and testing of 2 x2 smart pixels operating at 20 Gb/s, using the University of Illinois 100 GHz InGaP/GaAs HBT process. A test plan has been developed to demonstrate board to board data communication for the 8 x 8 MESFET/MSM/VCSELs and 2 x 2 HBT/PIN/VCSELs smart pixels operated at 10Gb/s per channel.

Task 3–Heterogeneous Material Integration:

Heterogeneous materials integration using direct-wafer fusion, epitaxial lift-off, and burripbonding techniques for packaging and assembly of components for board to board data communications.

Task 4–Avalanche Photodiode Array Development

Avalanche photodiode 2 x 2 arrays for 1330 nm detection will be designed and fabricated at Princeton University. They will be incorporated in smart pixels operating at 10 Gb/s per channel. High bandwidth, high sensitivity AllnAs/InGaAs mesa APIDs grown by gas source MIBE will be demonstrated. The bandwidth, excess noise figure and ionization rate as a function of gain will be characterized. In addition, primary and multiplied dark current will be characterized. A planar APD structure will be developed for bump-bonding integration in smart pixels.

3 SUMMARY OF THE MOST IMPORTANT RESULTS:

3.1 Task 1-VCSEL Development

a) 670 nm VCSEL development:

We have worked on the development of red vertical cavity surface emitting lasers (VCSELs) using metalorganic chemical vapor deposition (MOCVD). We took three different approaches: (1) Native-oxide distributed Bragg reflector (DBR) VCSELs using InAlP/AlGaAs DBRs; (2) conventional InAlGaP VCSELs using semiconductor DBR structures; (3) InAlGaP lasers using InP quantum dot active regions. Our research work in these areas led to important new concepts for visible red lasers. The most important result in this area is the demonstration of the quantum-well-assisted quantum-dot laser (QD + QW laser).

During this program, we have been studying the quantum-dot (QD) laser modified into a quantum-well-assisted quantum-dot laser (QD + QW laser). The auxiliary quantum well (QW) is coupled by tunneling to the QDs via a barrier. The purpose of the auxiliary QW layer, or layers, is to overcome the problem of carrier collection and rearrangement (QD to QD transport) in the QDs, problems that arise because of the disconnected form (from dot-to-dot) of the QD layers and the stochastic form of the QDs in size and geometry. A QW within tunneling distance of a QD layer collects carriers efficiently, allows rapid tunneling transfer of carriers to the QD layer (including rapid back-and-forth tunneling-assisted lateral charge re-adjustment) and, as a consequence, efficient recombination via the QDs. The expectation, the purpose of this work is to realize an improved form of QD laser.

The idea of a QW-assisted QD laser has been verified by experiments on visible-spectrum ($\lambda \sim 650$ nm) InP-QD/InGaP-QW/InAlP heterostructures and IR ($\lambda \sim 980$ nm) InAs-QD/GaAs-QW/AlGaAs heterostructures. Both photopumped and current-driven (diode) QD+QW lasers have been demonstrated in initial experiments. A patent

application has been filed on the QD+QW laser, and on a number of variations of the basic device structure. There clearly are many opportunities afforded by coupling one-dimensional confined quantum systems to three-dimensional confined quantum systems (as demonstrated by the publications of the last two years). This work is merely in its infancy and obviously requires more attention.

Specifically, we have demonstrated CW 300 K photopumped InP QD laser operation (656-679nm) realized by modifying and coupling, via tunneling, an auxiliary InGaP QW to the QDs of the InP-In(AIGa)P-InAlP heterostructure. Carriers collected (efficiently) in the QW, and thus localized near the QDs, transfer by resonance tunneling to the QDs. The lattice-matched $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ QW coupled to the InP QDs by a thin ($L_B \sim 20\text{\AA}$) $\text{In}_{0.5}\text{Al}_{0.3}\text{Ga}_{0.2}\text{P}$ barrier overcomes the limitations of carrier collection, lateral charge transport, and thermalization in the QDs, thus yielding a fundamentally different form of QD laser. These are the lowest threshold InP QD lasers and the first to operate CW at 300K. We have also established a record high characteristic temperature (T_0) for red-emitting injection lasers operating in the ~ 650 nm wavelength regime.

b) Fabrication of 1330 nm VCSEL:

Long-wavelength (1.3 and 1.55 μm) InGaAsP/InP VCSEL is the key component for the realization of high-speed and high-density optical communication systems. Unfortunately, the InGaAsP/InP material system doesn't possess efficient lattice-matched epitaxial DBR because the refractive index difference of InGaAsP/InP is as small as 0.3 and their thermal conductivity is low. In order to overcome the existing problems in long-wavelength VCSELs, we have developed ex-cavity bonding methods which incorporates semiconductor/Al-oxide DBR, such as GaAs/Al-oxide and Si/Al-oxide, into the VCSEL fabrication process.

Very-low temperature molecular beam epitaxy growth of substrate-independent DBRs:

Using very-low temperature molecular beam epitaxy (VLT-MBE) growth techniques, substrate-independent DBRs were fabricated for use in the visible spectrum. The microstructure of the semiconductor material was found to be either polycrystalline or amorphous depending on the group-V overpressure used as seen in Fig. 1. Higher overpressures resulted in amorphous material. Because the material was not single-crystalline, it can be deposited on any host substrate without causing defects in the underlying material. In addition, the two materials used in the DBR do not need to be lattice matched to each other thereby allowing much freedom in the design of the DBRs. VLT-GaP and AlAs were used as the materials for the visible spectrum DBR. Figure 2 shows the reflectivity of a DBR with only 6 pairs of poly-GaP/Al-oxide layers grown on a GaAs substrate.

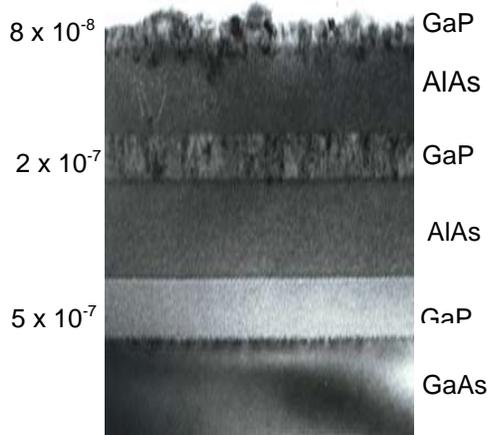


Figure 1 XTEM of a VLT-MBE grown (Ga,P)/(Al,As) heterostructure on GaAs substrate under different P overpressures.

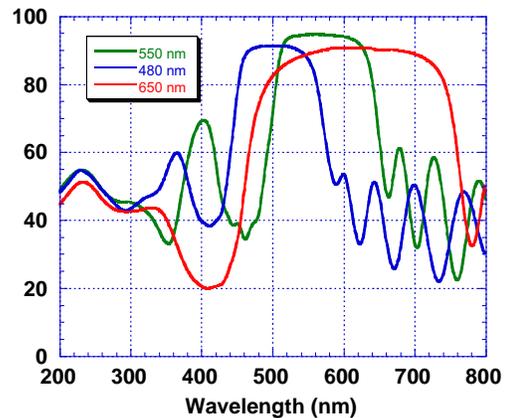


Figure 2. Reflectivity spectra for the six pair poly (Ga,P)/Al-oxide DBRs centered at 480, 550, and 650 nm.

1.55 μm VCSEL using metallic bonding:

To overcome the problem associated with the small refractive index difference in the GaInAsP/InP material system, a novel wafer bonding method using AuGeNiCr multi-layered metals as the bonding medium has been developed to fabricate 1.55 μm VCSELs on Si substrates. The bonding was performed at a low temperature of 320 $^\circ\text{C}$ without any special treatment of the bonding surfaces, and the bonding interface was located outside the VCSEL cavity. This metallic bonding process is straightforward and generous in process latitude which makes this process attractive for manufacturing. In addition, the feasibility of this process to fabricate long-wavelength VCSELs on Si makes it useful for potential applications on module integration.

The fabrication process is briefly described here. The 2λ -thick GaInAsP/InP active region of the VCSEL was grown on a (100) InP substrate. After crystal growth, a 6.5-period Al-oxide/Si lower DBR was deposited on the as-grown wafer by e-beam evaporation. The DBR/GaInAsP/InP wafer and a Si substrate were then coated with the AuGeNiCr metallic bonding

medium and bonded together at 320 °C under a uniaxial pressure. After bonding, the InP substrate was removed by HCl chemical etching and the GaInAsP/InP active region was exposed. Standard photolithography and selective chemical etching were used to define the VCSEL mesa. The p-type and n-type ohmic contacts were formed by Au/Zn/Au and AuGe/Ni/Au alloys, respectively. Finally, a 5-period Al-oxide/Si upper DBR was deposited on top of the device mesa to complete the VCSEL structure.

Figure 3 shows the cross-sectional scanning electron microscopy (SEM) micrograph of the fabricated long wavelength VCSEL. The room temperature current-voltage (I-V) and light-output versus injection current (L-I) curves of a 30 μm by 30 μm VCSEL are shown in Fig. 4. The VCSELs have a turn-on voltage around 0.8 volt and a threshold current of 12 mA. The pulsed lasina spectrum of the VCSEL at near room temperature was observed at 1.545 μm as shown in the inset of Fig. 4.

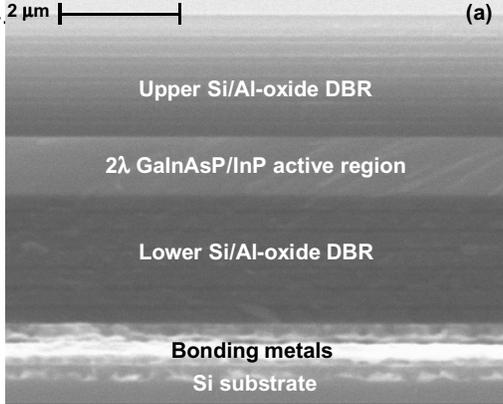


Figure 3. The cross-sectional SEM micrograph of the GaInAsP/InP VCSEL cavity.

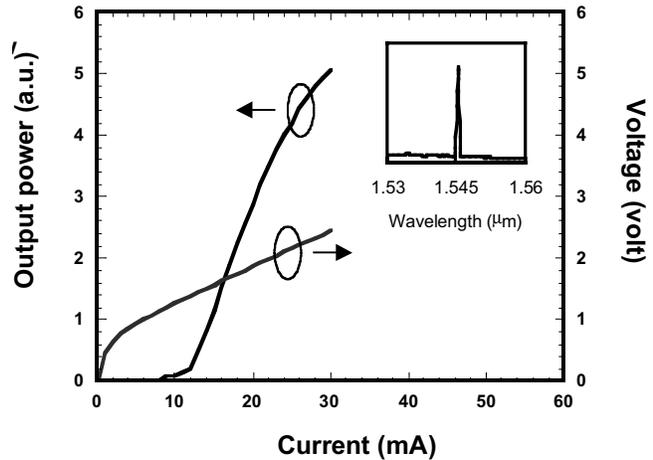


Figure 4. The room temperature I-V, L-I and lasing spectrum of a 30 μm × 30 μm VCSEL.

3.2 Task 2-Smart Pixel Development

a). HBT/P-I-N Fabrication:

The InGaP/GaAs HBTs grown under the optimized growth condition at the UIUC have demonstrated the highest dc current gain to date. We have achieved a dc current gain of 217 at collector current density of 1kA/cm² with the base sheet resistance $R_b = 262$ ohm/sq. The results (Table 1) surpassed that of Kopin (US), Ferdinand Braun Insititue (Germany), and Hitachi (Japan). The current gain to base sheet resistance ratio of 0.827 is the highest ever reported. The high current gain was accomplished by optimizing the growth of the base and emitter layer as well as tailoring the collector-subcollector doping concentration.

Table 1. HBT performance comparison.

Research group	Current gain	R_b (Ω/sq)	Gain/ R_b (sq/Ω)
UIUC	217 @ 1kA/cm²	262.3	0.827
Kopin	150 @ 1kA/cm ²	250	0.6
Hitachi	130 @ 40 kA/cm ²	250	0.52
Ferdinand-Braun-Institute	113 @ 10 kA/cm ²	200	0.56

In this work, photoreceivers using PIN/HBT are investigated for 20 Gb/s and 40 Gb/s OEIC applications. A 20-Gb/s and a 40 Gb/s short wavelength PIN/HBT photoreceivers are. Implemented using $f_T = 60$ GHz InGaP/GaAs HBT technology, PIN-TZ-1L4 has simulated 3-dB bandwidth of 17.4 GHz with 43.3 dB gain using a 25-μm diameter PIN photodetector. PIN-TZ-1L1-L using inductor peaking technique has simulated -3 dB bandwidth of 33.5 GHz with 49.3 dB gain using a 10-μm diameter PIN photodetector.

b). 20 Gb/s Photoreceiver Designs, Fabrication, and Testing:

PIN-TZ-1L4 transimpedance gain is given in Fig 5. The transimpedance gain is 43.3 dB-ohm which is equivalent to 146 ohm. The receiver -3 dB bandwidth is 17.4 GHz. PIN-TZ-1L4 is DC coupled with single-ended input and single-

ended output. The output return loss is simulated with the input open and output attached to 50-ohm load. The data is at 20-Gb/s data rate. The input data has extinction ratio of 10 dB and signal swings from 10 μ A to 100 μ A.

Figure 6 shows the layout of PIN-TZ-1L4. PIN with diameter of 25 μ m is used. The photodetectors are intentionally placed far away from the circuit to avoid the influence of the illumination on the transistors. The photodetectors are connected to the transimpedance amplifiers through coplanar transmission lines that have characteristic impedance matched to the equivalent input impedance of the transimpedance amplifiers. Figure 7 shows the layout of a 2 x 2 two-dimensional photoreceiver array for a real space interconnect. The distance between two adjacent horizontal and vertical photodetectors is 250 μ m. The total data rate is estimated to be 80 Gb/s.

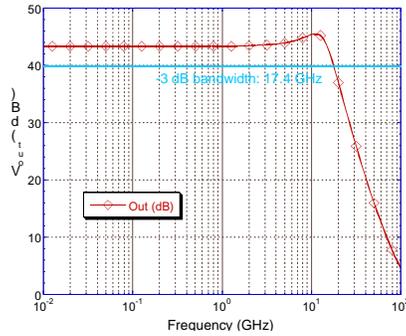


Figure 5. Simulated gain of PIN-TZ-1L4 transimpedance amplifier.

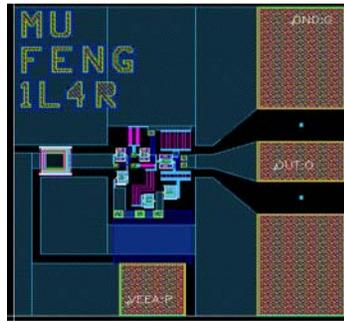


Figure 6. Layout of PIN-TZ-1L4 transimpedance amplifier.

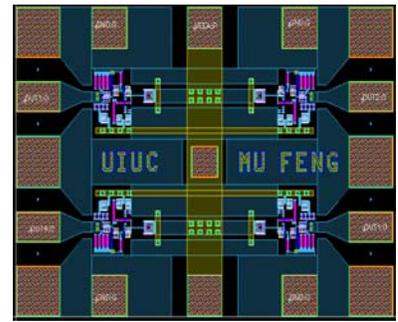


Figure 7. Layout of a 2x2 photoreceiver array.

The InGaP/GaAs chips, including the 10 to 40 Gb/s transimpedance amplifiers and photoreceivers arrays were fabricated by Network Device Inc.(NDI). Figure 8 shows the measured I-V curve for the InGaP/GaAs HBT H2. Figure 9 shows the measured Gummel plot for H2.

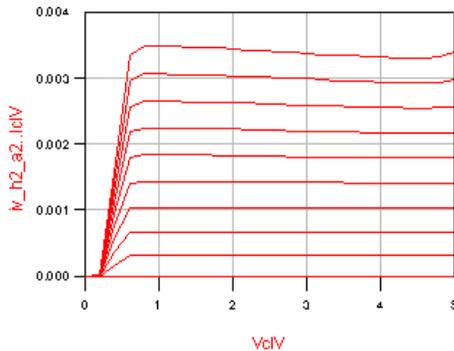


Figure 8. Measured I-V curve for InGaP/GaAs HBT H2.

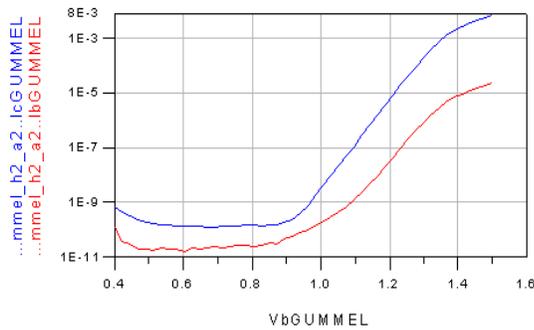


Figure 9. Measured Gummel Plot for InGaP/GaAs HBT H2.

Figures 10–12 show the tested s-parameters result of the transimpedance amplifier TZ-1A. The red line is the simulation result, and the blue line is the testing result by using a regular DC probe, while the black line shows the results with an improved DC probes with various capacitances on the probe needle. From the experimental results shown below, we can see the bandwidth of TZ-1A is around 8GHz and S21 is 8dB, which is close to design specification. The corresponding transimpedance gain is 44 dB Ω . S22 is less than -20dB, which makes the output impedance fairly close to 50 Ω .

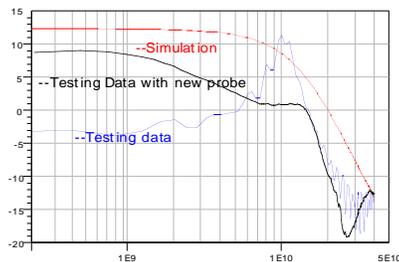


Figure 10. Measured S21 of TZ-1A.

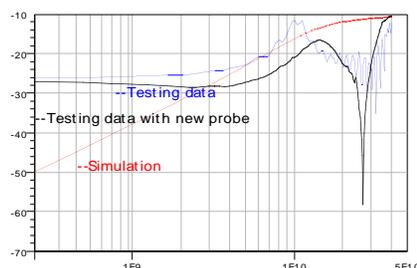


Figure 11. Measured S22 of TZ-1A.

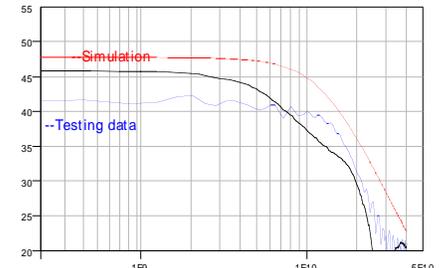


Figure 12. Measured gain of TZ-1A.

We also did the eye-diagram testing. The testing setup is shown on Figure 13. In this projectment, we did the electrical input and electrical output (E/E) eye-diagram. The test set has a measurement upper limit of 3GHz. Figure 14 shows an eye of TZ-1L with PBRS of 2¹⁵-1 pattern. The input data has amplitude of 500mV with high level at -3V. The eye is widely open with low jitter. The bit-error-rate calculated from this eye-diagram is lower than 10⁻¹⁵. It suggests our circuit should be able to work on speed higher than 3Ghz.

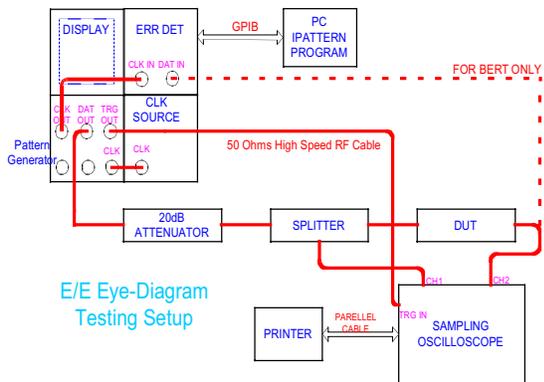


Figure 13. E/E Eye-diagram test setup.

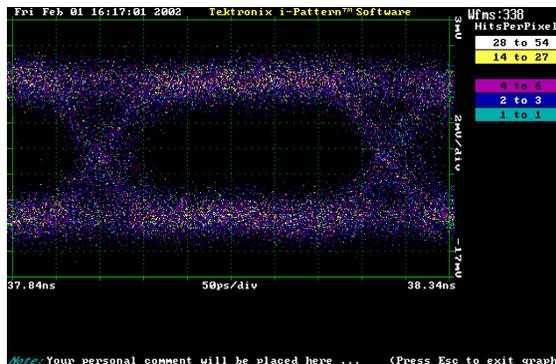


Figure 14. Measured eye diagram of TZ-1L.

3.3. Task 3-Heterogeneous Materials Integration

The goal of this research was to develop a bonding technique for the integration of an array of VCSELs to a photodetector array. The bonding would need to be performed at reasonably low temperatures (<450 °C) so that the process would not affect the performance of the sensitive devices. The bonding would also need to be electrically conductive and take up as little area as possible. For these purposes, a flip-chip bonding technique was investigated. In the flip-chip bonding process, a metallic solder is selectively deposited in certain areas referred to as bond pads. Bond pads of two separate samples are then brought together and the samples are heated to a point in which the solder on both samples melts together forming a conductive bond. The metal combinations that were used as the solders in this experiment are Sn/In, Sn/Zn, and Sn/Au. Lead was avoided as a solder material for environmental reasons. The process parameters that were investigated in these experiments were ease of processing, resistance of bonds, and temperature of bonding process.

Metals were deposited in thickness to target eutectic points in which the melting point would be at a minimum. Sn/In had a eutectic temperature of approximately 117 °C at a composition of 48 at. % Sn. This was the lowest melting point for any of the three solders. For Sn/Au combinations a composition of 72 at. % Sn was used and a composition of 60 at. % Sn was used for Sn/Zn. All metals were deposited by thermal evaporation and final thickness of the solder combinations were varied between about 1 and 2 μm. Thus the final bonded unit would have a gap distance up to 4 μm. These extremely thick metal depositions were necessary so that the gap between bonded samples would exceed the height of any device arrays being bonded. The VCSELs that would be bonded for this project were estimated to be as much as 2-μm tall. Initially there was some difficulty with the sticking of Sn/Zn and Sn/Au solders, however these problems were solved by that deposition of a thin Ti layer prior to solder deposition.

A simple mask was designed to simulate a 4x8 bonding array. Two different patterns were developed on the mask to process the top and bottom samples in the bonded pair. These patterns can be seen in Fig. 15.

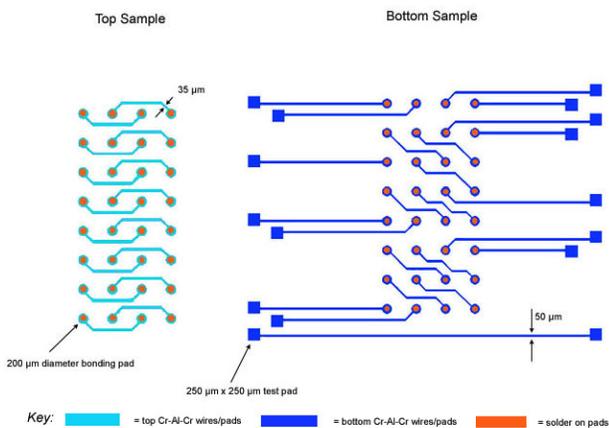


Figure 15. Masks of the 4x8 solder-array testing pad.

In Fig. 16, the results of the mask pattern are seen after bonding. A Nomarski optical micrograph of two glasses intentionally mis-aligned is shown in Fig. 17 to show the metal bonds. With this simple design it is possible to measure conduction through 2, 4, 6, and 8 bonds. At the very bottom of the mask patterns is a conduction path that does not pass through any bonds. The purpose of this pattern is to measure and calculate the resistance of the metal wire paths so that these results may be subtracted and the actual resistance of the bonds calculated. With the use of Sn/In as a solder, samples could be repeatedly bonded. Si was bonded to Si, glass was bonded to glass, and glass was bonded to Si. Using the simple mask design described above, the resistance of the bonds could be calculated. All bonds in the 4x8 array had bonded successfully with an average bond resistance of 0.75 Ω /bond as shown in Fig. 18.

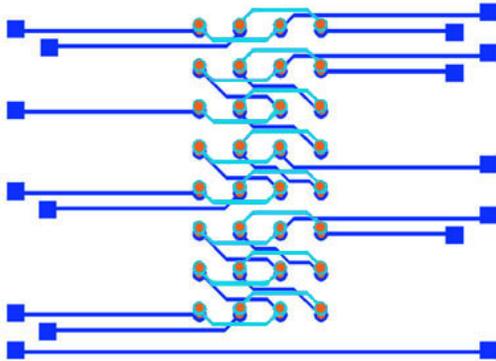


Figure 16. Overlay of top and bottom 4x8 solder pad.

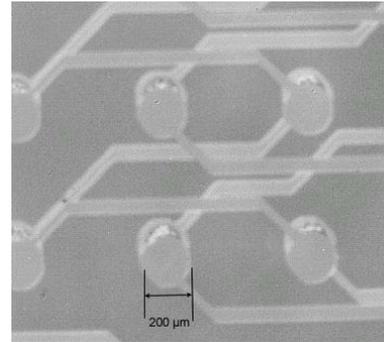


Figure 17. Normarski photograph of two pieces of glass bonded together. The sample is intentionally misaligned to show the bottom solder.

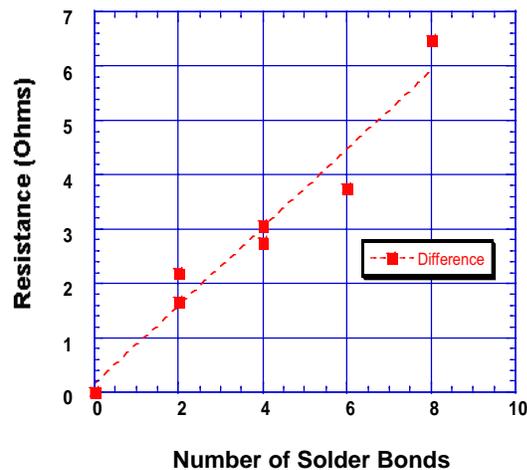
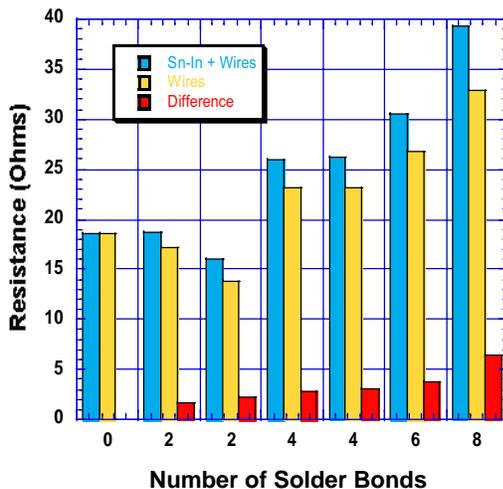


Figure 18. Measurement of solder ball resistance

3.4. Task 4-Avalanche Photodiode Array Development

During this program, the most significant advance was to model, and then demonstrate extremely low cost, high performance integratable avalanche photodiodes for use at long wavelengths based on our proprietary floating guard ring (FGR) planar structure. These InP/InGaAs separate absorption, grading and multiplication (SAGM) APDs operate at 10Gb/s. The advance comes from the finding that by appropriate design, the APDs can be made, for the first time, at extremely high yields and low cost, literally dropping the bottom out of the cost of APDs used at long-wavelengths from a few hundred dollars to <\$10 each! This technology was then successfully transferred to the industrial sector (Sensors Unlimited) who have been able to produce the APDs in very large quantities (tens of thousands). More importantly for the future of VLSI-photonics, Sensors Unlimited then went on to demonstrate large 2D arrays of APDs with no pixel drop outs, and extremely uniform breakdown voltages across the array. To my knowledge, this is the first time that APD arrays have been demonstrated, and is simply a result of the careful modeling and design of the FGR SAGM APD afforded by this program. It is difficult to over estimate the importance of this result on future, high density optical systems since APDs provide significant sensitivity advantages over alternative detection schemes, yet APDs, first successfully demonstrated

by the PI in 1981 for application to long wavelength systems, have always been prohibitively expensive and hence have not penetrated deeply into the optical fabric.

In other advances, we demonstrated the highest efficiency 40GHz detectors using our asymmetric twin waveguide technology, resulting in $\sim 1\text{A/W}$ sensitivity at a wavelength of 1.55 microns. This too is a significant improvement over previous attempts at demonstrating very high bandwidth and sensitive detectors. This technology was transferred successfully to ASIP, Inc.

Finally, considerable effort was devoted to demonstrating APD receivers based on integrating InAlAs/InGaAs SAM APDs with InP/InGaAs HEMTs. The receiver bandwidth was 5GHz. This integration work was only moderately successful, and it was our conclusion that flip-chip bonding of the detector and receiver is ultimately the most high yield, and simplest process. Indeed, our industrial partner, Sensors Unlimited, has made a large business out of high yield flip chip bonding of detector arrays to multiplexer circuits, and work during this program with them on this particular program is extremely promising. Undoubtedly, this is the solution in both the near and long term for VLSI photonic applications. In addition to the integration work, we explored the performance of InAlAs/InGaAs SAM APDs as a lower noise alternative to conventional InP/InGaAs SAGM-APDs. Indeed, we found that such was the case, with ionization coefficient ratios of $k\sim 0.2$ as opposed to 0.4-0.5 for InP. This suggests that an optimum gain of the InAlAs, and bandwidth of these same devices is improved by a factor of two, while the excess noise is halved compared to InP.

4 LIST OF PUBLICATIONS:

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1. J. H. Ryou, R. D. Dupuis, G. Walter, N. Holonyak, Jr., D. T. Mathes, R. Hull, C. V. Reddy, and V. Narayanamurti, "Properties of InP Self-Assembled Quantum Dots Embedded in $\text{In}_{0.49}(\text{Al}_x\text{Ga}_{1-x})_{0.51}\text{P}$ for Visible Light Emitting Laser Applications Grown by Metalorganic Chemical Vapor Deposition," J. Appl. Phys. (to be published).
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3. C. V. Reddy, V. Narayanamurti, J. H. Ryou, and R. D. Dupuis, "Current Transport in InP/ $\text{In}_{0.5}(\text{Al}_{0.6}\text{Ga}_{0.4})_{0.5}\text{P}$ Self-Assembled Quantum Dot Heterostructures Using Ballistic Electron Emission Microscopy/Spectroscopy," Appl. Phys. Lett. (to be published).
4. R. D. Dupuis, J. H. Ryou, R. D. Heller, C. V. Reddy, V. Narayanamurti, D. T. Mathes, R. Hull, G. Walter, and N. Holonyak, Jr., "InP Self-Assembled Quantum Dots Embedded in InAlGaP Grown by Metalorganic Chemical Vapor Deposition," Proceedings of Symposium H, 2001 Fall MRS Meeting, Boston MA (to be published).

5 SCIENTIFIC PERSONNEL:

5.1 PI's:

K. Y. Cheng, R. D. Dupuis, M. Feng, S. R. Forrest, N. Holonyak, Jr., and K. C. Hsieh

5.2 Graduate students:

K. L. Chang, T. Chung, J. Epple, J. Feng, Q. He, R. Heller, H. C. Lin, G. W. Pickrell, J. H. Ryou, J. Thomson, G. Walter, J. Wei

5.3 Honors and Awards:

- a. Professor Milton Feng received Outstanding Research Award in High Speed Microelectronics, Dr. Pan Wen Yuan Foundation, Taiwan, September 2000.
- b. Professor Milton Feng was named Nick Holonyak, Jr. Professor in Electrical and Computer Engineering at the University of Illinois.
- c. Professor K. Y. Cheng was elected to a Fellow of the IEEE.
- d. Professor N. Holonyak, Jr. received Frederic Ives Medal of OSA (2001).
- e. Professor Stephen Forrest received 2001 IEEE/LEOS Wm. Streifer Award.

5.4 Degrees Awarded:

- a. T. Chung, "High-gain InGaP/GaAs heterojunction bipolar transistors by low-pressure metalorganic chemical vapor deposition." MSEE, UIUC, 2000.
- b. G. W. Pickrell, "Growth and optimization of GaInAs-InP heterostructures by solid-source MBE," MSEE, UIUC, 2000.
- c. J. H. Ryou, "III-phosphide semiconductor self-assembled quantum dots grown by metalorganic chemical vapor deposition." Ph.D., U-Texas at Austin, 2001.
- d. J. Mu, "Monolithic High-Speed Optoelectronic Integrated Receivers for Greater than 10 Gigabits per Second Optical Communications", Ph.D., University of Illinois at Urbana-Champaign, 2000
- e. K.L. Chang, "Lateral Oxidation of Aluminum Gallium Arsenide Compound for Defects Reduction and Optical Applications", MSEE, UIUC, 2000
- f. J. Epple, "Low temperature wafer bonding using amorphous gallium arsenide", M.S., University of Illinois at Urbana-Champaign, 2001.
- g. John Thomson, "Integratable Long Wavelength Detectors and Electronics for Communications and Sensing", Ph.D., Princeton University, 2001
- h. Jian Wei, "Photodetectors Based on Novel Materials and Structures for Fiber Optical Communications and Long Wavelength Sensing", Ph.D., Princeton University, 2001
- i. Jae Hyun Ryou, "III-Phosphide Semiconductor Self-Assembled Quantum Dots Grown by Metalorganic Chemical Vapor Deposition", Ph.D., U-Texas at Austin, 2000.
- j. David E. Wohlert, "Temperature invariant photoluminescence and gain spectra of strained Gallium-Indium-Arsenide quantum wires," Ph.D., UIUC, June 2000.
- k. Gregory William Pickrell, "Compliant epitaxy of III-V compound semiconductors for optoelectronic device applications," Ph.D., UIUC, May 2002.
- l. Hung-Cheng Lin, "Design and fabrication of long-wavelength vertical-cavity surface-emitting lasers using wafer bonding technologies," Ph.D., UIUC, December 2002.

6 REPORT OF INVENTION:

- a. N. Holonyak and R. D. Dupuis: Provisional patent filed on quantum-well-assisted quantum-dot photonic devices (lasers, LEDs, etc.)

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