14. ABSTRACT

In this presentation, the major issues, which confronted the formation of very thin layers of silicon (30-100 nm) on sapphire substrates for application to sub 100-nm device technology, will be reviewed. The focus of the investigation was, and still is, to achieve a structure in which the modern CMOS technology, the mainstay technology and workhorse of the electronic revolution, can be affordably implemented. In this context, one approach to the obtention of crystalline, device-quality thin film silicon-on-sapphire (TFSOS), namely the double Solid Phase Epitaxy (DSPE), has achieved truly outstanding results which are presently incorporated into high-performance products, such as phase-locked loop (PLL) ICs for wireless communication, and analog-to-digital converters for space application.

Presented at the Lateral Epitaxial Overgrowth Workshop, Juneau, Alaska, August 2-6, 1999.

16. SUBJECT TERMS

thin film silicon-on-sapphire (TFSOS)
chemical vapor deposition (CVD)
Silicon-on-Sapphire

Abstract

The early sixties were at the beginning of the electronics revolution where silicon integrated circuits built their current dominance, fundamentally and pervasively on tailor-made materials, starting at the atomic level. Thin-film deposition techniques, particularly chemical vapor deposition (CVD) and molecular-beam epitaxy (MBE) were developed to provide control over material constituents "in atomic amounts", in order to form the active part of high-performance devices. Nonetheless, the CVD techniques failed to provide a crystalline silicon structure amenable to advanced devices on insulating substrates, particularly sapphire.

In this presentation, the major issues, which confronted the formation of very thin layers of silicon (30-100 nm) on sapphire substrates for application to sub 100-nm device technology, will be reviewed. The focus of the investigation was, and still is, to achieve a structure in which the modern CMOS technology, the mainstay technology and workhorse of the electronic revolution, can be affordably implemented. In this context, one approach to the obtention of crystalline, device-quality thin film silicon-on-sapphire (TFSOS), namely the double Solid Phase Epitaxy (DSPE), has achieved truly outstanding results which are presently incorporated into high-performance products, such as phase-locked loop (PLL) ICs for wireless communication, and analog-to-digital converters for space application.

Besides the materials properties, devices’ performances ($f_t >100$GHz) and circuits’ applications (analog and mixed signals), present investigations aimed at producing stressed layers of Si$_{1-x}$Ge$_x$ ($x>0.75$) grown on TFSOS will also be described. Based on the present results, TFSOS could become entrenched, as CMOS, as new materials and devices appear – witness the recent success in developing highly-engineered structures with SiGe on TFSOS (hole mobility, through Hall measurements, is in excess of 800 cm$^2$/V.sec) – using the established industrial infrastructure.

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Lateral Epitaxial Overgrowth Workshop
Silicon-on-Sapphire Technology

Juneau, Alaska--August 2-6, 1999

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• Introduction — A historical perspective
• The Vision: Thin Film Silicon on Sapphire
• Comparison with other SOI alternatives
• Recent results for SiGe – The march of Technology
• Prognosis-Trend
• Conclusion
Collaborators

- Space and Naval Warfare Systems Center, San Diego
- University of California at San Diego (UCSD)
- International Business Machines (IBM)
- Auburn University
- Oklahoma State University
- Saphikon
- Lawrence Semiconductor
- Massachusetts Institute of Technology (MIT)
- Lincoln Laboratory
- University of Florida, Gainesville
- Peregrine Semiconductor Corporation
- Northup Grumman
- Rockwell International (Science Center)
Conventional Microelectronics
A Historical Perspective

Bulk Silicon

SOURCE GATE DRAIN

 Parasitic Capacitor

Silicon on Sapphire (SOS)

SOURCE GATE DRAIN

 MOS

Sapphire

Parasitic Capacitor

 BIPOLAR

Parasitic Capacitor

Sapphire

Thin Film Silicon on Sapphire

TEM Images: Before & After Improvement Process

Before Improvement

After Improvement
Thin Film Silicon on Sapphire
The Vision

Scaling Limits

Low-Field Hole Mobility
\( t_{Si} = 100\text{nm} \)

Low-Field Electron Mobility
\( t_{Si} = 100\text{nm} \)

G.A. Garcia, R.E. Reedy. 

M. Roser, *et al.*. 50th Device Research Conference, June 22-24, 1992
ULTRATHIN SOS Improvement and Thinning Sequence

1) CVD Silicon as Grown

2) Si implant

3) Two-Step Anneal
   a) 550 °C SPE Regrowth
   b) 900 °C Defect Removal

4) Thermal Oxidation

5) Strip Oxide (HF)

Final Product:
Device Quality Single Crystal Silicon Film Under Compressive Strain

RBS Data, TFSOS

Auger Analysis, TFSOS

Thin Film CMOS/SOS vs. Other Silicon Implementations

Relative to Bulk CMOS
- Reduced parasitic capacitances
  - less junction capacitances and higher speed)
- Reduced short channel effects
- Better device isolation
  - Latchup suppression
  - Lower body effect
  - Wider operating temperature
- Simple mesa fabrication
- Radiation hardness

Relative to SIMOX/BESOI
- Lower loss dielectric substrate
  - Lower substrate capacitance
  - Higher Q passive elements
- Lower minority carrier lifetime
  - Parasitic bipolar suppressed
  - Higher S-D breakdown voltage
- Higher thermal conductivity than SiO₂
  - Reduced self-heating effects
- Enhanced hole transport properties
  - PMOS closer to NMOS in size, $f_T$, $f_{Max}$
  - Enhanced CMOS performance
- 6-in wafers available, 8-in also available
- Lower cost/Process Simplicity
- Much reduced Floating Body Effect
  - Low leakage Ioff (digital)
  - No Kink Effect in I-V (analog)
- No Transient Hysteresis (low frequencies)
Thermal Effects
Thin Film Silicon on Sapphire vs. SIMOX

$W_{eff} = 10 \mu m$
$L_{eff} = 0.3 \mu m$
$T_{st} = 70 \text{ nm}$
$T_{ox} = 10 \text{ nm}$
$T_{box} = 360 \text{ nm}$
$N_{sub} = 3 \times 10^{17} \text{ cm}^{-3}$

SOS Data:
M. Wetzel, UCSD Ph.D.
Thesis (to be published)

MIT data;
Courtesy Prof. D. Antoniadis
Radiation data for TFSOS MOSFETs

**TFSOS NMOSFET**

- Size: $4.2 \times 0.6 \, \mu m$
- Rad Bias: $V_{gs}=0 \, V$, $V_{ds}=3 \, V$
- Dose Rate: 100 krad(SiO$_2$)/min
- Measurement Bias: $V_{ds}=3.3 \, V$

**TFSOS PMOSFET**

- Size: $50 \times 0.6 \, \mu m$
- Rad Bias: $V_{gs}=0 \, V$, $V_{ds}=-3 \, V$
- Dose Rate: 100 krad(SiO$_2$)/min
- Measurement bias: $V_{ds}=-3.3 \, V$

---

**n-MOSFET**

**p-MOSFET**
Thin Film Silicon on Sapphire

- T-Gate used to decrease $R_g$
- Record high $f_t$, $f_{\text{max}}$ microwave transistor
- Record low noise microwave transistor

$$f_{\text{max}} = \frac{f_t}{2 \sqrt{2 \pi f_t R_g C_{gd} + G_o [R_g + R_s]}}$$

$$F_{\text{min}} = 1 + k L f \sqrt{g_m [R_s + R_g]}$$

<table>
<thead>
<tr>
<th>Device</th>
<th>$L_{g, \text{drawn}}$ (μm)</th>
<th>$f_t$ (GHz)</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>@ 2GHz</th>
<th>$F_{\text{MIN}}$ (dB)</th>
<th>$G_a$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.5</td>
<td>25</td>
<td>66/11</td>
<td>0.9</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>PMOS</td>
<td>0.5</td>
<td>14</td>
<td>41/7</td>
<td>0.9</td>
<td>13</td>
<td></td>
</tr>
</tbody>
</table>

# NOISE COMPARISON

<table>
<thead>
<tr>
<th></th>
<th>2 GHz</th>
<th></th>
<th>8 GHz</th>
<th></th>
<th>12 GHz</th>
<th></th>
<th>Lg(μm)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F_min</td>
<td>G_a</td>
<td>F_min</td>
<td>G_a</td>
<td>F_min</td>
<td>G_a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TFSOS: NMOS[9]</td>
<td>0.9</td>
<td>21</td>
<td>1.4</td>
<td>11</td>
<td>1.8</td>
<td>8.5</td>
<td>0.5</td>
<td>TF SOS</td>
</tr>
<tr>
<td>TFSOS: PMOS[9]</td>
<td>0.9</td>
<td>13</td>
<td>1.3</td>
<td>4.7</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>TF SOS</td>
</tr>
<tr>
<td>Other Si:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMOS [1]</td>
<td>1.5</td>
<td>18</td>
<td>3.25</td>
<td>8.5</td>
<td>-</td>
<td>-</td>
<td>0.25</td>
<td>MICROX</td>
</tr>
<tr>
<td>PMOS [1]</td>
<td>2.7</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.25</td>
<td>MICROX</td>
</tr>
<tr>
<td>NMOS [2]</td>
<td>0.8</td>
<td>17</td>
<td>1.6</td>
<td>9.8</td>
<td>2.2</td>
<td>6.8</td>
<td>0.6</td>
<td>MICROX</td>
</tr>
<tr>
<td>NMOS [3]</td>
<td>5.0</td>
<td>6.4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.0</td>
<td>BESOI</td>
</tr>
<tr>
<td>Other:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HBT [4]</td>
<td>0.5</td>
<td>12</td>
<td>0.8</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>2 x 6 x 8</td>
<td>SiGe</td>
</tr>
<tr>
<td>HBT [5]</td>
<td>0.46</td>
<td>11.6</td>
<td>1.4</td>
<td>-</td>
<td>2.0</td>
<td>-</td>
<td>3.5 x 3.5</td>
<td>InP/lnGaAs</td>
</tr>
<tr>
<td>PH[6]</td>
<td>0.2</td>
<td>-</td>
<td>.33</td>
<td>-</td>
<td>0.41</td>
<td>13</td>
<td>0.15</td>
<td>GaP/lnGaAs</td>
</tr>
<tr>
<td>JFET [7]</td>
<td>0.4</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>GaAs</td>
</tr>
<tr>
<td>MESFET [8]</td>
<td>0.4</td>
<td>23</td>
<td>0.5</td>
<td>15</td>
<td>0.5</td>
<td>13</td>
<td>0.11</td>
<td>GaAs</td>
</tr>
</tbody>
</table>

1. EDL, May 1993, pg. 219, Hanes et al.
2. MTT-S Workshop, May 1995, Agarwal et al.
8. TED, Feb 1999, pg. 310, Kimo et al.
Noise Figure Results for Different Technologies: Transistors and LNAs

Noise figures of FET’s based on GaAs and of Si CMOS transistors.

![Graph showing noise figure results for different technologies.](image)

Recent Results on Low Noise Amplifier Designs

<table>
<thead>
<tr>
<th>Technology</th>
<th>F (GHz)</th>
<th>NF (dB)</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 micron GaAs FET</td>
<td>1</td>
<td>2.2</td>
<td>Cioffi, IMMCS, 1992</td>
</tr>
<tr>
<td>1 micron GaAs FET</td>
<td>1.6</td>
<td>2.2</td>
<td>Cioffi, IMMCS, 1992</td>
</tr>
<tr>
<td>0.3 micron GaAs FET</td>
<td>1.9</td>
<td>2.0</td>
<td>Nakatsugawa, GaAs-IC Symp., 1993</td>
</tr>
<tr>
<td>1 micron GaAs FET</td>
<td>1.9</td>
<td>1.5</td>
<td>Heaney, GaAs-IC Symp., 1993</td>
</tr>
<tr>
<td>0.3 micron GaAs FET</td>
<td>1.6</td>
<td>2.5</td>
<td>Imai, IEEE-Trans. MTT, 1991</td>
</tr>
<tr>
<td>0.5 micron CMOS</td>
<td>0.9</td>
<td>2.2</td>
<td>Karanicolas, ISSCC, 1996</td>
</tr>
<tr>
<td>1 micron CMOS</td>
<td>0.9</td>
<td>3.5</td>
<td>Rofougaran, IEEE-JSSC, 1996</td>
</tr>
<tr>
<td>0.6 micron CMOS</td>
<td>1.5</td>
<td>3.5</td>
<td>Shaefver, IEEE-JSSC, 1997</td>
</tr>
<tr>
<td>0.5 micron CMOS/SOS</td>
<td>2.4</td>
<td>2.2</td>
<td>Johnson, R.A. et al., IEEE-TED, 1998</td>
</tr>
</tbody>
</table>
Thin Film Silicon on Sapphire
Wireless Communications Applications

- Demonstrate SOS technology application to L and S band Applications

- Test Vehicle: 2.4 GHz transceiver
  - Power Amplifier M. Wetzel et al., 1st Annual UCSD Conference on Wireless Communications, March 8-10, 1998
Why CMOS/SOS at Microwave/RF Frequencies

• Low power, high noise immunity
• Cost
  • High integration level (VLSI) / Mature technology
    ➢ Competitive manufacturing cost (7-10% higher than CMOS bulk Si)
    ➢ Complexity => Low cost per functional unit
    ➢ 6” wafers available with low defect density
  • Reduced processing steps (mesa isolation)
    ➢ Much lower cost than bipolar, HBTs (Si or III-V’s)
  • Inexpensive material (except vs. bulk silicon)
  • Leverage off Si manufacturing base
• Mixed analog / digital integration
  • Low loss dielectric substrate (isolation/ no latch up)
    ➢ Low substrate capacitance
    ➢ High Q passive elements
  • $f_{\text{max}} = 66$ GHz ($L_{\text{eff}} \sim 0.3 \mu m$), Noise Figure $< 1$ dB optically defined devices
  • $f_t > 100$ GHz ($L_{\text{eff}} \sim 0.1 \mu m$) (x-ray)
  • Very high linearity at low power (good IP3)
  • Excellent ESD protection with low parasitics
• SiGe/SOS, $m_h > 800$ cm$^2$/V.sec (pMODFET, $L_g = 0.1 \mu m$, $g_m = 420$ mS/mm)
  ➢ much higher speed CMOS with lower power
Why CMOS/SOS at Microwave/RF Frequencies

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  - Excellent ESD protection with low parasitics
- SiGe/SOS, $m_h > 800 \text{ cm}^2/\text{V} \cdot \text{sec}$ (pMODFET, $L_g = 0.1 \mu\text{m}$, fabricated; to be published)
  - $\Rightarrow$ much higher speed CMOS with lower power
Circuit Level SOS rf Results

FY98 Circuits Test Results
LNA, MIXER and T/R Switch Fabricated in TFSOS

<table>
<thead>
<tr>
<th>MEASURED</th>
<th>Operating Freq</th>
<th>Gain</th>
<th>NF (50 Ω)</th>
<th>IP3 (output)</th>
<th>Power@vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>2.4 GHz</td>
<td>11 dB</td>
<td>2.2 dB</td>
<td>14 dBm</td>
<td><a href="mailto:13.2mW@1.5V">13.2mW@1.5V</a></td>
</tr>
<tr>
<td>Mixer</td>
<td>Center=2.4 GHz</td>
<td>-5 dB</td>
<td></td>
<td>5 dBm</td>
<td><a href="mailto:8.4mW@1.5V">8.4mW@1.5V</a></td>
</tr>
<tr>
<td></td>
<td>IF=250 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Record high $f_t$ (> 105 GHz)
- CMOS inverter delay < 8 psec at RT; 6 psec @ 77K, close to JJ speed;
- Record low noise (0.9 dB NF @ 2GHz), resulting in low noise front end
  => MAKES HIGH SPEED, HIGH RESOLUTION A/DC possible
- Record BW (10 GHz) for distributed amplifier
TFSOS vs. TFSOI RF Data

C. Wann et al. ISSCC, Feb. 1998
C. Wann et al. EDL, 18(12), pg. 625-627, Dec. 1997

Unloaded 3-way NAND Delay vs. $V_{dd}$

Delay per Stage vs. $V_{dd}$
COMPARATIVE STUDY of CMOS on TFSOS vs. SIMOX vs. BULK SILICON
Accomplishment

Objective:
- Determine the comparative CMOS-based alternatives (bulk Si, SIMOX, TFSOS) to implement low power, high frequency, cost-effective VLSIC technology at \( \leq 100 \text{nm} \) regime in an environment conducive to manufacturing.

Accomplishment:
- Test vehicle: 4-bit, 10 Gsps A/DC.

<table>
<thead>
<tr>
<th>Comparator Bank Delay ( t_d \text{Ln} 2^n ) (pS)</th>
<th>Bubble Detector Delay (pS)</th>
<th>Encoder Latch Delay (pS)</th>
<th>Total Delay (pS)</th>
<th>Clock ( f_{\text{max}} ) (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS/Si Bulk 108</td>
<td>47</td>
<td>76</td>
<td>231</td>
<td>4.1</td>
</tr>
<tr>
<td>CMOS/SIMOX 86</td>
<td>37</td>
<td>60</td>
<td>183</td>
<td>5.5</td>
</tr>
<tr>
<td>CMOS/TFSOS 56</td>
<td>29</td>
<td>46</td>
<td>131</td>
<td>7.5-8</td>
</tr>
</tbody>
</table>

\( f_{\text{max}} = 10 \text{ GHz} \) goal; \( f_{\text{max}} = 7.5-8 \text{ GHz} \) experimental
13-GHz Tuned Amplifier

- Demonstrated Functional Samples (Body-Tied and Floating Body) on Bulk, SOI, and SOS wafers.
- The Peak Gain is ~15dB for SOS Samples.
- Amplifiers with Floating Body have ~5dB Higher Gains.
- Bulk Samples Have Less than 0dB Gain
- SOS Samples Have Significantly Better Characteristics than SOI and Bulk Samples.

Transducer Power Gain & Noise Figure
PD Floating-Body SOS and SOI
13-GHz Tuned Amplifier

S21 (SOI) < NF (SOI)
Distributed Amplifier

Brodest bandwidth ever reported for any Si-FET distributed amplifier
300 μm gate width, 4 stages

Schematic

Photograph of Amplifier

Power measurements at 1, 2, 5, & 10 GHz
NEAR FUTURE

Fabrication in Progress:
• LNAs, Mixers, VCOs for operation @18-40 GHz
• System-on-a-Chip @18 GHz
• Single-chip GPS receivers (~80-100 dB isolation)-SBIR '99
  • SiGe p-FET (> 100 GHz) & Logic

<table>
<thead>
<tr>
<th>SIMULATED</th>
<th>Operating Freq</th>
<th>Gain</th>
<th>NF (50 Ω)</th>
<th>IP3 (output)</th>
<th>Power@vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>18 GHz</td>
<td>15 db</td>
<td>3 dB</td>
<td>5dBm</td>
<td><a href="mailto:22mW@1.5V">22mW@1.5V</a></td>
</tr>
<tr>
<td>LNA/Differential</td>
<td>18 GHz</td>
<td>22 db</td>
<td>3.7</td>
<td>10 dBm</td>
<td>60mW@1.5</td>
</tr>
<tr>
<td>Mixer</td>
<td>Center=16-20GHz</td>
<td>7 db</td>
<td>10 dB</td>
<td>5dBm</td>
<td>40mW@1.5</td>
</tr>
</tbody>
</table>
Thin-film Silicon-on-Sapphire Characteristics

• Lower capacitance --> higher speed at lower power
• Fully depleted operation --> improved low voltage performance (esp. w.r.t. bipolar)
• Lower minority carrier lifetime
  • Parasitic bipolar suppressed
  • Higher S-D breakdown voltage
• Enhanced PMOS --> higher hole mobility than bulk Si, due to compressive stress (valence band splitting); better design flexibility for low power CMOS over GaAs (no p-channel)
• Excellent rf performance
  • $f_t > 100$ GHz for 0.1 $\mu$m $L_{\text{eff}}$ n-type transistors
  • $f_{\text{max}} > 66/45$ GHz for .4 $\mu$m n/p-channel
  • Extremely low-loss substrate at rf (loss tangent < .0001)
• No parasitic coupling to substrate for passive components
• Good thermal conductivity
  • Higher than SiO$_2$
  • Comparable to GaAs
UHV/CVD Grown FET Structures

- SOS layer is compressively strained ~ 0.35%
- Remains ~ 0.30% strained after UHV/CVD growth
- Low density of misfit dislocation at the Si/Al$_2$O$_3$ interface


X-ray diffraction

Planar-view TEM

Cross Section

No misfit dislocations observed in thinner regions
Misfit dislocations observed in thicker regions

Arrows point to Si/Al$_2$O$_3$ interface where misfit dislocations end
Triple-Axis X-Ray Diffraction Measurements

- Measured thickness and strain of Si layer, thickness and alloy composition of SiGe layer, and thickness of Si cap layer
- Showed that interdiffusion of Si and Ge at Si/SiGe interfaces occurs during thermal annealing at 850°C
- Demonstrated that SiGe layer structures were degraded by device fabrication processes at $T > 800°C$
  → Low temperature processing required

Ge concentration in strained SiGe Layer over time at 850°C

SiGe strained layer thickness over time at 850°C
SiGe FETs on Silicon-on-Sapphire Substrates

- **SiGe p-MOSFET Devices (Ge 20-30%)**
  - Hole mobilities 30 to 50% higher, up to 200 cm²/V-s

- **New Approach: p-MODFET Devices**
  - Room temperature hole mobilities up to 1050 cm²/Vs in modulation doped structures on bulk Si
    (K. Ismail et al., Appl./ Phys. Lett. 64, 3124 (1994))
  - $f_t = 70$ GHz for p-MODFETs on bulk Si
    (M. Arafà et al., Electron Devices Lett. 17, 586 (1996))
Modulation-doped p-FET layers on SOS

Strained Si$_{1-x}$Ge$_x$ device layer with unique profile, $x>0.75$

Uniform relaxed buffer layer Si$_{0.65}$Ge$_{0.35}$

Step-Graded buffer layers

Starting silicon surface

Sapphire substrate

Hole mobility (300K): 804 cm$^2$/V sec
Sheet hole density: $2.5 \times 10^{12}$ cm$^{-2}$

Active device layers are grown on top of a strain-relaxed SiGe buffer layer: total epi thickness approx. 1 micron

Mobility and Sheet Hole Density vs. T

- Gov31.6
  - 300K: $\mu=804$ cm$^2$/V sec, $N_s=2.93 \times 10^{12}$
  - 20K: $\mu=2243$ cm$^2$/V sec, $N_s=2.45 \times 10^{13}$
Nomarski image of p-MODFET wafer surface

Gov32.6: 4” Union Carbide SOS substrate
Gov32.8: 4” bulk silicon

- If not well-improved, large pits occur after SiGe growth at macro-twin defects in original SOS layer;
- Low defect density in SOS substrate required
- Wafer bonding methods have the potential to produce SOS substrates with
  - zero microtwin defects;
  - threading defect densities reduced by many orders of magnitude;
  - thin relaxed SiGe buffer layers on sapphire (required for fully depleted FETs)
Closing Thoughts

- TFSOS addresses present and long-term issues and needs in battery-operated wireless communication and S to K-band (~40 GHz) applications providing unique solutions for low power System-on-a-Single-Chip, integrating analog and digital functions
- Focus of present and near-term
  - Strained SiGe (>75% Ge) on SOS to achieve high $\mu_h$
    - $1/f_{p\text{-SiGe/SOS}} < 1/f_{p\text{-SiGe/Si}}$
    - Mixers with lower phase noise
  - $f_t$, $f_{\text{max}}$ highest ever, for low power CMOS and high performance A/DCs
- SiGe p-FETs with greater or similar n-FET mobility will significantly reduce device size/chip area
  - higher CMOS performance products ($f_t$, $f_{\text{max}} > 100$-200 GHz), for reduced system cost, using industrial IC infrastructure
- QHD simulation predicts similar device transconductance for SiGe on SOS FETs and AlGaAs/GaAs HEMTs (Prof. David Ferry, ASU, Seminar UCSD, May 26, 1998)
- World highest hole mobility (804 cm$^2$/V.sec @300 K) measured on modulation-doped p-FET structure on TFSOS substrate
- MOSIS accepts TFSOS designs
The Future

- Extend performance of silicon technology to K-band, benefiting from established industrial infrastructure resulting in lower cost

- TFSOS technology for digital and analog devices
  - 10 times lower power x delay product than conventional bulk technologies benefits in, e.g.,
    - Real-time sensor information processing
    - Radar image processing
    - Digital communication
  - Another factor of 5 reduction with low $V_{dd}$
    - Deployable/Unattended situation awareness systems
    - Extended operation of all battery-powered systems
  - 10x greater immunity to SEU which benefits
    - All space based electronics

- TFSOS, a technology to implement advanced components, such as A/D converters, and single chip wireless communication systems
The Future

• Extend performance of silicon technology with SiGe/TFSOS CMOS to K-band, benefiting from established industrial infrastructure resulting in lower cost, advanced components, such as A/DCs and wireless communication functions

• TFSOS, implementing a low power, lower cost, high performance technology for application to:
  • Space based electronics
  • Image processing
  • Digital communication
  • Extended operation battery-powered systems
  • Other commercial/military systems
What all the wise promised has not happened, and what all the damned fools said would happen has come to pass

William Lamb
Second Viscount Melbourne
(from Lord Melbourne, 1834)