Fabrication of sub-5nm silicon nano-wires and nano-devices

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Subject Terms:
- silicon nano-wire, nano-devices
Fabrication of sub-5nm silicon nano-wires and nano devices

Final Technical Report

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AASERT Grant #F49620-95-1-0418

Accomplishments/New Findings:

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The TEM analysis of a wide range of wires in <100> and <110> orientations revealed that the post oxidation aspect ratio is substantially different from the initial line's aspect ratio. Figure 1 shows a 1:1 aspect ratio line that resulted in a 4:1 aspect ratio wire. The single most important factor in determining the aspect ratio of the wire is the initial line orientation. Since (110) surfaces oxidize faster than (100) surfaces, lines in the <110> orientation fabricated on a (100) wafer oxidize faster laterally then from the top and bottom. Local stress distribution tends to lower the oxidation rate of the shorter dimension, making the change in the aspect ratio much larger then the 35% difference in the planar oxidation rates. The second factor that affected the geometry of the wire was the presence of the substrate oxide. When present during the stress-limited oxidation the substrate oxide inhibited oxidation of the bottom part of the wire producing a top/bottom asymmetry, as shown in figure 2.

In order to fabricate wires with a minimum diameter the initial <110> line has to be approximately 50% wider then it is tall, and be mostly free of the oxide substrate. For <100> wires the minimum diameter aspect ratio condition is 1:1 as expected since all sides are (100). Stress limited oxidation can be used to fabricate structures other then a small silicon wire. A deviation from the prescribed aspect ratios produces a rectangular profile, that can be further oxidized to produce two separate wires. This occurs because the longer sides of the rectangle oxidize faster in the middle due to lower stress distribution there.

An immediate problem with incorporating the silicon nanowire into a device is preventing the source/drain area from oxidizing away during the stress limited oxidation. A process that uses a thin silicon nitride layer to prevent oxidation of the source and drain regions during wire formation has been developed. Source and drain mesas at the ends of the silicon line are formed with the same etch step as the line itself. Then a pad oxide and nitride stack is deposited using CVD. A second lithography level is used to pattern
the nitride, opening a window to the silicon line, but leaving the mesas protected. The substrate oxide is undercut with an etch and the wire is formed by stress-limited oxidation. Then the nitride is removed and a polysilicon gate is deposited and patterned. SEM of the nanowire device is shown in figure 3. The mesa regions are to the right and left of the central 200nm wide gate. This device functions as a transistor with an ultra thin body and is expected to show excellent turn-off characteristics.

Figure 1) Left, TEM cross section of a 1:1 aspect ratio line prior to oxidation. Right 1:4 aspect ratio wire after the oxidation of a 1:1 aspect ratio line.

Figure 2) TEM profile of a post-oxidation profile with significant substrate oxide present. The profile shows significant top/bottom asymmetry.

Figure 3) SEM of a nanowire device. Source/drain mesas are on the right/left. The central gate is 200nm wide. The initial silicon channel line is 50nm wide and drawn in the <110> direction. After oxidation the channel should consist of a wire only 5nm in diameter.
PERSONNEL SUPPORTED:
Graduate students: Jakub Kedzierski, Troy Clear

PUBLICATIONS

NEW DISCOVERIES, INVENTIONS OR PATENT DISCLOSURES:
None

HONORS/AWARDS
J. Bokor is a Fellow of the Optical Society of America and the American Physical Society
ATTACHMENT

AUGMENTATION AWARDS FOR SCIENCE & ENGINEERING RESEARCH TRAINING (AASERT) REPORTING FORM

The Department of Defense (DoD) requires certain information to evaluate the effectiveness of the AASERT Program. By accepting this Grant which bestows the AASERT funds, the Grantee agrees to provide 1) a brief (not to exceed one page) narrative technical report of the research training activities of the AASERT-funded student(s) and 2) the information requested below. This information should be provided to the Government’s technical point of contact by each annual anniversary of the AASERT award date.

1. Grantee identification data: (R&T and Grant numbers found on Page 1 of Grant)
   a. University of California, Berkeley
      University Name
   b. F49620-95-0418
      Grant Number
   c. ____________________________
      R&T Number
   d. Professor Jeffrey Bokor
      P.I. Name
   e. From: 6/2/95  To: 5/31/98
      AASERT Reporting Period

NOTE: Grant to which AASERT award is attached is referred to hereafter as "Parent Agreement".

2. Total funding of the Parent Agreement and the number of full-time equivalent graduate students (FTEGS) supported by the Parent Agreement during the 12-month period prior to the AASERT award date.
   a. Funding: $200,000
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   a. Funding: $2000,000
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   a. Funding: $50,000
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VERIFICATION STATEMENT: I hereby verify that all students supported by the AASERT award are U.S. Citizens.

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Principal Investigator
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F49620-94-1-0387

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