III-V and IV-IV Materials and Processing Challenges for Highly Integrated Microelectronics and Optoelectronics

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III-V and IV-IV Materials and Processing Challenges for Highly Integrated Microelectronics and Optoelectronics

III-V and IV-IV Materials and Processing Challenges for Highly Integrated Microelectronics and Optoelectronics

Symposium held November 30–December 3, 1998, Boston, Massachusetts, U.S.A.

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CONTENTS

*Invited Paper

PART IV: <u>BONDING, DEVICES AND BACK-END PROCESSING</u>

PART V: <u>III-V PROCESSING AND GROWTH</u>

*Invited Paper

*Invited Paper

PREFACE

This proceedings volume contains papers based on oral contributions from two symposia, Symposium D: "Integration of Dissimilar Materials in Micro- and Optoelectronics," and Symposium I: "III-V and SiGe Group IV Device/IC Processing Challenges for Commercial Applications," which were held during the 1998 MRS Fall Meeting in Boston, Massachusetts. The joint publication of these two symposia stems from the technologically-driven desire to achieve new levels of device functionality, and higher levels of performance via integration of devices based on dissimilar semiconductors, where the constraint of lattice-matching on the breadth of attainable devices can be reduced. Integration, by its very nature, is a challenging materials issue starting at the level of epitaxial growth all the way through final processing. It is the purpose of this proceedings to elucidate the breadth and depth of critical materials issues related to integration covering III-V, IV-IV, II-VI, and wide-bandgap semiconductor systems.

Symposium D covered fundamental topics germane to integration of a wide range of dissimilar materials spanning wide-bandgap III-V nitrides, III-V/Si integration, II-VI and II-VI/III-V compounds, heterovalent structures, oxides, photonic bandgap structures, and others. A large number of presentations covered integration methods via heteroepitaxy, compositional grading, selective area epitaxy, wafer bonding, and lateral epitaxial overgrowth. Other presentations focused on the properties of defects which result from various integration methods, and how they impact material properties and device characteristics, while yet another group of papers focused on device processing. Current topics such as compliancy, dislocation control, selective area growth, bonding methodologies, etc. were extensively discussed in many talks, and contributions on the theory of such approaches provided for excellent discussion between experimentalists and theorists during the Meeting.

Symposium I dealt with processing issues in the manufacturing of III-V and Si-based heterostructures for commercial products. The challenges of heteroepitaxy on III-V substrates have been addressed for over three decades now, while those on silicon substrates were first encountered a quarter century ago. Commercial products in III-V materials have a relatively long history, while achievements in commercial products for SiGe, which is evidenced by the SiGe/Si heterojunction bipolar transistor (HBT), are only recent. These achievements have required the dedicated efforts of many creative materials engineers. This symposium has gathered together several workers from the fields of Si-based heteroepitaxy and process integration to illustrate a few of the innovative solutions developed in response to the fundamental issues of strained-layer epitaxy and thermal processing of metastable device architectures. The current success enjoyed by silicon germanium technology is contrasted by the tantalizing promise of silicon-carbon alloys which have a unique set of opportunities and challenges for this generation of process developers. New developments in III-V materials include oxidation and *in situ* monitoring of growth and processing steps. These topics,

along with conventional but important topics such as Schottky gate metal reliability and reactive-ion-etching-induced damage, are covered.

To represent the breadth of issues presented in these two symposia, this volume is divided into the following six parts, the first four covering Symposium D and the final two covering Symposium I: Lattice and Defect Engineering; Electronic Defects and Transitions in Mismatched Heterostructures; Integration and Defect Engineering for Wide-Gap Semiconductors; Bonding, Devices and Back-End Processing; III-V Processing and Growth; and Processing Issues in SiGe/Si and SiC/Si Heterostructures.

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April 1999

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MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS

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Part I

Lattice and Defect Engineering

A MECHANISM FOR THE REMOVAL OF DISLOCATIONS IN SOI COMPLIANT SUBSTRATE SYSTEMS

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ABSTRACT

It is demonstrated that the time required for strain transference during the post-growth anneal of a SOI compliant substrate system is much too long to explain the observed reduction in dislocation density in the resulting microstructure. A mechanism by which misfit dislocation segments are drawn out of the system through viscous dissipation in the bonding layer is proposed and demonstrated to be consistent with observation. The mechanism is modeled in the context of elastic dislocation theory and linear viscoelasticity.

INTRODUCTION

A recent approach for obtaining low dislocation lattice-mismatched epitaxial films is growth on a thin compliant layer. The intended function of the compliant layer is to allow for the relaxation of mismatch strain in the film by a means other than misfit dislocation formation. Several compliant substrate configurations have been considered,[1-3] but the essential idea is grow onto a layer which is constrained in a manner which provides structural support while retaining some lateral compliance. If the complaint layer thickness is on the order of the film thickness, a portion of the mismatch strain will be accommodated through deformation of the compliant layer. In this way, the residual strain in the film and hence the driving force for dislocation formation in the film is reduced. According to this argument, the critical thickness for dislocation formation in the film can be extended well in excess of that for a similar film grown on a conventional substrate.

The configuration addressed here is the silicon-on-insulator (SOI) compliant substrate system proposed by Powell, Iyer, and LeGoues[4] which has received some attention recently.[5-7] The system consists of a thin Si compliant layer ($\sim$60 nm thick) bonded to a much thicker supporting substrate through a SiO_2 bonding layer ($\sim$300 nm thick). The intended function of the bonding layer is to provide the means for strain to be transferred from the film to the compliant layer during a post-growth anneal. The film is grown on the compliant layer to a thickness above the critical thickness, but within a "metastable" regime where dislocation formation is minimal due to kinetic factors. The subsequent anneal causes the SiO_2 to flow viscously or the SiO_2/Si to slip thereby allowing the strain transference to occur. Following this process, Powell and co-workers observed threading dislocations in the compliant layer, while the film was apparently free of threading segments. Such a microstructure is desirable for devices utilizing lateral transport in the film.

Here it is demonstrated that the time for strain transference to occur over a large area of the wafer is likely to be much slower than typical annealing times, hence this cannot account for the reduced dislocation density. An alternative mechanism whereby dislocations are drawn out through the compliant layer is proposed and evaluated. It is concluded that this mechanism can operate over the experimental time scale.

3

Figure 1. Schematic of a SOI compliant substrate system. The film and the compliant layer are treated as elastic membranes with deformation characterized by a longitudinal strain $\epsilon = \partial u/\partial x$. The bonding layer is a Newtonian viscous material which deforms in shear $\gamma = \partial u/\partial y$. In each case u is displacement in the x-direction.
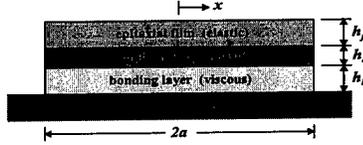
TIME SCALE FOR STRAIN TRANSFERENCE[8]

To estimate the time scale over which the transference of strain occurs though viscous flow of the bonding layer, the system is modeled as depicted in Figure 1. The film and compliant layer are treated as elastic membranes of thicknesses h_f and h_c, respectively, with the same tensile modulus E and Poisson ratio ν. Each membrane deforms with displacement u in the x-direction and strain $\epsilon = \partial u/\partial x$. The tensile stress in each membrane is $\sigma = E\epsilon/(1-\nu^2)$. The bonding layer is modeled as a Newtonian fluid of thickness h_b. The shear stress τ is related to the shear strain rate $\dot{\gamma}$ as $\tau = \eta\dot{\gamma}$ where η is the viscosity. The lateral dimension a is assumed to be much larger than the thickness of each component. The substrate is taken as rigid.

At the growth temperature, the bonding layer viscosity is large. Hence flow is minimal and over a large area of the wafer the residual strain in the film ϵ_f is equal to the mismatch strain ϵ_0 while the compliant layer is largely strain-free. This shall be the initial condition: $\epsilon_f(x, t = 0) = \epsilon_0$ and $\epsilon_c(x, t = 0) = 0$ with the system being at rest. Here ϵ_c is the strain in the compliant layer.

The relaxation rate is quite slow, as will be demonstrated; thus, a quasi-static analysis is applicable. As required by equilibrium, the stresses in each component are related by

$$h_c\frac{\partial \sigma_c}{\partial x} + h_f\frac{\partial \sigma_f}{\partial x} = \tau_b. \tag{1}$$

The subsequent displacements in the film and compliant layer must be compatible which is assured if $u_f(x, t) = u_c(x, t) + \epsilon_0 x$ and the displacement of the compliant layer must be equivalent to the bonding layer displacement at the shared interface, that is, $h_b\dot{\gamma} = \partial u_c/\partial t$. With these conditions, after some manipulation, (1) can be written in terms of the film strain as

$$\frac{\partial^2 \epsilon_f}{\partial x^2} = \frac{(1-\nu^2)\eta}{Eh_b(h_c + h_f)}\frac{\partial \epsilon_f}{\partial t} \tag{2}$$

which is simply the one dimensional heat equation (the pre-factor of $\dot{\epsilon}_f$ is positive definite). The boundary conditions are determined from equilibrium at the end points $x = \pm a$. This gives $h_f\sigma_f(\pm a, t) = -h_c\sigma_c(\pm a, t)$ or, from compatibility and the stress-strain relationships, $\epsilon_f(\pm a, t) = h_c\epsilon_0/(h_c + h_f)$. Using separation of variables, the solution, in non-dimensional form, is found to be $\epsilon_f(\overline{x}, \overline{t}) = \epsilon_0(h_c + f_\epsilon(\overline{x}, \overline{t})h_f)/(h_c + h_f)$ where

$$f_\epsilon(\overline{x}, \overline{t}) = \sum_{n=1}^{\infty} \frac{2}{\lambda_n}(-1)^{n+1}e^{-\lambda_n^2\overline{t}}\cos\lambda_n\overline{x}, \tag{3}$$

$\overline{x} = x/a$, $\overline{t} = t/a^2\alpha$, and $\lambda_n = \pi(2n-1)/2$. The strain in the compliant layer is $\epsilon_c = \epsilon_f - \epsilon_0$. At a given time, the function f_ϵ is a measurement of the spatial amount of relaxation across the wafer. This function is plotted in Figure 2 for several values of time $\overline{t}$. It is apparent

4
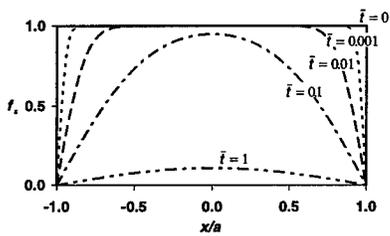
Figure 2. A plot of the relaxation f_ϵ due to the viscous flow of the bonding layer in a compliant substrate system versus x/a after several different annealing times $\bar{t}$.
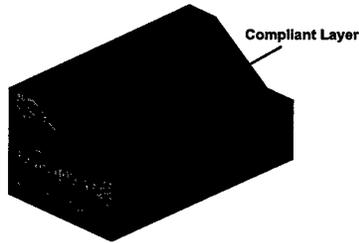
Figure 3. Schematic of a misfit dislocation being drawn through the compliant layer to the bonding layer. This results in two threading segments in the compliant layer which retreat continuing to pull the misfit dislocation out of the system.

that the relaxation begins at the edge of the system ($x/a = \pm 1$) and progresses inward towards the center. Prior to the time $\bar{t} \approx 0.1$, the center of the film experiences little relaxation and only for subsequent times is the relaxation significant over the full area of the film. To attach a physical time scale to the relaxation process, consider the material constants $E = 10^{11}$ Pa and $\nu = 1/4$ for Si and $\eta = 10^7$ Ns/m^2 for BSG (borosilicate glass)[9] at 800°C (a relatively low viscosity). For the structure used by Powell and coworkers the thicknesses are $h_f = 170$ nm, $h_c = 60$ nm, and $h_b = 300$ nm. For these values and a wafer of size $a = 1$ cm, the normalized time $\bar{t} = 1$ corresponds to about 38 hrs, a remarkably long time. It is concluded that even a moderate amount of relaxation by way of viscous flow of the bonding layer takes hours. The actual mechanism by which the system relaxes is unclear. Some have suggested that slippage may occur along the Si/SiO$_2$ interface, instead of by viscous flow of the bonding layer. But, in any case, it appears the transfer of strain from the film to the compliant layer takes a substantial amount of time to occur.

A MECHANISM FOR DISLOCATION REMOVAL

Prior to annealing the strained layer/compliant substrate system, dislocation nucleation may be limited due to kinetic factors. But, once the temperature is raised to anneal the system, dislocations may form and propagate in the film at a significant rate due to the additional amount of thermal activation supplied while the strain in the film is largely unchanged due to the slow transfer of mismatch strain . The SiO$_2$ becomes viscous at the elevated temperature and, hence, may relax allowing segments of a misfit dislocation to glide from the interface between the film and compliant layer towards the bonding layer and eventually be absorbed within the bonding layer/compliant layer interface. This process is illustrated in Figure 3 which depicts a cross section of system. An interface segment adsorbed through the bonding layer leaves two threading segments in the compliant layer which may then retreat, drawing an additional amount of the misfit dislocation out of the system. This will free up metastable dislocation configurations (for example those treated by Freund[10]) and may result in a decrease in the density of dislocations which thread through the film. The microstructure described here is of course that observed by Powell and coworkers. To determine if such a mechanism is possible, an estimate of the time required for a dislocation to be drawn to the bonding layer is needed. This is done next.

Figure 4. Schematic of a dislocation which extends indefinitely in the x_2-direction and is constrained to glide at an angle α with respect to the x_3-axis. The dislocation is contained within an elastic half-space (A) which is bonded to a viscoelastic half-space (B). The elastic and viscoelastic materials have different shear moduli (μ_A and μ_B) and Possion ratios (ν_A and ν_B). The viscosity the viscoelastic material is η_B.
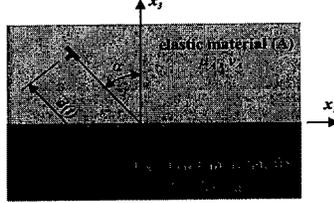
DISLOCATION MOTION NEAR THE SiO$_2$ LAYER

The physical system considered is depicted in Figure 4. A straight dislocation, parallel to the x_2-axis, is gliding at an angle α to the x_3 axis. At time t it is located a distance $d(t)$ from the intersection of the glide plane with the interface. The film and compliant layer are treated as an elastic half space with a shear modulus μ_A and Possion ratio ν_A. The bonding layer is as well treated as an elastic half space and it is modeled as a viscoelastic Maxwell material with shear modulus μ_B, Possion ratio ν_B, and viscosity η_A. The stress-strain relationship for (A) and (B) are, respectively,

$$\epsilon_A = \frac{1}{2\mu_A}\left[\sigma_A - \frac{\nu_A}{1+\nu_A}\mathrm{tr}(\sigma_A)\mathbf{I}\right] \tag{4}$$

and

$$\frac{\partial \epsilon_B}{\partial t} = \frac{1}{2\mu_B}\left[\frac{\partial \sigma_B}{\partial t} - \frac{\nu_B}{1+\nu_B}\mathrm{tr}\left(\frac{\partial \sigma_B}{\partial t}\right)\mathbf{I}\right] + \frac{1}{2\eta_B}\left[\sigma_B - \frac{\nu_B}{1+\nu_B}\mathrm{tr}(\sigma_B)\mathbf{I}\right]. \tag{5}$$

It is assumed that compliant layer is unstrained. This is a valid assumption as long as the time for the dislocation to reach the interface is significantly less than the strain transference time. Futhermore, the film is also treated as unstrained. Including mismatch strain in the film offers little new insight and does not affect the conclusions.

To address dislocation motion, a relationship between velocity and the state of stress in the vicinity of the defect is needed. Observations demonstrate that for stresses above some modest threshold stress the following kinetic relationship is suitable for dislocation motion in covalent crystals:[11] $\mathbf{v} = v_0 \exp[-Q_0/kT]\mathbf{f}/\mu b$ where v_0 is a material constant, Q_0 is the activation energy, k is Boltzmann's constant, T is temperature, b is the Burgers displacement, and $\mathbf{f} = -(\mathbf{b} \cdot \sigma_{ns}\mathbf{n})\mathbf{s}$ is the Peach-Koehler force on the dislocation. Here $\mathbf{n}$ is the glide plane unit normal, $\mathbf{s}$ is the dislocation line unit normal in the glide plane, and $\mathbf{b}$ is the appropriate definition of the Burgers vector with respect to these vectors. Since the problem is two dimensional, one can manage without carefully defining the direction of the Burgers vector (only the magnitudes of its components are important). The direction of the force can be checked by comparing it to a well known degenerate case. The stress σ_{ns} is the non-singular part of the stress at the dislocation core, that is, the total stress minus the stress about a dislocation in an unbounded medium. For Si, the material constants are taken to be $v_0 = 1.36 \times 10^5$ m/s and $Q_0 = 1.69$ eV.

To obtain an equation of motion for the dislocation, the stress in the elastic half space needs to be determined for an arbitrary position history $d(t)$ of the dislocation. For the sake of brevity, the solution is offered only for the case of a screw dislocation (Burgers vector in the x_2-direction). The general case and additional details can be found

Figure 5. Plots of position histories of a screw dislocation gliding in Si ($\mu_A = 43$ GPa and $b = 3.84$ Å) towards a BPSG bonding layer at 800°C ($\eta_B = 7 \times 10^8$ Ns/m^2) for several ratios of shear moduli μ_B/μ_A. The screw dislocation is inserted $60b$ from the interface and with the glide plane perpendicular to the interface.
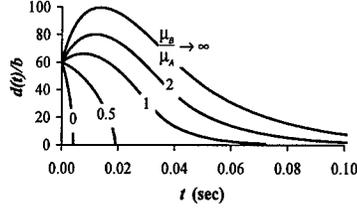
elsewhere.[12] The solution of the quasi-static viscoelastic problem can be obtained directly from the equivalent elastic solution through application of the correspondence principle.[13] By applying the correspondence principle to the solution of a screw dislocation near the interface of two joined elastic half spaces,[14] the out-of-plane displacement in the elastic half space is found to be

$$u_2^A(t) = \frac{b_2}{2\pi} \arctan\left(\frac{x_3 - d(t)\cos\alpha}{x_1 + d(t)\sin\alpha}\right) - \frac{b_2}{2\pi} \int_0^t C(t-p) \arctan\left(\frac{x_3 + d(p)\cos\alpha}{x_1 + d(p)\sin\alpha}\right) dp \quad (6)$$

where $C(t) = C_t(1 - C_e)e^{-C_t t} + C_e\delta(t)$. The function $\delta(t)$ is the Dirac delta function and the constants $C_e = (\mu_A - \mu_B)/(\mu_A + \mu_B)$ and $C_t = \mu_A\mu_B/\eta_B(\mu_A + \mu_B)$. In obtaining (6) it has been assumed that the dislocation is suddenly inserted at its initial position; prior to the time $t = 0$ the dislocation is not present. Other initial conditions can be extracted from this result by holding the dislocation at its initial position for a duration prior to its moving. The present initial condition leads to the longest accommodation times, so it is sufficient for the purpose of this analysis. In (6), the first term is due to the dislocation alone and results in the singular part of the stress, while the second term is a result of the boundary conditions and leads to the stress σ_{ns}; this is the part of the solution needed to determine the driving force on the defect. Denoting the second term as u_2^{ns}, the image stress is given as $\sigma_{2j}^{ns} = \mu_A u_{2,j}^{ns}$ and, from the Peach-Koehler formula, the glide force is given as $f(t) = -b_2[\sigma_{21}^{ns}\cos\alpha + \sigma_{23}^{ns}\sin\alpha)]_{x_1=-d(t)\sin\alpha, x_3=d(t)\cos\alpha}$ or

$$f(t) = -\frac{\mu_A b_2^2}{2\pi} \int_0^t \frac{C(t-p)\left[d(t) + d(p)\cos 2\alpha\right]}{d(t)^2 + 2d(t)d(p)\cos 2\alpha + d(p)^2} dp \quad (7)$$

directed away from the interface. Using this result in the kinetic relation gives the equation of motion $\dot{d}(t) = v_0 \exp[-Q_0/kT]f(t)/\mu b$.

Plotted in Figure 5 are position histories of a screw dislocation gliding in Si towards a BPSG (borophosphosilicate glass)[9] bonding layer having a viscosity $\eta_B = 7 \times 10^8$ Ns/m^2. The plots were obtained by solving the equation of motion numerically with the fourth-order Runge-Kutta method. A range of values for the shear modulus of the bonding layer are included since reliable values could not be found. The cases $\mu_B/\mu_A = 0$ and $\mu_B/\mu_A \to \infty$ correspond to a dislocation gliding toward a free surface and viscous fluid respectively. For the cases $\mu_B/\mu_A > 1$, the dislocation does not pass through the interface, but approaches it asymptotically. This is an artifact of the linear theory. One can consider a dislocation to have passed through the interface once it is closer than about 1-2 Burgers displacements.

Times for the screw dislocation to reach the interface in this example are much shorter than the hours it takes for the transference of strain to occur even though the viscosity

was taken to be significantly larger. This is generally the case. Over a wide range of physical parameters of interest, for a dislocation of mixed character gliding at an oblique angle to the interface, the accommodation times range from the order of milliseconds to seconds. A similar analysis was done for a screw dislocation gliding toward a bonding layer of finite thickness sandwiched between two elastic half spaces.[12] The conclusions remain unchanged.

Misfit dislocations can be drawn out through the bonding layer only while the strain in the compliant layer is less than a critical value. Towards the edges of the wafer, this critical value may reached rather quickly, as shown in Figure 2. Nonetheless, once the critical strain is reached, retreating threading dislocations in the compliant layer will continue to draw the misfit dislocation out of the system.[12]

CONCLUSIONS

The time required for strain to be transferred from the film to the compliant layer during the anneal of a SOI compliant substrate system is on the order of hours, much too long to explain the reduced dislocation density. An alternative mechanism by which misfit segments are drawn out through the compliant layer/bonding layer interface was found to occur within seconds. It is concluded that this mechanism is a viable explanation of the observed microstructure.

ACKNOWLEDGEMENTS

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Annihilation Radii for Dislocations Intercepting a Free Surface with Application to Heteroepitaxial Thin Film Growth

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ABSTRACT

One critical issue in heteroepitaxial, lattice mismatched growth is the inevitable appearance of threading dislocations which reside in the relaxing film and degrade its semiconducting properties. It has been shown in previous work that threading dislocations interact with each other through a series of annihilation and fusion reactions to decrease their density as the film thickness increases and follow a $1/h$ decay, where h is the film thickness. A characteristic reaction radius is associated with these interactions. In previous simulations, the reaction radius was taken to be a constant value estimated using a simple approximation based on infinite, parallel dislocation lines. Here, a continuum-based elasticity approach is taken to more accurately quantify the reaction radius by comparing the Peach-Koehler force of one dislocation acting on another at a free surface with the lattice resistance to dislocation motion. The presence of the free surface gives rise to a moderate reduction of the interaction force. Results are compared with preliminary experimental data for GaAs films grown on InP.

INTRODUCTION AND BACKGROUND

During heteroepitaxial growth of thin-films for electronic devices, misfit dislocations (MD) inevitably nucleate due to lattice mismatch stresses. Upon reaching a critical thickness, h, the film "relaxes" as misfit dislocations, and associated threading dislocations, appear and multiply. Misfit dislocations are equilibrium defects - *i.e.* they are necessary to relieve mismatch strain, while threading dislocations are non-equilibrium line defects that link a given MD to the surface. Threading dislocation densities for films with large mismatch (in excess of ~2%) can be on the order of 10^{10}-10^{11} cm^{-2} and as pointed out by Beltz *et al.* [1], their population is largely reducible while retaining the necessary MD density to sustain a relaxed film. A wealth of experimental work has been performed in an attempt to reduce TD densities. However, relatively few theoretical efforts have been carried out to understand TD density reduction mechanism.

There have been several experimental research efforts to characterize TD density reduction with film thickness for several material systems. Tachikawa and Yamaguchi [2] observed a $1/h$ dependence of TD density in GaAs films on Si substrate, where h is the film thickness. TD reduction has also been reported for InAs/GaAs, GaAs/Ge/Si, GaAs/InP, and InAs/InP by Sheldon *et al.* [3], showing similar $1/h$ dependence for all 4 material systems. They found TD density to be inversely proportional to film thickness for initial TD densities of 10^8-10^9 cm^{-2}. Additionally, the reduction behavior was found to be similar for all of the material systems, indicating that the fundamental mechanics of dislocation reduction are the same regardless of material system. Tachikawa and Yamaguchi also found dislocation density to be exponentially proportional to film thickness for initial TD densities of less than 10^7 cm^{-2}. Mathis *et al.* [4] have recently shown TD density data for GaAs grown on InP displaying the $1/h$ behavior, as shown in Figure 1.

In the recent theoretical work by Beltz *et al.*, a computer simulation was developed to study TD density reduction [1]. TDs are allowed to "react" with one another to reduce their overall density, giving results consistent with the $1/h$ density dependence and ultimate saturation predicted by earlier models [5] and observed experimentally by such groups as Tachikawa and Yamaguchi. A primary tenet in the theoretical models to date is that TDs within a reaction distance of each other spontaneously interact. Given the correct Burgers vector combination, annihilation ($b_1+b_2=0$) or fusion ($b_1+b_2=b_3$) of the TDs could occur, or the dislocations would simply continue following a trajectory to the surface, unimpeded or at most repelled by each other.

9

In conjunction with the computer simulation, an analytical approach was also taken to further understand TD reduction. Romanov *et al.* [6,7] present an analytical model for TD reduction based on the principal of chemical kinetics. They derived and solved a system of non-linear first order differential equations for the 24 types of TDs for FCC materials. Their numerical results recover the $1/h$ dependence as well as the saturation behavior that has been observed both experimentally and in simulations.
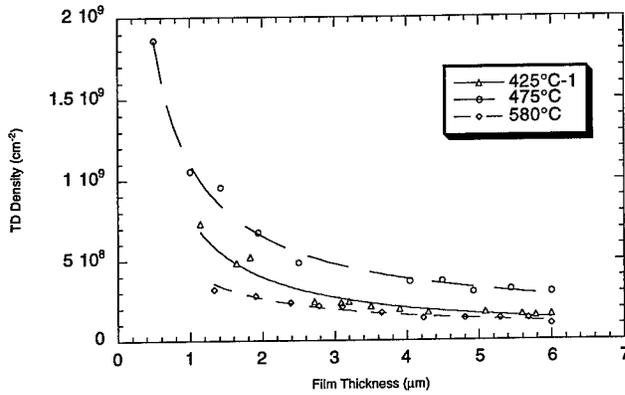
Figure 1. Threading dislocation density data for GaAs grown on InP via MBE.

SIMPLE REACTION RADIUS ESTIMATION

In the aforementioned theoretical work, the most critical physical parameters were left as unknowns against which the primary results were normalized. The reaction radius for annihilation and fusion reactions were assumed to be equivalent and were estimated by comparing the force acting between two dislocations, also known as the Poech-Koehler force, with the force opposing dislocation movement due to the lattice, also known as the Peierls stress. Since TDs are substantially of screw character, only the conditions for screw dislocations are considered here for simplicity. For the simple case of two parallel screw dislocations, the magnitude of the PK force is:

$$F^{PK} = \frac{\mu b^2}{2\pi r} \tag{1}$$

The lattice friction force per unit length of dislocation due to the Peierls stress, σ_p, is given as:

$$F_p = \sigma_p b \tag{2}$$

Dislocation motion will occur when these two forces are equivalent. Thus, the reaction radius, r_A, is approximated as:

$$r_A = \frac{\mu b}{2\pi\sigma_p} \tag{3}$$

Based on the parameters of typical semiconductor materials, r_A was set at 5000Å [1]. Figure 2 shows results by Mathis *et al.* [4] of the reaction radius from the GaAs on InP system previously mentioned, with the reaction radius varying from ~100-1200Å, agreeing fairly well with the predicted range. Since dislocation mobility increases with temperature, it is physically realistic for the annihilation radius to increase with temperature as shown in Figure 2. Peierls stresses for a few representative materials are listed in Table 1.
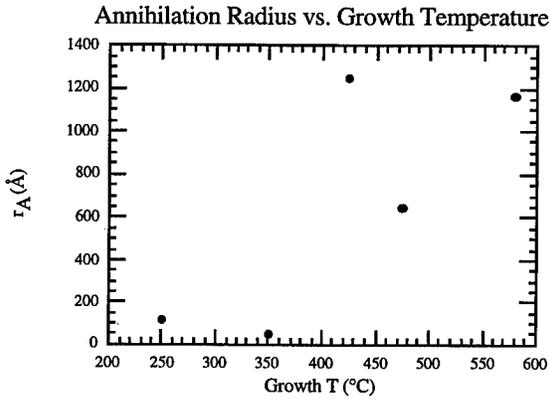
Figure 2. Experimental data for GaAs on InP system showing annihilation
radii at various growth temperatures.

Table 1. Peierls stress and shear modulus for various materials.

Material	Peierls Stress (MPa)	σ/μ (x10^{-3})	μ (GPa)	T (K)
Silicon [6]	110 (expt)	2.62	42	873
ZrO$_2$ [7]	100-150 (expt)	1.25-1.88	80	293
GaAs[8]	35-65	0.73-1.35	48	623
MgO [9]	60-170 (expt)	0.69-1.95	87	373-423

ELASTIC STRESS FIELD FOR A GENERAL DISLOCATION PERPENDICULAR TO A SURFACE

   To further enhance the simulation results, we wish to estimate the reaction radii, r_A and r_F, using a more rigorous approach from the mechanics of defects. Comparing the elastic force between two dislocations at a free surface with the friction force from the Peierls stress yields a value for the reaction radius. In addition, we get a feel for the range of values for reaction radii for various material classes with an ultimate focus on semiconductor materials.
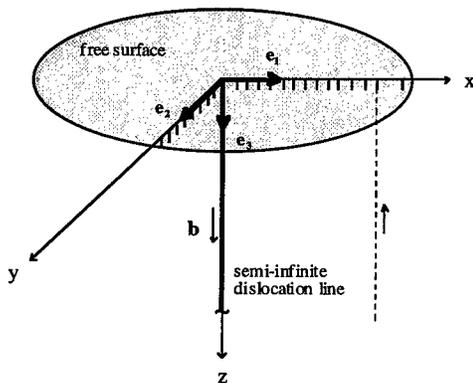
Figure 3. Straight dislocation intersecting a free surface.

11

A number of investigators have considered the problem of the stress field due to a straight dislocation intercepting a free surface (see Figure 3). The first, and best known work in this area is that due to Yoffe [10]. Thorough reviews of the methodology used for such solutions are provided by Bacon and Groves [11], Eshelby [12], Lothe [13], and Yu. Belov [14]. Unfortunately, the literature in this problem is infamous for the presence of a moderate number of misprints, especially in the equations for the dislocation stress field. As pointed out by Shaibani and Hazzledine [15], the approach of Yoffe lends itself well to concise expressions for the stress fields but misprints exist in that original work. They use Yoffe's method to reconstruct the fields; however, as mentioned by the same authors in a later paper [16], at least one misprint appears in their results. Rather than directly adopting the stress fields provided in the literature, we directly verify them. We derive the stress field due to a screw dislocation perpendicular to a free surface. Components of an edge dislocation perpendicular to a surface have also been derived, but will not be shown here.

Consider the coordinate system shown in Figure 3, with a single right-handed screw dislocation collinear with the z axis and the half-space occupying z > 0. Unit vectors along the three axes are denoted e_i, with the usual Einstein index convention. Our definition of "right-handed" is consistent with the usage of Hirth and Lothe [17], in that $e_3 \cdot b = b$, with the "positive" line sense of the dislocation in the positive z direction. The stress solution for the infinite screw dislocation,

$$\sigma_{\theta z} = \frac{\mu b}{2\pi r} \tag{4}$$

satisfies all of the boundary conditions for this problem *except* the traction free condition at z = 0; i.e., we require $\sigma_{\theta z} = 0$ for z=0. One could correct the solution in Equation (4) by integrating a point force $K(r, r')$ over the entire surface, weighted by the excess stress $\sigma_{\theta z}$ given by Equation (4), thereby nullifying the total traction on the surface. In polar coordinates, $K(r, r')$ gives the stress $\sigma_{\theta z}$ at position r due to a point force of unit magnitude applied parallel to the surface and tangential to a circle of radius r' about the origin and can be constructed from the concentrated tangential force solution found in Johnson [18]. The total stress field is thus given by

$$\sigma_{\theta z} = \frac{\mu b}{2\pi r} + \int_0^{2\pi} \int_0^{\infty} \frac{\mu b}{2\pi r'} K(r, r') r' dr' d\theta' = \frac{\mu b z}{2\pi r \sqrt{r^2 + z^2}}$$

$$\sigma_{r\theta} = -\frac{\mu b r^2}{2\pi \sqrt{r^2 + z^2} \left(z + \sqrt{r^2 + z^2} \right)^2} \tag{5}$$

These stresses agree with those for a screw dislocation in an infinite solid in the limit as z→∞, as well as give a traction-free condition $\sigma_{i3} = 0$ for z = 0. Moreover, they agree with the result of Hazzledine [12], except that care must be taken with the coordinate system, since their screw dislocation occupies the axis z < 0. Converting Equation (5) gives the following stress field in Cartesian coordinates:

$$\sigma_{11} = \frac{\mu b}{2\pi} \frac{2xy}{R(z + R)^2} \qquad \sigma_{12} = \frac{\mu b}{2\pi} \frac{\left(y^2 - x^2 \right)}{R(z + R)^2}$$

$$\sigma_{22} = -\frac{\mu b}{2\pi} \frac{2xy}{R(z + R)^2} \qquad \sigma_{23} = \frac{\mu b}{2\pi} \frac{xz}{Rr^2} \tag{6}$$

$$\sigma_{33} = 0 \qquad \qquad \sigma_{13} = -\frac{\mu b}{2\pi} \frac{yz}{Rr^2}$$

where $r=\sqrt{(x^2+y^2)}$ and $R=\sqrt{(x^2+y^2+z^2)}$. As a final check, Equations (6) satisfy the field equations of elasticity for an isotropic material:

$$\sigma_{ij,j} = 0$$

$$\varepsilon_{ij} = \frac{1}{2\mu}\left(\sigma_{ij} - \frac{\nu}{1+\nu}\sigma_{kk}\delta_{ij}\right) \tag{7}$$

$$\varepsilon_{ij,kl} + \varepsilon_{kl,ij} - \varepsilon_{ik,jl} - \varepsilon_{jl,ik} = 0$$

The stress field for an edge dislocation intercepting a surface is considerably more difficult to obtain due to the lack of rotational symmetry about the z axis. Combining the solutions for the screw and edge dislocation gives the stress field for a mixed dislocation impinging a free surface, which we will present in future work.

FREE SURFACE EFFECTS

The PK force is given by $-\varepsilon_{ijk}s_i\sigma_{jl}b_l$ where s_i are the components of the line sense of the dislocation in Einstein notation. Evaluation gives:

$$F_1^{PK} = -\frac{\mu b^2}{2\pi}\frac{xz}{r^2\sqrt{r^2+z^2}}$$

$$F_2^{PK} = -\frac{\mu b^2}{2\pi}\frac{yz}{r^2\sqrt{r^2+z^2}} \tag{8}$$

or expressed as a radial component,

$$F_r^{PK} = \frac{\mu b^2 z}{2\pi r\sqrt{r^2+z^2}} \tag{9}$$

i.e., a purely attractive force of magnitude $\dfrac{\mu b^2 z}{2\pi r\sqrt{r^2+z^2}}$. This force is independent of the relative angular position of the dislocations.

Equating the PK force with the Peierls force and solving for r_A gives:

$$\frac{r_A}{r_{A\infty}} = \frac{\sqrt{2}\pi\sigma_p \bar{z}}{\mu}\sqrt{-1+\sqrt{1+\frac{\mu^2}{\pi^2\sigma_p^2\bar{z}^2}}} \tag{10}$$

where $\bar{z} = z/b$. Note that as $z\to0$, i.e. the free surface, the attractive force vanishes. Equation (10) is plotted in Figure 4 for various values of σ_p/μ.

CONCLUSION

The annihilation radius for two opposite, parallel screw dislocations is given by $\dfrac{\mu b}{2\pi\sigma_p}$.

When experimental results on threading dislocation reduction are compared with the theory of Speck et al., the annihilation radius estimated here agrees within one order of magnitude with the value necessary for the theory to match the experiment. The effect of the free surface is to

diminish the interaction force between the dislocations, as well as the annihilation radius. For reasonable physical parameters, this decay only occurs near of the surface. It should be noted that the existence of any edge component in the reacting dislocations will increase the attractive force between the two dislocations since there is always an attractive force between two edge dislocations, even when z→0. In preliminary work by Beltz *et al.* [19], the reaction radius for edge dislocations is shown to have a maximum value near the free surface before decaying to steady state.
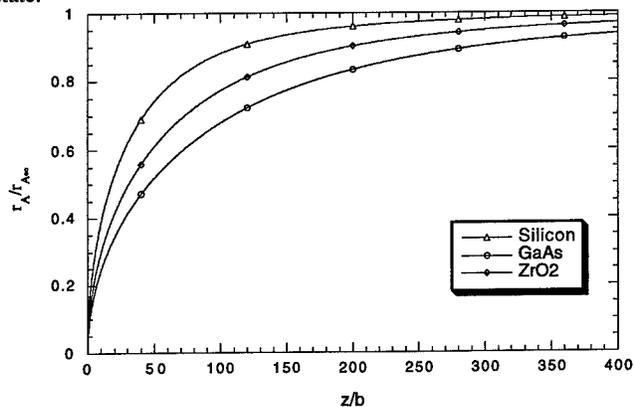
Figure 4. Free surface effect on reaction radius for various materials.

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QUANTITATIVE EXPERIMENTAL DETERMINATION OF THE EFFECT OF DISLOCATION – DISLOCATION INTERACTIONS ON STRAIN RELAXATION IN LATTICE MISMATCHED HETEROSTRUCTURES

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ABSTRACT

We present real time observations of the interaction of dislocations in heteroepitaxial strained layers using a specially modified ultrahigh vacuum transmission electron microscope equipped with *in-situ* deposition capabilities. These observations have led to delineation of the regime of epilayer thickness and composition where dislocation interactions result in blocking of the propagating threading segment. It is found that both the blocking probability as well as the magnitude of the dislocation interaction force are strongly dependent on the Burgers vectors of the dislocations involved, with the greatest effects observed when the Burgers vectors of the two dislocations are parallel with respect to each other. Frame-by-frame analysis of the motion of the dislocation threading segment during interaction is used to extract the magnitude of the interaction stresses as a function of both the level of heteroepitaxial strain and the dislocation geometry. Finally, by continuing growth following observations of blocking during annealing, we find that blocked dislocations are likely to remain in that configuration until substantial additional heteroepitaxial stresses are incorporated into the layer. These results have direct relevance to the successful integration of strained layer heterostructures into electronic device applications. This is because blocked threading segments result in the introduction of undesired band gap states, enhance impurity diffusion, modify surface morphology and act to limit the dislocation density reductions achievable in graded buffer structures.

INTRODUCTION

The kinetics of dislocation nucleation, propagation and interaction are the central parameters that define the rate of strain relaxation via misfit dislocation introduction in heteroepitaxial layers during both growth and annealing.[1] To date there have been a number of detailed theoretical treatments of dislocation interactions in these systems,[2-5] but limited experimental data exists which describes the specifics of how these interactions affect strain relaxation.

Dislocation motion in these systems is driven by the net excess stress on the dislocation threading segment, σ_{ex}, defined by Dodson and Tsao[6] as:

$$\sigma_{ex} = \sigma_a - \sigma_T$$

Equation (1)

where σ_a is the applied stress due to the epitaxial misfit and σ_T is the stress associated with the self-energy of the dislocation. Dislocations, because of the distortions they introduce into the crystalline lattice, have a strain field associated with them. As a result, when two dislocations approach each other these strain fields overlap, causing a stress to be exerted on each dislocation

15

by the other. The magnitude and direction of this stress is determined by the Burgers vectors of the dislocations as well as the distance between them.[7] Thus this interaction stress (σ_{int}) can act to either increase or decrease the net excess stress driving dislocation motion. If the inter-dislocation stress is sufficiently high during the interaction process, the threading segment will not be able to propagate past the interfacial segment and will become blocked. A schematic showing the interaction between threading and interfacial segments is shown in Figure 1.
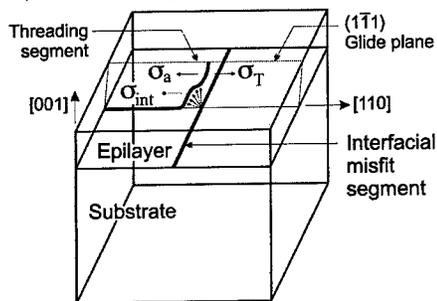
Figure 1 – Schematic of dislocation interactions in strained (001) heterostructures.

In this work, we report real-time observations of dislocation – dislocation interactions during both epitaxial growth and during annealing of SiGe heterostructures, utilizing the unique capabilities of a specially constructed ultrahigh vacuum transmission electron microscope equipped with *in-situ* UHV-CVD growth facilities. The range of epilayer thickness and composition where dislocation interactions result in blocking will be presented, and details of the dislocation interaction process will be reported.

EXPERIMENTAL DETAILS

Dislocation interactions were observed in real time using *in-situ* transmission electron microscopy. This was accomplished through use of an ultrahigh vacuum transmission electron microscope (UHV-TEM) equipped with *in-situ* chemical vapor deposition capabilities[8] and through post-growth anneals in a conventional TEM.[9,10] For the UHV-TEM experiments, Si (001) substrates were thinned to electron transparency using standard chemical methods, then subjected to a electronic grade chemical clean. The sample and sample holder were loaded into the ultrahigh vacuum system via a transfer loadlock, and the sample was flashed to temperatures in excess of 1250 °C to remove any remaining contaminants. After transfer to the microscope's objective lens, the sample was heated to 550 °C, after which 2×10^{-6} Torr disilane and between 2-4×10^{-8} Torr digermane were introduced into the objective lens region through small capillaries. (The digermane pressure used determined the germanium concentration in the $Si_{1-x}Ge_x$ layer.) This allows real time TEM observation of the epitaxial growth process at high spatial and temporal resolution. After the films were slightly above the critical thickness for dislocation motion,[11] film growth was halted by removing the gases. The sample temperature was then increased to 600 °C to obtain dislocation velocities on the order of 10 to 100 nm/s. Observations of the interaction between propagating threading segments and pre-existing interfacial segments were observed in real time and recorded on videotape.

RESULTS AND DISCUSSION

In Figure 2, we show the data points at which dislocation blocking and non-blocking interactions were observed during the UHV-TEM experiments as a function of epilayer strain (which is proportional to the composition via $\varepsilon = 0.041x$, ignoring any effects of plastic relaxation) and the logarithm of the epilayer thickness (h) normalized with respect to the Burgers vector (b). The data indicates that for a given epilayer thickness, dislocations are more likely to become blocked at lower germanium concentrations. This is as expected, because for a given epilayer thickness the net excess stress driving dislocation motion in the absence of interactions is lower for lower germanium concentrations. Thus, a lower interaction stress is required to cause $\sigma_{int} \geq \sigma_a - \sigma_T$. Superimposed upon the data are the Matthews-Blakeslee critical thickness criterion,[11] the numerical predictions for dislocation blocking of the Schwarz and Tersoff model,[5] and the analytical predictions of dislocation blocking of Freund for two different Burgers vector combinations.[3] This data shows that dislocation blocking can be a significant factor during the relaxation of heteroepitaxial strain, and that our experimental data is most consistent with analytical predictions of Freund.
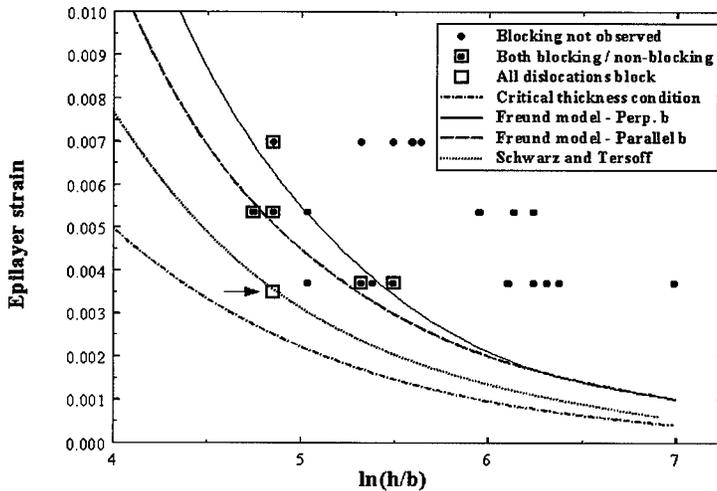
Figure 2 –   Epilayer thickness and strain at which dislocation blocking and non-blocking interactions were observed during UHV-TEM experiments.

It is worth noting that although the probability that a given interaction will result in blocking is higher for lower germanium composition films, the effect of dislocation blocking on the net rate of strain relaxation is expected to be more significant in higher germanium content samples. This is because at the lower concentrations, dislocation velocities are much slower than at higher concentrations. Thus, for the low concentration epilayers, it is unlikely that a dislocation threading segment will encounter an interfacial segment when the film thickness is low enough that blocking would be favored. Thus dislocation interactions are expected to have the strongest effect on the rate of strain relaxation in thin, high germanium content films.

Further inspection of Figure 2 reveals that only at the lowest composition and thickness did all dislocation interactions result in blocking of the propagating threading segment (this point is arrowed for emphasis). In the other films, only a fraction of the observed interactions resulted in blocking. Closer inspection of those dislocations that did become blocked revealed that the dislocations had split at the intersection node then reconnected thereafter. This splitting reaction is predicted to occur when the two dislocations have Burgers vectors which are parallel with respect to each other.[12,13] Analysis of the Burgers vectors using $(\mathbf{g} \cdot \mathbf{b})s$ diffraction contrast techniques confirmed that dislocation intersections which showed splitting did have image contrast consistent with the dislocations having parallel Burgers vectors.[14] This is in contrast to the model of Freund, who predicted that the blocking stresses should be highest when the two dislocations have Burgers vectors that are perpendicular with respect to each other.

Real time TEM observation of dislocation interactions allows information to be gained regarding the magnitudes of stress present during the interaction process. It is evident that as the threading dislocation approaches, then passes the pre-existing orthogonal interfacial segment its velocity can change as a function of position. In previous work we have systematically explored the dependence of dislocation velocity upon epilayer composition, thickness and temperatures during both growth and annealing.[15] The relationship between these quantities can be expressed mathematically as:

$$v^{*} = \frac{v_{m}}{\sigma_{ex}} \exp\left[\frac{-E_{v}^{*}(x)}{kT}\right] \approx \exp\left[-(14.45)\right] * \exp\left[-(1.74 \text{ eV})/kT\right] \text{ m}^{2}\text{s/kg} \qquad \text{Equation (2)}$$

where v_{m} is the actual dislocation velocity, v^{*} is the velocity normalized with respect to composition and stress, and $E_{v}^{*}(x)$ is the activation energy for dislocation motion, taken as a linear interpolation between the glide activation energies for pure silicon and germanium, i.e. $E_{v}^{*}(x) = (2.2 - 0.6x)$ eV.[16] From this functional dependence, we can therefore directly relate changes in dislocation velocity to changes in the net excess stress driving dislocation motion.

In Figure 3 we present an example of one such analysis for a pair of dislocations which exhibited the splitting reaction, taken from a 50 nm thick $Si_{86}Ge_{14}/Si(001)$ structure. Video frames were analyzed sequentially each 1/6 of a second, and the position of the dislocation threading segment with respect to the image of the interfacial segment was determined for each frame. In Figure 3a, the raw data for distance vs. time is presented. In Figure 3b, the velocity of the threading segment as a function of position is shown on the right hand side and the corresponding excess stress calculated from Equation 2 is shown on the left. In this film the far field excess stress (given by $\sigma_{a} - \sigma_{T}$) is approximately 250 MPa. This means that the interaction stress varies from as much as $\sigma_{int} = -160$ MPa before the intersection to $\sigma_{int} = +250$ MPa after the interaction. Additionally, from close inspection of the images, the dislocation threading arm appears to come to a complete halt for approximately 1 sec while the splitting reaction is occurring. There is also some evidence that the dislocation slows down following the splitting reaction, although additional experiments are needed to confirm that this behavior is systematic. Additional measurements of interaction stress using this technique have shown that the magnitude of the interaction stress decreases as the far-field excess stress decreases, and that when the two dislocation have Burgers vectors which make angles of either 60° or 90° with respect to each other the interaction stress is very small.
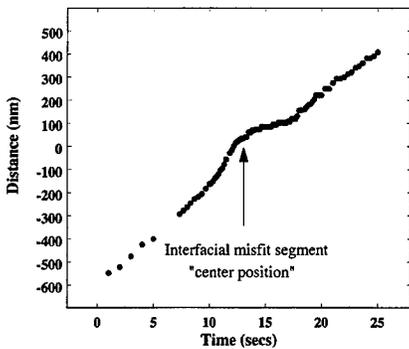
⇐ Figure 3a:
Raw data of interaction analysis
showing the distance the threading
dislocation has traveled versus
time. The approximate position
of the interfacial segment is noted.

Figure 3b: ⇒
Velocity of the threading dislocation and
the calculated excess stress driving its
motion. Velocity obtained via a fifth
order polynomial fit to the raw distance
versus time data in Figure 3a and
calculated via $v = \partial x / \partial t$.
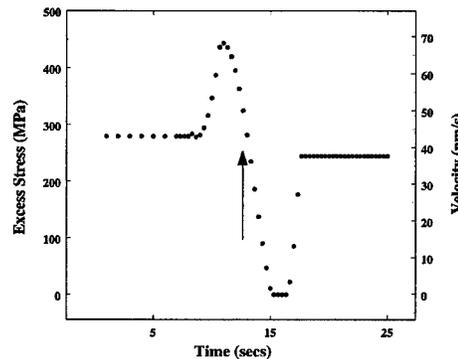
Finally, an additional set of experiments was performed in order to determine the magnitude of stress required to allow dislocations to release from their blocked configuration. After several blocking events were observed in a given sample during annealing at 600 °C, the sample was returned to the growth temperature of 550 °C and the gases were reintroduced into the objective lens permitting resumption of epilayer growth. As the film thickness increases, additional stress is incorporated into the growing epilayer. This additional stress should act to release the dislocation from the blocked configuration once the net driving stress is greater than the interaction stress (i.e. $\sigma_a - \sigma_T \geq \sigma_{int}$) over a sufficient portion of the threading segment.

We found, however, that the dislocation behavior was more complicated than predicted by this simple model. As the thickness of the film increased, it was observed that no additional blocking events were observed. Meanwhile, the dislocations that had become blocked earlier in growth were not able to release at these same thicknesses. The fact that these blocked arrangements are stable at the same thickness where dislocation blocking is not observed indicates that the interaction stress alone does not control the release of dislocations, but that a larger stress is required. Only in one experiment was it possible to increase the film thickness sufficiently to incorporate enough stress to release the blocked dislocations. It was found that even at additional stresses on the order of 100 to 150 MPa not all dislocations were released. It is not known whether the same behavior is observed when dislocations block during growth as when they block during annealing. It is conceivable that this resistance to release is either a result of point defect diffusion to the dislocation core during annealing or from the changes in either surface stoichiometry or morphology due to stress assisted diffusion. Pit formation at the intersection of threading segments with the surface has been observed in earlier studies of SiGe / Si

19

heterostructures.[17]   Additionally the persistence of blocked threading segments resulting from surface undulations is consistent with recent observations of dislocation "pile-ups" in graded buffer structures.[18]

In conclusion, we have used *in-situ* transmission electron microscopy to quantitatively observe the effects of dislocation interactions on heteroepitaxial strain relaxation. We have found the regime of epilayer thickness and composition where these interactions result in blocking of the threading segment, showing that blocking can significantly affect the rate of strain relaxation. The Burgers vector character of the dislocation is found to be more important that previously appreciated, with the strongest effects observed for dislocations with parallel Burgers vectors. Analysis of the change of velocity during the interaction process has permitted extraction of the magnitude of stress present. Finally, we find that dislocations that become blocked during annealing form stable configurations that persist through large increases in epilayer thickness.

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LATTICE ENGINEERING USING LATERAL OXIDATION OF AlAs: AN APPROACH TO GENERATE SUBSTRATES WITH NEW LATTICE CONSTANTS

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We demonstrate a new approach to the growth of dislocation free lattice-mismatched materials on GaAs substrates using Al_2O_3 interlayers obtained by lateral oxidation of AlAs. This is achieved by generating relaxed low threading dislocation density InGaAs templates which are mechanically supported but epitaxially decoupled from the host GaAs substrate. This process uses the phenomena of relaxation of strained coherent hypercritical thickness ($h > h_{critical}$) layer in direct contact with an oxidizing Al-containing semiconductor (i.e. AlAs or AlGaAs). 5000 Å $In_{0.11}Ga_{0.89}As$ layers were then grown on the $In_{0.2}Ga_{0.8}As/Al_2O_3/GaAs$ template which acts as a pseudo-substrate (lattice-engineered substrate). The epitaxial layers are partially relaxed and have extremely smooth surface morphology. Further TEM micrographs of these epitaxial layers show no misfit dislocations or related localized strain fields at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface. The absence of misfit dislocations or local strain contrast at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is attributed to both reactive material removal during the oxidation process and the porous nature of the oxide itself. We propose that the strain relaxation in $In_{0.3}Ga_{0.7}As$ is enhanced due to the absence of misfit dislocations at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface.

Introduction

The ability to grow strained pseudomorphic layers on commercially available substrates has enabled advances in GaAs pseudomorphic high electron mobility transistors (pHEMTs) and reduced the threshold current density in InGaAs/GaAs lasers. However the limit in the amount of strain still precludes the availability of technologically important devices such as 1.3 μm lasers on GaAs substrates. Growth of thick compressively strained InGaAs epitaxial layers on GaAs substrate results in relaxation via formation of misfit dislocations at the InGaAs/GaAs interface and associated generation of threading dislocations. Threading dislocation densities in excess of $\sim10^7/cm^2$, though acceptable for majority carrier devices such as field effect transistors, cause rapid degradation in the performance of minority carrier devices such as laser diodes and heterojunction bipolar transistors.

Growth of low threading dislocation density InGaAs epitaxial layers has been demonstrated through the use of graded buffers[1,2]. In this approach the misfit between the InGaAs epitaxial layer and the GaAs substrate is accommodated by dislocations which are distributed throughout the graded buffer layer. In the recent past, various other techniques have been investigated to accommodate the lattice mismatch between the substrate and the desired epitaxial layer. Wafer bonding has been recently reported to facilitate the growth of low threading dislocation density lattice-mismatched epitaxial layers on GaAs[3]. Use of viscous interlayers to facilitate lattice-mismatched epitaxy has been demonstrated by SiGe growth on SOI substrates[4].

We demonstrate a novel approach which utilizes the process of relaxation of a coherent hypercritical thickness ($h > h_{critical}$) strained semiconductor over-layer (InGaAs) in direct contact with an oxidizing Al-containing semiconductor (i.e. AlAs or AlGaAs). We propose that the porous and reactive interface between the semiconductor overlayer and the oxide enables extensive plastic strain relaxation due to efficient dislocation motion without interaction and generation of new dislocations. This results in the formation of a relaxed InGaAs template (**Lattice Engineered Substrate**) which is epitaxially decoupled from, but mechanically supported by the underlying GaAs substrate. Subsequent regrowth on this template (lattice engineered substrate) enables the fabrication of relaxed low threading dislocation density InGaAs buffers and device structures like 1.3 μm laser diodes and GaAs pHEMTs with high In content quantum wells.

This approach is scaleable to large substrate sizes with an appropriate grid structure. Also this technology can be implemented on InP substrates with $AlAs_{0.56}Sb_{0.44}$ as the oxidizing layer to obtain

lattice constants between InP and InAs. Implementation on GaSb substrates with $AlAs_{0.16}Sb_{0.84}$ as the oxidizing layer will enable the growth of low threading dislocation density arsenide-antimonide compounds for IR optoelectronics.

Strain Relaxation Mechanism in Lattice Engineered Substrates

Figure 1 explains the difference in strain relaxation mechanisms in conventional substrates and lattice-engineered substrates. In conventional heteroepitaxy (For example, InGaAs growth on a GaAs substrate) strain in the lattice-mismatched epilayer is relieved by formation and movement of misfit dislocations at the epilayer / substrate interface. The movement of the thread ends of a misfit dislocation is necessary to relieve the strain. However existing clusters of other misfit dislocations block this movement. Hence generation of additional misfit dislocations at the epilayer/substrate interface is required to relieve the strain in the epilayer. Thus a large number of dislocations are required to accommodate the lattice mismatch [5,6].

Rigid InGaAs /GaAs Interface   Porous InGaAs /Al$_2$O$_3$ Interface
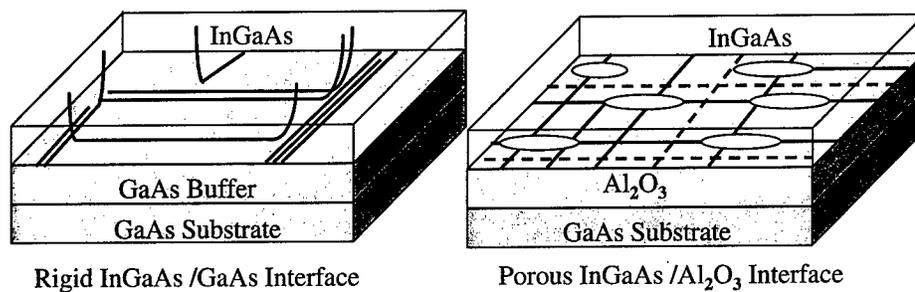
Figure 1: Strain relaxation mechanisms in conventional and lattice engineered substrates

In a lattice-engineered substrate, the strain in the epitaxial template is relieved by enhanced misfit dislocation movement at the template / oxide interface which is porous and has voids. Also some of the existing misfit dislocations are reactively removed during the process of lateral oxidation. As a result there are fewer barriers to misfit dislocation movement. This also prevents the generation of additional misfit dislocations as the existing misfit dislocations can relieve the strain. Hence the strain in the InGaAs epitaxial layer can be relieved with a fewer number of dislocations.

Growth and Processing of Epitaxial Templates for Lattice Engineered Substrates

An important component of the epitaxial structure used to generate the lattice engineered substrate is the growth of a low dislocation density highly strained template layer with smooth surface morphology over a AlAs oxidation layer. The epitaxial structure consists of a strained $In_{0.2}Ga_{0.8}As$ template layer grown on a AlAs oxidation layer. The LT GaAs buffer is grown underneath the AlAs oxidation layer to assist in oxidation. The $In_{0.2}Ga_{0.8}As$ template layer is grown at low temperature (430 °C) to minimize the formation of dislocations and maintain a two-dimensional growth front. The $In_{0.2}Ga_{0.8}As$ layer is capped with an AlGaAs etch stop layer and GaAs cap layer to protect it during oxidation. Figure 2 shows the layer structure and a TEM micrograph of the epitaxial structure. Though a few misfit dislocations are observed at the AlAs/InGaAs interface, there are no threading dislocations in the InGaAs template layer. The contrast in the TEM micrograph indicates that the InGaAs epitaxial layer is under strain.

After growth, the substrate is patterned using photolithography and reactive ion etching into 100 µm x 100 µm square mesas to enable lateral oxidation of the AlAs layers. Lateral oxidation was carried out in a furnace with steam generated by bubbling N_2 gas through water maintained at 90 °C[7]. The

oxidation temperature was 420 °C and the oxidation time was 20 minutes. The process of lateral oxidation results in relaxation of the InGaAs epitaxial layers[8]. After lateral oxidation the protective cap layers are

| 200 Å GaAs Cap |
| 50 Å Al$_{0.5}$Ga$_{0.5}$As etch stop |
| In$_{0.2}$Ga$_{0.8}$As template |
| 500 Å AlAs oxidation layer |
| LT GaAs Buffer |
| GaAs Buffer |
| GaAs Substrate |
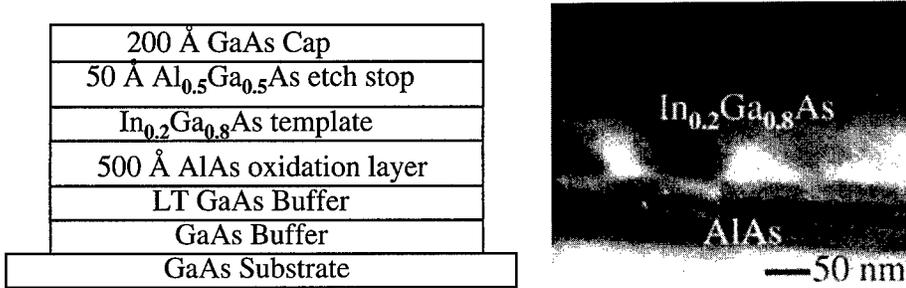
Figure 2: Layer structure and TEM Micrograph of the as-grown template
used to generate the lattice engineered substrate

removed by selective wet etching. Thus an epitaxially decoupled In$_{0.2}$Ga$_{0.8}$As template (lattice-engineered substrate) on a GaAs substrate is obtained. The substrate is then loaded in the molecular beam epitaxy system. The native oxide on the In$_{0.2}$Ga$_{0.8}$As template is removed using in-situ Ar ion cleaning. 5000 Å thick In$_{0.11}$Ga$_{0.89}$As buffer layer is grown on the In$_{0.2}$Ga$_{0.8}$As template at a growth temperature of 510 °C. For comparison the same epitaxial layer is grown on a GaAs substrate under the same growth conditions.

Structural Characterization of Epitaxial Layers grown on Lattice Engineered Substrates
• AFM Characterization

Surface morphology is a good indicator of dislocation generation mechanisms for epitaxial systems with low mismatch. The dislocation strain fields arising from misfit dislocations at the lattice mismatched interface result in surface roughening and crosshatched patterned morphology[9]. Figure 3 shows AFM scan of the In$_{0.11}$Ga$_{0.89}$As layer grown on the lattice-engineered substrate and on GaAs

In$_{0.11}$Ga$_{0.89}$As on GaAs Substrate   In$_{0.11}$Ga$_{0.89}$As on Lattice Engineered Substrate
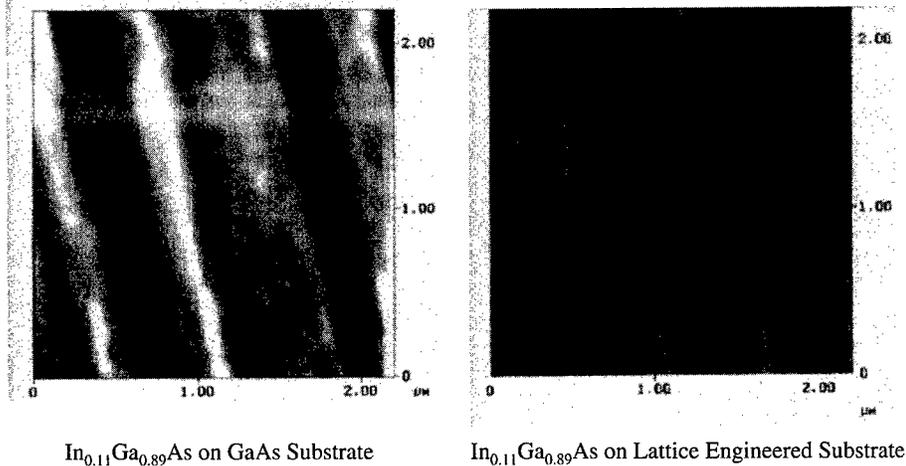
Figure 3: AFM Scans of InGaAs layers grown on GaAs substrate and Lattice Engineered Substrate

substrate. The RMS roughness of InGaAs layer grown on the lattice-engineered substrate is 3 Å. The maximum height difference between the surface features is 32 Å. For comparison the $In_{0.11}Ga_{0.89}As$ layer grown on GaAs substrate has a RMS surface roughness of 9 Å with a maximum height difference of 50 Å. The AFM scan of $In_{0.11}Ga_{0.89}As$ layer on GaAs shows undulations associated with clusters of misfit dislocations, we attribute the clustering of misfit dislocations to heterogeneous generation of threading dislocations. These dislocation pileups at the InGaAs/GaAs interface also result in increased surface roughness. The reduced height difference and the surface roughness for InGaAs grown on lattice engineered template indicates either less strain relaxation, or more homogeneous relaxation.

TEM characterization

Lattice-mismatched growth of $In_xGa_{1-x}As$ (x ~ 0.10) on GaAs results in the formation of misfit dislocations at the InGaAs interface when the $In_xGa_{1-x}As$ thickness exceeds the critical thickness. The strain due to lattice mismatch for these compositions of $In_xGa_{1-x}As$ is not enough to generate high threading dislocation densities in the $In_xGa_{1-x}As$ epitaxial layers. Figure 4 shows cross sectional TEM micrographs of the partially relaxed 5000 Å $In_{0.11}Ga_{0.89}As$ layers grown on both the lattice engineered substrate and directly on GaAs. The cross sectional TEM image of $In_{0.11}Ga_{0.89}As$ grown directly on GaAs shows misfit dislocations and the characteristic strain contrast associated with misfit dislocations at or

In_{0.11}Ga_{0.89}As on GaAs Substrate $In_{0.11}Ga_{0.89}As$ on Lattice Engineered Substrate
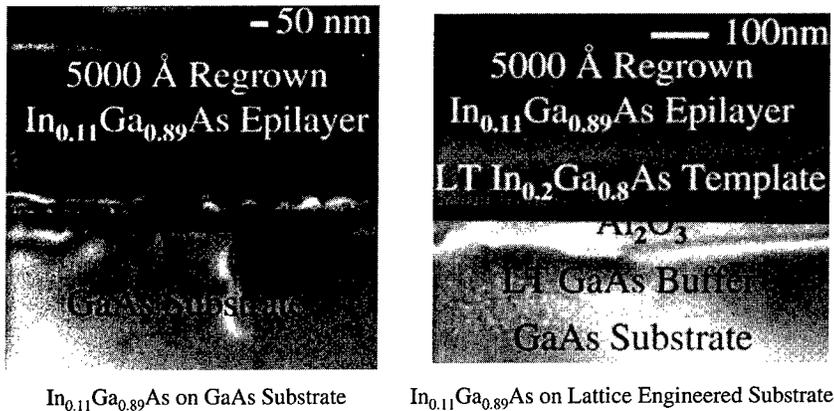
Figure 4: TEM Micrographs of InGaAs layers grown on GaAs substrate and Lattice Engineered Substrates

near the InGaAs/GaAs interface. For comparison, the thick $In_{0.11}Ga_{0.89}As$ layers grown on the lattice engineered substrate show neither misfit dislocations nor strain contrast at either the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface or the $In_{0.11}Ga_{0.89}As/In_{0.2}Ga_{0.8}As$ interface.

The absence of dislocation strain contrast in the TEM images of the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is the remarkable feature of this new approach to strain relaxed layers. Normally in plastic relaxation of strained layer, misfit dislocations act as barriers to the further strain relaxation, by blocking the motion of threading dislocations, which must generate the misfit dislocations[6,10]. We propose that the strain relaxation in $In_{0.2}Ga_{0.8}As$ is enhanced due to the absence of misfit dislocation at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface. The absence of misfit dislocations or local strain contrast at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is attributed to both the reactive material removal during oxidation and the porous nature of the oxide itself.

Thus the local strain associated with misfit dislocations at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is eliminated, or at least markedly reduced (note the absence of strain contrast in the cross sectional TEM) by effective removal of the misfit dislocation segments at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface. We must

emphasize, however that strain relaxation in the $In_{0.2}Ga_{0.8}As$ layers occurs by normal dislocation plasticity and not by any of the processes proposed for strain relaxation in compliant substrates[11]. For both structures, no threading dislocations were observed in the cross-sectional TEM images. Thus the threading dislocation density in both cases was less than 10^7 /cm^2. The mesa structure of the samples prevents the use of plan view TEM. Experiments using this approach to higher In content buffers are in progress.

Off-axis (115 and -1-15) X-ray diffraction was used to determine the in-plane and out-of-plane lattice constant and the strain state of the epilayers grown on the lattice-engineered substrate and the GaAs substrate. Self-consistency of the measurements was checked by on-axis (004) X-ray diffraction which was used to determine out-of-plane lattice constant independently. The InGaAs layer grown on the lattice-engineered substrate was relaxed to 66 % of its unstrained in-plane lattice constant. X-Ray analysis InGaAs grown on the GaAs substrate shows 60 % relaxation. The Indium composition as calculated from peak separation was 11 % in both cases.

Optical Characterization of 1.3 µm Quantum wells grown on Lattice Engineered Substrates

One of the major applications of GaAs based lattice engineered substrates is the fabrication of 1.3 µm lasers on GaAs substrates. Cost-effective high speed, short distance optical communication networks will be enabled by the fabrication of temperature-stable 1.3 µm lasers on large area GaAs substrates. At present these devices are grown on InP substrates using the InGaAsP/InP material systems. In addition to substrate size limitations, lasers based on the InGaAsP/InP material system are not temperature-stable due to the low band-offsets. Recently high temperature (210 °C) operation of 1.3 µm InGaP/InGaAs lasers on

| 200 Å $In_{0.16}Ga_{0.84}As$ |
| 1000 Å $In_{0.16}Al_{0.24}Ga_{0.60}As$ |
| 1000 Å $In_{0.16}Ga_{0.84}As$ |
| 100 Å $In_{0.43}Ga_{0.57}As$ |
| 2000 Å $In_{0.16}Ga_{0.84}As$ |
| 3000 Å $In_{0.16}Al_{0.24}Ga_{0.60}As$ |
| 1000 Å $In_{0.16}Ga_{0.84}As$ |
| $In_{0.2}Ga_{0.8}As$ Template with |
| AlAs Defect Diffusion Barrier |
| Al_2O_3 |
| LT GaAs Buffer |
| GaAs Substrate |
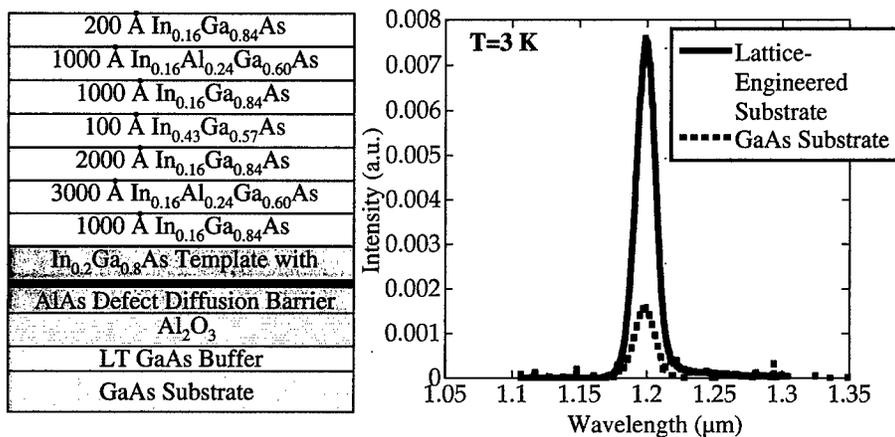
Figure 5 : Layer structure and Low temperature PL spectrum of 1.3 µm SCH structure grown on LES

InGaAs ternary substrates was demonstrated[12]. However this approach is currently limited by substrate size and composition control of the ternary substrate. GaAs based Lattice Engineered Substrates are a cost-effective viable alternative to InGaAs ternary substrates.

As a first step towards the fabrication of 1.3 µm laser on GaAs based lattice engineered substrate a SCH structure with $In_{0.16}Ga_{0.84}As/In_{0.43}Ga_{0.57}As$ quantum wells was grown. Figure 5 shows layer structure and low temperature PL spectrum of 1.3 µm SCH structure with $In_{0.16}Ga_{0.84}As/In_{0.43}Ga_{0.57}As$ quantum well. As seen from the figure the PL intensity of the quantum well grown on the lattice engineered substrate is about 7 times larger than on GaAs substrate. The low temperature PL peak is at

1.20 μm (1.29 μm at room temperature). The PL linewidth is 14 meV and is comparable to 1.3 μm quantum well structures grown on InP substrates.

Conclusion

In conclusion we have demonstrated that lateral oxidation of AlAs in conjunction with strained layers can be used generate epitaxial substrates with new lattice constants. The structural and optical quality of these layers is superior to those grown directly on GaAs substrates. These results suggest that lattice engineering through lateral oxidation of Al-containing compounds is a promising technique to generate substrates with new lattice constants for low threading dislocation density growth of technologically important semiconductors which cannot be grown on conventional substrates. This will enable the fabrication of long wavelength optoelectronic devices and high efficiency GaAs pHEMTs on GaAs based lattice engineered substrates. InP based lattice engineered substrates will enable the fabrication of low voltage, low power $Al_{0.3}In_{0.7}As/Ga_{0.3}In_{0.7}As$ HBTs and ultra low-power AlInAs/GaInAs on insulator HEMTs for satellite and wireless applications.

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OPTIMIZATION OF MICROSTRUCTURE AND DISLOCATION DYNAMICS IN In$_x$Ga$_{1-x}$P GRADED BUFFERS GROWN ON GaP BY MOVPE

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ABSTRACT

To engineer high-quality In$_x$Ga$_{1-x}$P graded buffers on GaP substrates (In$_x$Ga$_{1-x}$P/GaP), we have explored the evolution of microstructure and dislocation dynamics in these materials. We show that the primarily limiting factor in obtaining high-quality In$_x$Ga$_{1-x}$P/GaP is a new defect microstructure that we call branch defects. Branch defects pin dislocations and result in dislocation pileups that cause an escalation in threading dislocation density with continued grading. The morphology of branch defects is dominated by growth temperature, which can be used to suppress the strength or density of branch defects. In the absence of branch defects, we observe nearly ideal dislocation dynamics that are controlled by the kinetics of dislocation glide. This new understanding results in two primary design rules for achieving high-quality materials: 1) control branch defects, and 2) maximize dislocation glide kinetics. Combining these design rules into optimization strategies, we develop and demonstrate processes based on single and multiple growth temperatures. With optimization, threading dislocation densities below 5×10^6 cm^{-2} are achieved out to x = 0.39 and a nearly steady-state relaxation process is recovered.

INTRODUCTION

In$_x$Ga$_{1-x}$P graded buffers on GaP (In$_x$Ga$_{1-x}$P/GaP) are promising substrates for optoelectronic devices. In$_x$Ga$_{1-x}$P/GaP acts as a transparent substrate to devices integrated to the final composition. Direct bandgap light emission ranging from 560 nm into the infrared is accessible using a common substrate and without aluminum in the active layer of devices. In$_x$Ga$_{1-x}$P/GaP also offers higher thermal conductivity than GaAs-based systems for high power operation[1].

Graded buffers are used to efficiently relax the mismatch strain between a substrate and an epitaxial film of differing lattice constants[2]. In$_x$Ga$_{1-x}$P/GaP has been grown by hydride vapor phase epitaxy (HVPE) [3,4], gas-source molecular beam epitaxy (GSMBE)[5], and metal-organic vapor phase epitaxy (MOVPE) [6]. Stinson et al reported that the intensity of LEDs grown on In$_x$Ga$_{1-x}$P/GaP by HVPE dropped above 600 nm, likely due to increasing threading dislocation density, ρ_{thread}, with continued grading[4]. Chin et al reported a similar degradation in photoluminescence in In$_x$Ga$_{1-x}$P/GaP grown by GSMBE[5]. Degradation in all cases occurs at x ~ 0.33, which limits device applications since In$_x$Ga$_{1-x}$P has a direct bandgap only for x > 0.27[7].

We recently demonstrated that the primary cause of degradation with continued grading in In$_x$Ga$_{1-x}$P/GaP was the nearly exponential escalation of ρ_{thread} with continued grading beyond roughly x = 0.3[6]. This is surprising, because models of strain relaxation in graded buffers predict a steady-state process[8,9]. Samavedam et al demonstrated that escalating dislocation density in Ge$_x$Si$_{1-x}$/Si was caused by dislocation pileups that immobilize gliding dislocations and force additional dislocation nucleation[10]. In Ge$_x$Si$_{1-x}$/Si, the primary cause of pileups is an interaction between dislocations and surface roughness. In In$_x$Ga$_{1-x}$P/GaP, we discovered that a new defect microstructure that we call branch defects is primarily responsible for pileup formation[6]. In the absence of branch defects, we found that dislocation glide kinetics control dislocation dynamics.

In this paper, we will condense the understanding of the evolution of microstructure and dislocation dynamics in In$_x$Ga$_{1-x}$P/GaP into a set of design rules for achieving high-quality

27

materials. Through optimization, we will demonstrate defect density control over three orders of magnitude in ρ_{thread} down to $<5\times10^6$ cm^{-2} and the near recovery of steady-state relaxation.

EXPERIMENT

Undoped In$_x$Ga$_{1-x}$P graded buffers were grown on (001) GaP off-cut 10° towards a {011}. A Thomas Swan atmospheric pressure MOVPE reactor was used with trimethylgallium, solution trimethylindium, and PH$_3$ source gases carried in H$_2$ flowing at 5 slpm. Substrates were placed on a graphite susceptor in a horizontal, rectangular quartz reactor. Growth temperature was controlled by a halogen lamp under the reactor and a thermocouple inside the susceptor.

Samples began with a 0.5 µm GaP homoepitaxial buffer, followed by a graded composition buffer, and finished with a 4 µm uniform composition layer. An average grading rate of 0.4% strain/µm, which corresponds to 5% indium/µm, and growth temperatures ranging from 650°C to 810°C were used. Additional details are available in prior reports[6,11].

RESULTS

The primary cause of dislocation pileups in In$_x$Ga$_{1-x}$P/GaP is the formation of <110> branch-like defects with tensile local strain fields[11], which we call branch defects. Branch defects hinder or pin gliding dislocations, resulting in dislocation pileups. Figure 1 show branch defects and dislocation pinning, as seen in plan-view transmission electron microscopy (PVTEM).

Experiments show that branch defect morphology and evolution are dominated by growth temperature. The most obvious change is in the density of branch defects, ρ_{branch}, which decays exponentially with temperature, as shown in Figure 2. Typical dislocation pileup densities, ρ_{pileup}, in these samples range from 50 cm^{-1} to 2000 cm^{-1}, so clearly not all branch defects result in dislocation pileups. Figure 3 shows the trends in ρ_{thread} and ρ_{pileup}, which clearly indicate that more dislocation pileups occur with increasing temperature. Since ρ_{branch} decays exponentially with temperature, it must be that not all branch defects result in pileups and the ability of a branch defect to pin dislocations must increase with increasing temperature.

Differences in branch defect strength can be seen in PVTEM images: branch defects look sharper and stronger with increasing growth temperature. Furthermore, branch defects at high temperatures turn bend contours in PVTEM images much more sharply than at low temperatures, suggesting that the branch defects possess less strain at low temperatures. It is reasonable to assume that dislocation pinning ability depends on the strength of the branch defects.

Figure 1. PVTEM image of branch defects in In$_x$Ga$_{1-x}$P/GaP graded to x = 0.26. The branch defects pin dislocations and sharply turn bend contours.
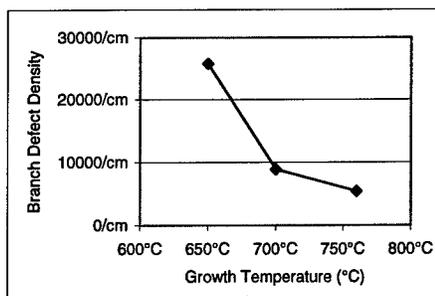
Figure 2. Average branch defect density plotted against growth temperature for In$_x$Ga$_{1-x}$P/GaP.

The relaxation model used to demonstrate the effects of branch defects[11] can be modified slightly to produce a quantitative figure for branch defect strength. Rather than simply equating mean dislocation glide length, L, to the inverse of the branch defect density, $1/\rho_{branch}$, the two quantities can be set proportional to each other by the branch defect strength, σ_{branch}:

$$L = \frac{\sigma_{branch}}{\rho_{branch}} \qquad\qquad (1)$$

Physically, σ_{branch} is the probability that a dislocation will be pinned by a branch defect. Alternatively, the inverse $1/\sigma_{branch}$ is the average number of branch defects a dislocation glides through before being pinned. Figure 4 plots σ_{branch} versus temperature. Clearly, the effect of branch defects on dislocation dynamics is dominated by changes in the branch defect strength.

Additional experiments show that branch defects have an evolution and appear only after some amount of grading. The onset of branch defect formation is dependent on temperature, hence a phase diagram can be developed, as shown in Figure 5. The later onset of branch defect formation at higher temperatures means that they can be avoided longer at high temperatures.

The evolution of branch defects highlights an important consideration in calculating σ_{branch}. Since branch defects evolve with grading, the strength of branch defects also changes with grading and calculated values for σ_{branch} represent integrated averages of branch defect strength. Furthermore, care must be taken to set the boundary conditions of the model within a regime where branch defects are actually present, otherwise false values will be calculated.

Figure 5 suggests an interesting possibility: at low compositions, branch defects are absent and nearly ideal dislocation dynamics should be observed. At x ~ 0.1, Figure 6 shows that ρ_{thread} decays exponentially with temperature, the opposite of the trend observed in Figure 3. Clearly, the limiting phenomena for relaxation are very different in the absence of branch defects.

Figure 6 suggests that relaxation becomes more efficient with increasing temperature. The change in surface morphology shown in Figure 7 also suggests an improvement of dislocation dynamics: the transition from a rough, cellular surface at low temperatures to a smooth, ordered crosshatch surface at higher temperatures is indicative of efficient strain relaxation in low-mismatch systems by dislocation glide. The exponential temperature dependence of ρ_{thread} also suggests that a kinetic mechanism limits dislocation dynamics in the absence of branch defects. If relaxation is envisioned as a process of dislocation nucleation and subsequent glide to relieve strain, it is apparent that if nucleation were rate limiting, then ρ_{thread} would increase exponentially with temperature. The observed trend is the exact opposite, suggesting that dislocation glide
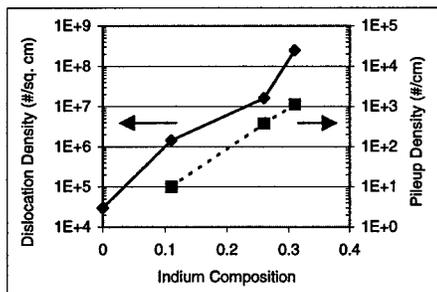
Figure 3. Threading dislocation density and dislocation pileup density versus final graded buffer composition.
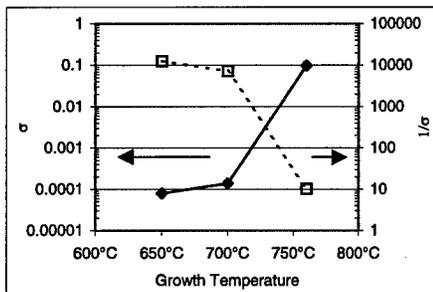
Figure 4. Branch defect strength and its inverse plotted versus growth temperature.
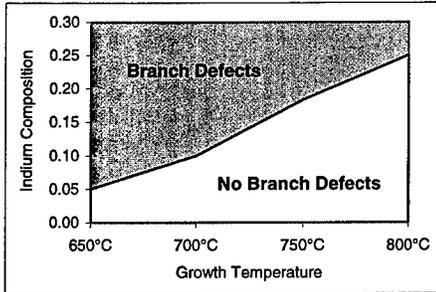
Figure 5. Phase diagram for branch defects at x ~ 0.3.
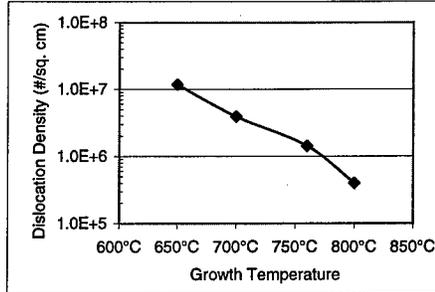
Figure 6. Threading dislocation density versus growth temperature x ~ 0.1, in the absence of branch defects.

kinetics limit relaxation in $In_xGa_{1-x}P/GaP$ in the absence of branch defects.

The newly acquired understanding of branch defect evolution and ideal dislocation dynamics in $In_xGa_{1-x}P/GaP$ is useful in process optimization. The simplest approach is to consolidate the data into one graph, as shown in Figure 8. At x > 0.3, increasing branch defect strength with temperature limits material quality, so a low growth temperature is preferable. At low compositions, dislocation glide kinetics limit material quality and a high growth temperature is desirable. Unless substrates are patterned or significant dislocation annihilation can be induced, dislocations generated at a low composition are retained with further grading. Therefore, the temperature dependencies of branch defect strength and dislocation glide kinetics combine to form a process window near 700°C for the growth of high-quality $In_xGa_{1-x}P/GaP$ with compositions of x > 0.3 at a single temperature.

Unfortunately, the process window is narrow and dislocation density increases exponentially in either direction. Clearly, the imperatives for any optimization strategy intended to open up the process window are to control branch defects and maximize dislocation glide kinetics. Our current optimization strategy incorporates both design rules into a two-step process.

First, the highest possible temperature is used initially. High temperatures maximize dislocation glide kinetics, resulting in low values of ρ_{thread}. Extrapolation of Figure 6 shows that $\rho_{thread} = 3 \times 10^4$ cm^{-2} at 926°C, which is equal to the measured ρ_{thread} of the GaP substrates, thus setting an upper bound for useful growth temperature. Furthermore, Figure 5 shows that the onset of branch defect formation occurs later at higher temperatures, therefore a high growth temperature avoids the formation of branch defects for as long as possible.

Then, just before the onset of branch defect formation at the initial high temperature, the growth temperature is dropped sharply. Since branch defects are inevitable at this point, lowering the temperature is used to suppress the branch defects strength. While it may appear that this would slow dislocation glide kinetics and result in higher ρ_{thread}, this does not occur in
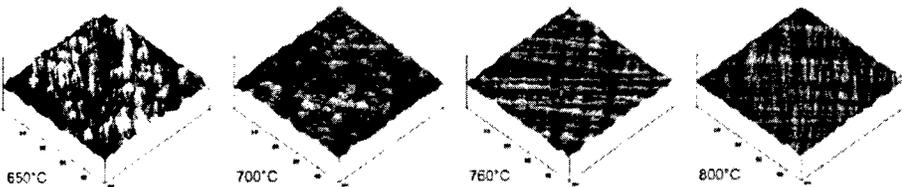
Figure 7. Atomic force microscopy images of surface morphology versus growth temperature at x ~ 0.1.

30

practice because dislocation glide kinetics increase with grading. While dislocation glide kinetics data is not available for $In_xGa_{1-x}P$, it can be estimated from existing data. Dislocation glide kinetics have been measured to be orders of magnitude faster in InP^{12} than in GaP^{13}. The equilibrium phase diagram for $In_xGa_{1-x}P$ in Figure 9[14] shows that most of the change in solidus temperature occurs between x = 0 to x ~ 0.3, so most of the change in materials properties between GaP and InP should occur in that range. Therefore, dislocation glide kinetics should increase orders of magnitude when grading $In_xGa_{1-x}P$ on GaP substrates, allowing a sharp temperature drop without increasing ρ_{thread} if the resulting dislocation glide kinetics are as fast as those at the beginning of the graded buffer. The largest allowable temperature drop can be calculated by estimating the change in dislocation glide kinetics with composition, as shown in Figure 10. A temperature drop of roughly 100°C to 150°C is possible at x = 0.2 without increasing ρ_{thread} due to slow dislocation glide kinetics.

An early optimized sample grown by a three-step process (760°C, 700°C, and 650°C) resulted in $\rho_{thread} = 4.7 \times 10^6$ cm^{-2} at x = 0.39, compared to $\rho_{thread} = 6.8 \times 10^6$ cm^{-2} at x = 0.34 in the best sample grown at a single growth temperature of 700°C. Optimization both decreases overall defect density and extends the useful range of indium compositions. Since branch defect strength dominates dislocation dynamics, a two-step process is likely to be an even better strategy. Figure 11 compares the escalation of ρ_{thread} with grading shown earlier in Figure 3 with results from optimized samples. The optimized samples appear to recover nearly steady-state behavior at $\rho_{thread} \sim 10^6$ cm^{-2} and further optimization may achieve $\rho_{thread} < 10^6$ cm^{-2}.
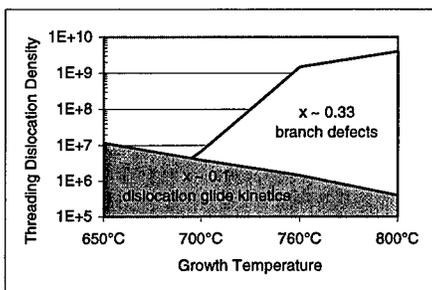
Figure 8. Consolidated graph of threading dislocation density versus growth temperature for $In_xGa_{1-x}P$/GaP.
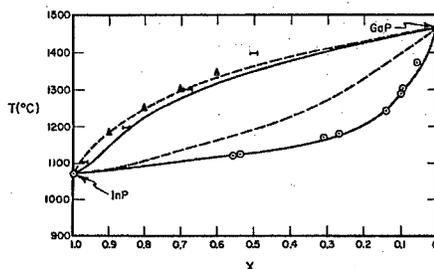
Figure 9. Equilibrium phase diagram for $In_xGa_{1-x}P$. Taken from Ref. 14 and digitally edited.
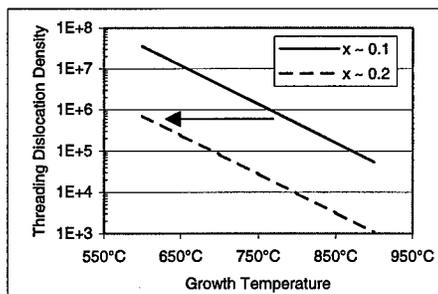
Figure 10. Plot used to estimate maximum allowable growth temperature drop for optimization.
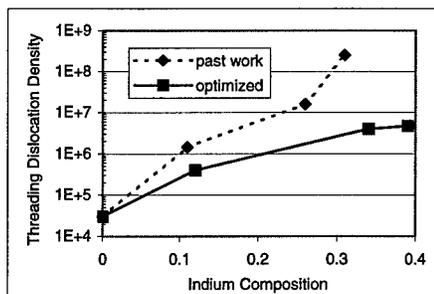
Figure 11. Comparison of threading dislocation density versus grading before and after optimization.

31

CONCLUSIONS

The evolution of branch defects has been mapped as a function of growth temperature and composition. Since a 0.4% strain/μm average grading rate was used in all of the samples, the composition dependence also corresponds to a total thickness dependence and further experiments are necessary to deconvolute the composition and thickness dependencies of branch defect morphology. Furthermore, the branch defect phase diagram allowed the exploration of nearly ideal dislocation dynamics at low indium compositions. Dislocation glide kinetics were identified as the limiting mechanism for relaxation in the absence of branch defects.

The new understanding of the evolution of microstructure and dislocation dynamics in $In_xGa_{1-x}P/GaP$ was condensed into design rules for achieving high-quality materials: 1) control branch defects and 2) maximize dislocation glide. For materials grown at a single growth temperature in our system, the two design rules combine to form a sharp process window near 700°C. More sophisticated optimization involves changes in growth temperature to open up the process window, resulting in reduced defect densities and increased grading range.

We are currently working on better optimization of growth processes to further improve material quality. Estimates made with our dislocation dynamics models suggest that values of $\rho_{thread} < 10^6$ cm^{-2} should be achievable in $In_xGa_{1-x}P/GaP$. Even in the current range of defect densities, high-quality LED operation should be possible and we have begun to test devices grown on $In_xGa_{1-x}P/GaP$. With further development, the promise of efficient LEDs based on entirely epitaxial transparent substrates of $In_xGa_{1-x}P/GaP$ should be fulfilled.

ACKNOWLEDGEMENTS

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KINETIC MODELLING OF THE SELECTIVE EPITAXY OF GaAs ON PATTERNED SUBSTRATES BY HVPE. APPLICATION TO THE CONFORMAL GROWTH OF LOW DEFECT DENSITY GaAs LAYERS ON SILICON

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ABSTRACT

The selective growth of GaAs by HVPE was studied on (001), (110), $(111)_{Ga}$ and $(111)_{As}$ GaAs patterned substrates by varying the III/V ratio. A kinetic modelling of the growth was developed, based upon the SEM observations of the growth morphologies as well as on experimental curve synthesis. The growth rate is written as a function of the diffusion fluxes of the adsorbed AsGa and AsGaCl molecules and takes into account the chlorine desorption by H_2. 1.5 μm thick GaAs films were then fabricated on Si (001) by a confined epitaxial lateral overgrowth technique. These conformal films exhibit intense and uniform luminescence signals, showing that the dislocation densities of GaAs are lower than 10^5 cm^{-2}. SEM analyses reveal that conformal growth fronts consist in (110) and $(111)_{As}$ planes under the III/V ratios (superior to 1) which were tested.

INTRODUCTION

Heteroepitaxial growth of high quality GaAs on Si offers great potentialities for high-power laser diode or field effect transistor applications. The monolithic integration of high-performance optoelectronic GaAs devices on Si could also be used for the optical interconnection of complex Si IC's. The conventional GaAs heteroepitaxy on Si leads to high defect density III-V materials due to the 4% lattice mismatch and to the difference in the thermal expansion of the GaAs and Si crystals. Reduced area growth on patterned substrates based upon selective epitaxy has revealed its efficiency in producing higher quality materials [1-2]. Selectivity is easily obtained by using the hydride vapor phase epitaxy (HVPE) (GaCl, As$_4$, HCl, H$_2$) vapor phase. HVPE makes use of near equilibrium partial pressures. The subsequent low supersaturation of the vapor phase is then sufficient to ensure nucleation on GaAs but is not high enough for nucleation on the Si-related surfaces where the nucleation barrier is much higher. The selective growth of GaAs was studied on GaAs (001), (110), $(111)_{Ga}$ and $(111)_{As}$ patterned substrates. The growth using chloride precursors is governed by the kinetics. The growth morphology and the growth rates are then mainly controlled by the growth anisotropy. A kinetic model is presented which describes the adsorption and desorption mechanisms involved in the growth process and takes into account the diffusion fluxes of the adsorbed species to the kinks. Experimental parameters were then optimised for the fabrication of low defect density GaAs/Si films by conformal growth based upon the selective confined lateral epitaxy of GaAs from GaAs seeds beforehand grown on Si.

GaAs/GaAs SELECTIVE EPITAXY

The selective epitaxy of GaAs was carried out in a hot wall horizontal HVPE reactor by using diluted arsine gas (AsH_3) and GaCl gaseous molecules, synthetised inside the reactor by the use of an HCl flow reacting with a Ga metallic source. The experiments were carried out at atmospheric pressure, under an H_2 vector flow of 3 l/min, on GaAs (001) and 2° misoriented (001) patterned substrates. Si_3N_4 masks were deposited in which stripes of various orientation from 0° up to a misorientation of 90° from [110] were periodically opened (5 μm wide, every 200 μm) resulting in an opened/masked area ratio of 2.5%. The growth temperature was varied from 685°C to 760°C. Given the diameter of the arsine supply quartz tube and the total (AsH_3, H_2) flow in the tube, the arsine gas was completely decomposed into As_2, As_4 gaseous species under the temperature profiles which were tested. The partial pressure of GaCl (written here [GaCl]) was varied from 1.6×10^{-3} to 6.4×10^{-3} atm, the partial pressure of As_4 ([As_4]) was varied from 3.0×10^{-4} to 7.2×10^{-4} atm, the partial pressure of additional HCl was varied from 2×10^{-5} to 1.2×10^{-3} atm. The results are discussed as a function of the III/V ratio defined here as the [GaCl]/[As_4] partial pressure ratio.

The SEM cross-section observation of selective GaAs [110] and [1$\overline{1}$0] oriented stripes grown at 730°C for 1<III/V<5 ratio on (001) substrates showed regular bands limited by {001} and {110} planes (Fig. 1). The thickness of GaAs epilayers were found in the [001] direction equal to 15 μm (in 30 minutes process) which was twice as large as the lateral extension. By using the same experimental conditions on 2° misoriented substrates, we observed that the stripes were systematically limited by $(111)_{As}$ faces (Fig. 2).
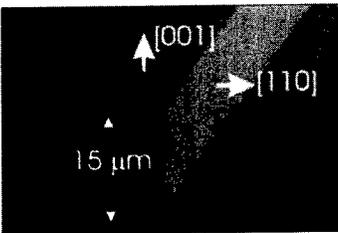
Fig. 1 : [1-10] oriented GaAs stripe on GaAs (001) for III/V = 5.
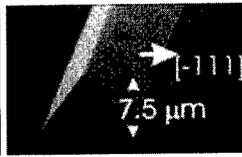
Fig. 2 : [110] oriented GaAs stripe on GaAs (001) 2° off for III/V = 5.
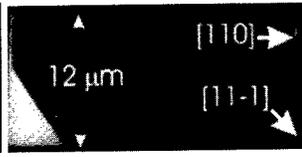
Fig. 3 : [1-10] oriented GaAs stripe on GaAs (001) for III/V = 9.

$(111)_{As}$ faces were found also developed on exactly (001) oriented substrates when higher III/V ratios (9 and 11) were used (Fig. 3). The evolution of the growth anisotropy as a function of the temperature has been assessed. When the temperature was decreased (715, 700 and 685°C), one observed a significant appearance of $(111)_{As}$ faces (Fig. 4a and 4b). The crystal shape developed under equilibrium conditions corresponds to the minimisation of the surface energy. In practical case, kinetic factors determine indeed the final growth shape which is limited by lower growth rate faces in the convex shaped growth. The hierarchy of the growth rates (R) as a function of the orientation of the faces can thus be determined as a function of the vapor phase composition. At 730°C and III/V=5, the following hierarchy $(111)_{Ga}>>(001)>(111)_{As} \geq (110)$ is assessed which is in agreement with the chloride and hydride VPE data published in the 70' and 80' [3-5]. R(110) becomes twice as large as
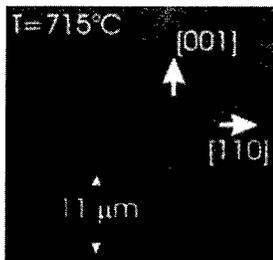
Fig. 4a : [1-10] oriented GaAs stripe on GaAs (001) for III/V = 5.
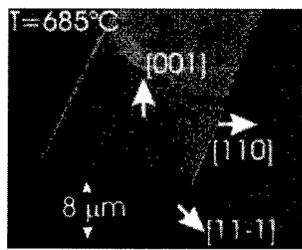
Fig. 4b : [1-10] oriented GaAs stripe on GaAs (001) for III/V = 5.
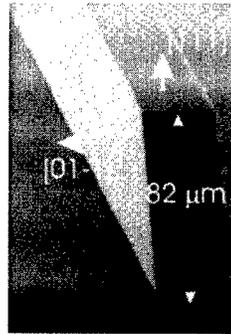
Fig. 5 : [-211] oriented GaAs stripe on GaAs (111)A for III/V = 9.

R(111)$_{As}$ when the III/V ratio is increased up to 9. The growth rate of (111)$_{As}$ also diminishes more quickly when the temperature is decreased. The same trend is observed when growth takes place on misoriented substrates, although one must notice that [110] oriented stripes grown with quite similar (110) and (111)$_{As}$ growth rates could develop in a knife shape. In order to clarify these different behaviors, GaAs growths on unmasked (001) as well as on (110), (111)$_{Ga}$ and (111)$_{As}$ unmasked and patterned substrates were carried out [6]. Fig. 5 displays a SEM picture of a [$\bar{2}$11] oriented GaAs stripe confirming the remarkably high growth rate of the (111)$_{Ga}$ face (82 μm/h). R(110) was found equal or slightly lower than R(111)$_{As}$ for III/V = 5 (mean values of 7 μm/h were measured for the pyramids growth regime on exact substrates) whereas it becomes larger than R(111)$_{As}$ when III/V = 9. The variations of the growth rate of (001) as a function of the temperature was determined at a constant III/V ratio of 5 (Fig. 6). R(001) was found to decrease when the III/V ratio was increased for the partial pressures which were tested. The kinetic modelling of the GaAs growth was first developed for the (001) face.

KINETIC MODELLING

For the (001) GaAs growth, one consider the adsorption of As molecules on the Ga atoms of the crystal followed by the adsorption of the GaCl molecules onto the As atoms. In a first mechanism, the chlorine desorption by H_2 into HCl leads to the formation of the GaAs crystal :

$$As_{4g} \leftrightarrow 2As_{2g} \qquad\qquad 2V + As_{2g} \xleftrightarrow{\text{R1}} 2As \qquad\qquad As + GaCl_g \xleftrightarrow{\text{R2}} AsGaCl$$

$$AsGaCl + H_{2g} \xleftrightarrow{\text{R3}} AsGa + HCl_g + \frac{1}{2}H_{2g}$$
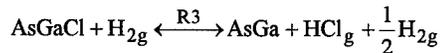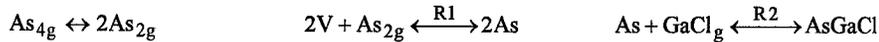
The net adsorption fluxes of As, AsGaCl and AsGa species $J_i = J_{+i} - J_{-i}$ are written considering the kinetics of the reactions R+i and R-i related to these adsorbed species. The adsorption fluxes (J_{+i}) and desorption fluxes (J_{-i}) per surface unit are written as a function of the kinetic

constants of the reactions k_{+i} and k_{-i} which regroup the partition functions of either gaseous molecules or adsorbed species which participate in the considered reaction. The fluxes depend also on the coverage ratio $\theta_{R\pm i}$ of the adsorbed species and vacant sites V on the surface as well as on the partial pressures of gaseous molecules $P_{R\pm i}$:

$$J_i = k_{+i} \times f(\theta_{R+i}, P_{R+i}) - k_{-i} \times f'(\theta_{R-i}, P_{R-i})$$

The growth depends then on the diffusion of the adsorbed GaAs and GaAsCl molecules to the kinks. The (001) face can be either misoriented, presenting terraces of length Y_0 determined by the misorientation angle, or exact, so that Y_0 represents the distance between the edges of a growth spiral corresponding to the growth pyramid regime. When the molecules are close to the steps, AsGa are directly incorporated while AsGaCl molecules do necessitate the chlorine desorption before being incorporated into the crystal. The surface diffusion fluxes are written as a function of the diffusion coefficients X_{di} and of the surface concentrations of the adsorbed species. Thus they depend upon the previous reactions $R\pm i$ which give indeed the adsorption and desorption frequencies of the involved species. The energetic parameters are the diffusion activation energies, the activation energies of the various adsorption and desorption processes which take into account lateral interaction parameters on the surface between adsorbed molecules. Considering in a first approach, that the kink steps are equally supplied by the surface diffusion fluxes of the up and down terraces, the growth rate of (001) can be written :

$$R(001) = \frac{2\Omega}{Y_0}(J_{0AsGa} + J_{0AsGaCl}) = R_{Max}\left[\sum_{i=AsGa,AsGaCl} \frac{2X_{di}}{Y_0} \tanh\left(\frac{Y_0}{2X_{di}}\right)\right]$$

with : Ω the molecular volume. R_{Max} is function of the temperature T, the surface coverage ratio in vacant sites, the partial pressures of HCl and H_2 and of the supersaturation of the vapor phase [7]. Fig. 6 displays the theoretical curve which was obtained after determining the activation energies by experimental curve synthesis.
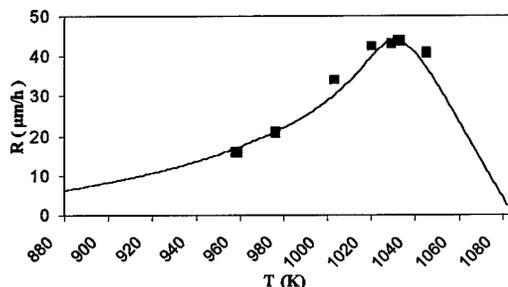
Fig. 6 : Experimental (■) and theoretical (-) GaAs (001) growth rate as a function of the temperature T at III/V = 5.

A second mechanism has been modelled for high III/V ratios involving the adsorption of GaCl in a second layer followed by a $GaCl_3$ desorption. The growth rate depends upon the surface diffusion fluxes of AsGa, AsGaCl and $GaCl_3$. The model is now developed for the growth of the (110), (111) Ga and As faces by fitting the activation energies for the adsorption/desorption and diffusion processes with respect with the various surface configurations.

CONFORMAL GaAs/Si

Conformal samples were prepared according to a general procedure previously described on 2° misoriented (001) silicon substrates on which 1.5 μm thick antiphase domain-free GaAs layers were grown by MOVPE [8]. These sacrificial GaAs layers usually exhibit dislocation densities of 10^7 cm^{-2}. The GaAs layer is covered by a dielectric cap layer in which [110] or [1$\bar{1}$0] oriented stripes are periodically opened (10 μm wide every 200 μm). The GaAs layer is then selectively underetched using an $H_2SO_4/H_2O_2/H_2O$ solution, so as to realise 125 μm wide oriented GaAs seed stripes (Fig. 7).
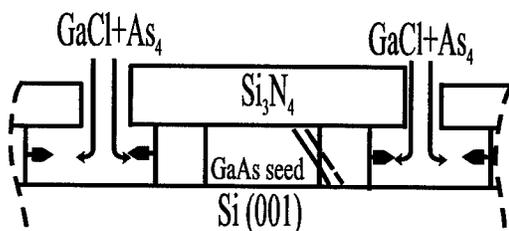
Fig. 7 : Schematic principle of conformal growth.
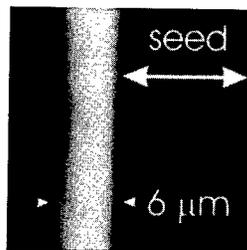
Fig. 8 : Luminescence imaging of a conformal GaAs stripe on Si.

The GaAs growth is initiated on the lateral sides of the GaAs seed stripes and develops inside the cavity formed by the silicon substrate and the overhanging dielectric cap layer. One has to note that the conformal growth technique allows for an independent control of the vertical and lateral extensions of the GaAs film as the vertical one is settled by the thickness of the GaAs sacrificial layer. The 60° type threading dislocations initially present in the GaAs seeds can not propagate far through the GaAs growing layer as they are rapidly blocked either by the cap layer or by the substrate surface. This constitutes an efficient geometrical defect-filter (Fig. 7).

1.5 μm thick GaAs films were grown on Si according to the conformal procedure. Fig. 8 displays a top view photograph of the luminescence of a typical sample under low illumination conditions (500 mW). The signal is completely quenched in the GaAs seed region due to the high density of dislocations acting as nonradiative recombination centers, whereas it is intense and uniform on the conformal GaAs film, thus revealing a high crystal quality characterised by a dislocation density lower than 10^5 cm^{-2}. Fig. 9, 10 and 11 display the SEM photographs of conformal GaAs stripes grown at III/V ratios of 5 and 9 at 730°C. {110} and {111}$_{As}$ faces constitute the conformal growth fronts in agreement with the GaAs selective growth study considering the growth was developed inside a cavity of height equal to 1.5 μm. Further characterizations (TEM, cathodoluminescence and photoluminescence spectroscopy) of the conformal GaAs films are in progress. The HVPE selective and conformal growths of GaAs and in particular, the evolution of the growth front morphologies, will be studied at III/V ratios inferior to 1.
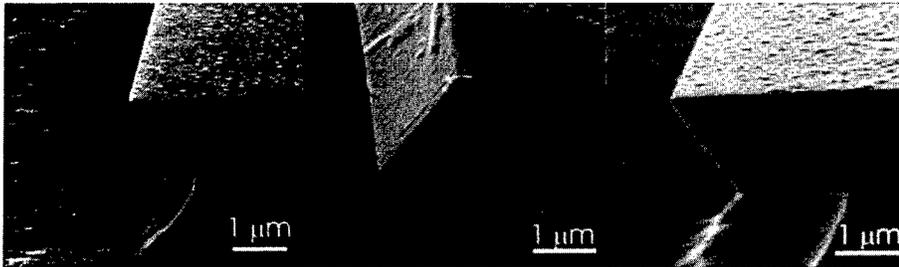
Fig. 9 : Growth front of a [1-10] oriented, 8 μm wide, conformal GaAs stripe on Si for III/V = 5.

Fig. 10 : Growth front of a [110] oriented, 17 μm wide, conformal GaAs stripe on Si for III/V = 9.

Fig. 11 : Growth front of a [1-10] oriented, 14 μm wide, conformal GaAs stripe on Si for III/V = 9.

CONCLUSION

The selective growth of GaAs by HVPE was studied on GaAs patterned substrates. A kinetic modelling was developed which takes into account the chlorine desorption by H_2 and the diffusion fluxes of the adsorbed GaAsCl and GaAs species to the kinks. Experimental parameters were then optimised for the fabrication of low dislocation density (below 10^5 cm^{-2}), 1.5 μm thick GaAs/Si films by a confined lateral overgrowth technique. The non random feature of the geometrical hindrance of the propagation of dislocations into the growing material, and the independent control of the lateral and the vertical extensions as the latter is settled by the thickness of the seed, are outstanding add-on advantages of the conformal growth technique compared to any other selective epitaxy processes. As a result, conformal GaAs films are now used for the subsequent vertical regrowth of high quality LED structures [9]. Conformal growth could also be used for the fabrication of lateral structure devices.

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GROWTH OF IMPROVED GaAs/Si: SUPPRESSION OF VOLMER-WEBER NUCLEATION FOR REDUCED THREADING DISLOCATION DENSITY

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ABSTRACT

The growth of reduced dislocation density GaAs/Si is performed by a novel two-step technique where the first epitaxy step takes place at 75° C and the second is performed at 580° C. The initial deposition is single crystal, continuous, and planar such that there is no contribution to the dislocation density from Volmer-Weber island coalescence and no trapping of dislocations in pinholes. Using this new growth technique, a reduced dislocation density the order of $10^6/cm^2$ was obtained. The improved crystallinity is indicated by the more narrow x-ray full-width-at-half-maximum (FWHM) value of 110 arc-seconds. GaAs p-i-n diodes were grown on the reduced dislocation density GaAs/Si and it was found that the resistivity of the intrinsic region for the heteroepitaxial diodes was similar to homoepitaxial ones for small mesa sizes.

INTRODUCTION

Technology for the direct integration of high-performance III-V compound semiconductor devices with charge handling functionality of modern silicon circuitry would enable monolithic optoelectronic/photonic integrated circuit fabrication. Such technology is not yet in hand. Toward this end, however, the heteroepitaxy of III-V materials (GaAs primarily) on silicon has been extensively pursued.[1-5] Heteroepitaxial devices exhibit some undesirable properties such as short "burn-out" lifetime for lasers[6] (though some last quite long). The relatively short life-to-failure of such devices has generally been attributed to the large threading dislocation density, the large residual strain, and the highly compensated epitaxial interface which is replete with anti-phase disorder.[7]

The large threading dislocation density is believed to arise because of the formation and coalescence of three-dimensional GaAs Volmer-Weber islands during initial deposition, and from the relatively large (about 4%) lattice mismatch. Post-growth annealing of the heteroepitaxial films can result in a ten- to one hundred-fold reduction in the dislocation density compared to as-grown films.[1-5] However, the high annealing temperature results in a much larger residual strain, which causes increased "cracking" of the GaAs heteroepitaxial films along [110].

In this work, we first demonstrate a novel low-temperature epitaxial technique for preventing GaAs three-dimensional Volmer-Weber island formation and coalescence during initial deposition on silicon. This new initial deposition technique (1.) eliminates the contribution to the total threading dislocation density from the Volmer-Weber island coalescence phase of crystal growth and (2.) realizes a flat, pinhole-free, continuous GaAs film which is believed to facilitate dislocation annihilation. These attributes yield the important result that thick film GaAs MBE on the new initial deposition yields films with reduced threading dislocation density, and consequently, less residual strain because of the lack of (otherwise necessary) thermal annealing.

EXPERIMENT

Samples were grown on (100) silicon substrates (arsenic terminated[10]) oriented 4° toward the nearest [110] in a VG-80H molecular beam epitaxy (MBE) system. A migration enhanced epitaxy (MEE) technique was used to deposit the Volmer-Weber-island-free new initial deposition to a thickness of 80 nm at 75° C. The deposition conditions are such that the film is single crystal and stoichiometric (in press, Journ. Appl. Phys.) The film was then heated to 580° C for thirty minutes under an arsenic overpressure; the GaAs film remained as a thermally stable, pinhole-free, planar epitaxial film.

The p-i-n light-emitting diode structure (MBE at 580° C) consisted of an 3μm n-type (silicon doped to $2 \times 10^{18}/cm^3$) layer, a 200 nm intrinsic region, and a 300 nm p-type layer doped with Be ($4 \times 10^{17}/cm^3$). Circular mesas ranging in diameter from 20 to 120 μm (a total of 7 different sizes) were then formed using standard photolithography techniques and a 1:8:40 (H_2SO_4:H_2O_2:H_2O) etching solution. Ohmic contacts were then formed using well-established gold-alloy-evaporation and annealing techniques.[11]

RESULTS
New Initial Deposition

As described more fully elsewhere,[28] amorphous and arsenic-rich GaAs would be expected by deposition at 75° C using conventional MBE techniques. The crystallinity of the GaAs grown by MEE at 75° C is indicated by the presence of the reciprocal lattice rods in the RHEED pattern of Figure 1. (Upon heating to 580° C, one obtains the (2x4) pattern.)
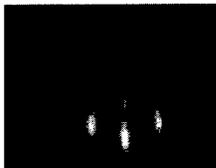
Figure 1: RHEED pattern (75° C) along an [110] azimuth from an 80 nm film.

In-situ Auger electron spectroscopy (AES) measurements were also made on the 80 nm GaAs MEE initial deposition. Shown in Figure 2 is an AES spectrum which demonstrates (1.) that the film is stoichiometric (see technique in Davis et al.[23]) to the detection limit of the PHI model 10-150 normal-incidence AES spectrometer; 0.002 ML and (2.) that the 80 nm GaAs film is continuous, and free from pinholes that extend to (or near) the silicon substrate surface (as indicated by the absence of Auger electrons emitted from the high-energy (KLL) and lower-energy (LMM) Auger transitions from silicon atoms which would be expected at 1604 eV and 92 eV respectively).
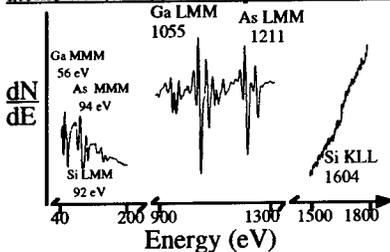
Figure 2: AES spectrum of the 80 nm GaAs Film on silicon
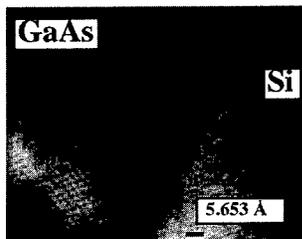
Figure 3: High-resolution TEM image of the GaAs/Si interface.

The work by Cho on low-temperature deposition[15] is important to note here because it was shown that stacking fault-type defects (from low-temperature GaAs/GaAs deposition in his case) could be removed from epitaxial films by thermal annealing at 580° C. For the GaAs/Si heteroepitaxial system of interest here, stacking fault defects are also observed as shown in Figure 3. Thermal annealing of the GaAs/Si film, however, causes a significant mass-transport governed morphology conversion driven by the misfit strain and imbalance of surface and interfacial energies between GaAs and Si. The initial two-dimensional GaAs film structurally converts to a discontinuous three-dimensional Volmer-Weber island surface (or at least to a rough pinhole-ridden surface).[16-17]

Morphological Instability

To prevent this deleterious morphology conversion of the initial GaAs deposit on Si and the possible large increase in dislocation density associated with it as described in detail by Stowell in Matthews,[18] a quantitative analysis of the conversion phenomenon was performed. For the analysis, a set of equally-spaced, non-faceted and volume-conserved Volmer-Weber islands (covering an area of the substrate given as A_{v-w}), are assumed to grow by surface diffusion out of an initially two-dimensional pinhole-free GaAs film on silicon which initially covers an area of A_m.

This quantitative analysis was solved using published surface diffusion, D, data[19] and published details of the contact angle Θ (Young's equation) of the GaAs Volmer-Weber islands on silicon.[20,21] Because the analysis discussed here is quantitative, a solution can be made for the experimental conditions under which the morphology conversion would *not* be expected to occur. The predictive expression is given in equation (1) where "t" is the annealing time.

$$\left[1 - \frac{A_{v-w}}{A_m}\right] = \left[1 - \left(\frac{\pi}{\left(4\sqrt{Dt}\right)^2}\right)\left(\frac{3\left(4\sqrt{Dt}\right)^2 h_o}{2\pi\left[1 - 3/2\cos(\Theta) + 1/2\cos^3(\Theta)\right]}\right)^{2/3}\left(1 - \cos^2(\Theta)\right)\right] \quad (1)$$

As shown in Figure 4, a planar GaAs film having a pre-annealing thickness, h_o, of 80 nm is predicted to be thermally stable (no silicon substrate exposed) and remain pinhole free at 580° C for three minutes. Also included in this figure is experimental data from previous work[16] which was independently obtained by analyzing their plan-view TEM images. There is good agreement between the results from the present AES work (squares), the prior experimental work (circles), and the predictions from equation 1 (lines).
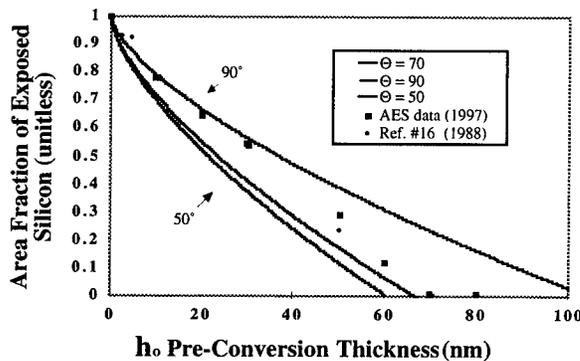
Figure 4: Predicted and measured thermal stability of thin GaAs/Si epitaxial films.

Thick Film and p-i-n Diode Device Properties

A large area plan-view image (centered dark field) of the thick-film structure before mesa processing is presented in Figure 5 which demonstrates a dislocation density on the order of $10^6/cm^2$ (dislocations enclosed with squares) and is reflective of other film areas.
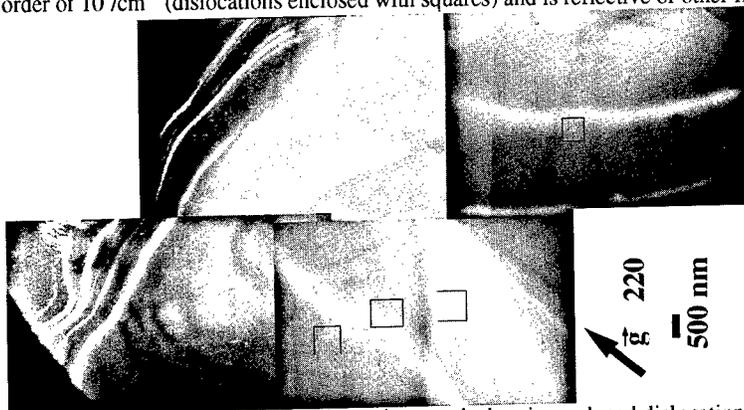
Figure 5: Large-area TEM plan-view micrograph showing reduced dislocation density.

In agreement with the TEM results, a dislocation density the order of $10^6/cm^2$ was measured by chemical etch pit counting.[12,13,14] An independent measure of the improved crystallinity is indicated by the x-ray FWHM value of 110 arc-seconds, which compares very favorably with the commonly found 200-300 arc-second value found for GaAs/Si films with a higher threading dislocation value using more conventional GaAs/Si initial deposition and growth technology.[22] The photoluminescence spectrum further indicated superior crystallinity by the FWHM value of 2.1 meV (4 Kelvin) which represents the narrowest reported value for heteroepitaxial GaAs on Si.
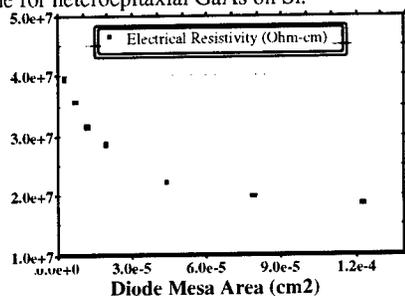
Figure 6: Resistivity of the intrinsic region as a function of p-i-n mesa size.

Dislocations passing through the intrinsic region of the p-i-n diodes can cause electrical short-circuit paths (presumably because of electrical conduction along the line-length of the dislocations, and dislocation band-tailing effects[26]) causing non-radiative recombination and less efficient electroluminescence. The resistivity of the intrinsic region was determined according to the procedure described by Sze.[24] The dependence of the intrinsic region resistivity on mesa size is plotted in Figure 6. Mesa sizes greater than, say, 2×10^{-5} cm^2 have poor resistivity values, but for mesa sizes smaller than that the onset of significant improvement in the resistivity is obtained. This might be expected since the

42

spacing of dislocations in the GaAs with a dislocation density on the order of $10^6/cm^2$ would be the order of micrometers, so mesa sizes on the order of micrometers may have no dislocations (on average).

CONCLUSIONS

In conclusion, we demonstrate an enabling technology for reduced threading dislocation density GaAs/Si heteroepitaxy with low-temperature processes. By preventing the formation and coalescence of three-dimensional GaAs Volmer-Weber islands during initial MEE deposition on silicon, a reduced threading dislocation density results. Plan-view imaging of thick GaAs/Si films demonstrates the reduced dislocation density the order of $10^6/cm^2$; a similar value is obtained by chemical etch pit counting. The improved crystallinity is also indicated by the narrow x-ray FWHM value of 110 arc-seconds, and the PL FWHM of 2.1 meV. p-i-n diodes fabricated from the improved GaAs/Si demonstrate the deleterious effect of threading dislocations passing through the intrinsic region of the p-i-n device. However, the performance as a function of diode area points to the exciting possibility of the monolithic integration of high performance 5 micrometer VCSEL (vertical cavity surface emitting laser) devices on silicon CMOS using demonstrated technology.[25]

These results are timely because the analysis of the morphological instability of dissimilar materials described here should find "universal" application for reduced dislocation density heteroepitaxy. One interesting system would be the III-nitrides where there is currently no lattice-matched substrate and there is a large contribution to the dislocation density from the coalescence phase of epitaxy. Taken further, the quantitative stability analysis (Equation 1) would seem to facilitate the extension of compliant substrate technology[8,9] to systems incorporating dissimilar materials. One might first deposit a thin, thermally stable 80 nm GaAs/Si film and then twist-bond to that. Otherwise, the thin twist-bonded GaAs layer directly on silicon would not be expected to remain thermally stable (e.g., it would undergo morphology conversion) at high temperature.

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STRAIN RELAXATION DURING HETEROEPITAXY ON TWIST-BONDED THIN GALLIUM ARSENIDE SUBSTRATES

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ABSTRACT

We realized "compliant" substrates in the square centimeter range by twist-wafer bonding of an (100) GaAs handle wafer to another (100) GaAs wafer with a several nm thick epitaxially grown GaAs layer followed by an appropriate back-etch procedure. The twist angle between the two GaAs wafers was chosen between 4 and 15 degrees. The twisted layers were characterized by area scanned X-ray diffraction, optical and electron microscopy and atomic force microscopy. Occasionally we observed regions showing pinholes in the transferred thin twist-bonded GaAs layer.

After epitaxial deposition of 300 nm InP and InGaAs films with different degrees of mismatch on these substrates, transmission electron microscopy revealed grains which are epitaxially oriented to either the substrate or the twist-bonded layer. The grain boundaries between the twisted and untwisted grains probably collect threading dislocations, thus reducing their density in the areas free of boundaries.

INTRODUCTION

A remaining challenge on growing strained heteroepitaxial thin films is to reduce the density of threading misfit dislocations which deteriorate device properties and which appear above a critical film thickness usually estimated from the Matthews-Blakeslee (MB) criterion [1]. A conventional approach to reduce this dislocation density is to make use of stoichiometrically graded buffer layers which adapt the misfit step by step [2, 3]. Alternatively, free-standing epitaxial substrates thinner than the MB thickness with regard to the deposited film were shown to behave as "compliant", i. e. to considerably relax the strain and the dislocation density of the deposited film [4,5]. However, this technique involves serious bending and complicated handling of the free-standing thin films.

During the recent years various attempts were published to cover wafers with thin films where the latter behave as "compliant substrates" i. e. substrates being able to relax the strain of heteroepitaxial layers which then can grow free of threading dislocations up to a thickness far beyond the critical MB thickness. - One kind of this approach is to use commercial SOI film systems (Si/SiO_2 on Si) where the amorphous Si oxide might be able to relax plastically and to prevent misfit dislocation segments from threading the heteroepitaxial film grown on the Si film [3,6,7,8]. - In a similar approach, a defect-rich layer, created by implantation of hydrogen ions, instead of an amorphous layer has been used to reduce the threading misfit dislocation

density in SiGe heteroepitaxial films [9]. - A third approach, chiefly initiated by a group at Cornell university [10,11,12], is to use a thin single crystal film, twist-bonded to a support wafer, as a "compliant universal substrate". A thin film of GaAs is first grown on a release layer on a GaAs sacrificial wafer. Then, the sacrificial wafer is bonded to a wafer (of the same material) at a certain twist angle and the sacrificial wafer is removed by back-thinning or is lifted off. In the latter case, the "smart-cut" procedure [13,14,15] might be used as an economic way. Some experimental evidence was presented showing that this kind of substrates can be used to grow highly lattice-mismatched material (1-15 %) with a negligible density of threading dislocations up to a thickness far beyond the MB critical thickness.

In spite of initial success, the question remains about the lateral extension of defect-free regions that can be achieved in heteroepitaxial films grown on compliant substrates [16]. Since it is hard to believe a thin film will relax by slipping across macroscopic distances of a wafer area, an alternative way of thinking is an overall strain relaxation within the heteroepitaxial film which avoids threading dislocations [17,18].

To obtain more experimental insight, the present study was undertaken on producing twist-bonded layers of GaAs on GaAs as "compliant layer" (CL) which were then used for the heteroepitaxial deposition of III-V compounds at various degrees of mismatch. X-ray diffraction (XRD) as well as various microscopical techniques were used to study the microstructure of the interfaces and the epitaxial layers.

EXPERIMENTAL PROCEDURE AND RESULTS

Epitaxial films of 10 nm GaAs on an 100 nm AlAs release layer were deposited on 3 inch (100) GaAs wafers by metal organic vapor phase epitaxy (MOVPE). The wafers were directly bonded to commercially available 3 " GaAs wafers, with a twist angle ranging between 6° and 14°. Bonding was performed in H_2 atmosphere at 500 to 600 °C for several hours without applying external pressure. Using a modification of the epitaxial lift-off (ELO) technique [19] we removed the intermediate AlAs release layer by lateral etching in 10 % HF supported by ultrasonic agitation. Specimens up to several cm² in size were obtained.

Checking of the specimen surface by XRD clearly revealed the presence of the twist-bonded layer as shown in Fig. 1. This pole figure clearly exhibits the four {220} diffraction peaks of the twist-bonded layer rotated 14° with respect to the 4 corresponding strong peaks of the substrate. Furthermore, area scanned XRD was used to map the coverage of the handling wafer by the bonded thin layer. Covered areas up to 3...4 cm² were detected as shown in Fig. 2.

Details of the bonding interface were studied by transmission electron microscopy (TEM). Cross-sections prepared prior to the lift-off procedure clearly resolved the epitaxial layers as shown in Fig 3. No foreign layers were found at the bonding interface. However, microbubbles appeared with bright contrast and revealed typical Fresnel fringes on defocusing the microscope. The bubbles occurred along the bonding interface at densities around 10^{10} cm^{-2} and with sizes less then or comparable to the thickness of the twist-bonded layer, depending on the annealing conditions after bonding. Also, the microbubbles were occasionally found to be aligned within the bonding interface. Thus we believe the bubbles can nucleate at initial surface steps and may collect gas or vacancies during bonding and heating. Similar defects were also found at the bonding interfaces of GaAs/sapphire [20], GaAs/Si [21], and GaAs/InP [22]. Hence they appear to be quite a common feature associated with GaAs bonding. More important, the screw dislocation network as expected in case of a twist boundary could be observed in plan-view TEM specimens prepared after the lift-off etching. Fig. 4 shows dark horizontal and vertical lines parallel to the mean <110> directions and with a mean distance of

2 nm as expected from the twist angle of about 10°. Half this distance is typical of Moiré fringes which are also present with weaker contrast. The microbubbles appear as bright round features. They always interrupt the network of dislocations but Moiré fringes cross those bubbles that do not penetrate the twist-bonded layer.
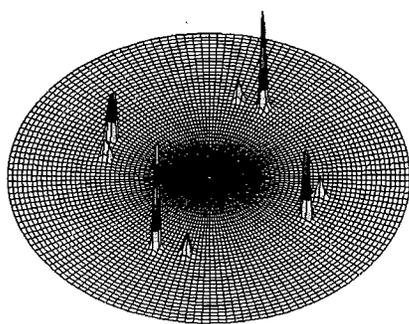
Fig. 1
XRD {220} pole figure of a twist-bonded (100) GaAs layer on an (100) GaAs substrate, the square-root of the intensity was plotted
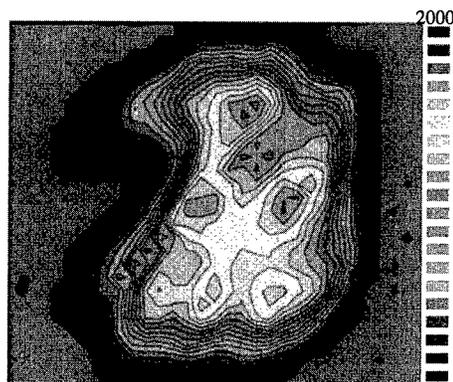
Fig. 2
Map of a 30 x 30 mm² specimen surface showing the XRD intensity of the {220} reflection of a twist-bonded GaAs layer
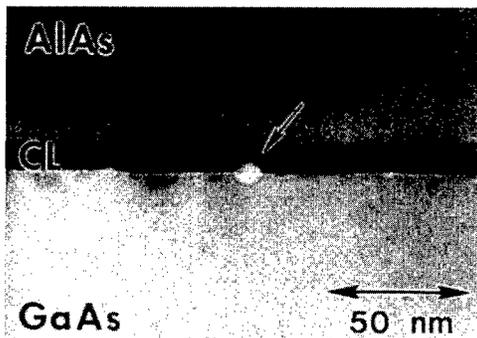
Fig. 3
TEM cross section of twist-bonded wafers. The bonding interface located between GaAs and CL contains microbubbles (arrow)
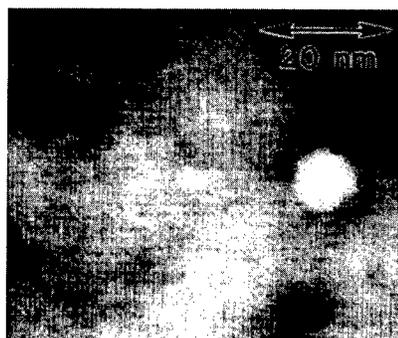
Fig. 4
TEM plan view of a twist-bonded thin (100) GaAs layer on an (100) GaAs substrate. The twist angle is close to 10°

To study possible mechanisms of strain relaxation in epitaxial films, MOVPE was used to deposit 300 nm InP (3.5 % misfit) or $In_xGa_{1-x}As$ (x = 0.28, 2 % misfit) on the thin GaAs layer at various twist angles of several degrees. A cross-sectional TEM bright-field image of the InGaAs film on the twist-bonded structure is shown in Fig. 5. Apparently the film is composed of dark and bright areas. They differ by crystallographic orientation according to the twist: Dark contrast appears in regions where the electron beam is along the [110] direction of the wafer or of the layers. On tilting the specimen according to the twist angle, the bright areas can be made dark (by aligning along [110]) while the dark ones become bright. This uniquely indicates the

47

existence of InGaAs grains which occur either twisted or untwisted with respect to the GaAs handling wafer. While the twisted parts grow on the twisted GaAs layer as expected, no such layer was found below the untwisted grains. This is evidenced by imaging of specimens as shown in Fig. 6 where the twisted layer CL and also some material of the GaAs substrate have disappeared on the right side. (The fringes visible in Fig. 6 are an artifact of scanning the photo). This removal of material occurred probably during the lift-off etching if a microbubble is present which can give rise to a pinhole. The InP film is always grown epitaxially on the twisted as well as on the untwisted area of the substrate. Thus a grain boundary, visible by dark and bright contrast in Fig. 6, is formed within the film. The site where the grain boundary merges the interfaces appears bright, indicating a preferential precipitation of voids or some amorphous material along this intersection line.

To check the degree of strain relaxation in terms of the tetragonal distortion of the InP film, XRD ($\Theta,2\Theta$) diagrams were recorded from the (226) and (622) reflections of the InP, including both the twisted and untwisted fraction of the film. As can be deduced from Fig. 7, both fractions reveal the same low degree of about 0.3 % residual tetragonal distortion. This means that the misfit strain is widely relaxed in both fractions of the film.

Discussing the mechanism of relaxation, it has to be pointed out that the epitaxial films were much thicker (up to 100 times) than the critical Matthews-Blakeslee-thickness [1] for introducing misfit dislocations. Hence misfit dislocations threading the film should occur very probably due to of the large extent of strain relaxation detected by XRD. However, TEM revealed almost no threading dislocations within the grains. It seems reasonable that the dislocations associated with plastic relaxation can easily accumulate at the grain boundaries of the film for two reasons: The slip distance - comparable to the grain size - is within a microscopic or mesoscopic scale, and the slip velocity [23] is in the order of several μm per second at the film deposition temperature near 600 °C. Hence the probability of blocking between intersecting dislocations [24] would be very low within one grain.
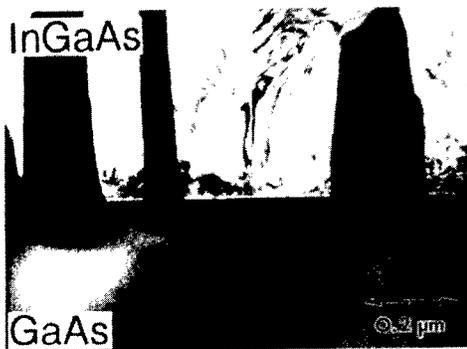
Fig. 5

Bright field cross-sectional TEM image showing a 2% mismatched InGaAs film grown on a twist-bonded GaAs layer containing pinholes
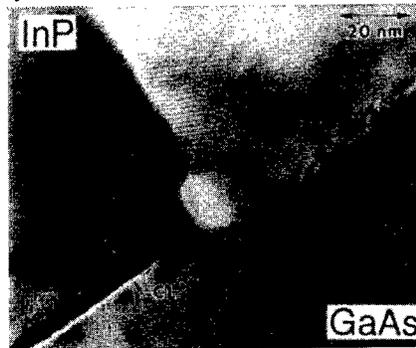
Fig. 6

TEM cross section of an InP film grown on a 10 nm thin GaAs twist-bonded layer (see left, CL) and locally grown directly on the handling wafer (see right)

A 2 % misfit InGaAs film was grown on a 10° twist-bonded substrate. Modulations on a lateral scale of few μm were observed by Nomarski interference contrast in an optical microscope. These modulations preferably occur along both the equivalent <110> directions of the film, resulting in the cross-hatched pattern. The example presented in Fig. 8 shows a similar

pattern also in an untwisted region, produced by scratching off a film stripe of about 10 μm width prior to deposition. Within this stripe, the pattern is rotated according to the twist angle. It seems quite probable that the modulations arise from piled-up threading dislocations. The cross-hatched pattern corresponds to the two-fold symmetry; the <110> type slip directions are perpendicular to each other. A reduced modulation can be noted along the vertical direction within the small untwisted region. Probably less pile-up occurs along this short distance perpendicular to the small stripe.
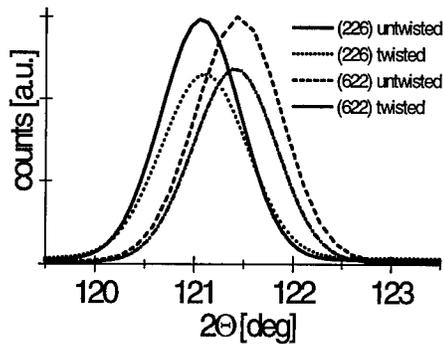
Fig. 7

XRD Θ-2Θ scans of an InP film epitaxially deposited on a twist-bonded layer containing pinholes
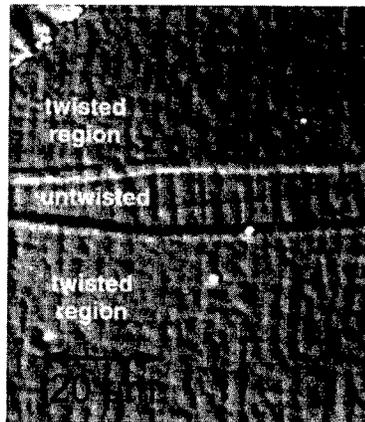
Fig. 8

Optical interference contrast micrograph showing a cross-hatched pattern along the <110> directions of both the twisted and an untwisted area of the epitaxial film

CONCLUSION

In conclusion, we observed that defects (precipitates/voids) at the GaAs bonding interface can lead to pinholes in the GaAs twist-bonded layer. Due to these pinholes, heteroepitaxial films can grow not solely twist-oriented but also untwisted directly on the GaAs handling wafer. As a consequence, twisted and untwisted regions separated by tilt grain boundaries are formed. These boundaries would be able to collect threading segments of misfit dislocations which slip during plastic relaxation of misfit strains. As a net result, the density of threading dislocations is lowered in the areas close to the boundaries.

ACKNOWLEDGMENT

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HETEROEPITAXY OF GaAs ON CaF$_2$/Si(111) BY SURFACE FREE ENERGY MODULATION METHOD

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ABSTRACT

An epitaxial GaAs layer was grown on a CaF$_2$(111) by means of surface free energy modulation of CaF$_2$ by one-monolayer-height island formation. An additional low-temperature growth at a final stage of growth of the CaF$_2$ layer on Si(111) produced high density islands whose height was one monolayer of CaF$_2$. This surface structure contributed to enhance wettability of overgrown GaAs. Two-step growth sequence was also examined in order to grow GaAs layer on the modified CaF$_2$/Si(111) with good crystallinity. The electron mobility of 2,000 cm^2/Vs in a Si doped GaAs layer (6×10^{17} cm^{-3}) was obtained by the combination of the surface energy modulation method and the two-step growth method.

INTRODUCTION

Heteroepitaxy of III-V semiconductors on crystalline insulator materials such as alkaline earth fluorides (CaF$_2$, SrF$_2$, BaF$_2$ and their compound) is attractive for future high performance devices. Heterostructures such as GaAs/fluoride/GaAs [1-3], InP/fluoride/InP [4] and GaAs/fluoride/Si [5-11] have been investigated. In these dissimilar material systems, it is well-known that growth of III-V semiconductor on CaF$_2$ is difficult because of a surface free energy disadvantage, that is, the surface free energy of CaF$_2$ is lower than that of the semiconductor layers. In order to solve this problem, several techniques have been investigated, e.g., use of an As$_2$ molecular beam for GaAs growth [6], insertion of a ZnSe ionicity-controlling layer [10] and surface modification by electron beam exposure [7-9,11]; however, the quality of these GaAs layers have not yet been good. We previously proposed a new approach to improve the wettability of GaAs on the CaF$_2$ surface where one monolayer height islands with high packing density were intentionally formed on the CaF$_2$ surface in order to increase its surface free energy [12]. In this work, the effects of this method to obtain the modified CaF$_2$ surface and two-step growth sequence for the overgrown GaAs layer are examined through observations of surface morphologies and electron mobilities of a GaAs layers grown on CaF$_2$/Si(111).

IDEA OF SURFACE FREE ENERGY MODULATION

The surface free energy of CaF$_2$(111) is extremely low, since F ions terminate the topmost surface sites. The free energy of the surface including the surface steps, γ, is given by

$$\gamma = \gamma_{ideal}(1 + Ld) + L\gamma_{step}, \tag{1}$$

where γ_{ideal} and γ_{step} are surface free energy of ideal surface without defects per unit area and step free energy per unit length, respectively. L is total length of the steps per unit area and d

51

is height of a step. In practice, Ld is much smaller than unity $(1 \gg Ld)$. We can expect two-dimensional growth of GaAs on the CaF_2 surface if γ of CaF_2 is increased by large L. The surface morphology of CaF_2 grown at low temperature or with a high flux molecular beam shows pyramidal (three-dimensional) islands with large L [13]; however, crystalline quality was poorer than that obtained by step flow growth mode [14]. Excessively rough surface is also considered to be undesirable for succeeding epitaxy on it. Islands with monolayer (ML:3.15 A) height are enough to enlarge $L\gamma_{step}$ if size of the islands is small enough to attain large L. So, we used kinetic roughening phenomena to increase surface free energy of CaF_2 with large L. It should be obtained when a few ML of CaF_2 were grown at low temperature on the CaF_2 grown on Si(111) substrate at high temperature.

EXPERIMENT

All of growth were carried out in a three-chamber MBE system in which a fluoride growth chamber was connected to a load lock chamber and a GaAs growth chamber. Base pressures of the fluoride growth chamber and the GaAs chamber were less than 1×10^{-8} torr and 1×10^{-9} torr, respectively. After a Si(111) substrate on-axis $\pm0.5°$ was cleaned by conventional chemical process finished with immersing into diluted HF solution, it was thermally cleaned at 870°C till a clear 7×7 superstructure in diffraction pattern was observed. Then 20-nm-thick CaF_2 was grown epitaxially on the substrate at 770°C and the surface was followed by 2 ML of CaF_2 at 150°C in order to obtain one-ML-height islands on the surface. Then, the 10-nm-thick GaAs was grown on the CaF_2 surface at 200–400°C and it was followed by 1.2-μm-thick GaAs at 600°C after in-situ annealing of the initial GaAs layer at 500–600°C for 30 min. Growth rate of CaF_2 and GaAs were 6 nm/min and 17 nm/min, respectively. Pressure of As_4 during the growth was estimated to be of the order of 1×10^{-5} torr. The surface morphologies of the samples were investigated by a NanoScope IIIa atomic force microscope (AFM). Electrical properties of the samples were evaluated by means of van der Pauw method for 1.2-μm-thick GaAs of which the surface layer of 500 nm was Si-doped.

RESULTS

Figure 1(a) shows an AFM image of the CaF_2 surface just after the growth at 770°C. Terraces and steps of which height was estimated to be 1 ML were observed. This morphology indicates that the CaF_2 layer was grown in step flow growth mode. In contrast, the surface was drastically changed as shown in Fig. 1(b) by a process of the surface free energy modulation, namely, 2-ML-thick CaF_2 growth at low temperature on the CaF_2 surface shown in Fig. 1(a). Multi-stacking of many triangular islands, of which each side length was 10–30 nm and height was 1 ML, were observed on the terraces. Phases of islands were coherent without a twin phase. We can find that 4 step-lines and 80 triangular islands of which average side length is 20 nm in the area of 250×250 nm². Thus, L increased 6 times as large as that on the original surface grown at high temperature, while the total surface area increased only 3% which corresponded to Ld.

The surface morphology and its cross-sectional profile of a 10-nm-thick GaAs layer grown at 200°C on the modified CaF_2 surface and annealed at 575°C for 30 min are shown in Fig. 2(a) and 2(c). For comparison, those on the CaF_2 surface without the modification as shown in Fig. 1(a) are shown in Fig. 2(b) and 2(d). It is found that GaAs wets well on the modified CaF_2 surface. It can be considered that mass transport of GaAs to minimize free
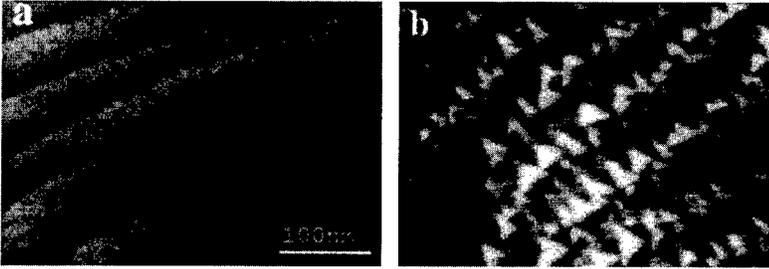
Figure 1: AFM images of 20-nm-thick CaF_2/Si(111). (a) An as-grown surface at 770°C. (b) A surface modified by 2 ML growth at 150°C on the surface shown in Fig. 1(a).

energy of the system during the annealing led to smoothing out the island surface structure in the case of Fig. 2(a) and to islands formation along the step edges of the CaF_2 surface in the case of Fig. 2(b). This result indicates that the CaF_2 surface modified by the island structure has higher surface free energy than that of original plane surface.

There exists a lattice mismatch of approximately 4% between GaAs and CaF_2. It can be considered that two-step growth method as shown in Fig. 3 is effective for solving this problem as well as in the case of other material systems [15]. Figure 4(a)–(d) show surface morphologies of 1.2 μm-thick GaAs layers grown on the modified CaF_2 layers obtained by the growth sequences shown in Fig. 3(a)–(d), respectively. Figure 4(a) and 4(b) show the dependence of the morphology on the initial growth temperature. Other condition such as thickness, annealing and second growth temperature were the same in both samples
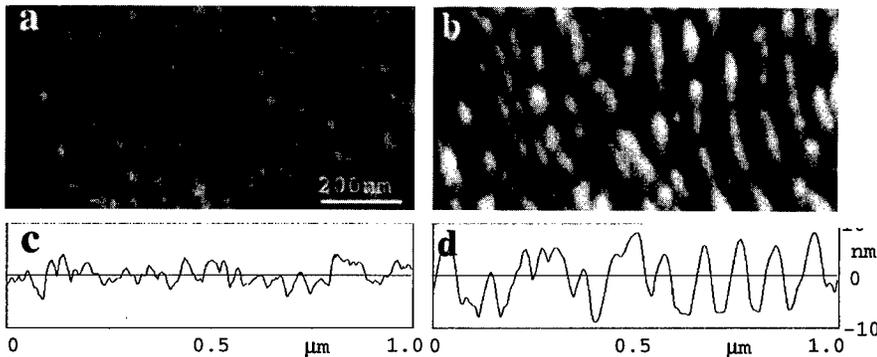
Figure 2: AFM images of surface and cross-sectional profiles of thin GaAs on CaF_2/Si after annealing. (a), (c) GaAs on the modified CaF_2 as shown in Fig. 1(b). (b), (d) GaAs on as-grown CaF_2 as shown in Fig. 1(a).
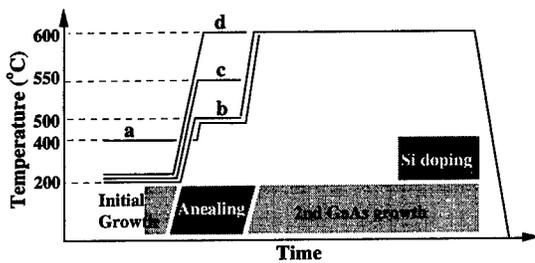
Figure 3: Two-step growth sequence for 1.2 μm-thick GaAs on modified CaF₂/Si(111).

as shown in Fig. 3. It is found that surface morphology of GaAs layer of which initial growth temperature was 200°C is rather good as shown Fig. 4(b), which is similar to that of homoepitaxial growth. On the other hand, the surface morphology with initial temperature
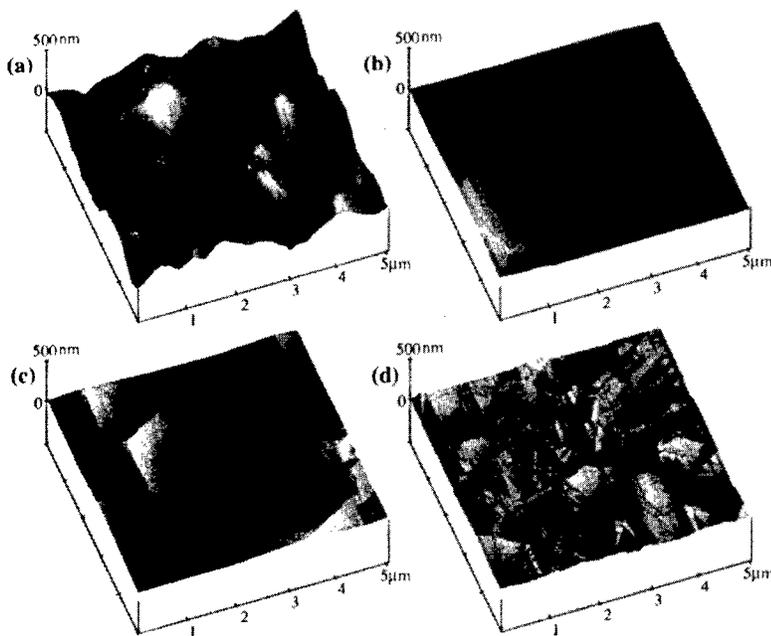
Figure 4: Surface morphologies of 1.2 μm-thick GaAs on modified CaF₂/Si(111). GaAs layers shown in Fig. 4(a)–(d) were obtained by the growth sequences shown in Fig. 3(a)–(d), respectively.

54

of 400°C is worse and the surface roughness is obviously large as shown in Fig. 4(a). The higher temperature just before the growth might smooth out the small structures and causes a reduction of L since the small islands are energetically unstable. So, low initial growth temperature, e.g., 200°C will be good condition.

Figure 4(b), 4(c) and 4(d) show the dependence of the morphology on the annealing temperatures for the initial growth layer. The temperatures were 500°C, 550°C and 600°C, respectively. The morphologies with annealing at 500°C and 550°C show a three-folded rotational symmetry shape and no twin phase and no pits on the surface. However, the surface of GaAs with annealing at 600°C shows rough morphology, and some twin phases were observed there. This might be a result that the islanding of the GaAs initial layer occurred by surface diffusion of Ga atoms during the high temperature annealing. Thus, the annealing temperature must be less than 600°C.

Figure 5 shows the dependence of electron mobility in the n-GaAs layer on annealing temperature of the 10-nm-thick initial layer grown at 200°C. The symbols of 'o', '$\triangle$' and '$\square$' are corresponding to the annealing at 500°C, 550°C and 575°C, respectively. The 1.2-μm-thick second layers were grown at 600°C for all sample. The symbol of '×' denotes the mobility obtained by homoepitaxial growth on the GaAs(100) substrate. It is found that the mobility is increased by raising the annealing temperature from 500°C to 550°C, and GaAs layer with 575°C annealing is better than that at 550°C considering the difference in their carrier concentrations. It can be said that quality of the initial layer is important to obtain high quality GaAs layer.

The value of 2,000 cm^2/Vs is comparable to the highest value reported so far in which the electron surface modification method was employed [9]. This island formation technique is much simpler than other surface modification technique and applicable to many kind of materials. Thus, this technique is very promising.
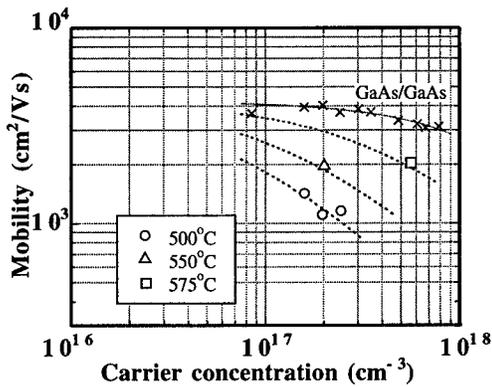
Figure 5: The dependence of the electron mobility in the n-GaAs layer on annealing temperature of the initial growth layer.

CONCLUSIONS

The surface modification of CaF_2 by surface free energy modulation using one-ML-height island formation was examined in order to improve the wettability of GaAs on CaF_2. The improvement of the wettability due to increase of surface free energy of CaF_2 was shown by means of annealing of the thin GaAs layer grown on the CaF_2 surface. The two-step method was introduced to GaAs growth on the modified CaF_2 surface and the importance of the quality of the initial GaAs layer was shown. An epitaxial GaAs layer with electron mobility of $2,000\,cm^2/Vs$ was obtained on the modified $CaF_2/Si(111)$ substrate when a second GaAs layer was grown at 600°C after that a 10-nm-thick initial layer was grown at 200°C and was annealed at 575°C for 30 min. The obtained value of mobility is comparable to the best value obtained for GaAs on CaF_2/Si using complicated surface modification process. Thus, this method new and simple is very promising to solve a problem of a surface free energy disadvantage.

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Part II

Electronic Defects and Transitions
in Mismatched Heterostructures

DEEP LEVEL DEFECT STUDIES IN MOCVD-GROWN $In_xGa_{1-x}As_{1-y}N_y$ FILMS LATTICE-MATCHED TO GaAs

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ABSTRACT

Deep level defects in MOCVD-grown, unintentionally doped p-type InGaAsN films lattice matched to GaAs were investigated using deep level transient spectroscopy (DLTS) measurements. As-grown p-InGaAsN showed broad DLTS spectra suggesting that there exists a broad distribution of defect states within the band-gap. Moreover, the trap densities exceeded 10^{15} cm^{-3}. Cross sectional transmission electron microscopy (TEM) measurements showed no evidence for threading dislocations within the TEM resolution limit of 10^7 cm^{-2}. A set of samples was annealed after growth for 1800 seconds at 650 °C to investigate the thermal stability of the traps. The DLTS spectra of the annealed samples simplified considerably, revealing three distinct hole trap levels with energy levels of 0.10 eV, 0.23 eV, and 0.48 eV above the valence band edge with trap concentrations of 3.5×10^{14} cm^{-3}, 3.8×10^{14} cm^{-3}, and 8.2×10^{14} cm^{-3}, respectively. Comparison of as-grown and annealed DLTS spectra showed that post-growth annealing effectively reduced the total trap concentration by an order of magnitude across the bandgap. However, the concentration of a trap with an energy level of 0.48 eV was not affected by annealing indicating a higher thermal stability for this trap as compared with the overall distribution of shallow and deep traps.

INTRODUCTION

Recently, the quaternary alloy semiconductor InGaAsN has drawn significant attention because of its potential applicability to infrared laser diodes and its possible use as a narrow band-gap layer in tandem solar cells. Long wavelength laser diodes are used as light sources for optical fiber communications because of their emission at the low-loss optical fiber windows of 1.3 and 1.55 μm [1]. Conventionally, GaInPAs/InP based laser diodes have been used for such applications. GaInPAs/InP laser diodes, however, show poor temperature characteristics due to the small conduction band offset of this material system [2]. Kondow *et al.* have instead proposed using the quaternary alloy InGaAsN grown on GaAs substrates for long-wavelength laser diodes [3]. They have demonstrated that InGaAsN/GaAs laser diodes display superior high temperature characteristics due to the type-I hetero-interfaces formed between InGaAsN and GaAs. Several research groups have concentrated on improving growth techniques to achieve better quality InGaAsN materials [3,4,5,6,7,8,9,10,11]. Recently, a 1.0 eV band-gap solar cell made of InGaAsN with an internal quantum efficiency greater than 70% has been reported [11]. However, because of the difficulty in growing N-containing quaternary materials, these materials may contain defects that impact their electrical quality. In this study, we report on deep level defects revealed by deep level transient spectroscopy (DLTS) in unintentionally doped p-type InGaAsN films grown on GaAs substrates. In addition, we investigate the thermal stability of deep traps by examining DLTS spectra before and after an anneal.

Figure 1. The device structure that was used for DLTS measurements. Hall measurements showed that the unintentionally doped InGaAsN layer is p-type [11].

EXPERIMENT

The samples used in this study were grown by MOCVD. Details regarding the growth can be found elsewhere [11]. The device structure used for DLTS measurements is shown in Figure 1. The indium content was 7.0 % and the nitrogen content was 2.2 % for the $In_xGa_{1-x}As_{1-y}N_y$ layers. Au-Be alloy ohmic contacts were evaporated on the p-GaAs substrate and Au-Ge-Ni alloy ohmic contacts were evaporated on the top n-GaAs layer. After the evaporation the diodes were mesa-etched around the contacts. The diode area defined by the mesa was 1.11 mm². Good rectifying current-voltage (I-V) characteristics were observed for the diodes. Annealed samples were prepared by annealing the devices at 650 °C for 1800 seconds under the presence of nitrogen gas. The details concerning annealing also can be found elsewhere [11].

DLTS was used to detect deep level defects. The trap concentrations were calculated from the well-known formula:

$$N_T = \frac{2N_A \Delta C}{C_0} \frac{r^{r/(r-1)}}{1-r}, \tag{1}$$

where N_A is the doping density, ΔC is the capacitance change between DLTS sampling times, C_0 is the steady state capacitance value under the applied reverse bias, and $r=t_2/t_1$, where t_1 and t_2 are the initial and final DLTS sampling times, respectively. The p-type background doping concentration was measured from capacitance-voltage (C-V) profiling and had a value of 3.5×10^{16} cm^{-3} for the unintentionally doped layer of the as-grown samples and 1.1×10^{17} cm^{-3} for the annealed samples. Hall measurements were carried out to verify the doping type of the InGaAsN layer and showed that the material is p-type [11]. The increase of doping concentration in p-InGaAsN after annealing has been observed, the source of which is under investigation [12]. Steady state capacitance measurements as a function of temperature were performed to obtain $C_0(T)$. The steady state C-T measurements were done under the same reverse bias condition (-0.8 V) as were the DLTS measurements.

RESULTS

Figure 2 shows DLTS spectra of the as-grown p-InGaAsN for the different rate windows used. There are two interesting features to be pointed out in these spectra. The first is that the peaks are very broad and the second is that the trap density depends on the rate window. The above results strongly suggest that the energy distributions of the defect levels are not well defined at a single energy but are instead band-like. Band-like defect states typically appear in material with extended defects such as threading dislocations [13]. Figure 3 shows a typical cross sectional TEM of p-InGaAsN. The TEM image shows no sign of dislocations within the
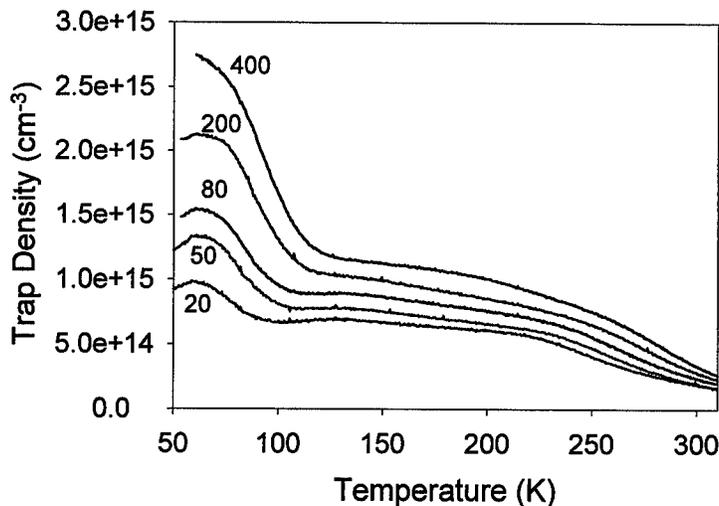
Figure 2. DLTS spectra of as-grown p-InGaAsN. The quiescent bias and fill pulse voltages were –0.8 V and –0.15 V, respectively. The fill pulse width was 1 msec. Numbers shown in the figure indicate rate windows in the unit of sec^{-1}.

TEM resolution limit of 10^7 cm^{-2} demonstrating the good structural quality and lattice-matching of these thick layers. Hence, a more likely source is a high density of distributed point defects and/or point defect clusters. More intensive study of the physical nature of the defect sources, including the dependence of trap density on fill pulse width, is currently underway.

Figure 3. Cross sectional TEM of an as-grown p-InGaAsN showing no sign of dislocations within the resolution limit of 10^7 cm^{-2}.

Figure 4 shows DLTS spectra of the annealed sample for the different rate windows used. Unlike the spectra for the as-grown sample, the peaks are narrow enough to be easily resolved. Figure 5 shows Arrhenius plots from which the activation energies of the traps were calculated. To find the peak positions and the densities of each trap, we fit the N_T vs. T curves using Gaussian functions. Three majority carrier (hole) traps were found with energy levels of 0.10 eV, 0.23 eV, and 0.48 eV above the valence band edge. The concentrations of these traps were found to be 3.5×10^{14} cm^{-3}, 3.8×10^{14} cm^{-3}, and 8.2×10^{14} cm^{-3}, respectively. Comparison of the DLTS spectra of the as-grown and the annealed samples for a fixed rate window shows that
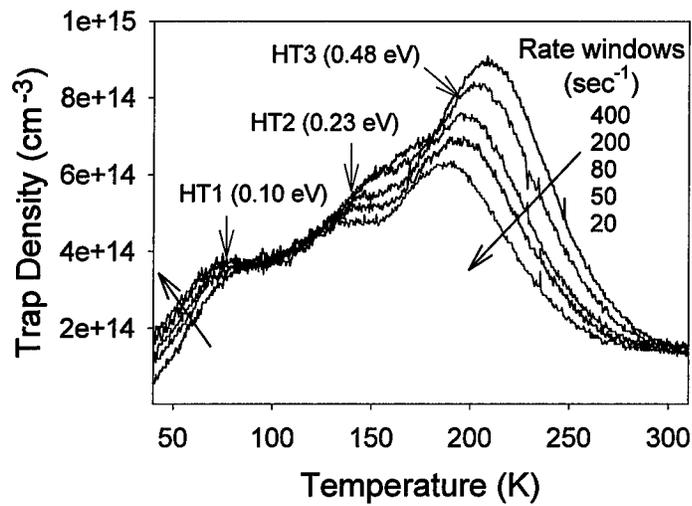
Figure 4. DLTS spectra of annealed p-InGaAsN. The quiescent bias and fill pulse voltages were –0.8 V and 0.0 V, respectively. The fill pulse width was 1 msec. Unlike the DLTS spectra for as-grown p-InGaAsN samples, peaks are narrow and resolvable.
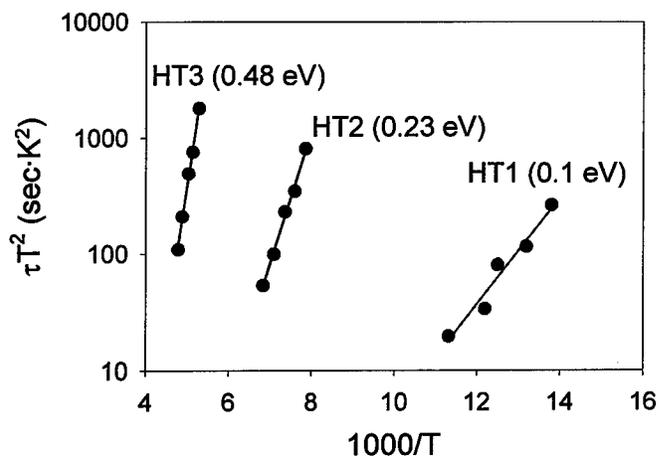
Figure 5. Ln(τT^2) versus 1000/T plots for annealed p-InGaAsN. The energy values in the parentheses are measured from the valence band edge since these are hole traps.

the broad deep level distribution throughout the bandgap is reduced due to the post-growth annealing. In particular, the densities of the shallower traps (those with energy levels of 0.10 eV and 0.23 eV) are significantly reduced, and their thermal annealing behavior suggests that thay are likely to be related to point defects within the InGaAsN. Correlating with this reduction in the trap density, InGaAsN was observed to have improved bulk properties, with large increases in photoluminesence and quantum efficiency following the anneal [11]. This indicates that the as-grown deep levels severely degrade carrier diffusion lengths in p-InGaAsN. However, close inspection of Figures 2 and 4 reveal that the concentration of the hole trap of Ev + 0.48 eV is not affected by the anneal, indicating a greater thermal stability for this defect as compared to the several distribution of shallow and deep traps. Moreover, this trap has been detected in p-InGaAsN grown under a wide range of MOCVD growth conditions, implying its source may be of a different nature than the thermally unstable deep levels. Since this trap is the dominant level after annealing, and since it is near midgap, it is likely to be important in limiting minority carriers lifetimes of the annealed p-InGaAsN, and perhaps subsequent device performance.

CONCLUSIONS

DLTS measurements were performed on unintentionally doped p-type InGaAsN films grown on GaAs. Broad DLTS spectra measured in as-grown p-InGaAsN suggest that there exists a distribution of deep defect states throughout the band-gap of the as-grown p-InGaAsN material. Moreover, the densities of the traps in the as-grown samples exceed 10^{15} cm^{-3}. Cross sectional TEM measurements indicate that, within the TEM resolution limit of 10^7 cm^{-2}, the traps are not likely to be due to threading dislocations. DLTS revealed three distinct hole traps in annealed samples. The energy levels of these traps are 0.10 eV, 0.23 eV, and 0.48 eV above the valence band edge and the concentrations are 3.5×10^{14} cm^{-3}, 3.8×10^{14} cm^{-3}, and 8.2×10^{14} cm^{-3}, respectively. The concentrations of the two distinct shallower traps at 0.10 eV and 0.23 eV and the overall trap distribution were reduced considerably following the anneal, indicating that these traps are not thermally stable. In contrast, the concentration of a deep trap at 0.48 eV is unaffected by the anneal. The overall reduction in trap density is correlated with improved photoluminescence and quantum efficiency. However, since the 0.48 eV hole trap is both a midgap level and the dominant remaining trap after annealing, it is likely to be an important defect for limiting minority carrier properties in this material.

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UNIQUE DEFECT-INDUCED DONOR STRUCTURE AT THE LATTICE MISMATCHED InAs/GaP HETEROINTERFACE

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ABSTRACT

We have investigated the direct growth of narrow-gap InAs on wide-gap GaP by Molecular Beam Epitaxy. InAs and GaP have the largest mismatch among all the III-arsenides and the III-phosphides – 11%. A perfect epitaxial relationship is maintained between the InAs and the GaP despite the large lattice mismatch. Moreover, a reproducible defect structure with unique electronic properties is developed at the heterointerface. A point defect associated with the intersection of 90° misfit dislocations may act as an ordered, structural dopant. This dopant is fully ionized with a constant, high sheet carrier density of 10^{13} cm^{-2}, independent of InAs layer thickness, and exhibits no freeze out even at 5 K. Device applications for such a system include temperature insensitive Hall sensors. We have also demonstrated high electron mobilities (over 10000 cm^2/V-sec) in nominally undoped thick InAs layers grown on GaP. The explanation of this effect is presented to emphasize the exciting possibilities of band gap engineering in this system.

INTRODUCTION

InAs is a narrow band gap semiconductor whose high theoretical electron mobility (33000 cm^2/V-sec) makes it an attractive candidate for high speed device applications. The lack of a suitable lattice matched substrate has hampered the development of InAs based devices. Traditionally, the use of lattice mismatched substrates has been avoided since dislocations and other defects have an adverse impact on device performance [1]. However, the electronic properties of dislocations in InAs have not been thoroughly investigated.

In the present study, we have grown InAs layers on (001) GaP substrates by Molecular Beam Epitaxy (MBE). This system possesses both a high mismatch in lattice parameter (a_{InAs}: 6.06 Å, a_{GaP}: 5.45 Å) and a large difference in band gap (InAs: 0.36 eV, GaP: 2.25 eV). The strain due to lattice mismatch is relaxed by the generation of misfit dislocations at the heterointerface. Hence, both the interfacial defect microstructure and the large band offsets are expected to contribute to the electronic behavior of the heterojunction.

EXPERIMENT

InAs/GaP heterostructures were grown by Solid Source Molecular Beam Epitaxy (SSMBE) using a Varian Gen-II MBE system. The details of the crystal growth have been described elsewhere [2,3]. Samples with (nominally undoped) InAs layers ranging from 3 nm to 2 μm were grown and capped with a 5 nm layer of $Al_{0.2}In_{0.8}As$ to suppress carrier generation due to surface states. Figure 1 is a schematic of the multilayer structure grown by MBE.

In₀.₈Al₀.₂As Cap - undoped		5 nm

In$_{0.8}$Al$_{0.2}$As Cap - undoped	↕ 5 nm
Relaxed InAs - undoped	↕ 3 nm - 2μm
GaP Buffer - undoped	↕ 200 nm
GaP/AlGaP Superlattice (20 period)	
n-GaP Substrate	
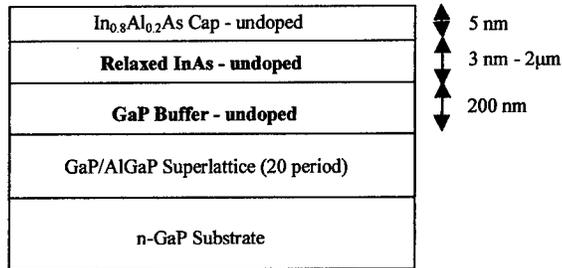
Figure 1: Schematic of the multilayer structure grown by MBE.

Cross-sectional Transmission Electron Microscopy (TEM) studies were performed using a JEOL 2000 FX microscope with an accelarating voltage of 200 kV. The large misfit strain is accommodated by the generation 2-D network of interfacial misfit dislocations, which are expected to be of 90°, pure edge character with in-plane Burgers vectors of ½ [110] and ½ [$\bar{1}$10] [4]. High Resolution TEM (HREM) images confirm the existence of such an interface microstructure. Figure 2 is a HREM image showing a number of approximately equally spaced dislocations at the heterointerface. The dislocations appear as bright spots due to their strain contrast. The atomic positions in the core of the misfit dislocations are resolved in Figure 2. A careful construction of the Burgers circuit around several misfit dislocations revealed them to mostly be of 90°, edge dislocations.
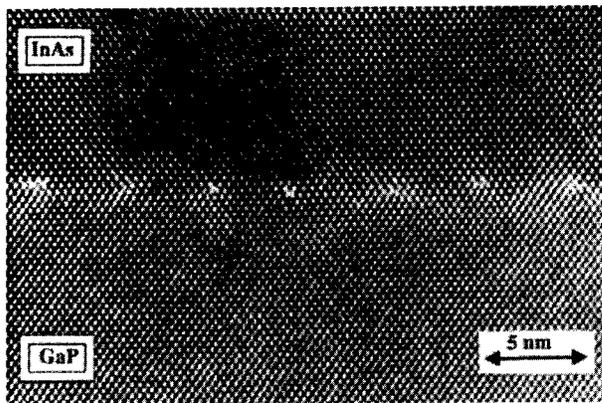
Figure 2: HREM micrograph of InAs/GaP hetrostructure.

No definite identification of isolated 60° mixed dislocations has been made in this system. However, in a few instances (less than 5% of the dislocations examined), a narrowly dissociated pair of 60° misfit dislocations was observed. A Burgers circuit taken around the pair yields a closure gap of ½[110]. A dislocation reaction of the type:

$$\frac{1}{2}[01\bar{1}] \text{ on } (\bar{1}11) + \frac{1}{2}[101] \text{ on } (1\bar{1}1) = \frac{1}{2}[\bar{1}10] \text{ on } (001) \tag{1}$$
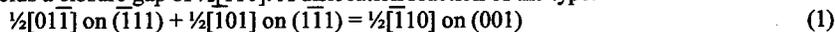
could result in these two dislocations forming a sessile 90° dislocation [4]. The HREM images also show that the InAs layer maintains an epitaxial relationship with the GaP substrate despite

the very high lattice mismatch. The misfit appears to be entirely accommodated by the dislocations and the regions of the interface between the dislocations are free of distortions.

Plan view TEM was carried out on a JEOL 200 CX microscope. Both 200 and 220 weak beam dark field images were employed to enhance the strain contrast of dislocations in the epilayer. Given the high density of misfit dislocations at the interface, a high threading dislocation density is expected in the InAs layer. Figure 3 is a 220 dark field image of a 0.5 μm InAs epilayer. The threading dislocation density is estimated to be $\sim 10^{10}$ cm^{-2}.
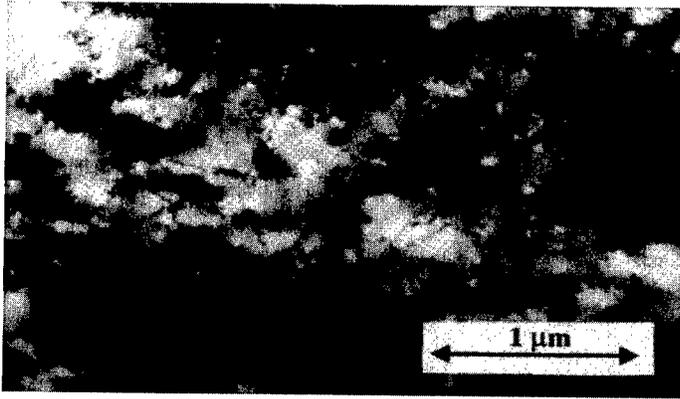
Figure 3: Plan view TEM micrograph showing threading dislocations in the InAs epilayer

Systematic Hall effect measurements were performed at both 300 K and 77 K on undoped InAs/GaP heterostructures using a van der Pauw geometry, and a few specimens were also examined at 5 K. The majority carrier type, concentration and mobility were extracted from the data in the standard manner. For all the samples measured, the majority carriers were n-type (electrons). The sheet carrier concentration is obtained from the carrier concentration by:

$$N_s \text{ (cm}^{-2}) = N \text{ (cm}^{-3}) * t \text{ (cm)} \tag{2}$$

Table I displays the sheet carrier concentration (N_s) and the Hall mobility (μ) for all the samples tested at both room temperature (300 K) and at 77 K [3,5].

Sample #	InAs layer thickness (nm)	300 K		77K	
		Sheet density (cm^{-2})	Hall mobility (cm^2/V-sec)	Sheet density (cm^{-2})	Hall mobility (cm^2/V-sec)
1	5	1.2×10^{13}	40	1.2×10^{13}	25
2	10	1.1×10^{13}	500	1.0×10^{13}	360
3	15	0.75×10^{13}	340	0.75×10^{13}	310
4	20	0.8×10^{13}	460	0.8×10^{13}	430
5	30	1.0×10^{13}	800	0.9×10^{13}	730
6	250	1.0×10^{13}	4000	1.0×10^{13}	3780
7	500	1.2×10^{13}	5310	1.1×10^{13}	5390
8	1000	1.5×10^{13}	7620	1.3×10^{13}	8120
9	2000	2.0×10^{13}	9920	1.6×10^{13}	10900

Table I: Sheet carrier density and mobility data for InAs epilayers of varying thicknesses.

Carrier concentration depth profiling was carried out using an electrochemical capacitance voltage (ECV) profiler. Figure 4 is a semilog plot of the carrier concentration vs. depth for an ~ 1 µm InAs layer grown on GaP. Carriers accumulate on the low band gap side (InAs) and are depleted on the high band gap side (GaP) of the heterojunction.
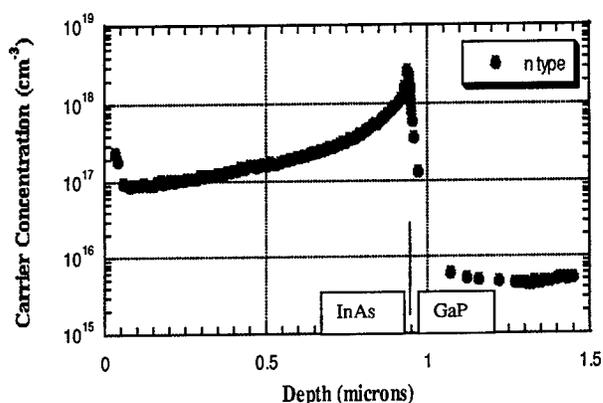
Figure 4: Electrochemical Capacitance Voltage profile of undoped InAs grown on GaP.

RESULTS AND DISCUSSION

The results presented above suggest that the electrical behavior of the InAs/GaP heterointerface is strongly influenced by the misfit dislocation microstructure. Several trends emerge from the data of Table I. Samples 1 through 5 (ranging from 3 nm to 30 nm in the InAs layer thickness) can be classified as the "thin layer" samples and samples 6 through 9 as the "thick layer" samples.

The sheet carrier concentration for the thin layer samples is very high (~ 10^{13} cm^{-2}) and does not vary with epilayer thickness. There is also no freeze out at 77 K. This implies a high density of electrons localized either at the InAs/GaP interface or at the free surface. Since the surface is capped with a layer of $Al_{0.2}In_{0.8}As$, carrier generation due to surface states can be ruled out. In addition, the ECV profile of Figure 4 shows carrier accumulation at the heterointerface. Thus, the Hall effect experiments measure carriers due to interface states. The lack of freeze out at 77 K indicates that these states may be above the conduction band edge. The possible sources of these carriers are:

1) Atomic sites along 90° misfit dislocations: There are a total of 10^{14} sites along 90° misfit dislocation lines per cm^2, but the measured sheet carrier concentration, N_s, is an order of magnitude lower. Since the energy states responsible for these carriers does not display freeze out, it is unlikely that a fractional ionization event occurs. The common 7–5 ring core structure of a 90° dislocation is shown in Figure 5(a).

2) Atomic sites along 60° misfit dislocations: A small fraction (< 5%), of pairs of 60° misfit dislocations have been observed. However, the sites along these dislocations would not be sufficient in number to account for 10^{13} carriers per cm^2.

3) Threading dislocations: While threading dislocations may be electrically active, they are not sufficiently dense ($\sim 10^{10}$ cm^{-2}) to account for the carriers in thin layer samples. Additionally, threading dislocation contribution would result in a thickness dependence of N_s, which is not observed.

4) Intrinsic band bending: InAs and GaP have large conduction and valence band offsets. However, calculations carried out using the band structure simulator ADEPT show that the intrinsic band bending would result in the Fermi level being pinned mid gap in the InAs at the interface and, consequently, low carrier accumulation. A high density (10^{13} cm^{-2}) sheet of electronic charge at the interface requires the Fermi level to be pinned 0.2 eV above the conduction band edge of InAs at the interface [3].

5) 90º misfit dislocation intersection sites: Mostoller et al. [6] proposed that an extended defect of the "driedl" configuration should occur at the intersection of ½<110> 90º misfit dislocations at the Ge/Si interface. A similar defect structure could exist at the InAs/(001) GaP interface, forming a square lattice with a periodicity of $\sim$ 4 nm. These would appear with a density of $\sim 10^{13}$ cm^{-2}, a numeric match with the N_s values of Table I. Thus, the misfit dislocation intersection sites may act as an array of ordered structural dopants. The driedl structure is shown in Figure 5(b). This structure in III-V compounds would contain a strong internal dipole, which may be the carrier generation source.

The carriers generated at the interface are confined to a two dimensional electron gas (2DEG) near the interface. They are strongly scattered by the dislocation network, which results in low mobility values. As the temperature is decreased, the confinement would be stronger, i.e., the mobility could even decrease with decreasing temperature, which is consistent with our observations.
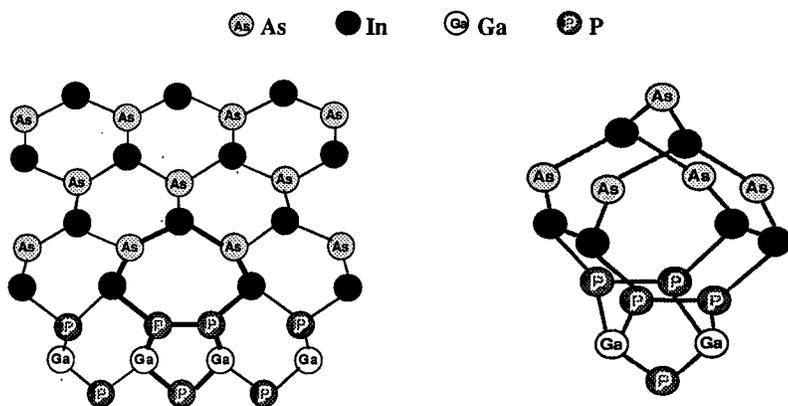
Figure 5(a): 7-5 ring structure of a 90º misfit dislocation.   Figure 5(b): The 18 atom driedl.

For the thick layer samples (#6 through #9), the sheet carrier concentration increases with thickness. N_s is plotted vs. thickness in Figure 6. The N_s-t plot is linear with a zero thickness intercept of 9.0×10^{12} cm^{-2}. This is indicative of a further carrier contribution, from the bulk (InAs epilayer). The comparative flatness at 77 K indicates that the bulk carriers are subject to some freeze out. The most likely source of these carriers is the states associated with

threading dislocations in the epilayer. The electrical activity of threading dislocations merits further investigation.

To account for transport properties of the thin and thick layer samples, Chen [5] proposed a dual channel model. Two parallel pathways of lateral carrier transport exist in the InAs epilayer: 1) a high carrier density, low mobility 2DEG confined near the interface, and 2) a high mobility, lower carrier density bulk channel. At lower thickness, the interfacial channel dominates, N_s is constant and the mobility is low. As thickness is increased, the bulk channel becomes dominant, as shown by the dramatic increase in mobility for the thick InAs samples. Using this model, the mobility for the bulk layer has been found to be over 20000 cm^2/V-sec in some thicker samples [5].

This implies that the carriers in the bulk channel are not strongly scattered by the highly dense (10^{10} cm^{-2}) network of threading dislocations in the InAs epilayer. This suggests that high defect densities can be tolerated in InAs, and that this heterostructure system has promise for some high speed device applications.

CONCLUSIONS

We have demonstrated the existence of a high density sheet of electron charge at the InAs/GaP heterojunction. This effect was linked with a periodic network of misfit dislocations occurring at the lattice mismatched interface. A number of likely sources for the carrier accumulation were discussed, including the possibility of electrically active defects at the intersection of 90° misfit dislocations. Lateral carrier transport in InAs epilayers was proposed to occur through two parallel conducting channels – a high carrier density, low mobility interface channel and a higher mobility bulk channel. Mobility values higher than 10000 cm^2/V-sec have been achieved in thick layer samples (where bulk conductivity dominates) despite a high threading dislocation density.

ACKNOWLEDGEMENTS

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OPTICAL ABSORPTION IN
ZnSe-GaAs HETEROVALENT QUANTUM STRUCTURES

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ABSTRACT

ZnSe-GaAs(001) heterovalent quantum structures, multiple quantum wells (MQWs), were fabricated. Since the band offsets in this heterovalent heterostructure are controllable, different offsets can artificially be put at both sides of the GaAs wells, which may lead to modification of the electronic properties of the MQWs. This hypothesis was examined by the optical absorption measurement. Consequently, by changing the valence band offset at the GaAs-on-ZnSe interface from 0.6 to 1.1 eV, while keeping that at ZnSe-on-GaAs constant at 0.6 eV, the absorption edge energies of the MQWs shifted from 1.43 to 1.37 eV. This indicates the presence of an internal electric field and the capability of controlling the electronic properties of heterovalent MQWs with the completely same structural parameters. The numerical analyses of the Poisson and Schrödinger equations well explain the trend of this experimental result.

INTRODUCTION

Heterovalent heterostructures such as ZnSe-GaAs and GaAs-Ge possess an attractive characteristic that band offsets between the constituent materials are variable. Different from isovalent heterostructures, the heterovalent heterostructures include interface electronic dipoles owing to inevitably formed donor and acceptor bonds, which play a crucial role in determining the band offset. The strength and direction of the dipoles depend sensitively on the microscopic interface atomic configuration and, thus, so do the band offsets. Variations of the band offsets for ZnSe-GaAs, Ge-GaAs, and Si-GaP have been theoretically predicted to be as large as 1.0[1,2], 0.6[3,4], and 0.8 eV[3], respectively.

Experimentally, the effect of the interfacial properties on the tunability of the band offsets has already been investigated for several prototypical lattice-matched and theoretically well-understood heterostructures[1,5-8]. We have recently demonstrated the controllability of the band offsets in ZnSe-on-GaAs(001) [ZnSe/GaAs(001)][5,9] and GaAs-on-ZnSe(001) [GaAs/ZnSe(001)][6] heterostructures; the valence band offsets could be tuned from 0.6 to 1.1 eV by manipulating the interfacial atomic geometry through precise control of the flow sequence of the source precursors at the interfaces. These studies opened a way to fabricate ZnSe-GaAs multilayered quantum structures whose properties regarding carrier transport and confinement can be designed.

In this study, in order to confirm whether or not the properties of ZnSe-GaAs multiple quantum well (MQW) structures can be modified based on the controllability of the band offsets, MQWs in which the band offsets on both sides of the GaAs wells are designed to be different are fabricated. If the band offsets are actually different, the MQWs should contain an electric field and their optical absorption edges should shift toward lower energies[10]. We will perform theoretical analyses to illustrate the electronic properties of the heterovalent MQWs including an *intrinsic* electric field, and then compare them with the experimental

71

results of the absorption properties measured at room temperature (RT).

THEORETICAL CONSIDERATIONS

The electronic properties of a QW with an electric field are described by the one-dimensional Poisson and Schrödinger equations. Strictly, these equations should be solved self-consistently, though for simplicity, the following approximation has been made in this study. The quantum confinement effect was not considered in the Poisson equation and the carrier concentrations were written in classical formulations using the Ehrenberg approximation[11]. Within the limitation of this classical approximation, the band lineups are uniquely defined only by the Poisson equation. Therefore, eigenstates are, then, calculated by solving the Schrödinger equation, where carriers experience the band lineup derived from the Poisson equation. Although this procedure is not self-consistent and may degrade the quantitative accuracy, the electronic properties of the heterovalent MQW can be outlined relatively easily.

The Poisson equation is solved with the periodic boundary conditions. First of all, we investigated the effect of impurity concentration on the band lineup. Surprisingly, it was found that the band lineup hardly depended on the impurity concentration and that it was determined by the difference of the valence band offsets at both sides of the GaAs wells. Figure 1 shows some of the calculated band lineups of the MQWs. The dimensions of the GaAs wells and the ZnSe barriers are 100 and 110 Å, respectively, which are the same parameters with those in the fabricated MQWs. The pairs of the valence band offsets at both sides of the GaAs wells are (a) 0.6/0.6, (b) 0.6/0.9, and (c) 0.6/1.1 eV. ZnSe is assumed to be n-type with donor concentration of $1 \times 10^{11} \mathrm{cm}^{-3}$, while GaAs is p-type with $5 \times 10^{17} \mathrm{cm}^{-3}$. These quantities are the experimental results from Hall effect measurements of thick layers, but are not essential as was mentioned. It is obvious from the figure that the electric field becomes stronger by increasing the difference of the valence band offsets. The average electric fields in the well and the barrier regions are estimated to be 0.11 and
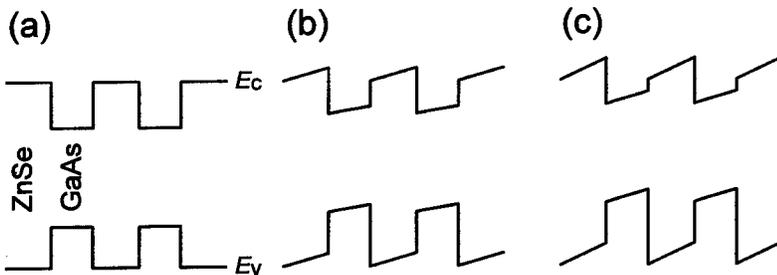
Figure 1: Calculated band lineups of the ZnSe-GaAs heterovalent MQWs with different pairs of the valence band offsets at both sides of GaAs; (a) 0.6/0.6 eV, (b) 0.6/0.9 eV, and (c)0.6/1.1 eV. E_c and E_v indicate the conduction and the valence band, respectively.

0.18 MV/cm for (b), and 0.18 and 0.29 MV/cm for (c), respectively.

Under the presence of the electric field revealed by the Poisson equation, the Schrödinger equation was solved by the variational method[12]. The single QW with ZnSe barriers of infinite width was used as a model for the calculation. This seems to be valid in this study because the penetration of the calculated wave function into the ZnSe barrier regions was totally within about 100Å, which is narrower than the ZnSe barrier width in the fabricated MQWs of 110 Å. Therefore, the wave function in each well of the MQWs hardly interacts and is thoroughly isolated one another. The used variational wave functions are basically the same with those in Ref. [12], though were modified to satisfy the boundary conditions of $\psi_{GaAs} = \psi_{ZnSe}$ and $m^*_{GaAs}{}^{-1}(d\psi_{GaAs}/dz) = m^*_{ZnSe}{}^{-1}(d\psi_{ZnSe}/dz)$ at the interfaces, where ψ and m^* denote the wave functions and the effective masses for the indicated material. The result of the calculation will be shown in the next section along with experimental results.

EXPERIMENTAL RESULTS AND DISSCUSION

The ZnSe-GaAs MQW structures were fabricated on GaAs(001) substrates by metalorganic vapor phase epitaxy (MOVPE). The source precursors for GaAs and ZnSe were triethylgallium (TEGa) and tertiarybutylarsine (TBAs), and diethylzinc (DEZn) and dimethylselenium (DMSe), respectively. The sample structure is schematically shown in Fig. 2. Growth of the samples was initiated by a GaAs buffer layer 1500 Å thick at 700°C. To obtain an atomically flat surface, post-growth annealing was conducted at 700°C for 10 min. Next a 500 Å thick ZnSe region was grown at 450°C primarily to act as an etch stop layer for substrate removal. Finally, an 8 periods MQW consisting of 110 Å ZnSe barriers and 100 Å GaAs wells was grown at 450°C. The detailed growth conditions are found in Refs. [5], [6], and references therein. The valence band offsets in both ZnSe/GaAs and GaAs/ZnSe heterostructures are controllable. In this study, however, to simplify the discussion, the former was kept constant at 0.6 eV for all MQWs, while the latter was changed between 0.6 and 1.1 eV. For this control of the band offset, the interval duration between the ZnSe and GaAs growth, during which only hydrogen was supplied for purging the ZnSe source precursors, was set at 5 sec, and the GaAs growth was initiated after the
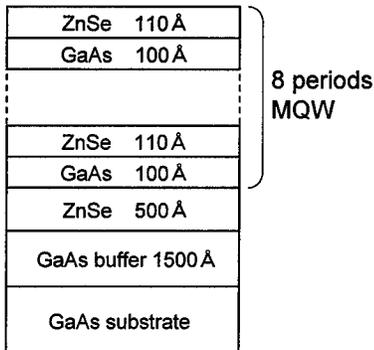
Figure 2: Schematic diagram of the fabricated ZnSe-GaAs MQWs.

exposure of ZnSe to TBAs for 2 – 20 sec (see Ref. [6] for more details). The influence of this artificial control of the valence band offset on the optical properties was assessed by optical absorption measurements at RT. For the absorption measurements, the substrate of the samples was removed by a selective $NaOH(1N) : H_2O_2 = 1 : 1$ (in volume) etching solution. The light from a halogen lamp passed through a 10 cm monocromator and a chopper was irradiated to the MQWs and the transmitted light was detected by a Si photodetector and was processed by a lock-in amplifier.

In order to extract differences of the optical properties due to the interface engineering, it is important to clarify the structural properties, because the structural properties may also contribute to the modification of the optical properties of the MQWs. For this purpose, the surface morphology and the crystallinity were investigated by means of atomic force microscopy (AFM) and x-ray diffraction (XRD), respectively. The AFM observation was carried out in air immediately after the growth. There is no evident difference associated with the interface control, and the surfaces for all MQWs exhibited atomically flat terraces and monomolecular steps (2.8 Å in height). This result suggests that regardless of the manner to prepare the interfaces, the growths of both ZnSe/GaAs and GaAs/ZnSe are in the two dimensional growth mode under the conditions employed here and the interfaces are abrupt. The XRD patterns were taken in the vicinity of the GaAs 004 diffraction, using Cu $K\alpha_1$ (1.5405 Å) radiation as an x-ray source. In addition to a fundamental peak, well-defined satellite peaks are clearly detected. The peak intensity ratio between the satellite and the fundamental peaks and the full width at the half maximum (FWHM) agree well with those derived from a dynamical simulation, indicating the high crystalline quality, high periodicity, and high interface abruptness in the MQWs. In the simulation, ZnSe was assumed to be deformed so as to maintain coherent growth, and the agreement with the experimental results supports this assumption. The entire region of the MQW is grown coherently on the GaAs substrate with few dislocations. It should be emphasized that the XRD profiles obtained from the MQWs with different interface properties are almost identical, which allows us to attribute the difference appearing in the optical properties to the interface properties.

We will move to the discussion on the optical absorption measurements. Figure 3 shows a typical RT absorption spectrum of the ZnSe-GaAs heterovalent MQW in which the valence
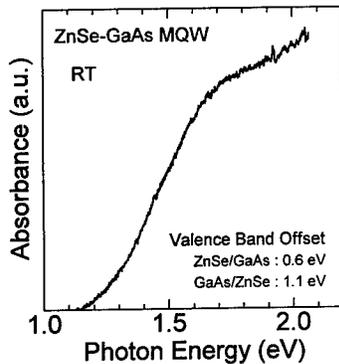
Figure 3: Typical absorption spectrum of the ZnSe-GaAs heterovalent MQW measured at RT. The valence band offsets at ZnSe/GaAs and GaAs/ZnSe are designed to be 0.6 and 1.1 eV, respectively.

band offsets at ZnSe/GaAs and GaAs/ZnSe are 0.6 and 1.1 eV, respectively. Since excitonic absorption peaks were not detected, the discussion has been done based on the absorption edge, which was defined as the energy determined by extrapolation of linear dependence of the square of the absorbance on irradiated photon energy into zero absorbance. It is worth noting that the absorption edge may be smaller than the energy gap to some extent because of the influence of impurities and excitons. Indeed, the absorption edge of GaAs 1150 Å thick grown on ZnSe/GaAs was estimated to be 1.40 eV, and this value is smaller by 30 meV than the energy band gap of GaAs at RT, 1.43 eV.

The absorption edge energies of the MQWs with different pairs of the valence band offsets at both sides of the GaAs wells are compared in Fig. 4. The theoretically calculated energy gap as well as the experimental results (open circles) is indicated by the solid line. As stated before, the valence band offset at the ZnSe/GaAs interface is 0.6 eV and the quantity indicated at the transverse axis is that at the GaAs/ZnSe interfaces. Accordingly, for example, the valence band offset of 0.6 eV in the figure corresponds to the flat band condition. It is explicitly seen that the MQW with the larger valence band offset exhibits the lower absorption energy. The plausible curve representing the behavior of the experimentally determined absorption edges against the valence band offsets is illustrated by the broken line in the figure. This line is almost parallel to the theoretical calculation of the energy gap and is located at the lower energy by about 40 meV. Considering that in the case of GaAs, the difference of 30 meV was observed between the absorption edge and the energy band gap as was mentioned in the previous paragraph, a major factor for the discrepancy of about 40 meV in Fig. 4 may be ascribed to the fatal difference due to impurities and/or excitons. Therefore, we consider that the experimental results agree reasonably with the theoretical calculation and that the electronic properties in the heterovalent MQWs are well described by the lineups shown in Fig. 1 and by the energy eigenvalues determined by the lineups. Namely, the larger difference in the valence band offsets at both sides of the GaAs wells induces the stronger electric field (Fig. 1), which causes the more red shift of the absorption energy.

The core of this preliminary study is the capability of controlling the electronic properties of heterovalent quantum structures with the completely same structural parameters, which differs considerably from isovalent systems.
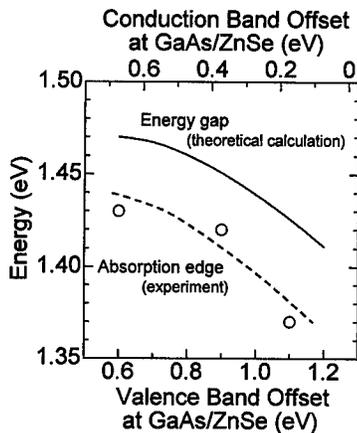
Figure 4: The absorption edge energies of the MQWs with different pairs of the valence band offsets at both sides of the GaAs wells. The valence band offset at the ZnSe/GaAs interfaces is constant at 0.6 eV. Together with the experimental results (open circles), the theoretically determined energy gap is indicated by the solid line.

CONCLUSIONS

ZnSe-GaAs(001) heterovalent MQWs were fabricated and their optical properties were assessed by the optical absorption measurements at RT. The absorption edges of the MQWs shifted toward lower energy by enlarging the difference of the valence band offsets at both sides of the GaAs wells. This is an indication of the presence of the internal electric field. The theoretical calculation based on the Poisson and Schrödinger equations provided a well explanation for this experimental result.

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DEEP LEVEL CHARACTERIZATION OF INTERFACE-ENGINEERED ZnSe LAYERS GROWN BY MOLECULAR BEAM EPITAXY ON GaAs

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ABSTRACT

Deep level defects have been detected and analyzed in epitaxial ZnSe layers grown by molecular beam epitaxy (MBE) on GaAs and on $In_{0.04}Ga_{0.96}As$ using deep level optical spectroscopy (DLOS). A series of samples, which differ only in the initial Zn:Se beam pressure ratio (BPR = 1:1, 1:10, 10:1) during the growth nucleation step, were characterized by DLOS in order to assess the dependence of bulk deep level formation on interface nucleation conditions. The transient and steady state photocapacitance measurements were performed using 100 W Quartz Halogen and 450 W Xe lamps as light sources, in the spectral range of 0.9 to 2.9 eV with a resolution better than 0.02 eV. The capacitance transients were recorded for time windows of 10 msec to 5 sec after light excitation of the sample, which was kept at a temperature of 100 K. Using semi-transparent Au Schottky contacts, several deep levels in the ZnSe layer were detected for all BPR's, with optical threshold energies of 1.1, 1.46 and 1.9 eV below the conduction band. These energies were obtained from the slope of the capacitance transient at different time intervals and were confirmed by steady state photocapacitance. The concentration of the levels was in the range 10^{12} to 10^{14} cm^{-3}. Both the 1.1 and 1.46 eV trap concentrations were found to depend strongly on lattice mismatch conditions, whereas the latter was shown to largely depend on BPR. The optical threshold of the 1.9 eV trap correlates well with a ~1.9 eV cathodoluminescence (CL) peak, which has been previously associated with either Zn vacancies or Ga_{Zn} substitutional defects in Zn-deficient material.

INTRODUCTION

By virtue of their large band gap II-VI semiconductor materials such as ZnSe have received great interest for optoelectronic devices operating in the blue-ultraviolet regime. Device efficiency and reliability however have been limited by various crystalline defects that can arise from growth conditions and choice of substrate. Correlating the electronic properties of these defects to those conditions can lead to a better understanding of the physics behind the device characteristics. Thus, studying the bulk deep level states in ZnSe and their dependence on interface nucleation conditions is important. Photo- and cathodo-luminescence (PL and CL) have been previously used to determine interface states on ZnSe grown by molecular beam epitaxy (MBE) on GaAs [1] whereas photocapacitance measurements have been used before to study bulk deep levels in similarly grown n-type ZnSe [2]. However, a study of how deep levels within the ZnSe bulk relate to those interface states and initial nucleation conditions has not been reported to date.

In this work we describe the properties of deep levels in ZnSe grown by MBE on GaAs and $In_{0.04}Ga_{0.96}As$/GaAs substrates for ZnSe layers nucleated under initial Zn-rich, stoichiometric and Se-rich conditions. Deep level optical spectroscopy (DLOS) was used to electrically characterize the deep levels since it can probe levels far from each band on wide gap materials, that are undetectable for other techniques such as deep level transient spectroscopy (DLTS).

77

Correlation between ZnSe bulk and ZnSe/GaAs interface deep levels are investigated by means of cathodoluminescence spectroscopy (CLS) measurements on thin ZnSe films grown on GaAs under the same BPR conditions as those heterojunctions used for the DLOS measurements.

EXPERIMENT

The DLOS heterostructures were grown by solid source MBE in a system with interconnected chambers used for the III-V and II-VI growth. GaAs(001) substrates were used, on which 0.5 μm thick GaAs and, when required, 1 μm thick $In_{0.04}Ga_{0.96}As$ buffer layers were grown (both $n=3\cdot10^{18}$ cm^{-3}). ZnSe overlayers 2 μm thick were deposited on the III-V buffer layers. The Zn:Se beam pressure ratios (BPR's) were changed between 0.1, 1 and 10 during the initial 2 nm ZnSe growth [3]. The ZnSe layers were unintentionally doped, with a net n-type background doping of $2-9\cdot10^{15}$ cm^{-3} as determined by C-V analysis on the deposited contacts. The CLS specimens were also deposited on GaAs substrate wafers. For these experiments buffer layers of 500 nm thick GaAs ($n=1\cdot10^{17}$ cm^{-3}) were first grown, followed by 2 nm thick ZnSe overlayers under BPR's of 0.1, 1 and 10 [1].

Front semitransparent Schottky contacts were fabricated on the DLOS samples by electron beam evaporation of 80 Å thick Au films after ZnSe native oxide removal [4]. The contact area was ~3.33 mm^2. A small 1000 Å Au contact (~0.2 mm^2) which served for probing purposes was next deposited inside the previous contact area, aligned to its perimeter.

The CLS measurements were done using electron beam energies between 0.5 keV and 4.5 keV, on a 100 μm diameter spot. The luminescence was focused onto a monochromator set to a 25 meV resolution, and detected by a Ge photodetector. The spectra were corrected for the optical system response [1].

Photocapacitance measurements were performed using 440 W Xe and 100 W Quartz-Halogen lamps as sources. The light was monochromized and focused onto the sample, which was maintained in an evacuated probe station chamber. Photon fluxes in the range $2-7\cdot10^{15}$ sec^{-1}cm^{-2} were obtained from the system with an energy resolution of 0.02 eV or better. The sample temperature was kept at 100 K at all times in order to minimize thermal emission from deep states so that only optical emission/capture processes were active, to first order. A zero bias across the Au/ZnSe Schottky contact was used for all measurements, yielding a depletion region depth of ~ 0.8 μm from the Au/ZnSe interface.

The DLOS experiments were done by measuring the photocapacitance transients from smaller to larger excitation energies. The capacitance transients were recorded for time windows 10 msec to 5 sec after illumination. The samples were kept in the dark for 10 sec as a carrier filling pulse for the deep levels was applied. Since the background doping was n-type, the traps near the depletion edge were thus filled with electrons before illumination.

The transients were studied in two ways. First, the slope was calculated at different time windows by performing a linear fit to the extracted data. Since different traps have different optical emission rates, changes in the slope at given energies is an indication of an emission from a new trap [5]. This approach was used to deduce the optical threshold energies for the different traps in an accurate fashion [6]. Second, the steady state photocapacitance was extracted from the longer time windows. When using light with energies smaller than half the band gap, only emission of electrons from the deep levels to the conduction band can occur for these n-type samples. Under these conditions, and assuming an abrupt transition from full depletion to undepletion, the concentration of each trap is related to the increase in the steady state photocapacitance spectrum by [5]:

$$N_T \cong 2N_d \frac{\Delta C}{C} \qquad (1)$$

Therefore, every new step in the photocapacitance spectrum, going from smaller to larger energies, corresponds to a deep level whose concentration is proportional to the magnitude of the step. On the other hand, when the excitation energy is larger than half the band gap, emission of holes to the valence band can compete with electron emission to the conduction band, and the measured change in the steady state capacitance only provides a lower limit for the concentration of the given trap [5].

RESULTS AND DISCUSSION

The optical threshold energies of all deep levels were obtained from the study of the slope of the photocapacitance transients during different time windows as a function of illumination energy [6]. For all samples, three deep levels with optical threshold energies of 1.1, 1.46 and 1.9 eV below the conduction band are observed. To serve as an example, Fig. 1 shows the photocapacitance transients for three different light excitation energies measured from ZnSe/InGaAs/GaAs. For a light energy of 1.3 eV only the 1.1 eV trap is excited, whereas for a 1.6 eV illumination energy both the 1.1 and 1.46 eV traps are excited (Fig. 1a). The change in the slope of the transient as a function of incident light energy within a 1 to 10 msec time window revealed an optical threshold energy of 1.10 ± 0.04 eV, and that of a 0 to 1 msec time window indicated an optical threshold at 1.46 ± 0.02 eV. Finally, the photocapacitance transient for a 2.2 eV excitation energy is shown in Fig. 1b. At this illumination energy, the 1.9 eV trap is also being excited, and a very slow photocapacitance transient is observed. The change of the transient slope in the 20 to 200 msec time window revealed an optical threshold energy of 1.9 ± 0.04 eV.
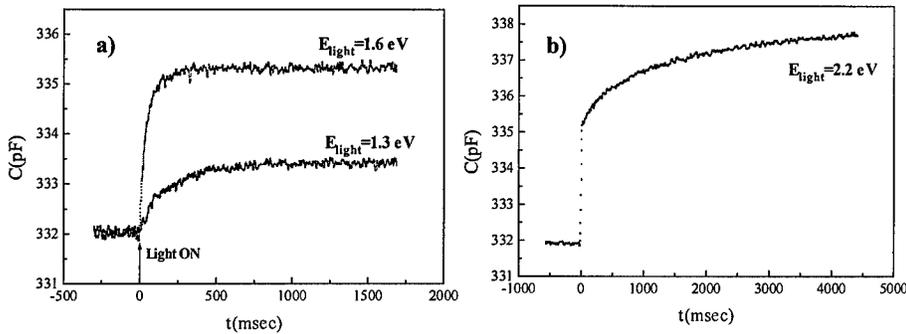
Figure 1. Photocapacitance transients from the ZnSe grown on $In_{0.04}Ga_{0.96}As$ sample for three different light excitation energies: **a)** 1.3 and 1.6 eV; **b)** 2.2 eV.

To obtain trap concentrations, steady state photocapacitance measurements were performed. All photocapacitance spectra shown in this paper were plotted for $2N_d \Delta C/C$ in order to account for changes found in the background doping concentration from sample to sample. Fig. 2 shows steady state photocapacitance spectra for the same sample (open circles) used in Fig. 1 (ZnSe/InGaAs/GaAs BPR=1) compared with ZnSe grown directly on GaAs (solid circles), for the same BPR conditions. A large decrease in concentration of the traps at 1.1 and 1.46 eV is observed for ZnSe/InGaAs/GaAs. This decrease is consistent with a reduction in extended defect

density that may be attributed to a lattice-matched ZnSe/InGaAs interface. However, earlier reports have suggested that the 1.1 eV trap is associated with a Se vacancy complex [1]. It is not clear how this defect is affected by the ability to lattice-match the ZnSe layer, and further analysis of potential physical sources is still needed. The trends are summarized in Table I where it is seen that the concentration of the 1.1 and 1.46 eV traps reduces by over an order of magnitude with the lattice-matching InGaAs buffer layer in place. In contrast, the concentration of 1.9 eV trap did not change for either substrate.
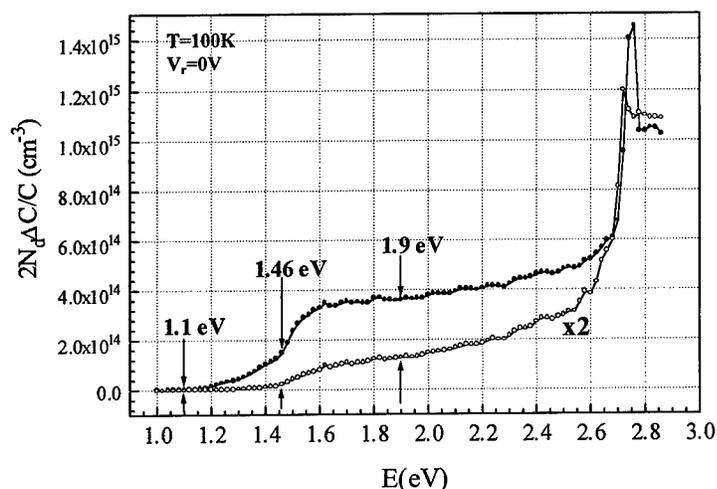
Figure 2. Steady state photocapacitance spectra from ZnSe grown on GaAs (solid circles) and ZnSe grown on $In_{0.04}Ga_{0.96}As$/GaAs (open circles) with BPR=1. The optical threshold energies shown in this figure are consistent with the results obtained from the study of the transient slopes.

Table I. Comparison of concentration (cm^{-3}) for deep levels present in ZnSe grown on GaAs and $In_{0.04}Ga_{0.96}As$.

	$E_c-E_t=1.10$ eV (±0.04 eV)	$E_c-E_t=1.46$ eV (±0.02 eV)	$E_c-E_t=1.90$ eV (±0.04 eV)
ZnSe/GaAs	$1\cdot10^{14}$	$2\cdot10^{14}$	$1\cdot10^{14}$
ZnSe/InGaAs/GaAs	$1\cdot10^{13}$	$5\cdot10^{13}$	$9\cdot10^{13}$

Next, we considered the effect of various BPR's, looking exclusively at the ZnSe/$In_{0.04}Ga_{0.96}As$/GaAs structures. The same deep levels were also found for the ZnSe layers grown under initial Se and Zn rich conditions (Fig. 3) as in the stoichiometric layers, with the critical difference only in relative trap concentrations. The concentration of the 1.1 eV trap exhibited no clear dependence on BPR. However, the concentrations of the traps at 1.46 and 1.9 eV systematically decrease as the Zn:Se ratio during nucleation is decreased (Table II). The 1.46 eV trap was found to be particularly sensitive to BPR conditions, decreasing in concentration by a factor of 8 as the BPR is varied from 10 to 0.1. This behavior is consistent with a decrease in Se vacancy concentration under Se-rich conditions, and correlates well with [3], where it was shown

that growing under Se rich conditions largely reduces the density of stacking faults. However a definitive correlation requires further experimentation. While the defect responsible for the 1.46 eV trap is not yet known, measurements were performed which ruled out the GaAs band edge as
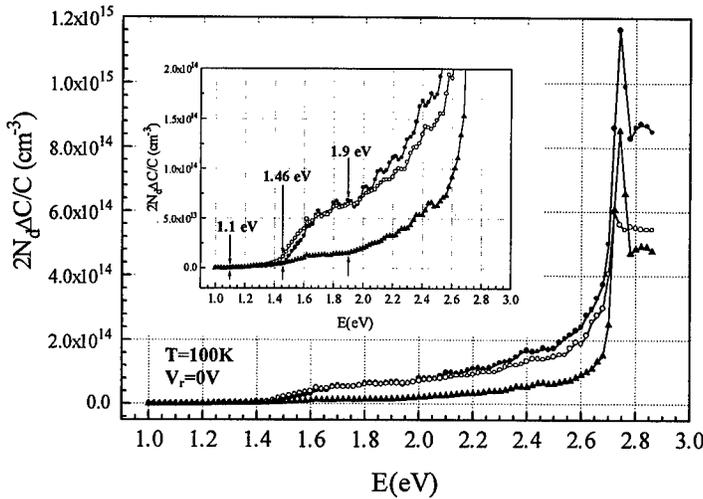
Figure 3. Steady state photocapacitance spectra from ZnSe grown on InGaAs with initial BPR=10 (solid circles), BPR=1 (open circles) and BPR=0.1 (solid triangles). A magnified view of the spectra is shown in the inset.

the source, which was a suspect due to its 1.45 eV bandgap. This was concluded due to three observations. First, if it was a GaAs band to band transition, the BPR should not affect the 1.46 eV emission as seen in Table II. Second, no photocurrent at any energy below the ZnSe band edge was observed. And third, we did not observe any resistive contributions to the photocapacitance for illuminations near the bandgap energy.

Table II. Comparison of concentration (cm^{-3}) for deep levels present in ZnSe grown on $In_{0.04}Ga_{0.96}As$ with initial BPR's of 0.1 (Se rich), 1 and 10 (Zn rich).

	$E_c-E_t=1.10$ eV (±0.04 eV)	$E_c-E_t=1.46$ eV (±0.02 eV)	$E_c-E_t=1.90$ eV (±0.04 eV)
ZnSe/ZnSe BPR=0.1/InGaAs/GaAs	$5 \cdot 10^{12}$	$7 \cdot 10^{12}$	$5 \cdot 10^{13}$
ZnSe/InGaAs/GaAs	$1 \cdot 10^{13}$	$5 \cdot 10^{13}$	$9 \cdot 10^{13}$
ZnSe/ZnSe BPR=10/InGaAs/GaAs	$5 \cdot 10^{12}$	$6 \cdot 10^{13}$	$1 \cdot 10^{14}$

The presence of a trap at $E_c-1.9$ eV also closely matches CLS and PL studies of thin ZnSe layers as a function of BPR. In these studies, a broad luminescence peak is observed at ~1.9 eV, whose intensity was an order of magnitude larger for Se-rich (Zn-deficient) vs. Se-poor nucleation conditions [7]. This emission was only obtained for heat treated samples, and had a lower temperature onset for the Se-rich interfaces. The magnitudes of the peak height and width

largely increased as a function of increasing annealing temperature. Thus, this state was associated to a point defect source and was attributed to either Ga_{Zn} substitutional or Zn vacancy defects.

CONCLUSIONS

We have used photocapacitance measurements to study the influence of different growth conditions on the bulk deep level spectra of ZnSe grown by MBE on GaAs. We found deep levels at 1.1, 1.46 and 1.9 eV from the conduction band with concentrations between 10^{12} and 10^{14} cm^{-3}. The inclusion of an InGaAs layer lattice matched to GaAs decreases the concentration of the 1.1 and 1.46 eV traps by over an order of magnitude. Growth of the ZnSe film under initial Se and Zn rich conditions shows the same deep levels as for stoichiometric growths. The concentration of the trap at 1.46 eV is decreased by almost an order of magnitude for Se rich ZnSe nucleation. We thus believe that this deep level may be related to Se vacancies or vacancy complexes. The 1.9 eV trap may be correlated to a broad ~1.9 eV emission found with CLS measurements that was associated with Zn vacancies and Ga_{Zn} substitutional defects.

ACKNOWLEDGMENTS

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SPATIAL DISTRIBUTION OF LUMINESCENT CENTERS IN ORGANOMETALLIC VAPOR PHASE EPITAXY GROWN $Zn_xCd_{1-x}Se$ / InP (001)

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ABSTRACT

Zincblende $Zn_xCd_{1-x}Se$ alloys were grown on (001) InP by organometallic vapor phase epitaxy (OMVPE) using various VI / II precursor flow ratios, ranging from 0.95 to 12, at a temperature of 420°C. Spatial distribution of luminescent centers in the epilayer was characterized by cathodoluminescence (CL) spectroscopy and imaging. Both near band-gap (NBE) and deep level (DLE) emissions were observed in the spectra, with the width of the NBE peak increases with the VI / II flow ratio. Monochromatic CL images showed that the broadening of the NBE peak has its origin in the spatial inhomogeneity of the luminescent centers of the epilayer. Extended defects responsible for the DLE was only found in pyramidal hillocks seen in the CL images. The density of these defects was found to increase with the VI / II flow ratio.

INTRODUCTION

The $Zn_xCd_{1-x}Se$ ternary alloy is a direct band gap semiconductor and has been successfully grown in the zincblende structure with a full range of composition $0 \leq x \leq 1$.[1] By adjusting x, its band gap can be varied from 2.7 eV for ZnSe to 1.66 eV for CdSe at room temperature. Therefore, it is a promising material for optoelectronic devices that can operate in the whole visible region. Recently, room temperature continuous wave (cw) operation of ZnSe-based laser diodes[2] with a lifetime of about 100 hours has been demonstrated. This is a great achievement, but their lifetime is still far shorter than what is required for practical applications. Early studies of III-V semiconductor lasers show that misfit dislocations and point defects in the active layer are often responsible for the short life times.[3,4,5] Therefore, understanding defect generation and distribution in II-VI materials, and searching for optimal growth conditions are of importance to their potential applications. However, crystal growth is a complicated process, many parameters need to be considered and optimized. For the OMVPE growth, It has been shown that the anion/cation flow ratio has a great influence on the quality of the layer grown. For the III-V system, this flow ratio is typically kept much larger than unity; otherwise, the molten metal would form during growth.[6] The II-VI system is somewhat different from the III-V semiconductors. It has been reported that CdTe can be grown with a VI / II flow ratio below unity.[7] This is interpreted as due to the higher vapor pressure of the group II element at the growth temperature. In this work, we study the influence of VI / II flow ratio on the luminescent properties of OMVPE grown $Zn_xCd_{1-x}Se$ layers nearly lattice matched to InP.

EXPERIMENT

$Zn_xCd_{1-x}Se$ layers of thickness around 0.2-0.3μm were grown on nominal (001) InP by an OMVPE system with a horizontal reactor. The reactor pressure was kept at 100

torr. Six samples were grown with different VI / II precursor flow ratios at the same temperature of at 420°C. The Zn, Cd, Se precursors used were diethylzinc (DEZn), dimethylcadmium (DMCd) and diethylselenide (DESe), respectively. Before the growth, the InP substrates were steamed in 1-1-1 trichloroethane vapor for about 30 minutes, then etched in a mixture of (5:1:1) $H_2SO_4:H_2O_2:H_2O$ solution for 5 minutes at room temperature. Between each step, the substrates were rinsed in de-ionized water for 4 minutes, followed by drying with N_2 gas. To perform deoxidization the cleaned substrate was preheated to 470°C for 10 minutes under hydrogen flow just prior to the actual growth. DEZn and DMCd flow rates were kept constant during the growth; different VI / II flow ratios were obtained by varying the DESe flow rate.

CL measurements were performed in a Cambridge S-360 scanning electron microscope fitted with an Oxford MonoCL system. A CCD detector attached to a spectrometer of 0.5 nm resolution recorded the spectra. The spectral response of the CCD and the spectrometer was not corrected in this study. A photo-multiplier tube was used for CL imaging. Samples were mounted on a liquid nitrogen cooling stage and cooled to about 80·K. Characterization of the epilayers routinely involves X-ray diffraction (XRD), optical reflectance spectroscopy (RS), and atomic force microscopy (AFM). XRD was used to investigate the composition of and the strain within the epilayer, RS to determine the epilayer thickness, and AFM to characterize the surface morphology.

RESULTS AND DISCUSSION

Fig.1 shows the CL spectra of six samples grown with different VI / II precursor flow ratios. The spectra were taken from an area of $30\times22.5\mu m^2$ on the sample using an electron beam voltage of 10 kV and current of 100 pA. The intensity of the NBE peak first increases with the flow ratio, but eventually drops after passing through a maximum at the flow ratio of 1.64. The intensity of the DLE peak, however, increases monotonically with the flow ratio. To facilitate the comparison of the spectra, the peak intensity of the NBE was normalized to a same value. From the figure, we see that, besides the strong NBE, there is also a broad deep level emission (DLE) whose energy ranges from about 1.3 to 1.8 eV. The DLE is about 0.4~0.5 eV below the NBE and may have a similar origin as the cation-vacancy related complexes in ZnSe[8, 9]. For the sample grown with a VI / II flow ratio of 0.95, the DLE is weak but still observable in the spectrum. However, with the increase of the VI / II flow ratio, the DLE is getting relatively weaker and finally becomes hard to detect for the sample grown with a VI / II flow ratio of 1.64. Further increase in the VI / II flow ratio results in a decrease of the absolute intensity of NBE, and an increase of DLE. The small variation in the energy of the NBE peak reflects the slight changes in the composition x as the flow ratio changes.

The intensity ratio of DLE to NBE, as a function of the VI / II precursor flow ratio, is shown in Fig. 2. This intensity ratio is often used to characterize the quality of the epilayers. For our growth, the smallest intensity ratio, hence, the best epilayer occurred at a flow ratio of about 1.64. It increases rapidly when the flow ratio is above 1.64, indicating that too high a flow ratio actually facilitates the generation of DLE associated defects. Since it is more likely to have cation-vacancy than anion vacancy during growth in a Se-rich environment, it is reasonable to suggest that cation vacancy related complexes are responsible for the DLE. Also shown in Fig. 2, is the almost linear increase of the width (FWHM) of the NBE with the flow ratio.
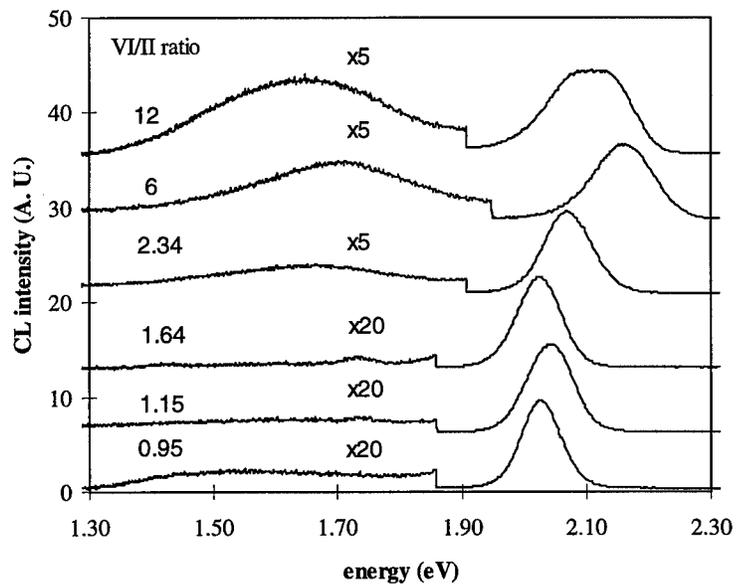
Fig.1 80 K CL spectra obtained from a 30 x 22.5 μm^2 area on $Zn_xCd_{1-x}Se$ epilayers grown with various VI / II precursor flow ratios. Excitation Electron beam voltage and current were 10kV and 100pA respectively. The intensity of the NBE peak is normalized.
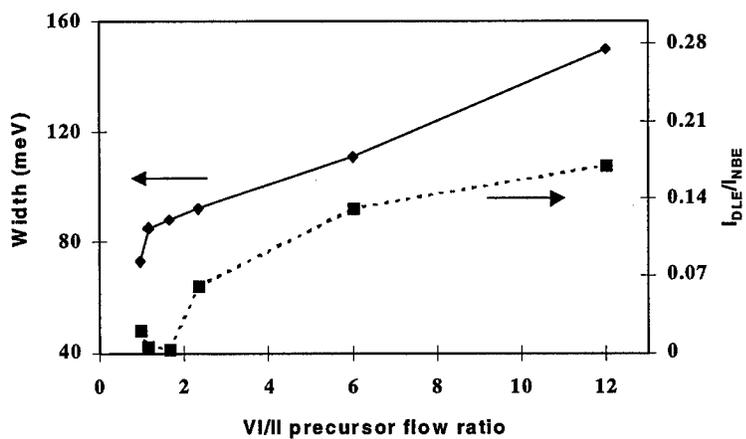
Fig.2 The width of NBE peak and the DLE to NBE intensity ratio as a function of VI / II precursor flow ratio.

The origin of the broadening of NBE is made clear by studying monochromatic CL images of the epilayer. Micrographs of a typical area of the sample grown with a flow ratio of 1.64 are shown in Fig. 3. Micrograph A is a secondary electron image; B, C, and D are CL images formed from 2.1, 2.06, and 2 eV photons, respectively. Pyramidal growth hillocks with a rectangular base, the longer side of which lies along the [1 -1 0] direction, are found on the surface. AFM imaging (not shown) indicates that the apex of the prism is about 70~150 nm higher than surrounding smooth area. The density and size of the structures were found to depend on the VI / II flow rate, when other conditions of growth were maintained. At a flow ratio of 1.64, its density is estimated to be around 6×10^6 cm^{-2} and size 1x 2 μm^2. Increase in flow ratio results in a high density of smaller hillocks. Moving from CL images B to D, the pyramidal hillocks are getting brighter and its surrounding smooth area darker. We note that two images B and D, which were formed by photons slightly above and below the NBE peak energy, are nearly complementary to each other. The high contrast of the two images indicates the different spatial origin of the photons. The NBE peaks of Fig. 1 are made up of photons originated from the prismatic hillocks and from their surroundings. In micrograph C, imaged at the peak energy of NBE, both areas contribute, resulting in reduced contrast.
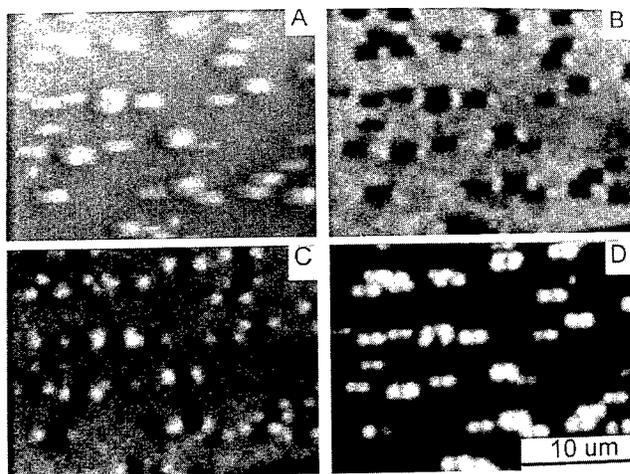
Fig.3 Micrographs of the same area of $Zn_xCd_{1-x}Se$ epilayer grown with a VI / II flow ratio of 1.64. A is the SEM image, showing pyramidal growth hillocks whose rectangular base are elongated and point along the [1 -1 0] direction; B, C and D are the monochromatic CL images formed from 2.1eV, 2.06eV and 2eV photons respectively.

With the knowledge that the NBE is actually made up of at least two peaks, we have fitted its shape with two Gaussian functions. Fig. 4 shows the NBE peak (A) and its two resolved components (B and C) for the sample grown at a flow ratio of 1.64. We ascribe peak B to luminescence from the prismatic hillocks and C the surrounding area. The measured width of the NBE peak is thus a composite quantity, strongly affected by the

density of the hillocks on the epilayer. At low VI / II flow ratios, there are less hillocks per unit area of the sample and C dominates the NBE peak. As flow ratio increases, so does the density of the hillocks. B becomes prominent in comparison to C and contributes significantly to the width of the NBE peak. At the flow ratio near 12, the hillocks coalesce and become indistinguishable, resulting in a very rough surface of the epilayer. The NBE peak becomes noticeably broader and clearly features a flat top, reflecting its composition of two nearly intense peaks.
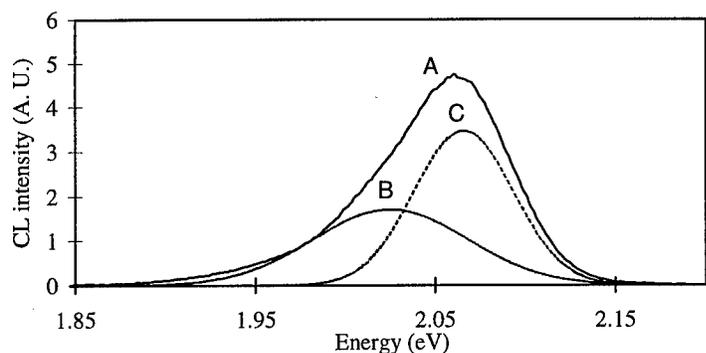
Fig.4 The NBE peak A is shown resolved into two Gaussian peaks B and C. The lower energy peak B was found to originate from around the hillocks, as shown in Fig. 3D, while C from the surrounding area as shown in Fig. 3B

Concomitant with the broadening of the NBE peak, there is an increase in the intensity of the DLE relative to that of the NBE. The reason of this concomitance is clear when we study the distribution of the centers that are responsible for the DLE. Using a long pass optical filter, we allowed only photons from the DLE to form CL images of the epilayer. Fig. 5A shows an example of such an image. Fig. 5B is a SEM micrograph of the same area of the sample. We note that the DLE comes entirely within the growth hillocks. An increase in the density of the hillocks as a result of growth in a higher VI / II flow ratio would cause an increase in the DLE intensity.
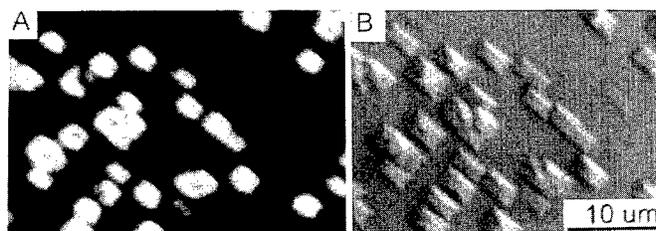
Fig.5 SEM (A) and room temperature CL image formed from DLE (B). The [1 −1 0] direction is along the diagonal of the micrograph.

It is known that non-stoichiometric growth conditions generally result in pits or hillocks on the epilayer. The density of the hillock and pits was found to increase with the deviation from stoichiometry. In a group VI rich environment, growth of B planes is faster than both the (001) and A planes, resulting in a pyramidal hillocks of elongated rectangular base. The fact that both the low energy NBE and DLE are found only within the hillocks strongly suggests they are related to non-stoichiometric defects such as cation vacancies. The DLE is possibly related to complexes associated cation vacancies and the low energy NBE band to acceptor recombination, with the cation vacancy acting as an acceptor.

CONCLUSIONS

In conclusion, we have studied a series of nearly lattice matched $Zn_xCd_{1-x}Se/InP$ growth at 420°C with different VI / II flow ratio using CL spectroscopy and imaging. We find that there is often a broad DLE in addition to the NBE in the CL spectra. The width of the NBE peak and the intensity of the DLE relative to that of the NBE increase with the VI / II precursor flow ratios during the growth. The origin of the broadening of NBE is due to a spatial average of contributions from the pyramidal growth hillocks and their surrounding smooth area on the epilayer. The DLE is probably associated with Zn or Cd-vacancy related complexes and is found only within the hillocks. The density of the hillocks tends to increase with the VI / II flow ratio until it becomes so high that the hillocks coalesce, resulting in an epilayer of rough surface.

ACKNOWLEDGMENTS

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Part III

Integration and Defect Engineering for Wide-Gap Semiconductors

GROWTH AND CHARACTERIZATION OF GaN AND AL$_X$GA$_{1-X}$N THIN FILMS ACHIEVED VIA LATERAL- AND/OR PENDEO-EPITAXIAL OVERGROWTH ON 6H-SIC(0001) SUBSTRATES

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ABSTRACT

Discrete and coalesced monocrystalline layers of lateral- and pendeo-epitaxially grown GaN and Al$_x$Ga$_{1-x}$N layers originating from GaN stripes deposited within windows contained in SiO$_2$ masks or from side walls of GaN seed structures containing SiN$_x$ top masks have been grown via organometallic vapor phase deposition on GaN/AlN/6H-SiC(0001) substrates. Multilayer heterostructures of GaN and Al$_x$Ga$_{1-x}$N were also achieved. Scanning and transmission electron microscopies and atomic force microscopy were used to evaluate the microstructures, the type and distribution of dislocations and the surface roughness of the resulting films. The extent and microstructural characteristics of the laterally overgrown GaN regions were a strong function of stripe orientation and temperature. These regions contained a low density of dislocations. The RMS roughness of the ($11\bar{2}0$) sidewall plane of the pendeo-epitaxial structures was approximately 0.100 nm.

INTRODUCTION

It has been a necessity for investigators in the III-nitride community to grow films of GaN and related nitride materials using heteroepitaxial growth routes because of the dearth of bulk substrates of these materials. This results in films containing dislocation densities of 10^8-10^{10} cm^{-2} because of the mismatches in the lattice parameters and the coefficients of thermal expansion between the buffer layer and the film and/or the buffer layer and the substrate. These high concentrations of dislocations may also limit the performance of devices.

Several groups [1-9], including the present authors, have conducted research regarding selective area growth (SAG) and lateral epitaxial overgrowth (LEO) techniques for GaN deposition, specifically to reduce significantly the dislocation density. Increased emphasis in this research topic was fueled in part by the announcement by Nakamura, et al. [10] of the dramatic increase in projected lifetime of their GaN- based blue light-emitting laser diodes fabricated on LEO material. Using these approaches, researchers have been able to grow GaN films containing dislocation densities of $\approx 10^5$ cm^{-2} in the areas of overgrowth. However, to benefit from this reduction in defects, the placement of devices incorporating LEO technology is limited and confined to regions on the final GaN device layer that are located on the overgrown regions.

Recently we have pioneered a new approach to selective epitaxy of GaN and Al$_x$Ga$_{1-x}$N layers, namely, pendeo- (from the Latin: to *hang* or be *suspended*) epitaxy (PE) [11-16] as a promising new process route leading to a single, continuous, large area layer; multilayer heterostructures or discrete platforms of these materials. It incorporates mechanisms of growth exploited by the conventional LEO process by using an amorphous mask to prevent vertical propagation of threading dislocations; however, it extends beyond the conventional LEO approach to employ the substrate itself as a *pseudo-mask*. This unconventional approach differs from LEO in that growth does not initiate through open windows on the (0001) surface of the GaN seed layer; instead, it is forced to selectively begin on the sidewalls of a tailored microstructure comprised of forms previously etched into this seed layer. Continuation of the

pendeo-epitaxial growth of GaN or the growth of the $Al_xGa_{1-x}N$ layer until coalescence over and between these forms results in a complete layer of low defect-density GaN or $Al_xGa_{1-x}N$. This is accomplished in one (GaN), two ($Al_xGa_{1-x}N$) or multiple (multilayer heterostructure) re-growth steps. And the need to align devices or masks for the growth of the subsequent layers over particular areas of overgrowth is eliminated, unless deposition only in certain areas is desired.

The following sections describe the experimental parameters necessary to achieve GaN films via LEO and PE and $Al_xGa_{1-x}N$ layers via PE. The microstructural evidence obtained for the resulting films is also described, discussed and summarized.

EXPERIMENTAL PROCEDURES

The LEO of GaN stripes patterned in SiO_2 masks deposited on a GaN film/AlN buffer layer/6H-SiC(0001) substrates has been achieved in the manner shown in schematically in Figure 1. The GaN was deposited on the underlying GaN layer through the windows in the SiO_2 mask. The deposited material grew vertically to the top of the mask and then both laterally over the mask and vertically until the lateral growth fronts from many different windows coalesced and formed a continuous layer. The underlying 1.5-2.0 μm thick GaN films were grown at 1000°C on high temperature (1100°C) AlN buffer layers previously deposited on 6H-SiC(0001) substrates in a cold-wall, vertical and RF inductively heated OMVPE system. Additional details of the growth experiments have been presented in Ref. [17]. Each 100 nm thick SiO_2 mask layer was subsequently deposited on each GaN/AlN/6H-SiC(0001) sample via low pressure chemical vapor deposition at 410°C. Patterning of the mask layer was achieved using standard photolithography techniques and etching with a buffered HF solution. The pattern contained 3μm and 5μm wide stripe openings, both spaced parallel at various distances (3-40μm), and oriented along <11$\bar{2}$0> and <1$\bar{1}$00> in the GaN film. Prior to lateral overgrowth, the patterned samples were dipped in a 50% buffered HCl solution to remove the surface oxide of the underlying GaN layer. The lateral overgrowth was achieved at 1000 -1100°C and 45 Torr. Triethylgallium (13-39 μmol/min) and NH_3 (1500 sccm) precursors were used in combination with a 3000 sccm H_2 diluent.

Each pendeo-epitaxial GaN and $Al_xGa_{1-x}N$ film, underlying GaN seed layer and AlN buffer layer were grown in the MOVPE system used for the LEO research. Each seed layer consisted of a 1 μm thick GaN film grown on a 100 nm thick AlN buffer layer previously deposited on a 6H-SiC(0001) substrate. A 100 nm silicon nitride growth mask was deposited on each seed layer via plasma enhanced chemical vapor deposition. A 150 nm nickel etch mask was subsequently deposited using e-beam evaporation. Patterning of the nickel mask layer was achieved using standard photolithography techniques followed by dipping in HNO_3 for approximately five minutes. The samples were subsequently cleaned by consecutive dips in trichloroethylene, acetone, methanol, and HCl for five minutes each and blown dry with nitrogen. The final, tailored, microstructure consisting of seed forms was fabricated via removal of portions of the nickel etch mask via sputtering and by inductively coupled plasma (ICP) etching of portions of the silicon nitride growth mask, the GaN seed layer and the AlN buffer layer. The etching of the seed-forms was continued into either the 6H-SiC substrate or the 3C-SiC layer, thereby removing all III- nitride material from the areas between the sidewalls of the forms. This step was critical to the success of the pendeo-epitaxial growth. The seed-forms used in this study were raised rectangular stripes oriented along the <1$\bar{1}$00> direction, thereby providing a sequence of GaN sidewalls (nominally (11$\bar{2}$0) faces). Seed form widths of 2 and 3 μms coupled with separation distances of 3 and 7 μms, respectively, were employed. The remaining nickel mask protecting the seed structures during the ICP etching process was removed using HNO_3. Immediately prior to pendeo-epitaxial growth, the patterned samples were dipped in a 50% HCl solution to remove the surface oxide from the walls of the underlying GaN seed structures.
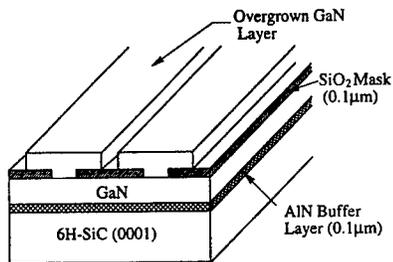
Figure 1. Schematic diagram showing lateral epitaxial overgrowth of GaN layer on SiO$_2$ mask from GaN deposited within striped window openings on GaN/AlN/6H-SiC substrates.

Schematics of the pendeo-epitaxial growth of GaN(0001), Al$_x$Ga$_{1-x}$N(0001) and layered structures of these materials are illustrated in Figure 2. There are three primary stages associated with the pendeo-epitaxial formation of the first layer of each of these materials: (i) initiation of lateral homoepitaxy (GaN) or heteroepitaxy (Al$_x$Ga$_{1-x}$N) from the sidewalls of a GaN seed layer, (ii) vertical growth and (iii) lateral growth over the silicon nitride mask covering the seed structure. Pendeo-epitaxial growth of GaN and Al$_x$Ga$_{1-x}$N was achieved within the temperature range of 1050-1100°C and a total pressure of 45 Torr. The precursors (flow rates) of triethylgallium (23 -27 μmol/min) and NH$_3$ (1500 sccm) were used in combination with a H$_2$ diluent (3000 sccm). The introduction of triethylaluminum at flow rates of 2.5 μmol/min and 5.8 μmol/min into the growth chamber produced Al$_x$Ga$_{1-x}$N layers containing Al concentrations of approximately 5% and 10%, respectively. Additional experimental details regarding the pendeo-epitaxial growth of GaN and Al$_x$Ga$_{1-x}$N layers are given in Refs. [11] - [16].

The morphologies and defect and surface microstructures for both types of samples were investigated using scanning electron microscopy (SEM) (JEOL 6400 FE), transmission electron microscopy (TEM) (TOPCON 0002B, 200 KV) and atomic force microscopy (AFM) (Digital Instruments, Inc. Dimension 3000). The AFM was operated in the tapping mode with an Olympus tapping mode etched silicon probe.

RESULTS AND DISCUSSION

Figure 3 shows the surface and cross-sectional morphologies of the homoepitaxial GaN stripes grown for different growth times on stripe openings oriented along <11$\bar{2}$0> and <1$\bar{1}$00>. The morphologies of the stripes were very similar after the 3 min of growth regardless of stripe orientation, as shown in Figures 2 (a)-(d). The stripes subsequently developed into different shapes as the growth proceeded. Triangular stripes having {1$\bar{1}$01} side facets were observed for window openings along <11$\bar{2}$0>, while rectangular stripes having a (0001) top facet and {11$\bar{2}$0} side facets developed for those along <1$\bar{1}$00>. The amount of lateral growth also exhibited a strong dependence on stripe orientation. Results obtained under various growth conditions showed that the lateral growth rates of the <1$\bar{1}$00> oriented stripes were much faster than those along <11$\bar{2}$0>. Additional studies regarding the dependence of the morphological evolution and the lateral and vertical growth rates of the GaN stripes on growth conditions as well as stripe orientation are underway.

Parallel 3μm wide stripe openings spaced 3μm apart were used to achieve continuous GaN layers by lateral overgrowth. Continuous 5 μm thick GaN layers were obtained, as shown in Figure 4. Atomic force microscopy of the surfaces revealed an average RMS roughness of the pit-free overgrown layers to be 0.25 nm which is similar to the RMS roughness values obtained for the underlying GaN films. Each black spot in the overgrown GaN layer shown in Figure 3 (a)
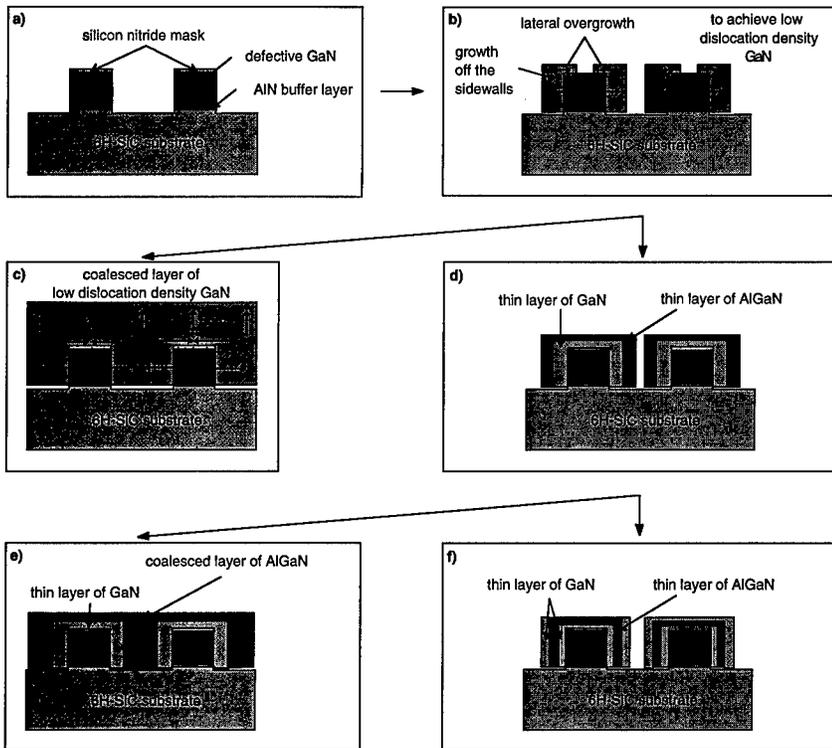
Figure 2. Schematic diagrams showing the steps necessary to form pendeo-epitaxial layers and structures. The process routes move from (a) the etched columnar forms in the GaN seed layers to (b) lateral growth from the side walls of the seed layer and lateral overgrowth over the silicon nitride mask, to the growth of either (c) a continuous coalesced GaN film, or (d) a discrete bi-layer of GaN and $Al_xGa_{1-x}N$ from which further growth results in either (e) a continuous coalesced layer of $Al_xGa_{1-x}N$ or (f) a multi-layered structure of GaN and $Al_xGa_{1-x}N$ layers.

is a void which forms when two growth fronts coalesce. These voids were most often observed under the lateral growth conditions wherein rectangular stripes having vertical $\{11\bar{2}0\}$ side facets developed.

A cross-sectional TEM micrograph showing a typical laterally overgrown GaN layer is presented in Figure 5. Threading dislocations, originating from the GaN/AlN buffer layer interface, propagate to the top surface of the regrown GaN layer within the window regions of the mask. By contrast, there were no observable threading dislocations in the overgrown layer. Microstructural studies of the areas of lateral growth obtained using various growth conditions indicated that the overgrown GaN layers contained only a few dislocations. These dislocations formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations did not subsequently propagate to the surface of the overgrown GaN layers.

Cathodoluminescence of selected regions using a scanning electron microscope indicates that yellow emission originates from the regrown regions having high dislocation densities; however, only strong band edge emission was observed from the overgrown layers.
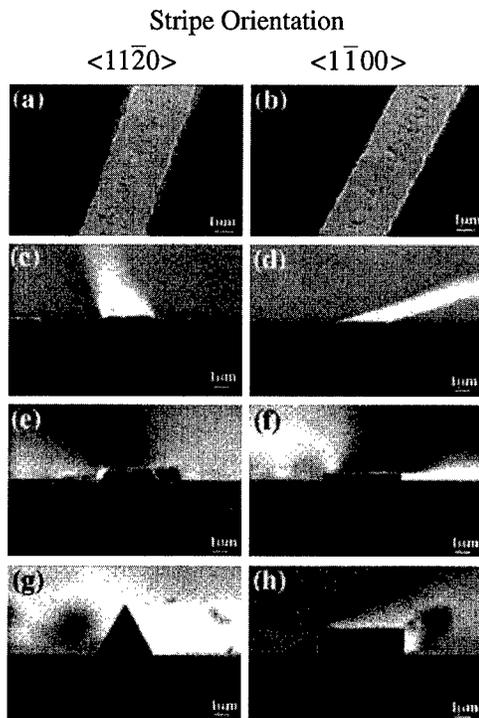
Figure 3. Scanning electron micrographs of GaN layers grown on 3 μm wide stripe openings oriented along <11$\bar{2}$0> and <1$\bar{1}$00> for the growth times of (a)-(d) 3 min, (e)(f) 9 min, and (g)(h) 20 min.

     The pendeo-epitaxial phenomenon is made possible by taking advantage of growth mechanisms identified by Zheleva et.al.[7] in the conventional LEO technique, and by using two additional key steps, namely, the initiation of growth from a GaN face other than the (0001) and the use of the substrate (in this case SiC) as a mask. By capping the seed-forms with a growth mask, the GaN was forced to grow initially and selectively only on the GaN sidewalls. Common to conventional LEO, no growth occurred on the silicon nitride mask covering the seed forms. Deposition also did not occur on the exposed SiC surface areas at the higher growth temperatures employed to enhance lateral growth. The Ga- and N-containing species more likely either diffused along the surface or evaporated (rather than having sufficient time to form GaN nuclei) from both the silicon nitride mask and the silicon carbide substrate. The pronounced effect of this is shown in Figure 6 wherein the newly deposited GaN has grown truly suspended (*pendeo*-) from the sidewalls of the GaN seed structure. During the second PE event (ii), vertical growth of GaN occurred from the advancing (0001) face of the laterally growing GaN. Once the vertical growth became extended to a height greater than the silicon nitride mask, the third PE event (iii) occurred, namely, conventional LEO-type growth and eventual coalescence over the seed structure, as shown in Fig. 7. A cross-sectional TEM micrograph showing a typical pendeo-
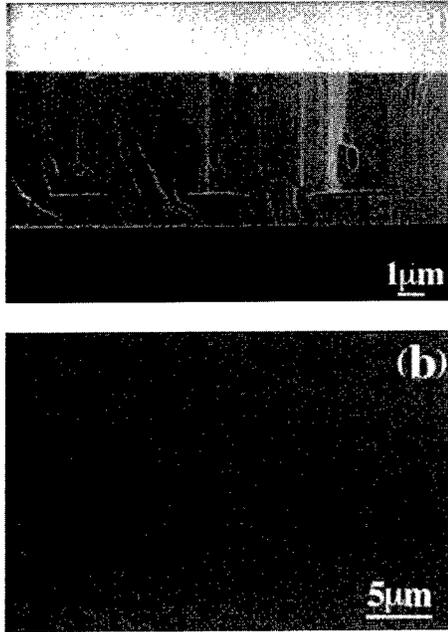
Figure 4. (a) Cross-section and (b) surface SEM micrographs of the coalesced GaN layer grown on 3 μm wide and 3 μm spaced stripe openings oriented along <1$\bar{1}$00>.
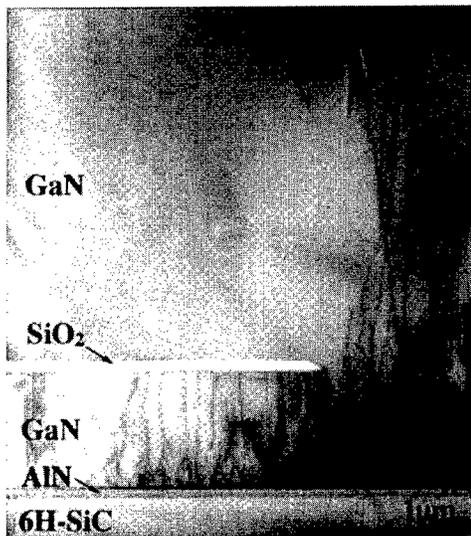
Figure 5. Cross-section TEM micrograph of a laterally overgrown GaN layer on a SiO$_2$ mask.

96
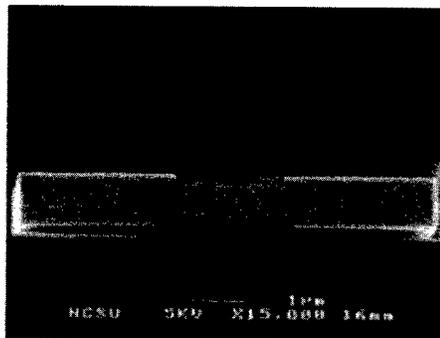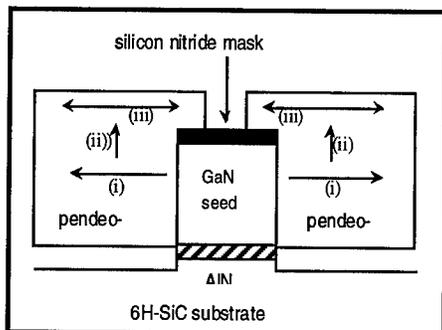
Figure 6. Cross-sectional SEM of a GaN pendeo-epitaxial growth structure with limited vertical growth from the seed sidewalls and no growth on the seed mask.
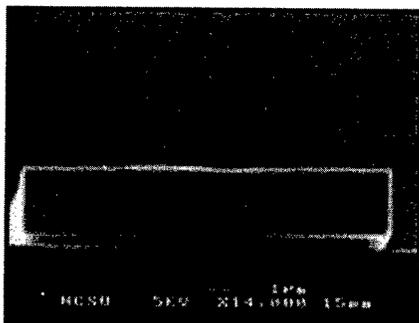
Figure 7. Cross-sectional SEM of a GaN/AlGaN pendeo-epitaxial growth structure showing coalescence over the seed mask.
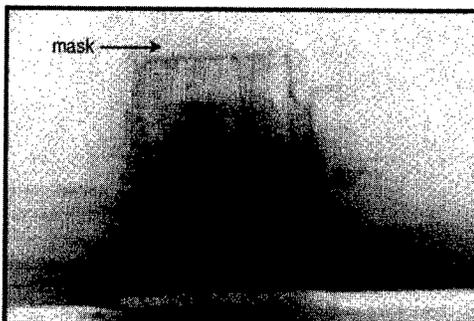
Figure 8. Cross-sectional TEM of a GaN pendeo-epitaxial structure showing confinement of threading dislocation under the seed mask, and a reduction of defects in the regrown areas.

epitaxial growth structure is shown in Fig. 8. Threading dislocations extending into the GaN seed structure, originating from the GaN/AlN and AlN/SiC interfaces, are clearly visible.

The silicon nitride mask acted as a barrier to the further vertical propagation of these defects into the laterally overgrown pendeo-epitaxial film. Since the newly deposited GaN is suspended above the SiC substrate, there are no defects associated with the mismatches in lattice parameters between GaN and AlN and between AlN and SiC. Preliminary analysis of the GaN seed/GaN pendeo-epitaxy interface revealed evidence of threading dislocations or stacking faults within the (0001) planes. This indicates evidence of the lateral propagation of the defects; however, there is yet no evidence that the defects reach the (0001) surface where device layers will be grown. As in the case of LEO, there is a significant reduction in the defect density in the regrown areas.

The continuation of the pendeo-epitaxial growth results in coalescence with adjacent growth fronts and the formation of a continuous layer of GaN, as observed in Figure 9. This also

(a)   (b)
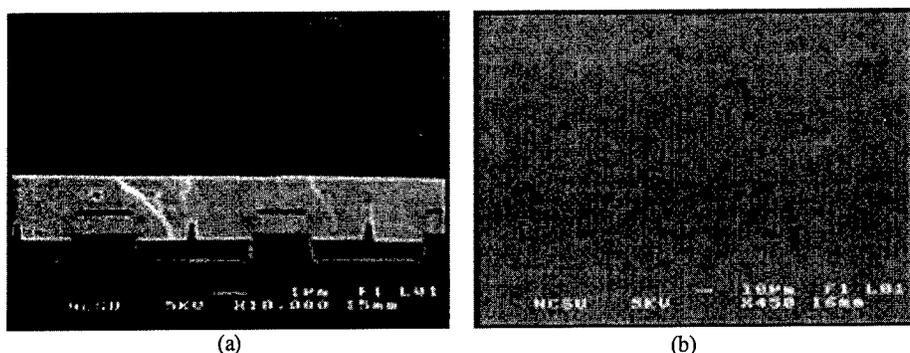
Figure 9. Micrographs taken via (a) cross-sectional SEM and (b) plan-view SEM of examples of pendeo-epitaxial growth with coalescence over and between the seed forms resulting in a single GaN layer.

results in the practical elimination of all dislocations stemming from the heteroepitaxial growth of GaN/AlN on SiC. Clearly visible in Fig. 9(a) are the voids that form when adjacent growth fronts coalesce. Optimization of the pendeo-epitaxial growth technique should eliminate these undesirable defects.

Each of the microstructures depicted in Figures 2(d), (e) and (f) has been realized in this research. It was necessary to refine the experimental procedure described above to achieve the different microstructures. To produce the heterostructure shown in Figure 2(e) a thin GaN layer was grown for 2 min at 1070°C and for 2 min at 1090°C. The $Al_{10}Ga_{90}N$ was deposited using three growth steps at the susceptor temperatures and times of 1090°C and 2 min., 1110°C and 50 min and 1090°C and 30 min. The second step was employed to force the $Al_{10}Ga_{90}N$ to grow laterally and coalesce; the third step was used to grow the film vertically. The growth rate of the $Al_{10}Ga_{90}N$ films was markedly lower at both 1090 and 1100°C than that of the GaN at any temperature employed in this study. The multi-layered structure shown in Figure 2(f) was also realized using several different growth parameters. The first layer of GaN was grown at susceptor temperatures of 1075°C for 3 min and 1090°C for 2 min. The subsequent layer of $Al_{10}Ga_{90}N$ was grown using susceptor temperatures of 1090°C for 10 min and 1075°C for 5 min. The temperature during the $Al_{10}Ga_{90}N$ growth was not increased to 1110°C to limit the lateral growth. The additional layer of GaN was grown at a susceptor temperature of 1075°C for 10 min.

SUMMARY

Continuous GaN films having very low dislocation densities have been achieved via lateral growth and coalescence of GaN homoepitaxial stripes over SiO_2 masks. The results suggest that lateral overgrowth of GaN via OMVPE is a promising technique for obtaining low defect density layers and could be useful for optoelectronic and microelectronic device applications. The pendeo-epitaxial technique has been developed as an alternative and more simple approach of growing uniformly low-defect density thin films over the entire surface of a substrate. In particular, we have demonstrated the growth of both discrete structures and coalesced GaN and $Al_xGa_{1-x}N$ films and multilayer heterostructures using pendeo-epitaxy on etched GaN seed layers previously grown on AlN/6H-SiC substrates.

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GROWTH OF GaN ON THIN SI {111} LAYERS BONDED TO SI {100} SUBSTRATES

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ABSTRACT

We have demonstrated the ability to bond thin layers of Si{111} onto either silicon dioxide or silicon nitride coated Si{100}. This was achieved using a "Smart-Cut" process. The integration of SiN required chemical mechanical polishing. The growth of GaN on a thin Si{111} on oxide on Si{100} stack was demonstrated.

INTRODUCTION

We are interested in developing integrated systems able to process information, sense, act and communicate. Eventually, all these capabilities will co-exist on a single die. At present, we are able to integrate Si-based electronics with various sensors and Si surface micromachined actuators. However, silicon's indirect band gap makes it unsuited to the manipulation of light for photonics and communications applications. GaN and its alloys are emerging as important optically active materials. They are relatively chemically and physically stable and defect insensitive. These unique properties, and reports that the growth of GaN on {111} Si is possible [1-3] have motivated us to try to integrate GaN with silicon technologies. However, while growth on {111} Si has been proven, typical CMOS technologies are based on {100} and not {111} silicon. As a first step, we have demonstrated the bonding of a thin layer of Si {111} material onto a thin silicon dioxide layer on a Si {100} substrate. This was done using a process developed by the French and often referred to as "Smart-Cut" [4-6] in which, in our case, a {111} wafer undergoes a high dose H implant. The dose is sufficiently high to nucleate bubbles at the range of the implant during heating. The stresses generated are sufficient to slice off a thin layer of silicon. Wafer bonding is initiated after implantation and the bond is strengthened by later heat treatments. We have subsequently used such hybrid substrates to grow epitaxial GaN. In order to address the potential problem of Ga diffusing into the silicon and degrading the CMOS we have demonstrated the insertion of a thin SiN diffusion barrier between the two layers of silicon.

APPROACH and RESULTS

Our final objective is the integration of standard CMOS technology with GaN. We proposed to achieve this through the combination of CMOS fabrication on Si{100} and the deposition of GaN on Si{111}. This is schematically outlined in Figure 1. This will require the integration of two different Si orientations and the introduction of Ga diffusion barrier between

the Si layers. SiN has been demonstrated to be an effective Ga barrier [7] and we have used integrated this material in the work presented here.
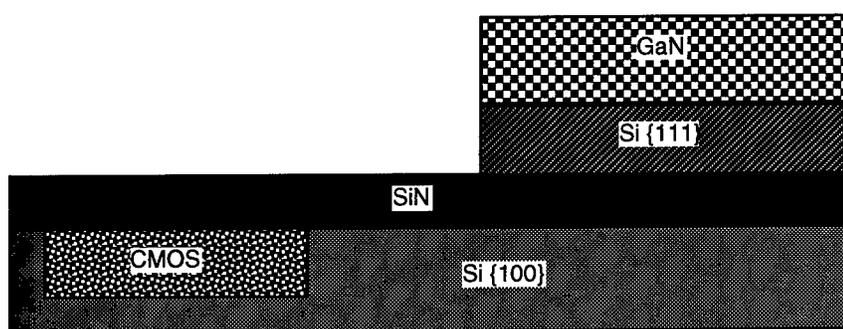
Fig. 1

Schematic of our proposed approach, CMOS will be fabricated on Si {100} and will be protected by a thin layer of SiN. The GaN will then be grown on a thin layer of Si{111} bonded to the Si{100}.

The "Smart-Cut" process is the technology we have explored to integrate the two different orientations of Si onto a single substrate. The process is schematically rendered in Fig. 2. In our work we have typically used a dose of 4×10^{16} of H_2^+ at 60keV. This results in layers which are ~350nm thick. We have used interlayers of either thermal silicon dioxide or silicon dioxide coated silicon nitride. The silicon dioxide samples were bonded as grown following a combination of a SC-1/megasonics (1:4:9, ammonium hydroxide: hydrogen peroxide: water, 5 minutes, 45 C) followed by a SC-2 (1:1:10, HCl: hydrogen peroxide: water, 5 minutes, 40 C) clean of both wafers. Upon being brought together, the wafers remain joined as a result of hydrogen bonding. We then heated the joined wafer stack to 900°C for 1 hour in N_2. We did not separate out the cutting heat treatment from the bonding heat treatment. The process works well over the vast majority of the wafer. Unbonded regions result from particles on the surface or physical defects, such as wafer scribe marks. In the unbonded regions the silicon cleaving process still takes place, however here the silicon delaminates and shatters into small fragments. Periodically there are also millimeter diameter size bubbles present. In these cases we speculate that the areas remained bonded up through the delamination process, however, at higher temperatures some other contaminant began to desorb, debonding the layer and forming the bubbles. Figure 3 shows a oblique SEM crossection of a bonded stack.

Implant H into the Si substrate which will donate the bonded layer.

Join the implanted wafer to a second "handle" wafer which is coated with an insulator.

Clean, flat, chemically active surfaces will bond at room temperature.

Upon heating to ~500°C, the H forms bubbles and the film cracks off at the range of the implant.

Further heat treatments strengthen the bond. The active wafer surface is then polished.

Figure 2.

The "Smart-Cut" process after M. Bruel [4].

The same process was used to integrate a thin SiN layer between the two sheets of silicon. However, due the surface roughness of this deposited film, additional surface preparation was required. The silicon nitride was deposited onto the handle {100} wafer using a chemical vapor deposition process at 800°C. The reactants were dichlorosilane and ammonia. The ratio of reactants was adjusted to result in a slightly silicon rich film (refractive index of 2.1) which has a lower level of stress than stoichiometric silicon nitride. The thickness of the layer was 400nm. The as-deposited film was sufficiently rough to prevent bonding. This problem was addressed through the addition of a chemical mechanical polishing (CMP) step, Fig. 4. This eliminated the grosser surface roughness. In order to create a thin oxide surface layer to aid in bonding, the wafers were then subjected to a 900°C, 30 minute steam oxidation process. The wafers were then cleaned, bonded and heat treated as described above. Again the process was successful on the whole, however, there were numerous small unbonded regions spread across the wafer. The origin of these defects is unclear, they may be the result of CMP slurry remaining on the surface of the wafer, or residual film roughness. This problem was addressed through the deposition of a thin film of silicon dioxide on top of the polished silicon nitride layer. The silicon dioxide was deposited by plasma enhanced chemical vapor deposition using a TEOS (tetraethoxysilane) precursor. The film was 120nm thick and, following deposition, was stabilized by a 1050°C, 20 second rapid thermal anneal in a Ar/O_2 ambient. Approximately half of this thermal oxide film was then polished back using CMP. The motivation behind this was that the thin oxide layer would bury any small defects on the wafer

surface. The wafers were then bonded using the process outlined above. In this case, the bonding was successful and there were no small circular unbonded regions.
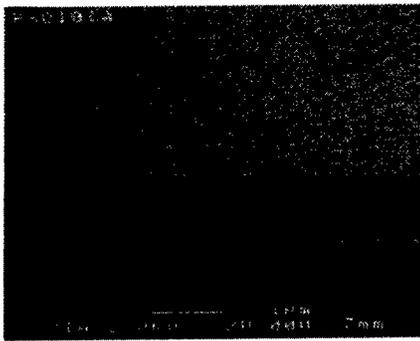
Fig. 3.
Oblique cross section scanning electron micrcrograph showing a an oxide interlayer and the bonded layer.
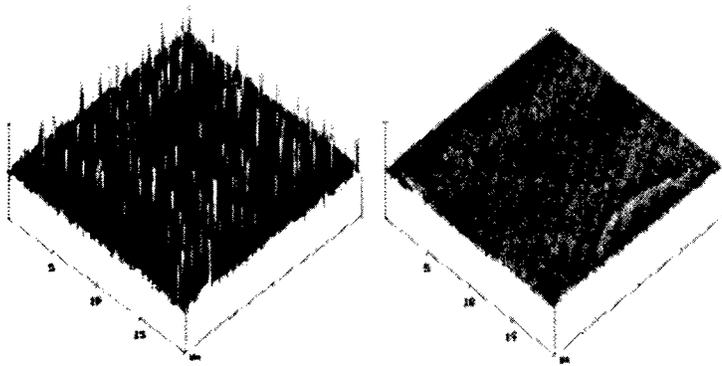
Fig. 4
AFM traces of pre and post CMP on a 400nm thick low stress SiN film. The horizontal scale is 10 nm.

Following the cleaving process, the surface of the wafers was specular to the naked eye. However, scanning electron microscopy revealed a regularly roughened surface on both {100} and {111} substrates, Fig 3. AFM measurements determined the RMS roughness to be ~6nm. In order to prepare the samples for deposition, the {111} bonded layers were subjected to a ~5 second etch in a 6M 65°C KOH solution. KOH effectively does not etch {111} Si planes. However, the {111} substrates used were ~3.5 ° off the {111} and as a result the surface consisted of a series of scalloped steps, Fig. 5.
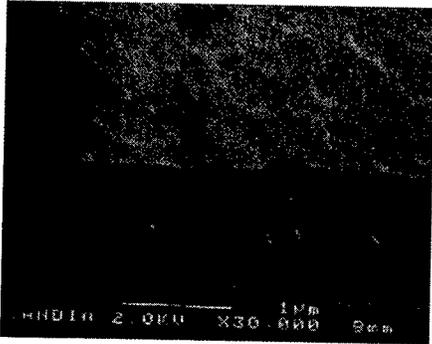
Fig. 5

SEM micrograph showing the surface morphology of a stack following a KOH treatment to remove damage at the cleavage interface. The {111} wafer was cut ~3.5 ° off orientation resulting in a scalloped-step morphology.

Layers of GaN/AlN (buffer) were grown in a high speed (~ 1000 rpm) rotating disc MOCVD reactor. Two-inch diameter substrates were placed on a molybdenum (Mo) susceptor that is RF inductively heated using a SiC-coated graphite coupling block. Temperature was monitored by a pyrometer focusing on the Mo susceptor surface, which is nearly co-planar with the wafer surface. Ammonia, TMGa (Trimethlygallium), and TMAl (Trimethylaluminum) were used as the N, Ga, and Al precursors, respectively. Hydrogen was used as the carrier gas and to supplement the ammonia in making up the required flow rate as determined by the reactor pressure and rotation rate. Metal-organic precursors were separated from hydride gases before being injected into the top of the growth chamber. An in-situ reflectometer used to monitor surface roughness and layer thickness used a tungsten lamp as a light source. The source illuminates a spot, of 6 mm in diameter, on the sample surface through a reactor port window. Both AlN and GaN were grown at a pressure of 30 Torr. The temperature for GaN growth was varied from 1050 to 1080C and for AlN growth was varied from 1050 to 1150C. Figure 6 shows an example of a deposited layer of GaN on AlN on Si {111} on thermal oxide on Si {100}. The major problem encountered has been cracking due to thermal expansion mismatch between the GaN and the Si.

CONCLUSIONS AND FUTURE WORK

In conclusion GaN has been successfully deposited on Si{111} bonded to Si{100} with either oxide or silicon nitride interlayers. This process was enabled using "Smart-Cut" technology. The next step in the process will be the reduction in cracking, possibly using epitaxial overgrowth techniques to create isolated islands of GaN instead of continuous sheets.
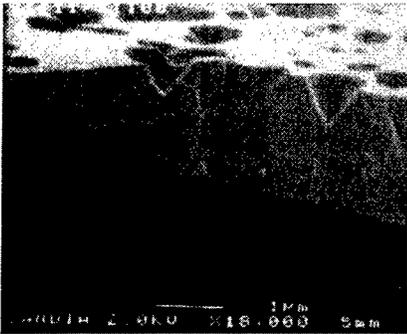
Fig. 6

Oblique view scanning electron micrograph of a thin film of GaN deposited on Si {111} on thermal oxide on Si {100}. The major problem encountered was cracking due to thermal expansion coefficient mismatches. The cracks terminate in the thermal oxide layer, probably due to the compressive nature of the oxide film.

ACKNOWLEDGEMENTS

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CHARACTERIZATION OF SINGLE-CRYSTAL 3C-SIC EPITAXIAL LAYERS ON SI SUBSTRATES

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ABSTRACT

In this paper we discuss the growth and characterization of 3C-SiC epitaxial layers grown on both a Si substrate as well as on a novel substrate. The growth uses a typical three step process. First an etch of the Si surface is performed, second the surface of the Si is carbonized and third 3C-SiC is grown on the carbonized surface. Several characterization techniques were used to verify the quality of the 3C-SiC film. Microscopy was used to investigate the surface morphology, X-ray and electron diffraction were used to determine crystal structure, cross section TEM was used to verify crystal structure and highlight twinning, and x-ray topography was used to measure the strain fields induced in Si substrate at the 3C-SiC/Si interface.

INTRODUCTION

Commercially available SiC substrates are made using the modified Lely method[1] and are available in both the 4H and 6H SiC polytypes. To date numerous devices have been demonstrated on both 4H and 6H substrates. However, a major concern is the fact that these substrates have a high density of defects such as micropipes ($\sim$ 200 per cm^2) along with other crystallographic defects that can lead to device failures.[2] Although further materials processing can be used to improve these substrates such as a method being researched to fill in micropipes,[3,4] it is doubtful that SiC substrates will approach the quality of Si wafers in the near future.

The 3C polytype of SiC is the only polytype that can be grown on Si wafers because the growth temperature for the hexagonal polytypes is above the melting point of Si (1410°C at STP). Clearly the development of a device epilayer process that can take advantage of inexpensive yet mature high-quality Si technology is advantageous if the tremendous potential of SiC is to be utilized in devices and systems in the near future. This work was therefore undertaken to assess the state-of-the-art of 3C-SiC epi on Si which will lead to the establishment of novel heteroepitaxy techniques to realize 3C-SiC device layers on large-area, low-cost, high-quality Si substrates.

3C-SiC on Si GROWTH EXPERIMENTS

Heteroepitaxy of 3C-SiC on Si is believed to require three distinct steps: first any native oxide is removed using a in-situ hydrogen etch, second a carbonization step is performed to form the initial layer of SiC, and third the 3C-SiC film is grown.[5,6] Growth of SiC films on (100) Si substrates were conducted in an radio frequency (rf) induction heated horizontal APCVD reactor

using the process schedule shown in Figure 1. After a RCA clean the Si substrates were placed on a SiC coated graphite susceptor. After the reaction chamber was evacuated of all residual gases a hydrogen carrier gas flow of 3 SLM was established. The substrate was then heated to 1000° C over a 3 minute interval and a 10 minute native oxide etch then performed. At the end of the 10 minute in-situ etch the rf power is turned off, and the susceptor is allowed to cool for 5 minutes to approximately room temperature. The Si substrate is now ready for the carbonization step. With the RF energy still switched off, 50 sccm of propane (3% C_3H_8 in ultra-high purity hydrogen) is added to the hydrogen carrier gas. After a 1 minute delay to allow the propane to stabilize in the reactor, the RF power is turned on and the susceptor temperature ramped to 890° C in 3 minutes. The temperature is then maintained at 890° C for 5 minutes after which the substrate temperature is ramped to 1335 °C in 1 minute while the propane is maintained at 50 sccm for 1.5 minutes. This completes the carbonization procedure. Next the 3C-SiC epilayer growth is begun by reducing the propane flow to 11 sccm while silane (SiH_4 3% in ultra-high purity hydrogen) is simultaneously introduced into the reaction chamber at a flow rate of typically 15 sccm. The growth process may be continued for any length of time but usually was performed for 120 minutes resulting in a 3C-SiC layer of approximately 4 μm (typical growth rate is ~ 2 μm/hour). To terminate the growth process the SiH_4 flow is discontinued and after a 1 minute delay the hydrogen carrier gas and the propane is discontinued, and the reaction chamber is purged with argon. After a 5 minute argon purge at the growth temperature of 1335 °C, the susceptor is allowed to cool to approximately room temperature. This completes the 3C-SiC on Si baseline process that was developed during this research.
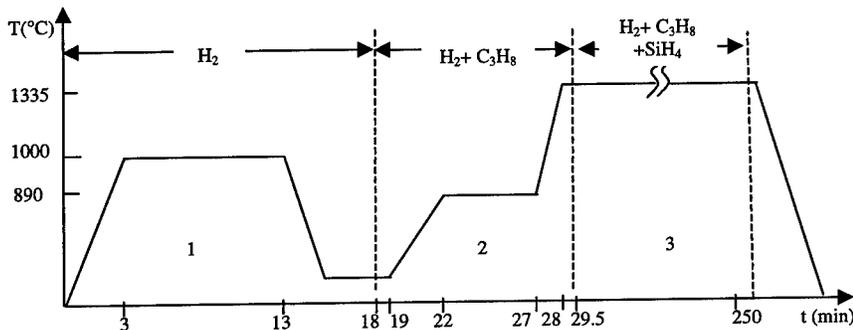
Figure 1 3C-SiC on Si Baseline Growth Schedule. The oxide etch, carbonization and 3C growth are indicated as 1, 2, and 3 respectively.

3C-SiC EPITAXIAL LAYER CHARACTERIZATION

Since the primary limitation of device layers grown from 3C-SiC on Si pertains to the crystal morphology, numerous crystallographic characterization tools were used to characterize the 3C-SiC on Si epitaxial layers developed during this research. These are namely scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-Ray and electron diffraction, Synchrotron White Beam X-Ray Topography (SWBXT) and optical microscopy. A LEO S360 SEM was used in the secondary electron mode to take the micrograph in Figure 2. The advantage of SEM is that it provides a good measure of the surface morphology. This is particularly important for 3C-SiC on Si because SiC is transparent to visible light, while

electrons at the accelerating voltage used for these micrographs only penetrate a short distance into the 3C-SiC film (less than .01 μm). The micrograph taken on the optimized baseline process described above show that the surface of the 3C-SiC film is smooth with some shallow depressions and a few deep depressions; however, no polycrystalline defects were seen and the film texture appeard to be single crystalline.

X-ray diffraction (XRD) data was taken at SUNY Stony Brook on the baseline 3C-SiC material. Two-theta scans displayed peaks associated with both the Si substrate (100) and 3C-SiC (200) film but no peaks were observed for 3C-SiC (111) or (220) orientations. This suggests a single crystalline epitaxial 3C-SiC film on the (100) Si substrate comparable to that reported by Goleck et al.[7] Rocking curve data indicate that the 3C film is likely of reasonable quality due to the well-defined peak shape observed.

Electron diffraction and TEM experiments were performed at the University of Alabama using a 200 keV system by Hitachi. In Figure 3(a) is selected area electron diffraction pattern indicating that the 3C-SiC crystal structure is orientated parallel to the Si (100) substrate. Figure 3(b) is a cross-section TEM micrograph showing the 3C-SiC/Si interface and well-defined twin boundaries in the 3C film. Samples must be thinned to electron transparency to be characterized by TEM to allow the electrons to be transmitted through the sample. Therefore the electrons must be accelerated by a large voltage to perform TEM measurements; a beam acceleration voltage as high as 200 kV was used to take these micrographs.

Voids at the 3C-SiC/Si interface were observed with optical microscopy and were noted to appear as spots in the synchrotron white beam x-ray topograph (SWBXT) in Figure 4. Therefore these voids do indeed affect the Si substrate crystal structure since SWBXT data displays a change in contrast whenever there is any disturbance in the atomic separation (i.e., a change in the lattice constant at a localized region in the crystal). Strain lines due to dislocation groups caused by the lattice mismatch between 3C-SiC and Si are clearly evident in the SWBXT data. An extended area of polycrystalline material in the SiC film (see Fig. 4, top of photo) appears as an area with no strain lines, but dark in color. The total penetration depth of the x-rays was approximately 50 μm for the crystal orientation used in this experiment, while the SiC film is only approximately 4 μm thick. In addition the extinction length is longer in SiC than for Si. Therefore, most of the contrast in the SWBXT is due to the Si substrate and not the 3C-SiC film. Since contrast in the SWBXT is caused by any change in the inter atomic spacing of the Si substrate, localized stress at the 3C-SiC /Si interface is clearly evident in the data. Data shown was taken at the National Synchrotron Light Source, Brookhaven National Labs, Beam Line X-19C.

Figure 2 SEM micrograph of 3C-SiC film on (100) Si. Note the smooth surface texture with minimum evidence of polycrystalline defects present.
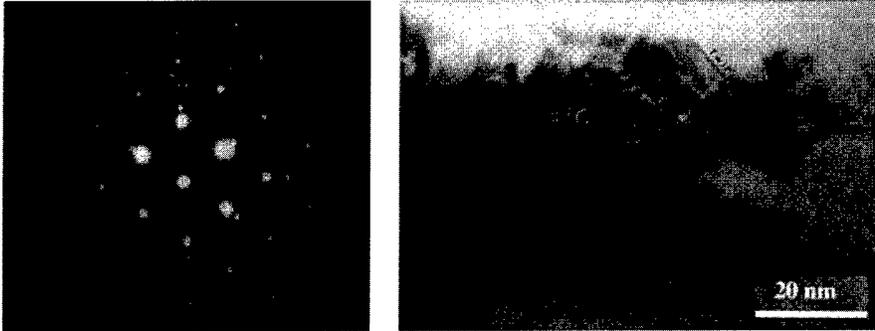
Figure 3 TEM data taken on baseline 3C-SiC on Si epi layer. (a) Electron diffraction pattern indicating 3C-SiC on Si cubic symmetry, (b) cross-section TEM image showing the 3C-SiC/Si and the associated twin boundary defect structure.
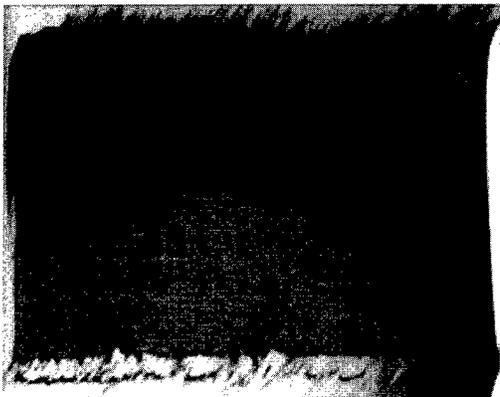
Figure 4 SWBXT data showing the strain field present in the Si substrate resulting from the 3C-SiC epi layer. The cross-hatched pattern is caused by dislocation groups at the 3C-SiC/Si interface. Sample size is approx. 1 cm × 1 cm.

The films discussed above show that one can grow single crystal "cube-on-cube" 3C-SiC on Si with reasonable morphology. These films are far from "device-quality" and some method for relaxing the stress caused by the 20% lattice mismatch must be developed to achieve device grade films.

3C-SIC GROWTH ON A Si CU SUBSTRATE

Compliant Universal (CU) Substrates have been proposed by numerous researchers with impressive results in III-V compounds recently reported by Lo et al.[8] The technique developed by Lo consists of a thin layer of bonded semiconductor material at an angle with respect to a thicker supporting substrate. In principle this arrangement allows the thin "twist bonded" layer to absorb the strain created by growing a subsequent film that has a lattice mismatch with the

original substrate. The thickness and twist angle must be engineered carefully. Ejeckam *et al* discussed how to choose the thickness and twist angle of the CU layer with respect to the support substrate as well as the bonding mechanism of the CU layer to the support substrate.[9] Ejeckam *et al* have demonstrated the benefits of this technique with the growth of an InSb film on a GaAs CU substrate.[10] InSb and GaAs have about a 15 % lattice constant mismatch thus this work appears to be promising for 3C-SiC on Si which has about a 22 % mismatch.

For this work a Si CU substrate was fabricated by Cornell University by twist bonding a (100) Si SOI layer at 45° with respect to a (100) Si substrate. The SiO_2 layer was then removed and the Si film thinned to a thickness of approximately 100 Å.[11] A 3C-SiC film was then grown on this Si CU substrate using the 3C-SiC baseline process described earlier. The growth time was 120 minutes with a growth temperature of 1335°C.

Cross-section TEM data on the 3C-SiC epi film was taken with a result similar to the baseline data shown in Fig. 2. Again, microtwins were evident in the 3C-SiC layer, which would indicate that the lattice mismatch has not been accomodated at the interface by the CU layer. However, the spacing between the microtwins was farther apart for the 3C layer grown on the CU Si substrate, indicating that a modest improvement in defect structure was achieved. In addition, SEM micrographs on this sample also showed a slight improvement in surface morphology. In the optical micrograph shown in Figure 5(a) the 3C-SiC film is oriented 45° from the support substrate (bottom right-hand corner) which was the twist angle for the CU layer. A large circle appears in the center of the SiC film (Fig 5(a), upper left corner) which was caused by thickness uniformity variations in the twist-bonded CU layer. Figure 5(b) shows the corresponding SWBXT data for this sample. As before for the baseline 3C-SiC on Si process, strain lines associated with dislocation groups caused by the lattice mismatch are evident in the SWBXT data. The strain lines are parallel to the (100) and (010) directions in the bulk Si substrate thus suggesting that the CU layer may have relaxed to the underlying Si support substrate orientation. An extended area of polycrystalline material in the SiC film appears as an area with no strain lines as was the case for the baseline topographs (upper left and lower right corners in the figure).
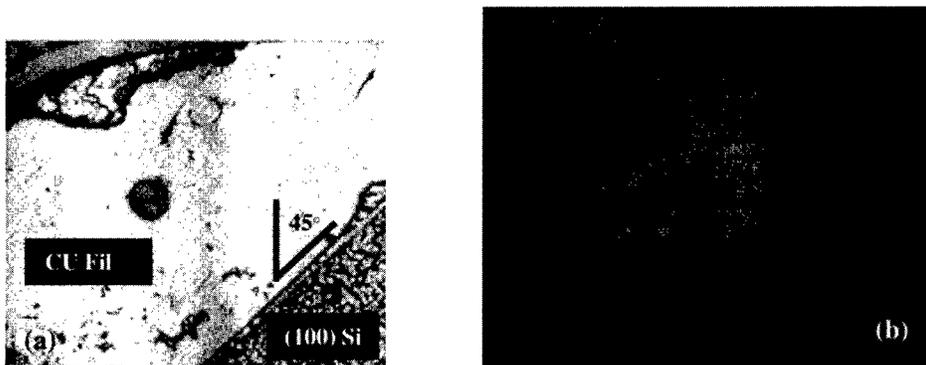
Figure 5 SWBXT image of the 3C-SiC on CU film. Lack of contrast in bulk Si material (upper left hand and lower right hand corners) due to polycrystalline 3C-SiC growth. Single-crystal 3C film in center region where dislocation groups are clearly evident and along substrate (100). Sample size approx. 5 mm × 5 mm.

111

CONCLUSIONS

A three step process was used to grow 3C-SiC on (100) Si substrates. First an etch was performed, second the Si surface was carbonized and third 3C-SiC was grown on the carbonized surface. Several characterization techniques were used to verify that the film grown was of high quality. SEM was used to demonstrate that the surface was smooth and lacking of polycrystalline defects. XRD (2-theta scans) and RHEED suggested a single crystalline film that is oriented "cube on cube" with respect to the substrate. Cross section TEM confirmed that the film was single crystalline with twinning being the dominant defect present in the epitaxial layer. SWBXT highlighted dislocation groups at the 3C-SiC/Si interface.

A 3C-SiC epi layer was grown on a Si substrate using the baseline process described above. The SWBXT data indicate that the CU layer appeared to have relaxed to the orientation of the support substrate; however, further characterization is required to determine the exact orientation of the CU layer. If CU film relaxation did indeed occur, this is likely due to the 3C-SiC setpoint temperature of 1335° C being too close to the Si melting point of 1410°. Lo at Cornell also had problems with the CU substrate relaxing at moderate temperatures during the Si CU substrate fabrication process so this is likely the explanation for the result observed in this work. Clearly further development of this promising approach is needed.

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GROWTH OF AlN ON Si(111) BY PLASMA-ASSISTED MOLECULAR BEAM EPITAXY: APPLICATION TO SURFACE ACOUSTIC WAVE DEVICES

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ABSTRACT

Epitaxial wurtzite aluminum nitride (AlN) films have been grown on (111) oriented silicon substrates by plasma-assisted solid source molecular beam epitaxy (MBE). The growth has been performed in the two-dimensional (2D) growth mode. Occuring surface reconstructions have been monitored by reflection of high-energy electron diffraction (RHEED).
The films have been characterized by atomic force microscopy (AFM) and transmission electron microscopy (TEM). 2D grown films exhibit atomically smooth surfaces, are single-crystalline and void of oriented domains. High-resolution (HR) TEM micrographs of the heterointerface show the presence of an interfacial atomic arrangement where (5:4) unit cells coincide along the AlN[2̲110]/Si[1̲10] direction.
Surface acoustic wave (SAW) properties of MBE-grown AlN(0001)/Si(111) have been studied for the first time. The AlN film exhibits very good piezoelectricity. The SAW time response indicates low scattering of the waves during their propagation. An electromechanical coupling coefficient (EMC) of 0.07% has been measured for the present interdigital transducer (IDT) geometry.

INTRODUCTION

AlN is a refractive material of excellent piezoelectricity [1,2] with high surface and bulk acoustic wave velocity [3,4].
Heteroepitaxial growth of AlN has been adressed by many researchers since the seventies. Besides its application as nucleation layer for the growth of III-nitrides on sapphire [5] or silicon [6,7], application to SAW devices was the focus of the early works. SAW properties of AlN grown on sapphire by various methods such as metalorganic vapor phase epitaxy (MOVPE) [3,4], VPE [8], reactive rf sputtering [9] and gas-source MBE [10] had been studied in detail.
For its promising application to SAW filters operating at over 1GHz in wireless telecommuni-cation technology (where quartz with EMC of 0.14% is widely used) the interest in AlN has regained [11-16]. SAW properties of AlN/Al₂O₃ systems produced by sputtering [11], by VPE [12], MOVPE [13] and MBE [14] have been reported recently.
A step toward the fabrication of monolithic on-chip SAW devices is the growth of piezoelectric films directly on silicon. Little work has been published on AlN/Si SAW filters.

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High growth temperatures required by MOVPE (around 1200°C) hamper the cointegration into conventional wafer processing technology [1]. However, promising results have been achieved by reactive rf sputtering, where the AlN growth temperature could be decreased to below 500°C [11,15-17].

The SAW propagation loss is argued to be due to surface roughness and defects in the AlN film [1,11], reportedly even surface polishing had been necessary [1,4,12]. Whereas only IDT structures with finger periods p of some μm can be fabricated on rough AlN surfaces, structures in the order of 0.5μm can be realized on smooth films, which is a great merit in practical application [11,13]. For this motivation we have employed MBE to grow possibly smooth and defect free AlN films two-dimensionally on silicon. In this paper we present SAW properties of AlN obtained by this approach.

EXPERIMENT

The crystal growth has been carried out in a home-made three chamber MBE system, equipped with a standard Knudsen source for the evaporation of aluminum (6N purity), a rf plasma source (Oxford MPD 21) for the supply of activated nitrogen (6N purity) and a 10kV RHEED gun. The substrates have been cleaned following a modified Shiraki procedure [18] prior degassing at 920°C in the UHV environment. The growth process has been started by the deposition of 1/3 monolayer Al on the 7×7 reconstructed Si(111) surface at 700°C, as indicated by a transition to streaky 1×3 RHEED pattern [19].

Subsequently the growth temperature has been increased. The impinging Al flux has been controlled by maintaining streaky 1×1 RHEED pattern of the unreconstructed wurtzite AlN surface. N_2 flow rates between 0.75 and 1sccm, corresponding to nitrogen partial pressures between 0.75 and 1×10^{-5}mbar in the growth chamber, have been used. Samples with thicknesses between 0.2 and 1μm have been grown with the plasma source operating at 500W rf forward power, equivalent to a flux of N radicals to the substrate of ~1.8 to 2.4×10^{14}cm^{-2}s^{-1} [20].

AFM as well as cross-sectional TEM and HRTEM investigations have been carried out *ex situ* using Topometrix TMX-2010, JEOL JEM-1200 and JEM-4000 microscopes.

A 1040nm AlN film was grown with a growth rate of 3nm min^{-1} at 900°C under stabilization of 1×1 RHEED pattern and by using a N_2 flow rate of 1sccm. Aluminum IDTs of 100nm thickness with each 20 finger pairs and a finger period of 8μm were patterned on top. The delay line length was 2986μm.

RESULTS

First we have investigated the surface reconstructions occuring on AlN as function of Al flux and substrate temperature during the growth. N_2 flow rate and the rf power were both held constant.

At high nitrogen excess only spotty wurtzite RHEED pattern have been observed, reflecting three-dimensional (3D) growth of AlN. However, we observe 2D growth of AlN under reduced nitrogen excess, recognized by streaky 1×3 RHEED pattern. 2D 1×1 and 2×6 RHEED patterns become visible under further increase of the Al-flux [20]. Under continued increase of the Al-flux a decreasing RHEED intensity due to the formation of Al-droplets is observed. In Fig.1 the Al-flux required to stabilize the described surface reconstructions is plotted against the reciprocal growth temperature for a given flux of atomic nitrogen. From the slope of the dotted line we determine an activation energy for Al desorption of 1.3eV.
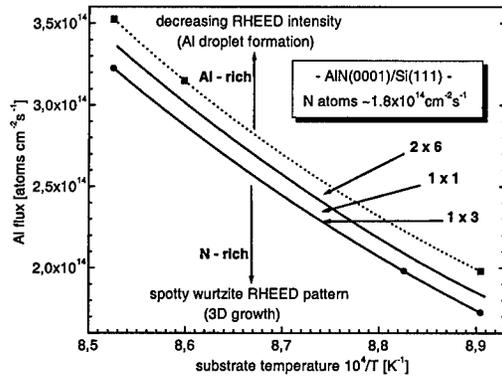
Fig.1 Phase diagram of surface reconstructions occuring in the growth of AlN(0001) on Si(111). The Al-flux Φ required to stabilize the Al-rich 2×6, the stoichiometric 1×1 and the N-rich 1×3 RHEED patterns is plotted as function of the inverse growth temperature T^{-1}. Plasma excitation (500W) and N_2 flow rate (0.75sccm) were held constant. The upper points, fitted by the dotted curve according to $\Phi/\Phi_o = \exp[E_A/k_B \, (T^{-1}- T_o^{-1})]$ yield an activation energy E_A for Al desorption of 1.3eV. Increasing the yield of atomic nitrogen by increasing the N_2 flow rate up to 1sccm leads to a shift of the phase transitions toward higher Al fluxes.

1×1 RHEED pattern represent best growth conditions. They are envisaged to indicate surface stoichiometry. Any deviation from the stable 2D RHEED patterns, namely the 1×3, the 1×1 and the 2×6 pattern, lead to the formation of Al-droplets or to 3D growth, respectively.

2D grown films exhibit atomically smooth surfaces (Fig.2 (a)). The films are void of oriented domains. The present defect structure consists of threading dislocations of mixed character (Fig.2 (b)). The interface between epilayer and substrate is abrupt and atomically flat. The misfit is accomodated within the very first monolayers on either side (Fig.3 (a)).

We explain 2D nucleation and growth in the present heterosystem by the reduction of the strain energy ϵ and the interface energy σ_i due to the occurrence of a magic lattice match [21,22] as suggested by Fig.3 (b). The misfit, given by $f(m,n)=(ma_s-na_e)/ma_s$, is $f=$ -0.013 taking an atomic arrangement of (4,5) into consideration. a_s and a_e are the lattice constants of the substrate and the epilayer, respectively.
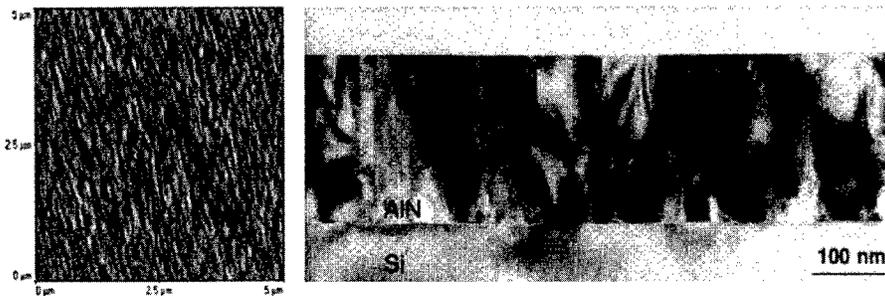
Fig.2 (a) Internal sensor AFM image of a 2D grown AlN film. The root-mean square roughness of the surface is 1.8Å (peak-to-valley height: 1nm). The residual wavy structure could not be resolved any further.
(b) Cross-section bright field TEM image of a 195nm 2D grown AlN film, taken along the [11$\underline{2}$] axis of silicon.
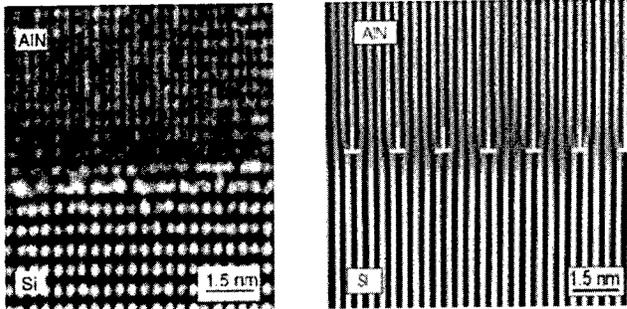
Fig.3 (a) HRTEM image taken at the heterointerface along the Si[11$\underline{2}$] axis. The blurred contrast in the interfacial region indicates misfit relaxation within the first monolayers on either side.
(b) Invers fourier transform of the 220 Si and 2110 AlN and reflections depicts the (4:5) atomic arrangement at the interface. Silicon introduces a step dislocation between each four unit cells of AlN.

The condition (1) for 2D nucleation in heteroepitaxial growth [23] merely depends on the free surface energies σ_s of Si and σ_e of AlN, as well as on the change of the chemical potential $\Delta\mu$ (where A is the basal plane size of the unit cell, G the shear modulus, ν Poisson's ratio and h the thickness of the nuclei), since:
1st, the interface energy σ_i is minimal where the lattice constants are in the ratio of small integers [24],
2nd, the strain energy $n\varepsilon$ (times the number n of lateral bonds in the growth plane) is nigligible in case of the small misfit $f(m,n)= -0.013$ ($\nu_{(0001)}$=0.366 [18], using the elastic constants as measured by Deger et al. [14] and the biaxial modulus [21]).

$$\sigma_s > \sigma_e + \sigma_i - (\Delta\mu - n\varepsilon) / 2A \tag{1}$$
$$\varepsilon = 2AG_{(0001)}hf^2 (1+\nu_{(0001)}) / (1-\nu_{(0001)}) \tag{2}$$
$$\Delta\mu = k_B T \ln(p_i/p_o) \tag{3}$$

Besides theoretical calculations [25] no experimental data about AlN surface energies are available. We observe, however, purely 2D nucleation of AlN with Al beam equivalent pressures p_i of the impinging Al atoms in the order of 10^{-7}mbar at 700°C substrate temperature. Hence (1) yields as a rough estimation of the free surface energy σ_e<2Jm^{-2}, using σ_s =1.2Jm^{-2} [19] and Al vapor pressure values p_o given in [26,27].

The propagation of Rayleigh waves along the AlN surface has been investigated. Time and frequency response have been measured. The EMC as well as the phase velocity of the SAW have been compared with theoretical predictions. Defined by the IDT geometry we have worked with an acoustic wavelength of 16µm, which is twice the value of the finger period p. This corresponds to a center frequency of 286MHz and a SAW phase velocity of 4569ms^{-1} propagating along the [2110] direction. The EMC of 0.07% stands in good agreement with the predicted ideal value. It hence confirms the excellent piezoelectricity of the crystal, viable for application to SAW filters.
From the fact that the transmitted time response signal is very distinct from the background, we conclude that the SAW experiences low scattering along its way. The occurrence of relatively strong parasitic frequencies in the frequency response might be due to film thickness fluctuations. They may cause distortions of the SAW wavefronts along their path of propagation, which is nearly 3mm. The frequency characteristic is not yet as good as achieved in AlN/Al$_2$O$_3$ systems, recently [13,14]. In comparison with sputtering [16], it means, however, improved SAW properties obtained on silicon under our experimental conditions.
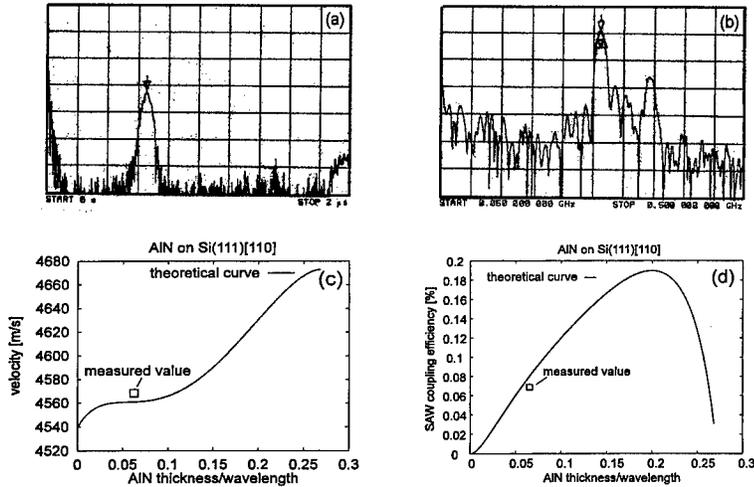
Fig.4 (a) Time response of the SAW filter (y-scale: 10dB/div.), recorded between $t=0$ and $2\mu s$ (200ns/div., marker at 653.5ns). The excellent distinction between signal and background by nearly 40dB indicates low scattering of the waves. The signal at $t=0$ is due to the electromagnetic crosstalk.

(b) Frequency response of the SAW filter (y-scale: 10dB/div.), recorded between $f=50MHz$ and $500MHz$ (45MHz/div., marker at 285.57MHz).

(c,d) The measured values of the SAW phase velocity v and the EMC in $AlN(0001)[2\bar{1}\bar{1}0]/Si(111)[110]$ agree well with theoretical predictions using $c_{11}=345$, $c_{12}=125$, $c_{13}=120$, $c_{33}=395$, $c_{44}=118GPa$, $e_{31}=-0.58$, $e_{33}=1.55$ and $e_{24}=-0.48Asm^{-2}$ [1,2] and confirm the good piezoelectricity of the $h=1040nm$ AlN film.

(c) SAW phase velocity vs. h/λ.

(d) EMC vs. h/λ. Ideal adaption with an EMC of 0.19% is predicted for $h/\lambda=0.2$, corresponding to $\lambda=5.2\mu m$, $v=4630ms^{-1}$, and $f=890MHz$.

CONCLUSIONS

Wurtzite AlN thin films can be nucleated two-dimensionally on clean, 7×7 reconstructed Si(111) surfaces by means of plasma-assisted MBE. 2D growth of AlN under N-rich conditions is indicated by streaky 1×3 RHEED pattern. Growth under conditions of surface stoichiometry is indicated by streaky 1×1, and Al-rich conditions by 2×6 pattern. We have determined the activation energy of Al desorption to be 1.3eV between 850 and 900°C.

The films are atomically smooth and free of oriented domains. An atomic (4,5) arrangement at the heterointerface along the $Si[\underline{1}10]/AlN[\underline{2}110]$ direction is argued to be responsible for the reduction of the interface energy σ_i and the strain energy $n\epsilon$ alike, enabling 2D nucleation at high supersaturation p_i/p_o. The free surface energy of the AlN growth plane is estimated to be lower than $2Jm^{-2}$.

MBE is a feasible technique to produce piezoelectric III-nitride films on silicon substrates. We have successfully demonstrated the propagation of SAW in AlN grown 2D on Si(111) by MBE. The AlN film shows very good piezoelectricity, viable for device application. The time response of Rayleigh-type SAW shows low scattering of the waves during propagation.

ACKNOWLEDGEMENTS

117

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Part IV

Bonding, Devices and Back-End Processing

PHOTONIC BANDGAP FORMATION BY WAFER BONDING AND DELAMINATION

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ABSTRACT

A new approach for one-dimensional photonic bandgap formation is introduced. The method consists of wafer bonding and delamination, which is capable of stacking single crystalline semiconductor layers on non-crystalline insulator layers. Si and SiO_2 layers with sub-wavelength periodicity are successfully stacked to form photonic crystals consisting of 3 pairs without a defect layer and of 4.5 pairs with a defect layer. The transmittance spectra are well reproduced by transfer matrix calculations. This clearly verifies the potential of the wafer bonding and delamination method.

INTRODUCTION

Photonic bandgap (PBG) attracts considerable attention from many aspects of photon manipulation in otherwise impossible ways and is on the point of revolutionizing the industrial world. Since the concept proposal in 1987[1], various ideas have been proposed such as low threshold laser diodes, 90 degree bending of wave guides with no loss, one dimensional PBG wave guides, and so on.[2] Thus, the impact of PBG is expected not only to establish new devices but to open an entirely new field to be referred to as "microphotonics".[3] The present paper describes physics and applications of PBG and especially focuses on PBG formation based on Silicon on Insulator (SOI) structures.

PHOTONIC BANDGAP

It is well known that minigaps are generated in dispersion relation of electrons in "electronic" bandgap of semiconductors with modulated structures. Figure 1 shows typical examples of modulated structures, i.e., multi-dimensional superlattices. Since photons have been known as electromagnetic waves prior to the proposal of matter waves by de Broglie, it is rather natural that such modulated structures could generate bandgaps in a dispersion relation of photons. The bandgap is referred to as photonic bandgap.

1-Dimension   *2D*   *3D*
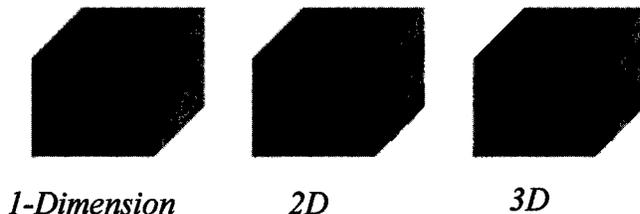
Figure 1 Photonic Crystals

Refractive indices are the subjects to be modulated and the modulated structures are referred to as photonic crystals shown in Fig.1. Figure 2 shows schematics of PBG in one-dimensional photonic crystals of semiconductors and air. It is recognized that PBG is generated to be ΔE in energy at the edge of the Brillouin Zone. This indicates that the presence of photons is forbidden in 3-dimensional structures if the photon energy corresponds to the PBG. The bandgap is proportional to the difference between the
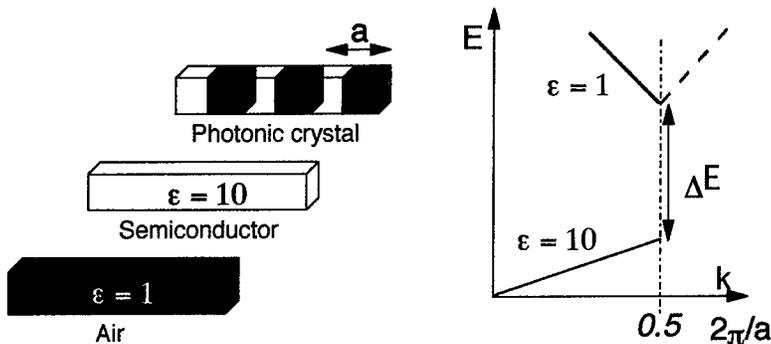
Fig. 2 One dimensional photonic crystal and photonic bandgap

refractive indices (n) of periodic dielectrics. This is why combination of semiconductors ($n = \sim3.5$) and insulator ($n = \sim1.5$) is frequently used for attaining a large PBG.

In electronic materials, defects play important roles to function the materials. Shallow donors and acceptors are typical examples. This is also true in photonic crystals. Defects in photonic crystals are local disorders in periodicity of refractive indices. A typical example is shown in Fig. 3. Photon localization and evanescence at the defect introduces filter functions in PBG. This is identical to resonant electron tunneling in electron devices. Recently, 1-D PBG wave-guides have successfully been realized by using a Si on insulator (SOI) substrate with

Waveguide   defect
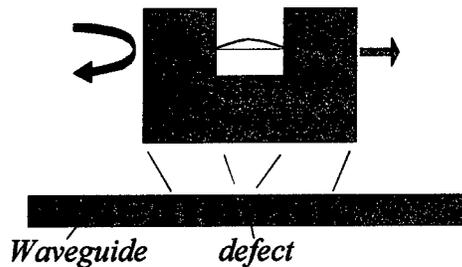
Figure 3 One dimensional photonic crystal. Photon localization at defect

insulator (SOI) substrate with a defect and demonstrated a filter with an ultra-small dimension and a high Q factor.[3] Because of weak interaction of photons with matters, such functions featuring PBG are independent of system temperatures, which is also very different from the functions of electronic nano-structures. Finally, it is worth mentioning

that radiative recombination of electrons and holes should be entirely suppressed if electronic bandgap lies within PBG in energy. Thus, defects in photonic crystals act as radiative recombination channels as well as localize states of photons. This suggests that band engineering considering both electronic materials and photonic crystals will be a fundamental issue for future materials science and device physics.

MATERIALS ISSUES

In order to utilize excellent features of photonic crystals, it is quite important to control qualities of the periodic dielectrics. Combination between semiconductors and insulators (including air) is a most feasible material choice for photonic crystals as noted above. This material choice increases coherency of technologies between electronics and "microphotonics". However, the choice also makes it difficult to obtain high quality semiconductors in between insulators. In other words, if the periodic dielectrics are fabricated by deposition techniques, it is quite difficult to get the semiconductor layers without grain boundaries and dislocations. This is a new challenge in material science.

In the present paper, wafer bonding and delamination techniques are applied to fabricate PBG. PBG essentially free of grain boundaries and dislocations is realized.

WAFER BONDING AND DELAMINATION

The quality of these layers should be electronic- and optoelectronic device grades. In order to meet such requirement as well as accurate thickness control, we have chosen the technique called "SmartCut®".[4] This is the technique developed for fabrication of silicon on insulator (SOI) substrates and basically consists of wafer bonding and delamination; here referred to as WB/D method. The procedure to form stacking structures of several Si/SiO$_2$ pairs is following:
1. Preparation of Substrate A with an SiO$_2$ layer implanted hydrogen, and Substrate B,
2. Wafer bonding of Substrate A on Substrate B,
3. Delamination of the Si surface layer of Substrate A, leaving the Si/SiO$_2$ layer pair on Substrate B,
4. Touch-polishing of the surface Si layer,
5. The procedures 2) to 4) repeated by using new Substrate A.

The method can provide surface layers of CZ silicon wafers as Si layers, and thermally grown SiO$_2$ as the dielectrics, i.e., Si-LSIs grade. The WB/D method is capable of precise thickness control of the Si layers in terms of hydrogen implantation energy. The SiO$_2$ layer thickness was also precisely controlled by thermal oxidation. These features are adequate for PBG fabrication.

ONE DIMENSIONAL PHOTONIC CRYSTALS
Photonic crystals without defect.

Figure 4 shows the periodic dielectrics of Si and SiO$_2$ by the WB/D method.[5] In clear contrast to deposited and annealed Si/SiO$_2$ structures, no grain boundaries are observed in the scanning reflection electron micrograph image. The transmittance spectrum shows clear PBG in the wavelength region of 3000 and 4500 cm^{-1}. The arrows show the bonded interfaces. Calculation based on transfer matrix method has indeed predicted the PBG in this region.

This indicates that the WB/D method is applicable for fabrication of Si/SiO$_2$ periodic dielectrics.
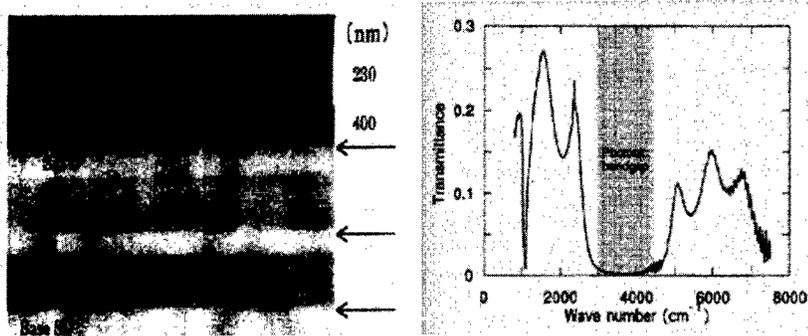
a) Reflection Electron Micrograph   b) Transmittance

Fig. 4 One dimensional photonic crystals by the WB/D method

Photonic crystals with defect.

In order to introduce a defect layer in PBG, defect states are calculated in Si/SiO$_2$ periodic dielectrics. Here, the defect layers ranges from 0 to 450 nm in thickness. As shown in Fig. 5a) the calculation clearly shows that midgap states would be also formed in PBG with a thinner defect as well as that with a thicker defect shown in Fig. 5b). It should be noted that photons are mainly confined in low refractive index layers next to the defect in the PBG with thinner defect layers. In other words, photons are confined in SiO$_2$ layers. In thick defect layers, photons are confined in high refractive index layer, i.e., defect layer. Thus, another application could be expected. In order to verify the prediction, PBG with a thinner defect is fabricated. Figure 6 shows cross-sectional transmission electron micrograph of the periodic dielectrics. The thin defect layer, 45 nm thick, is clearly visualized. It is rather surprising that 45 nm thick layer has been achieved by the WB/D method. This verifies the potential of the WB/D method.

CONCLUSION

The concept and impact of photonic crystals are briefly explained. The material issue is described in obtaining high quality of PBG as well as electronic bandgap. The wafer bonding and delamination method is applied for PBG fabrication. PBG with and without a defect are fabricated. These successfully form PBG free of grain boundaries and dislocations, verifying unique features of the method. The PBG quality is esentially the same as Si-LSIs. The method will allow us to integrate electronics and "micro-photonics"
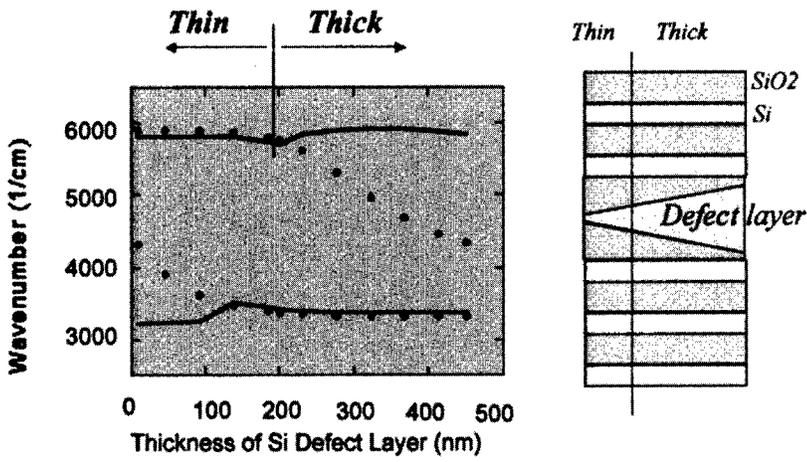
a) Defect states v.s. layer thickness   b) Structure

Figure 5 Calculation of defect states in Si/SiO$_2$ photonic crystals

The dots in Fig. 5a) are results of calculation for various thickness of defect layers as schematically shown in Fig.5b). The lines correspond to the air band and dielectric band.

Figure 6 Cross sectional transmission electron micrograph of Si/SiO$_2$ photonic crystals. The light layers are Si and the dark layers are SiO$_2$. The defect layer is 45 nm thick.

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A MODEL OF WAFER BONDING BY ELASTIC ACCOMMODATION

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ABSTRACT

Two clean and flat wafers can adhere spontaneously. The technique has recently led to novel electronic and optoelectronic devices. The adhesion arises from short-range interatomic forces between wafer surfaces, which can be represented by a reduction in surface energy associated with the transformation of two surfaces into one interface. The wafers, however, are seldom perfectly flat; the misfit has to be accommodated by elastic distortion, plastic deformation, or mass transport. We model elastic accommodation in this paper. The distortion causes the wafers to gain elastic energy. If the surface energy reduction dominates over the elastic energy gain, the wafers will bond. We solve the three dimensional elastic field in the misfit wafers analytically. The conditions for bonding are established, and practical implications discussed.

INTRODUCTION

Two clean and flat wafers can adhere spontaneously at room temperature. If heated for sometime, they would unite to a single piece, which could not be separated without breaking the bulk. The technique has recently been developed to bond semiconductor wafers, leading to electronic and optoelectronic devices of much superior performance; see [1] for a list of examples. The main advantage of the technique is that it can integrate dissimilar materials while retain their crystalline perfection—that is, if one or both wafers are perfect crystals before contact, the perfection is retained after bonding, except for a few atomic layers at the interface.

The basic cause for bonding is the attractive interatomic force between two surfaces. Being short ranged, the force acts like a zipper: the adhesion starts from one point of initial contact, and spreads over a macroscopic area. The effect of the force can be represented by surface energies. Let γ_1 and γ_2 be the surface tensions of the two wafers before bonding, and γ_{12} be the interface tension after bonding. Provided the sum of the two surface tensions exceeds the interface tension, $\gamma_1 + \gamma_2 > \gamma_{12}$, when the two surfaces unite to form the interface, the net free energy reduces. It is this reduction, known as the Dupré work of adhesion,

$$\Gamma = \gamma_1 + \gamma_2 - \gamma_{12}, \tag{1}$$

that motivates bonding. The necessary condition for the two wafers to adhere, $\Gamma > 0$, can often be satisfied after surface treatment.

Yet the two solid surfaces never match perfectly. The surface misfit can be accommodated by mass diffusion or viscous flow at an elevated temperature, or by plastic deformation at a low temperature. However, the above procedures have limitations. Heat treatment may induce high residual stresses upon cooling or even destroy dopant profile in semiconductors. When both wafers are brittle, as semiconductors are, plastic accommodation is impossible. On such occasions, one has to join wafers without the aid of intense heat or large force.

For wafers to bond at the low temperature, in the absence of large external pressure, the misfit gap between the wafers must be accommodated by elastic distortion. Prior to contact two wafers are not perfectly flat. Once brought together, they contact at a few points first. In this

127

state, the total surface area is large, and so is the free energy. To reduce the free energy, the wafers deform elastically and transform the two surfaces into one interface. If the misfit is large, the wafers gain too much elastic energy, and will bond only over patches of the surface area, leaving the rest of the area unbonded. If the misfit is small, the wafers gain a small amount of elastic energy, and will bond over the entire area. This paper analyzes the elastic field in the misfit wafers, and establishes bonding conditions.

THE MODEL

Tong and Gösele [2, 3] considered the effect of elasticity on wafer bonding. They gave expressions of bonding conditions in the limits of very thin and very thick wafers. In this paper, we will analyze the model of Tong and Gösele [2, 3] in full ranges of parameters. With reference to Fig. 1a, the interface is nominally perpendicular to the z direction, and the misfit gap is taken to be sinusoidal in both the x and y directions. Figure 1b sketches a cross section of the joint, where for clarity the ratio H/L has been greatly exaggerated. The solid curves represent the surfaces before bonding, with the sinusoidal gap of wavelength L and amplitude $2H$. The dotted curve represents the interface after bonding. The upper wafer, wafer 1, has Young's Modulus E_1, Poisson's ratio v_1, and thickness t_1. The corresponding values for the lower wafer are E_2, v_2, and t_2.

We assume that the wafers will bond over the entire area if the elastic energy gained in closing the gap is less than the surface energy reduction. The following dimensional considerations reveal several main features of the problem. For the time being we consider the case where the misfit wavelength is much smaller than the thickness of either wafer, $L \ll t_1$ and $L \ll t_2$. Consider one period of the bonded wafers, namely, a column of material normal to the interface, of a square cross-sectional area L^2. After bonding, the misfit induces an elastic strain field of magnitude scaled as H/L; the larger the gap height and the smaller the wavelength, the
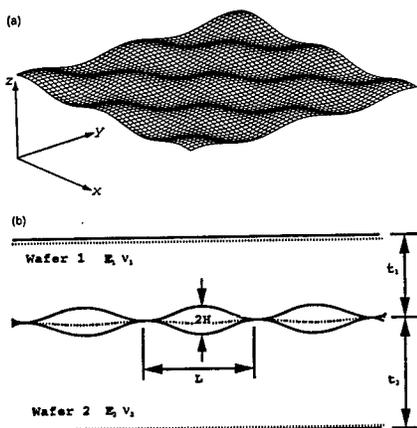
Figure 1(a) The misfit gap varies sinusoidally in the plane of the interface. (b) The geometry of a cross section normal to the interface. Solid lines: unbonded and undeformed configuration. Dotted lines: bonded and deformed configuration.

larger the strain. The elastic energy per unit volume scales as $E^*(H/L)^2$, where E^* is an appropriate elastic modulus. Under the assumption that $L \ll t_1$ and $L \ll t_2$, the stress field is localized near the interface, and decays in the z direction beyond the length scale L. Consequently, the elastic energy per period of the bonded wafers, U, scales as

$$U \propto E^*(H/L)^2 L^3 .$$

The surface energy reduction per period of the joint is ΓL^2. The dimensionless ratio of the two energies is

$$\eta = \frac{E^* H^2}{\Gamma L} . \tag{2}$$

When the ratio is below a critical value, denoted as η_c, the wafers will bond over the entire area. When the ratio is above the critical value, the wafers will bond over patches of the area. The analysis in a later section will show that $\eta_c = 3.60$ for thick wafers. Taking representative values, $\Gamma = 1\,\mathrm{N/m}$ and $E^* = 10^{11}\,\mathrm{N/m}^2$, one concludes from (2) that, for example, when $L = 10$ μm, $2H_c = 38$ nm is the largest gap height that can be accommodated by elasticity. When $L = 1$ mm, $2H_c = 380$ nm. Complete bonding is more likely for wafers with low elastic moduli, small misfit height, large misfit wavelength, and large Dupré work of adhesion. Also note that the absolute length scale of the misfit is important: for two geometrically similar gaps (i.e., having an identical ratio H/L), the gap with a smaller length scale is more likely to bond completely.

ELASTIC FIELD

The ratio H/L is taken to be so small that the linear elasticity theory applies. We solved the elastic fields in two wafers analytically. Here we highlight the main features of the solution; the solution procedure and the complete results can be found in [4].

Examine the stress component σ_{zz}. The stress varies periodically in the x and y directions, and decays exponentially in the z direction. The maximum is at the middle of the gap, where the mismatch has the largest value. Figure 2 displays the stress magnitude, $(\sigma_{zz})_{max}$, for wafers of various thicknesses, assuming that the two wafers having similar elastic modulus and equal thickness t. Noting the normalization group, the stress is proportional to the amplitude of the sinusoidal misfit. For a fixed wavelength, the stress increases with the wafer thickness, and reaches plateau when the wafers are sufficiently thick, say, $t/L > 0.5$, corresponding to the case analyzed in THE MODEL. If the both wafers are thick, the magnitude of the maximum stress is

$$\left(\sigma_{zz}\right)_{max} = \frac{\sqrt{2}\pi H \overline{E}_1 \overline{E}_2}{L(\overline{E}_1 + \overline{E}_2)} , \tag{3}$$

where $\overline{E} = E/(1-\nu^2)$. Taking the representative values, $\overline{E}_1 = \overline{E}_2 = 10^{11}\,\mathrm{N/m}^2$, one finds the magnitude of the stress to be 222 MPa when $H/L = 10^{-3}$. The stress magnitude is linear in H/L.
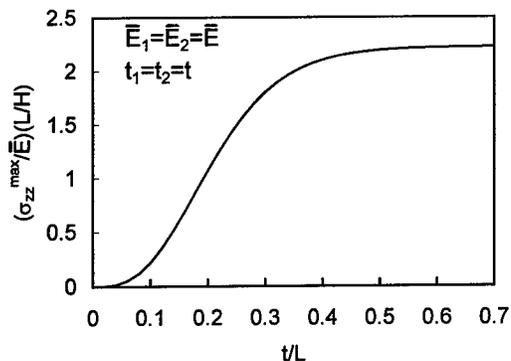
Figure 2 Magnitude of the stress on the interface.

We also examined wafers with dissimilar elastic modulus and thicknesses. Assume wafer 2 is thicker than wafer 1, $t_2 > t_1$. When wafer 2 is stiffer than wafer 1, the thickness of wafer 2 has negligible effect on stress. When wafer 1 is stiffer than the wafer 2, the thickness of wafer 2 can have appreciable effect on stress.

CRITICAL CONDITION FOR BONDING

The elastic energy stored in the two wafers after complete bonding can be computed by the work done by σ_{zz} at the interface to close the misfit gap. Denote the elastic energy per period of the joint by U. When the two surfaces transform into one interface, the free energy per period of the joint changes by $U - \Gamma L^2$. Complete bonding occurs if this free energy change is negative, namely,

$$U - \Gamma L^2 < 0. \tag{4}$$

By computing U from the elastic solution, we find the critical condition for bonding. The general expression of the bonding condition with full range of parameters can be found in [4].

Consider the limit where the two wafers both are thick relative to the misfit wavelength, $L \ll t_1$ and $L \ll t_2$. If the elastic constants of the two wafers are identical, the bonding criterion is simplified to

$$H_c = 1.90 \left(\frac{\Gamma L}{\bar{E}} \right)^{1/2}. \tag{5}$$

Here $2H_c$ stands for the critical misfit amplitude. If the misfit amplitude is above the critical value, the two surfaces will only bond over patches of the area, and the bonding is not complete. This result has the same form as that given by Tong and Gösele [2, 3], except for the coefficient.
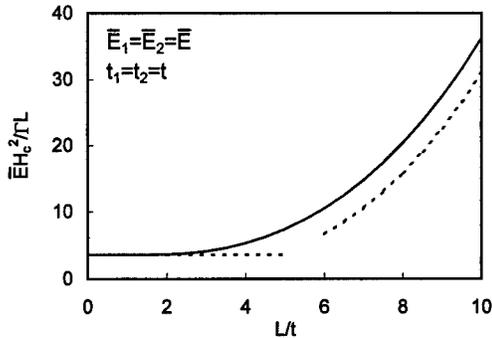
Figure 3 The critical conditions for the wafers to bond over entire area. Two dashed lines correspond to the approximation (5) and (6) for two limiting cases.

Next consider another limit where the two wafers are thin and identical, i.e., the thickness, $t_1 = t_2 = t$, is much smaller than the misfit wavelength, $t \ll L$. The bonding condition is simplified to

$$H_c = 0.176 \sqrt{\frac{\Gamma L^4}{\bar{E} t^3}} .$$ (6)

The result is the same as that given by Tong and Gösele [2, 3], who derived it by using the thin plate theory .

Figure 3 displays the critical bonding condition as a function of the reduced misfit wavelength, L/t, for two identical wafers. Judging from the figure, it is evident that the short wavelength limit, eqn. (5), is a good approximation if, say, $L/t < 2$. Everything else being equal, thinner wafers are easier to bond. We also checked the effects of the relative thickness, and of elastic modulii of the two wafers. When the thinner wafer is less stiff, the thickness of the thicker wafer affects bonding negligibly. The thickness of the thicker wafer affects bonding significantly only when the thinner wafer is very stiff.

DISCUSSION

Surface geometry aside, surface chemistry plays an important role. The Foreign molecules usually adsorb on wafer surfaces, and lower the work of adhesion. Obreimoff [5] observed that a smaller force could split mica in air than in vacuum. An "optical contact" formed in the air at room temperature most likely arise from van der Waals or other weak bonds between the adsorbed molecules. Heat treatment can activate reactions at the interface to convert the weak bonds into strong bonds. Stengl et al. [6] discussed in some details such interfacial reactions in silicon wafer bonding. At room temperature water molecules adsorbed on the surfaces form hydrogen bonds. At about 700°C, the water molecules diffuse away from the interface, and strong Si-O-Si bonds form. Using a double-cantilever-beam fracture specimen, Maszara et al. [7] measured the work needed to separate a pair of silicon wafers (i.e., the work of fracture) as a function of annealing temperature. The work of fracture increases with the annealing temperature even when temperature is too low to activate viscous flow. The data clearly show

the role of interfacial chemical changes on wafer bonding. The model discussed in the present paper does not specify the type of bonding, so long as the work of adhesion is positive. The effects of the chemical changes on the surfaces enter the model through the value of the work of adhesion.

Two points are of practical significance. First, the temperature of heat treatment in wafer bonding is set by the chemical change on the interface. The temperature to activate the interfacial reactions may be much lower than that to activate mass transport to match the geometry. Thus, if before contact two wafers are polished so flat that elasticity will accommodate the misfit, one should expect that the wafers would attain a strong bond at a low temperature. Second, procedures may be applied to the wafers before contact to activate the surfaces, namely, remove molecules that prevent strong bonds. For examples, placing wafers in ultrahigh vacuum [8]. Immediately after "surface activation", the wafers can be placed together to form strong bonds at room temperature.

CONCLUDING REMARKS

Two wafers can adhere spontaneously if (a) the Dupré work of adhesion is positive, and (b) the shapes of the two surfaces sufficiently match. The work of adhesion can be modified by chemical reactions at the interface. When one has to bond wafers without the aid of mass transport or plastic flow, elastic distortion may accommodate a small amount roughness. For a given misfit wavelength, we give the maximum misfit height that can be accommodated elastically. The stress field in the bonded wafers due to misfit is localized near the interface, in a region of a thickness scaled with the misfit wavelength. The model does not specify the bonding type. Consequently, it applies to all the variations of the wafer bonding technique, including optical contact formed at room temperature due to van der Waals or other weak bonds, strong bonds formed at the room temperature after "surface activation" prior to bonding, and strong bonds obtained by changing weak bonds at a moderate temperature where mass transport is negligible. Furthermore, intentionally patterned misfit may lead to novel devices, where the interplay of adhesion and elasticity should play an equally important role. In this connection, it would be useful to analyze the extent of bonding when the surfaces do not bond completely.

ACKNOWLEDGMENT

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INTEGRATION OF SILICON AND DIAMOND, ALUMINUM NITRIDE OR ALUMINUM OXIDE FOR ELECTRONIC MATERIALS

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ABSTRACT

Material integration for the formation of advanced silicon-on-insulator materials by wafer bonding and etch-back will be discussed. Wafer bonding allows combining materials that may not be possible to grow on top of each other by any other technique. In our experiments, polycrystalline diamond, aluminum nitride or aluminum oxide films with thickness of 0.1-5 μm were deposited on silicon wafers. Bonding experiments were made with these films to bare silicon wafers with the goal of forming silicon-on-insulator structures with buried films of polycrystalline diamond, aluminum nitride or aluminum oxide. These silicon-on-insulator structures were aimed to address self-heating effects in conventional silicon-on-insulator materials with buried layers of silicon dioxide. The surfaces of the deposited diamond films were, by order of magnitude, too rough to allow direct bonding to a silicon wafer. In contrast the deposited aluminum nitride and aluminum oxide films did allow direct bonding to silicon. Bonding of the diamond surface to silicon was instead made through a deposited and polished layer of polycrystalline silicon on top of the diamond. In the case of the aluminum nitride electrostatic bonding was also demonstrated. Further, the compatibility of these insulators to silicon process technology was investigated.

INTRODUCTION

Wafer bonding [1] is a versatile technique for forming solid-state structures. Two pieces of material that may be pre-processed are brought into intimate contact. If the surfaces of the materials are clean and smooth enough they will stick to each other. A subsequent annealing step stabilizes the bonded interface and increases its mechanical strength. Within silicon technology wafer bonding has been used for formation of silicon-on-insulator (SOI) materials [2,3], power devices [4] and sensors [5]. Wafer bonding has also been used with other materials than silicon, such as III-V semiconductors [6]. In principle, wafer bonding is possible with any material having smooth and clean enough surface. The method thus opens possibilities of combining materials not possible to grow on top of each other by any other means. In this paper we will summarize bonding experiments aiming at fabricating novel SOI materials by bonding of silicon to electrically insulating films exhibiting high thermal conductivity. We have studied bonding of aluminum nitride [7,8], aluminum oxide [9,10] and polycrystalline diamond films [11]. Further, we have investigated the compatibility of these materials to silicon device manufacturing.

Currently, SOI materials receive increasing attention for mainstream CMOS as well as for high frequency and high voltage applications [12]. The advantages of SOI come from dielectric isolation, process simplifications and better device performance and reliability [3,12]. On the other hand, concerns are the availability and cost of the SOI wafers as well as the floating body effect and the low thermal conductivity [3,13] of the buried silicon dioxide film. In applications where high power dissipation is expected, it is found that self-heating in the devices limit the applicability of SOI. This may occur in bipolar devices where high local current densities, for instance at emitter fingers, cause device instability if the heat spreading is insufficient. [13,14]. The use of a buried insulator with good thermal conductivity can improve the performance.

Several materials with interesting properties are available. Both diamond and aluminum nitride (AlN) are wide bandgap semiconductors exhibiting high electrical resistivity combined with high thermal conductivity. Also aluminum oxide (Al_2O_3) exhibits high thermal conductivity as compared to silicon dioxide and the material has been used in silicon technology for a long time in the form of sapphire (silicon-on-sapphire materials). In Table I some properties of silicon, silicon dioxide, polycrystalline diamond, aluminum oxide and aluminum nitride are summarized.

TABLE I. Properties of silicon, silicon dioxide, polycrystalline diamond and aluminum nitride.

Property	Si	SiO_2	Diamond	Al_2O_3[2]	AlN
Bandgap (eV)	1.1	9	5.5	7	6.2
Dielectric constant	11.9	3.9	5.7	9.3	9.1
Thermal conductivity (W/Kcm) at RT	1.5	0.015	15[1]	0.3	1.5

[1] Single crystal diamond. [2] Sapphire.

INSULATOR DEPOSITION

Bonding experiments was made with the goal of forming silicon-on-insulator structures with buried highly thermally conductive insulators. The formation of the SOI structures by a wafer bonding and etch-back procedure using wafers with buried etch-stop layers is outlined in figure 1.

Polycrystalline diamond films were deposited on 100 mm silicon wafers by hot filament chemical vapor deposition [15]. The thickness of the deposited diamond layers were about 3-5 μm. The silicon surface was prepared for diamond deposition using different seeding procedures, which involved abrasive treatment by a diamond powder or deposition of diamond growth seeds on the silicon surface. For the diamond deposition an ambient of 1-2% of CH_4 in H_2 and a substrate temperature of 650-750° C were used. Other process parameters were a pressure of 4000-6500 Pa, a filament temperature of 2100-2200° C and a distance between the filament and the wafer of 1 cm. Cross section scanning electron microscope images of the as deposited diamond layers showed a columnar grain structure with an average diamond grain size of less than 1 μm.

Aluminum nitride films were deposited on 3" and 100 mm silicon wafers by reactive sputtering. A 6" aluminum target of 99,999% purity clamped to a water-cooled copper cathode was used for DC magnetron sputtering. Aluminum nitride films with thickness ranging from 100 nm up to almost 2 μm were deposited. For the deposition a pressure of 0.5-1.4 Pa, an argon flow of 40 sccm, a nitrogen flow of 10 sccm, a target power of 450 W (2.5 W/cm^2), a substrate to target distance of 6.5 cm and a substrate power of 100 W (40 mW/cm^2) were used. To improve the surface smoothness, both the target power and the substrate power were decreased in two steps during the latter part of the deposition procedure. Refractive indices in the range of 1.95 to 2.20 were obtained using ellipsometry, confirming that the films consist of aluminum nitride.

Aluminum oxide (Al_2O_3) films were deposited on 3" silicon substrates using Atomic Layer Epitaxy (ALE) [16]. ALE is a digitally controlled layer-by-layer deposition method for the production of compound thin films with atomic layer accuracy. In an ALE process, mutually reactive percursors are presented sequentially to a substrate surface held at an elevated temperature. Within a given temperature range, the surface chemisorbs one saturated layer of the precursor. When the next mutually reactive precursor is introduced to the surface, an exchange reaction occurs where the ligand of the first precursor is exchanged with the missing component of the compound. Thus at each reaction sequence an atomic layer of the thin film is attached to the surface. For the Al_2O_3 deposition Tri-Methyl-Aluminum (TMA) and water vapor were used as reactive gases. The deposition temperature was in the range of 250-400° C and the duration of each gas pulse was 0.2-3 s. A preliminary study of the deposited films using X-ray diffraction shows that that the as-deposited films were amorphous. However, some crystallization occurred during a post-deposition anneal at 900° C for 30 minutes.

WAFER BONDING

The wafer bonding and etch-back procedure to form an SOI material is shown in figure 1. Characterisation of the bonded structures was made by use of transmitted infrared (IR) light for detection of non-bonded areas and by use of the crack opening method introduced by Maszara et al [18] for determining the surface energy of the bond.
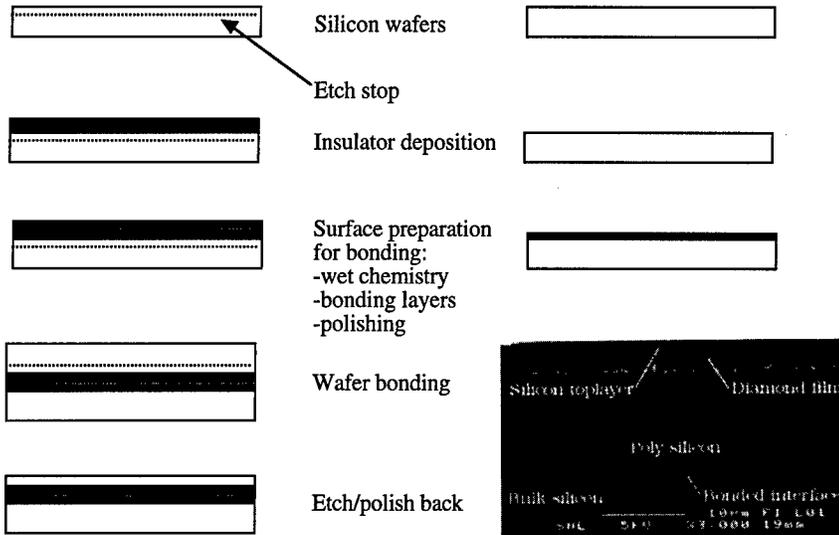
Figure 1. Formation of SOI materials by wafer bonding and etch-back. A cross-section SEM image of the SOI structure with a buried diamond film is shown.

For successful bonding the deposited films must exhibit low stress and low surface roughness. Atomic Force Microscopy (AFM) was used to characterize the surface roughness. The AFM (Parc Scientific Instruments SFM-BD2-210) operates at room temperature under a flow of dry nitrogen gas. The instrument was used in the contacting mode, wherein the sample acts to deflect the Si_3N_4 tip and cantilever by a repulsive force. The tip was scanned across areas ranging from 0.2x0.2 μm to 10x10 μm. Surface micro-roughness of the order of 10 Å or less is required for direct bonding. The rms roughness for a polished silicon wafer is of the order of 0.5 Å. In figure 2 AFM scans obtained for diamond, aluminum nitride and a fresh silicon surface are shown. To summarize the results, the surfaces of the deposited polycrystalline diamond films were, by order of magnitude (see figure 2), too rough to allow direct bonding to a silicon wafer while the deposited AlN and Al_2O_3 films did allow a direct bonding.

The rms roughness value obtained for the diamond films (10x10 μm scan area) is of the order of 100 Å. In addition, the diamond film showed a small number (~10 per 100 mm wafer) of very distinct diamond peaks raising approximately 10 μm above the surrounding film. An obvious solution to the problem would be to polish the diamond surface to a smooth bondable finish, but this approach requires non-standard manufacturing equipment [17] and is under all circumstances difficult. Instead a thick (~15 μm) polycrystalline silicon layer was deposited on top of the diamond film [11]. The polycrystalline silicon surface was polished using chemical-mechanical polishing to prepare a smooth surface. This surface was bonded to another silicon wafer followed by lapping, etching and polishing of the silicon wafer onto which the diamond film was deposited to obtain the device layer, as is outlined in figure 1. Both the silicon surfaces were made

135

hydrophobic by dipping in a diluted HF solution followed by a water rinse before wafer bonding. Surface energies above 1 J/m^2 was achieved after annealing at 1000° C. In figures 1 and 3a the resulting structure is shown. Also with the polycrystalline silicon layer as a bonding medium we encountered bonding problems and void generation. Furthermore, in some early runs of diamond deposition the diamond films were highly stressed, severely warping the silicon wafer. By tuning the seeding procedure as well as the deposition parameters the stress problem was reduced.
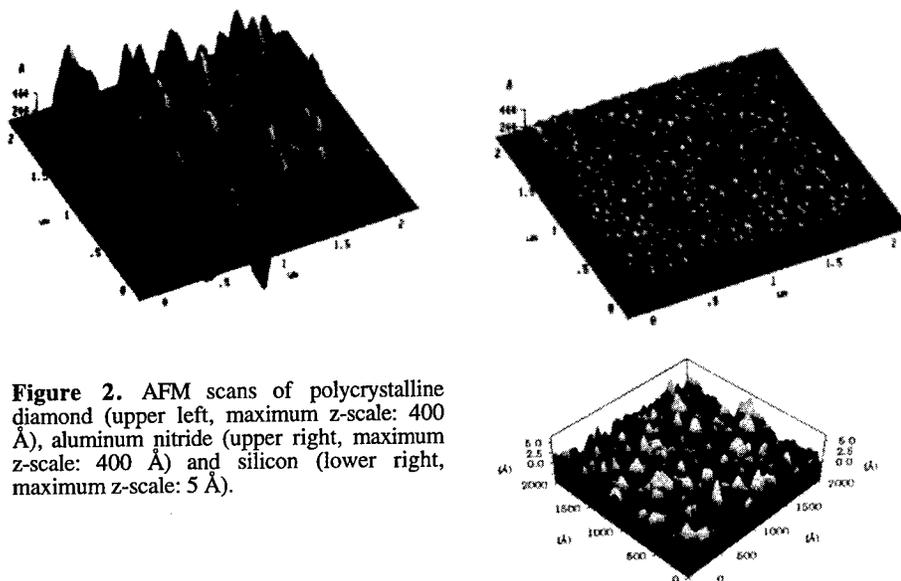
Figure 2. AFM scans of polycrystalline diamond (upper left, maximum z-scale: 400 Å), aluminum nitride (upper right, maximum z-scale: 400 Å) and silicon (lower right, maximum z-scale: 5 Å).

Both direct bonding and electrostatic bonding experiments were made using the aluminium nitrid films. Films used for the experiments exhibited low stress and surface roughness corresponding to rms values about or lower than 1 nm (0.2x0.2 μm scan area). Such surfaces are possible to bond directly to silicon without polishing. In these particular experiments the aluminium nitride surface was rinsed in deionized water and blown dry in nitrogen before bonding. The silicon wafer was cleaned in an APM solution of 1:1:5 NH$_4$OH:H$_2$O$_2$:H$_2$O at 70 - 80° C for 10 minutes followed by water rinsing and drying. The surface of the aluminium nitride was contacted to the silicon wafer and a slight pressure was applied using a pair of tweezers. Using this procedure a weak room temperature bond formed. Some bonded structures were annealed at 800° C for 30 minutes in nitrogen. The surface energy of this bonded interface was about 0.8 J/m^2 after the annealing procedures. Wafer bows of less than 10 μm corresponding to a stress of about $5 \cdot 10^7$ Pa were obtained for structures consisting of approximately 1.5 μm of aluminum nitride on standard 100 mm wafers. These results were obtained by using a deposition process at 1.33 Pa with 10 sccm of nitrogen, 40 sccm of argon, a target power of 450 W and a RF-power of 120 W. In the case of electrostatic bonding an electric field and elevated temperature are used to bond the materials. This method is similar to anodic bonding [20] although in this case the bonding mechanism may be different. Here the aluminium nitride acted as the insulator and was contacted to a silicon wafer in a special set-up allowing heating and connection of bias voltage. Temperatures of approximately 400° C for 15 minutes were used in combination with an electric field of about 0.5 MV/cm. The surface energy of this bond, as measured by the razor blade method, was about 0.2 J/m^2. A schematic picture of an SOI material with a buried layer of AlN is shown in figure 3b.

Wafers with as-deposited aluminum oxide were rinsed in de-ionized water, dried and contacted to bare hydrophilic silicon wafers. Although desirable from particle removal considerations APM cleaning solutions could not be used since they etched the as-deposited films too rapidly. When the wafers were contacted the bonded area spread spontaneously and a few voids over a 3" wafers was monitored using IR transmission. The surface energies of the bonded interfaces were measured with the crack opening technique. The surface energy after room temperature contacting was 50 mJ/m² and it increased to about 600 mJ/m² after annealing at 330° C for 60 minutes. After annealing at 500° C, attempt to insert the blade lead to fracture of the wafers. Annealing at higher temperatures caused de-bonding of the wafers probably because of de-lamination of the deposited film. A schematic picture of an SOI material with a buried layer of aluminum oxide is shown in figure 3c.
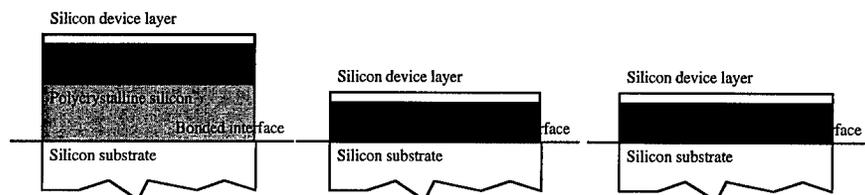
Figure 3. Schematic structure of the formed SOI structures, a) with diamond, b) with aluminum nitride, c) with aluminum oxide as buried insulator.

SILICON PROCESS COMPATIBILITY

The diamond films were exposed to standard wet chemical and plasma treatments used in silicon device manufacturing. Raman spectroscopy was used to ensure that the diamond film was not degraded [20]. We conclude that RCA cleaning, HF and buffered HF etching, etching in KOH, and wet aluminum etching (H_3PO_4:CH_3COOH:HNO_3, 29:5:1 at 40° C) do not adversely affect the diamond film to any measurable extent. Plasma processing was investigated using a Cl_2 plasma as well as plasma stripping of resist in oxygen. The chlorine plasma slowly etched the diamond with a selectivity to silicon of about 1:100. Oxygen plasma etches the silicon although a resist stripping in oxygen plasma may be done without any large structural changes. The influence of annealing steps on the diamond film was investigated. For uncovered polycrystalline diamond films annealing at 1000° C or above, even in an inert atmosphere, caused massive phase conversions in the films. Annealing at 950° C in nitrogen was possible without any measurable change in structure or electrical properties. A method based on encapsulation with silicon nitride was developed [20] to protect the diamond during high temperature processing. To evaluate this method, parts of the diamond film was encapsulated in silicon nitride and a LOCOS oxidation was made in water vapor. Raman spectroscopy was used to monitor changes in the diamond film. LOCOS oxidation at 1000° C did not affect the diamond film, while LOCOS oxidation at 1100° C caused a small increase in the graphite signal. Hence, diamon   in inert ambient and resistant against most chemicals, but form carbon oxide in the presence of oxygen at
further evaluate the silicon/diamond material, resistors, diodes and MOS-transistors were manufactured in the silicon films [11,14,20]. Electrical characterization showed well functioning devices. Thermal characterization of the structures showed that the SOI material with a buried diamond layer exhibited thermal conductivity similar to bulk silicon [11,14].

The aluminum nitride films was not affected by exposure to DI water, HF (50%), HNO_3 (65%), HCl (37%), HF: HNO_3:CH_3COOH etching mixtures, acetone or H_2O_2 (30%) at room temperature. However, RCA mixtures as well as exposure to strong acids at elevated temperature (80° C) resulted in etching of the AlN film with etch rates in the region 30–100 Å/min. Furthermore, NH_4OH (28%) and an aluminum etch mixture (H_3PO_4:CH_3COOH:HNO_3, 29:5:1) etched the film even at room temperature. Annealing of the deposited films at temperatures of 1000° C or 1100° C made them more stable during exposure to wet chemistry at 80° C.

The aluminum oxide films were sensitive to chemical cleaning steps like the RCA cleaning. Upon annealing a densification of the films took place at temperatures above 600° C. The densification was accompanied by increased stress, possibly caused by a partial crystallization.

CONCLUSIONS

We have shown the possibility of using wafer bonding for formation of novel SOI structures with buried films of diamond, aluminum nitride or aluminum oxide. The major problem encountered was the deposition of stress-free films with low surface roughness. Of the investigated films the polycrystalline diamond was the most difficult to bond. Without the deposition of polycrystalline silicon followed by polishing it was impossible to incorporate diamond films into the structure. All the studied insulating films showed a reasonable compatibility to temperature ranges and chemical steps used in silicon device manufacturing, although special considerations need to be taken in some cases. There is no reason why more mature deposition techniques would not be able to solve the problems related to surface roughness, silicon process compatibility and the diamond peaks. Therefore the main problems we faced during this project will probably be possible to overcome in the future.

ACKNOWLEDGEMENTS

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MONOLITHIC INTEGRATION OF III-V MICROCAVITY LEDs ON SILICON DRIVERS USING CONFORMAL EPITAXY

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ABSTRACT

Conformal epitaxy is an epitaxial growth technique capable of yielding low dislocation density III-V films on Silicon. In this technique, the growth of the III-V material occurs parallel to the silicon substrate, from the edge of a previously deposited III-V seed, the vertical growth being stopped by an overhanging capping layer. As an example, conformal GaAs layers on Silicon, presenting dislocation densities below $10^5 cm^{-2}$, have been obtained using selective vapor phase epitaxy. These layers have then been used as high quality GaAs on Si substrates for subsequent vertical MBE regrowth of active structures.

In this paper, we report on the integration of surface-emitting microcavity LEDs with their silicon drivers using this conformal growth technique. The global technology concept and the design of the active structures are first presented. The compatibility of the conformal growth technique with CMOS technology is then checked: the impact of the integration process on the performances of the drivers is for example quantified. Characterisations of the high crystalline quality of the conformal layers and of the LEDs structures grown on it are then shown. The electro-optical characteristics of the LEDs on Si are finally compared to those of reference LEDs on GaAs substrates in order to prove the efficiency of the integration procedure.

INTRODUCTION

Current trends toward increasing complexity and performance in integrated circuits have led to a situation where the electrical interconnects are the bandwidth bottlenecks in state-of-the-art computing systems. Optical interconnects, which are, among many other advantages, free of capacitance and inductance loading, free from cross talk and clock skew and reconfigurable, appear very promising to solve this problem [1,2].

The realisation of such interconnects requires first the integration of compound semiconductor optoelectronic devices with silicon circuits. So far, two types of technologies have been used. First, hybrid integration has been performed using for example solder-bonding [3]. Direct heteroepitaxial growth of optoelectronic devices on processed silicon substrates has also been studied [4, 5]. In this latter technique, the performances of the silicon ICs have been unaffected by the epitaxial step but the poor crystalline quality of the heteroepitaxial structures has never allowed the fabrication of optoelectronic devices exhibiting performances and reliability levels compatible with industrial requirements.

In this paper, we report on the integration of efficient top-emitting microcavity LEDs (µCLEDs) on processed Si substrates by using a special heteroepitaxial technique, called conformal growth, capable of yielding low dislocation density III-V films on Silicon [6, 7, 8]. In this technique, the growth of the III-V layers occurs parallel to the silicon substrate, from the edge of a previously deposited III-V seed, the vertical growth being stopped by an overhanging

capping layer. As an example, conformal GaAs layers on Silicon, presenting dislocation densities below $10^5 cm^{-2}$, have been obtained using selective vapor phase epitaxy [6, 7]. Such layers are used here as high quality GaAs on Si substrates for subsequent vertical MBE regrowth of active µCLED structures.

We describe first the whole technological process used to integrate the opto-devices on the Si circuits. We demonstrate then that the performances of the Si devices are unaffected by the use of misoriented substrates and by being submitted to a thermal budget equivalent to the µCLED integration procedure. Finally we evidence the crystalline quality of the µCLED structures integrated on Si and present the performances of obtained devices.

EXPERIMENT

The general technology concept developed in this work is summarised on figure 1. Our integration procedure starts with the process, using a 1µm CMOS technology, of the driver circuits on 6" misoriented (100) Silicon wafers (2° and 3° off towards (011)). Exactly oriented (100) substrates are also processed as reference. The process is stopped just before the final metallisation steps (except for test samples, metallised and characterised after application or not of a thermal budget nearly equivalent to the integration procedure, i.e. 750°C 5h). The elementary transistors obtained are then covered by a SiO2 passivation layer in which windows are opened for subsequent GaAs growth.
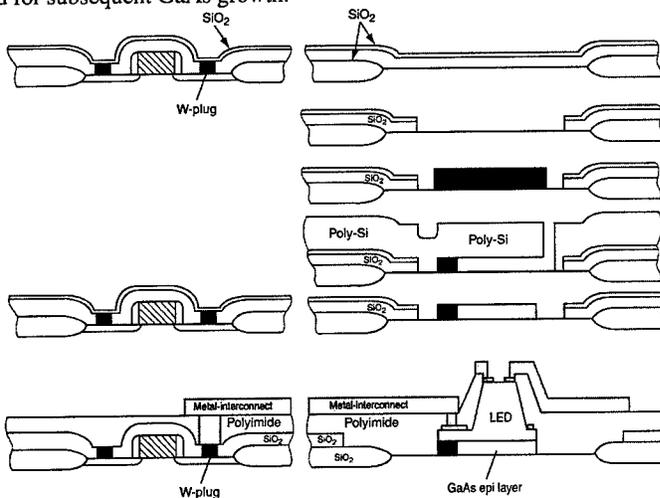
Figure 1: Monolithic integration procedure of top-emitting micro-cavity LEDs on 1µm CMOS drivers. Conformal growth of high quality GaAs on Si is the essential intermediate step.

After having sawn the 6" substrates into $36 \times 36 mm^2$ samples, the GaAs integration is conducted using the two-step conformal growth method [6, 7, 8]. First, after a standard RCA cleaning and an in situ thermal deoxidation at 600°C of the Si surface, a 50-100nm thick nucleation GaAs layer is grown by Migration Enhanced Epitaxy (MEE) at low temperature (150-225°C), followed by a 1.4µm-thick buffer layer grown by Molecular Beam Epitaxy (MBE) at higher temperature (375-465°C) and finally annealed at 580°C during 1h. This GaAs layer is

highly defective as state-of-the-art GaAs on Si material and is replaced in the second step by high quality material. So, after removal of the poly-GaAs deposited outside the windows, after deposition and opening of a poly-Si capping layer and after partial chemical under-etching of the defective GaAs leaving 2 to 200µm-wide seed stripes, conformal growth is performed by selective Hydride Vapor Phase Epitaxy (HVPE) at 700-750°C. The quality of the 30-40µm-wide conformal GaAs layers obtained is systematically checked by non destructive characterisation techniques (optical and scanning electron microscopies, photoluminescence imaging).

After removal by SF6 reactive ion etching of the capping layer and chemical cleaning (including successively deoxidation using HCl, degreasing in organic solvents and 200nm etching by a H2SO4/H2O2/H2O solution), the conformal layers are used as high quality substrates for subsequent regrowth of active structures. We focus in this paper on top-emitting µCLEDs because of the key role of these components in optical interconnects. Light at 942nm is generated in our µCLEDs by radiative recombination of carriers injected into three 7.5 nm thick strained $Ga_{0.84}In_{0.16}As$ quantum wells (QWs) situated at the anti-node positions of a λ_{FP} -size $Ga_{0.9}Al_{0.1}As$ planar cavity. The cavity is surrounded by top and bottom distributed Bragg reflectors (DBRs) centred at λ_{FP}=960nm. The top DBR is Be-doped and contains 3 λ_{FP}/4 GaAs/AlAs pairs, the bottom DBR is Si-doped and contains 15.5 GaAs/AlAs pairs. 15 nm thick $Ga_{0.5}Al_{0.5}As$ layers are inserted at each GaAs/AlAs interface to improve electrical conductivity. The number of pairs in the DBRs were chosen after detailed simulations for optimum light extraction efficiency, using a program based on the model proposed by Benisty et al.[9] to calculate the radiation of classical dipoles embedded in a planar structure. The value of the detuning (-18nm : difference between the emitted wavelength and the Fabry-Perot mode) was also chosen to maximise the extraction efficiency.

Conventional MBE using standard Al, Ga, In and As_2 sources was used to regrow at 520°C on top of the conformal layers an n+ GaAs buffer layer followed by the µCLED structure. Finally, a classical technological process is realised, including a mesa etching, the p- and n-contacts realisation, a planarisation step and a final metal interconnection with the test pads and the drivers circuits. The electro-optical characterisations of the devices together with physical analyses by cross-section Transmission Electron Microscopy (TEM) or Emission Dispersion Spectrometry (EDS) are then carried out to evaluate the quality of the integrated µCLEDs.

RESULTS

We have first investigated the influence of the misorientation and of the additional thermal budget on the performances of the processed MOS transistors. Let us first underline that no impact of misorientation on the technological process was noticeable. As an example, the 1 sigma uniformity of the gate oxide thickness (20nm) is better than 2% whatever the substrate misorientation. So, 1µm NMOS and PMOS transistors have been fabricated and characterised in terms of static device parameters. First of all we investigated the statistical distribution of the threshold voltage V_T , the maximum linear transconductance g_m and the on-state current I_{on} across the wafer. All the measured values are within a narrow statistical bandwidth and mean values of V_T and I_{on} are summarised in table I. From the V_T wafer mapping it can be seen that for the misoriented wafers a slight increase of V_T values can be observed in the NMOS case, compared to the reference samples. The maximum V_T deviation for 3° misoriented devices was below 40mV (<20mV for 2° off). This slight V_T dependence on misorientation is not critical, since the values are in the range of the technological deviation. In the PMOS case the V_T shift is negligible, due to the buried channel type of device with reduced impact on substrate misorientation. No parameter shift was observed, due the thermal treatment at 750°C.

Table I: Mean values for V_T, I_{on} and D_{it} for 1μm NMOS (left values) and PMOS transistors

Type	Thermal treatment 750°C, 5 h	Threshold voltage $V_{ds}=0.1V$ [V]		On current I_{on} (μA) $V_G=V_D=5V$		Interface state density D_{it} (10^{10} cm^{-2}eV^{-1})	
Standard	yes	0.9134	-1.132	701	323	1.5	0.8
<100>	no	0.9155	-1.143	697	313	1.51	0.73
Misoriented	yes	0.9252	-1.136	688	315	1.5	0.92
2° off	no	0.9286	-1.136	683	311	1.52	0.77
Misoriented	yes	0.9438	-1.126	673	311	1.5	0.91
3° off	no	0.9478	-1.131	667	306	1.46	0.83

In addition to these measurements, we determined the interface state density D_{it} by charge pumping measurements. All D_{it} values were determined below $2x10^{10}$ and $1x10^{10}$cm^{-2}eV^{-1} for NMOS and PMOS respectively. Here, no impact of misorientation on D_{it} values is observed.

We have then checked the long term reliability of these devices by performing high field hot carrier stress measurements. For these electrical stress measurements, the worst case stress conditions were applied by static dc-bias stress. For this purpose the PMOS transistors were biased at a gate voltage for maximum gate current stress. Under this condition a drain sided hot-electron injection occurs. In contrast, the NMOS transistors were biased under maximum bulk current condition, which results in avalanche hot-hole injection into the gate oxide from the drain space-charge region. With the gate bias conditions described, the transistor under test is then driven at a drain voltage as long as a 10% shift of the maximum transconductance $\Delta g_{max}/g_{max0}$ or threshold voltage $\Delta V_t/V_{t0}$ occurs. The required time necessary to reach this criteria is monitored in a log(lifetime)-$1/V_{d\,stress}$ plot. Since the lifetime for normal supply voltage ($V_D=5V$) conditions is needed to be determined, which in minimum has to amount over 10 years, the stress drain voltage used was adjusted between 8-11 V, in order to reach the 10% criteria in a reasonable time. An extrapolation up to 10 years lifetime (3 10^8 sec) gives the maximum drain voltage for operation under the condition of <10% transconductance or threshold voltage degradation. For the measurements carried out here, the maximum transconductance shift in the linear region was used. Figure 2 exhibits lifetime versus $1/V_{Dstress}$ plots for 1μm NMOS and PMOS transistors with or without thermal treatment, for standard and misoriented substrates.
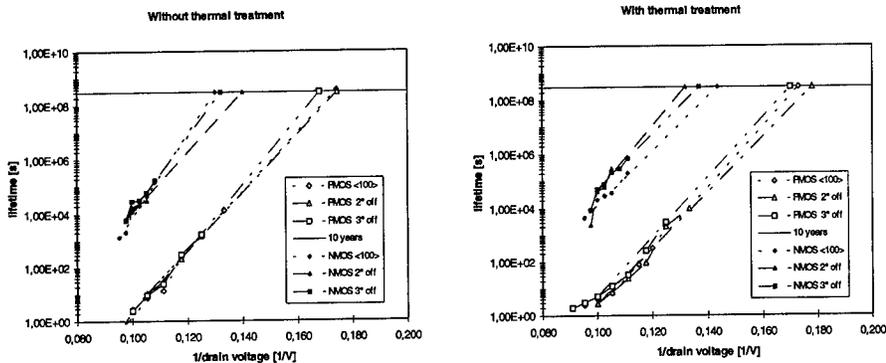
Figure 2: Lifetime versus $1/V_{Dstress}$ of 1μm PMOS and NMOS transistors.
Stress conditions: maximum gate current (PMOS), maximum bulk current (NMOS), lifetime criterion for degradation: 10 % shift in $\Delta g_{max}/g_{max0}$ (standard, 2° off and 3° off, with or without thermal treatment (750°C, 5 h)).

From the figure 2 it can be seen that the lifetime criteria of $< 10\%$ transconductance shift for a stress drain voltage $V_D=5V$ $(1/V_D=0.2V)$ is fulfilled in all cases. The deviation in lifetime between standard and misoriented substrates is not significant. Here, it has to be considered that an extrapolation over orders of magnitude implies a certain degree of deviation.

Once demonstrated that the drivers can withstand the integration procedure including misorientation, we have optimised the GaAs growth steps. According to our previous results, high quality conformal layers can only be obtained if the MBE-grown seeds have suitable properties like a small roughness and an homogeneous density of defects along the thickness (i.e. no too highly defective areas on the seed edges, particularly near the GaAs-Si interface). A low roughness is achievable only if a two-dimensional growth mode is kept. Therefore we used MEE for the nucleation step followed by a low temperature MBE step. We found that the optimum procedure consists in a 100nm-thick nucleation layer grown at 225°C, the growth temperature being then raised to 440°C. The post annealing at 580°C during 1h is required to obtain a suitable crystalline quality for the seed layers. The RMS roughness is about 5nm, the FWHM measured by High Resolution X-Ray Diffraction is about 470 Arcsec and the dislocation density is in the range 10^7-$10^8 cm^{-2}$. Conformal layers have then been grown from these seed layers using selective HVPE (figure 3). Optimum growth rates of 8µm/h at 750°C and 5µm/h at 720°C are used. The produced layers appeared defect free using PL imaging and TEM cross section.

We have then regrown µCLED structures on conformal layers using the MBE procedure developed on GaAs substrates without modifications. The surface morphologies obtained are excellent. No defects can be evidenced in these structures either by cross-section TEM (figure 4) or by EDS. After process, the electro-optical properties of µCLEDs on Si and on GaAs substrates are evaluated and compared [11]. The detuning and the lobe emission pattern are similar. The I-V characteristics showed no difference except a serial access resistance higher on Si due to the current injection through a second electrode in place of the GaAs substrate.

Finally the optical output power and the external quantum efficiency for the µCLEDs on the conformal layers on Si are lower by a factor of 3 to 5 compared to the reference ones on GaAs substrates (figure 5), but one order of magnitude higher than for the same devices on GaAs seeds on Si (not shown). This confirms the superior quality of the conformal GaAs/Si material over MBE GaAs/Si. Nevertheless the observed increase of the efficiency with current density for the conformal devices indicates the presence of recombination centers saturating at high current density. Further investigations are needed to identify and suppress these defects lowering the performances of the devices on Si. The connection of the conformal µCLEDs with their drivers is under progress, so dynamic measurements will be performed in the next months.
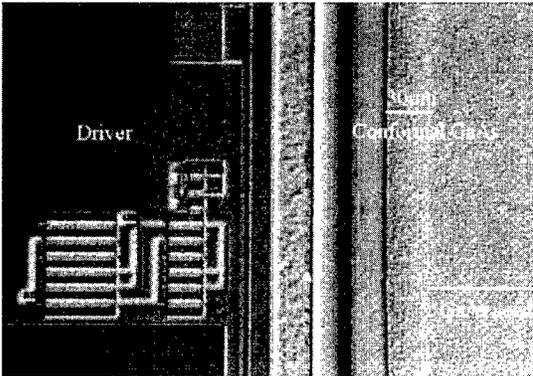
Figure 3: High quality conformal layer (30µm wide) integrated near a 1µm CMOS driver circuit.

Figure 4: Cross-section TEM of the active region of a μCLED grown on a GaAs conformal layer on Si. No dislocations are visible within the structure.
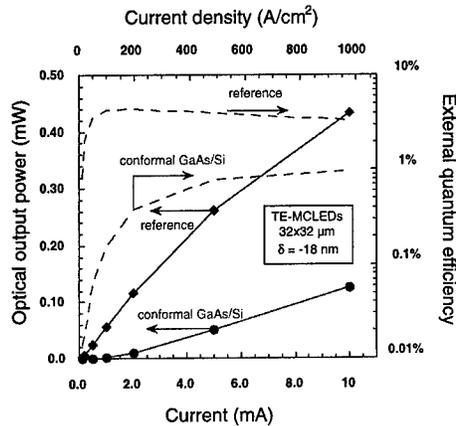
Figure 5: Comparison of L-I curves and external efficiencies (dashed curves) of devices processed on conformal GaAs/Si layers and on reference GaAs substrates.

CONCLUSIONS

We have developed a monolithic integration procedure based on the conformal epitaxy technique, in order to integrate μCLEDs on CMOS drivers. We have shown that both the use of misoriented wafers and the addition of the thermal budget equivalent to the μCLED integration steps have no impact at all on the technological process, the performances and reliability of 1μm CMOS devices. High quality μCLEDs have been integrated on Si by this technique. Their efficiency is improved by an order of magnitude compared to devices directly grown on Si.

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METALORGANIC MOLECULAR BEAM EPITAXY OF GaAsP FOR VISIBLE LIGHT-EMITTING DEVICES ON Si

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ABSTRACT

GaAs$_{1-x}$P$_x$ ($0.2 < x < 0.7$) was grown by metalorganic molecular beam epitaxy with a GaP buffer layer on Si for visible light-emitting devices. Insertion of the GaP buffer layer resulted in bright photoluminescence of the GaAsP epilayer. Pre-treatment of the Si substrate to avoid SiC formation was also critical to obtain good crystallinity of GaAsP. Dislocation formation, microstructure and photoluminescence in GaAsP grown layer are described. A GaAsP pn junction fabricated on GaP emitted visible light ($\sim$1.86 eV). An initial GaAsP pn diode fabricated on Si emitted infrared light.

INTRODUCTION

Heteroepitaxial growth of III-V semiconductors on Si showed progress in this decade: an InGaAsP laser emitting infrared light with a long life has been successfully fabricated on Si with a thick ($> 10\mu$m) InP intermediate layer[1]. Visible light-emitting diodes (LED's) of AlGaAs[2] and InGaP[3] have been fabricated on Si substrates with a GaAs intermediate layer by metalorganic and metalorganic-chloride VPE, respectively.

For further expansion of Si-based devices to a new field of microphotonics such as optical parallel processing[4, 5] or man-machine interfaces, it is important to realize a new combination between Si and dissimilar materials showing bright luminescence. Heteroepitaxial growth of a luminescent semiconductor on Si can lead to monolithic integration of a light-emitting device and Si devices. Visible light emission from a device on Si is essential for man-machine interface, and preferable to set an alignment among Si chips to be assembled.

GaAsP has an interesting nature in terms of luminosity against defect density. Based on a recent report[6], the luminosity of a GaAs LED began to decrease at a low etch pit density of 10^3 cm^{-2}. On the other hand, a GaN LED kept high emission regardless of a high dislocation density in an order of 10^{10} cm^{-2}. GaAsP or GaP showed an intermediate nature between GaAs and GaN. A GaP LED did not show a distinct degradation of the luminosity up to an etch pit density of 10^6 cm^{-2}. A GaAsP LED kept 10 % luminosity of that with a low etch pit density, up to an etch pit density of 10^7 cm^{-2}. In practice, GaAsP has been used in conventional LED's on GaAs or GaP for more than two decades due to its tough nature against lattice mismatch.

In this study, GaAsP was grown on a Si substrate with a GaP buffer by metalorganic molecular beam epitaxy (MOMBE) for fabrication of a visible LED on Si. Dislocation and photoluminescence (PL) in GaAsP are described in this report. GaAsP pn diodes are also presented. MOMBE has an advantage of *in situ* monitoring of crystal growth, in particular an initial stage of heteroepitaxy, using reflection high-energy electron diffraction (RHEED). As and P fluxes can be controlled precisely in MOMBE. Furthermore, GaAsP can be grown selectively on Si at a low temperature where Si devices are fabricated beforehand, which is suitable for a monolithic integration of light-emitting devices and Si devices.

GROWTH OF GaAsP ON Si

Pre-treatment of Si substrates

GaAsP was grown on Si by MOMBE with triethylgallium (TEGa) as a group-III source, PH_3, and tertiarybuthylarsine (tBAs) as group-V sources. PH_3 and tBAs were thermally cracked at 950°C and 750°C, respectively. TEGa was introduced into the growth chamber without thermal cracking. The flow rates of the source gases were controlled by mass flow controllers without H_2 carrier gas.

Si(001)-oriented substrates with an off-angle of 2 or 4° toward the [110] direction were used. The substrate was degreased and treated by a modified RCA cleaning method: Si substrates were dipped in the echant I ($NH_4OH:H_2O_2:H_2O=1:1:5$), the echant II ($HCl:H_2O_2:H_2O=1:1:5$) and HF, alternately. The thermal flush of the Si substrate was performed at a substrate temperature (T_{sub}) of 950°C at 1×10^{-8} Torr. In the case that the Si treatment is finished with HF dip, the RHEED pattern of the Si surface after the thermal flush shows formation of SiC as shown in Fig. 1(a). The SiC formation on the Si substrate results in a rough surface of GaAsP epilayer with a mean square roughness, R_{ms}, of 20 nm in atomic force microscope (AFM) observation as shown in Fig. 1(b), and a large full width of half maximum (FWHM) of X-ray rocking curve ((004) GaAsP diffraction) of 3000 arcsec for a GaAsP epilayer.

The formation of SiC after the thermal flush was suppressed, and the Si surface shows a twofold streak pattern in RHEED in the case that the pre-treatment was finished without HF dip as shown in Fig. 1(c). The absence of SiC on Si substrate leads to a smooth surface of a GaAsP epilayer as shown in Fig. 1(d) with a R_{ms} of 7 nm, and a FWHM of X-ray rocking curve of 1000 arcsec. A chemical oxide formed in the echant I or II on Si presumably prevents a reaction with adsorbed carbon species. The adsorbed carbon species and the chemical oxide may be desorbed in series during the thermal flush. In the case of HF dip, the carbon species adsorbed directly on Si without a chemical oxide may easily react with a Si surface.

GaP buffer layer

In the case of $GaAs_{1-x}P_x$ ($0.2 < x < 0.7$) growth on a GaP(001) substrate at T_{sub} in a range of 550-650 °C, twofold superstructure indicating a flat surface was observed in RHEED during growth. GaAsP on GaP showed bright PL at an energy close to its band gap. On the other hand, neither twofold superstructure during GaAsP growth nor PL was observed regarding GaAsP on Si (001)4° off and Si(001) just. The FWHM of the X-ray rocking curve increased from 720 arcsec for GaAsP(0.6 μm thick)/GaP to 3600 arcsec for GaAsP(1.0 μm thick)/Si.

Based on the AFM observation of an initial stage of GaAsP growth at 500°C with a thickness less than 10nm, the surface of GaAsP on GaP is kept smooth as shown in Figs. 2(a)-(c) with a R_{ms} less than 0.8 nm. In the case of GaAsP directly on Si, the surface of GaAsP becomes rough as GaAsP grows (Figs.2(d)-(f)). The value of R_{ms} reached to 1.2 nm at a growth time of 30 sec. In this study, therefore, GaP was selected as a buffer layer to obtain a smooth surface at an initial stage of GaAsP growth. Since very thin (< 10 nm) GaAs showed a rougher surface than very thin GaP in the AFM observation, we excluded GaAs as a buffer layer. Although a thin GaAsP layer with the same composition of the epilayer may be applicable to the buffer layer, GaAsP was excluded because of a change in the P composition of GaAsP by T_{sub} that makes optimization of the growth condition for the buffer layer complex.
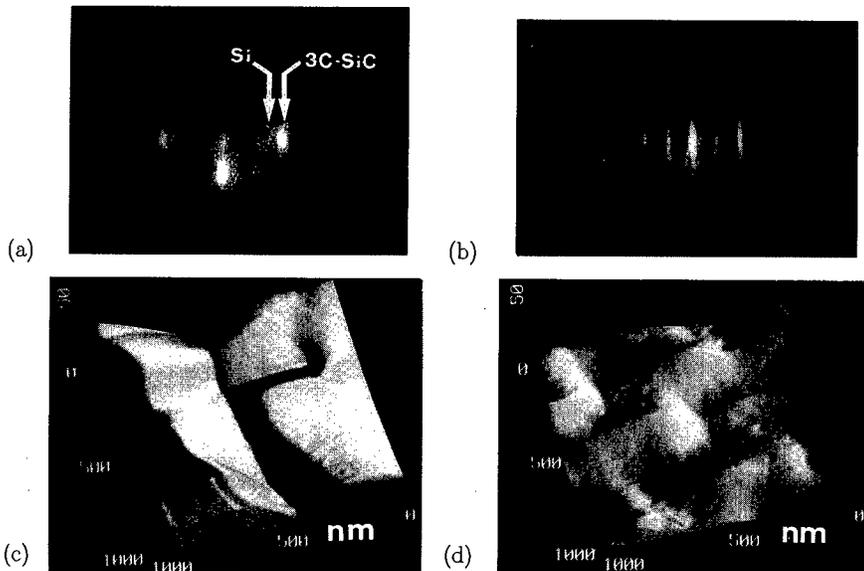
Figure 1: RHEED pattern of Si surface finished (a) with HF dip, and (b) without HF dip after thermal flush. Surface of GaAsP epilayer on Si finished (c) with HF dip, and (d) without HF dip.

GaAsP epilayers with a thickness between 0.5 and 3.0 μm were grown at T_{sub} of 500–600°C with a GaP buffer layer grown at T_{sub} of 280–420°C on Si(001)4°off. The RHEED pattern changed from the streak pattern of Si substrate immediately changed to a spot pattern of GaP during the growth of a buffer layer above 340 °C. The RHEED pattern became a spotty streak after buffer-layer growth below 320 °C. This indicates that a buffer layer grown below 320 °C has a smoother surface than that grown above 340 °C. Further, the FWHM of the X-ray rocking curve of the (004) GaAsP diffraction spectra became smallest at 1000 arcsec with a buffer layer grown at 300°C[7]. Therefore, the growth temperature for the GaP buffer layer was fixed at 300 °C.

The FWHM of the X-ray diffraction does not have a distinct dependence of the thickness of the GaP buffer layer in a range of 3 - 10 nm. In terms of the FWHM of X-ray diffraction, the optimum V/III ratio of [flow rate of PH_3]/[flow rate of TEGa] for the GaP buffer was found to be smaller than the optimum V/III ratio ([flow rate of TBAs]+[flow rate of PH_3])/[flow rate of TEGa] for the GaAsP epilayers. The small V/III ratio for GaP buffer growth probably results in an enhancement of Ga migration under a low pressure of phosphorus on the growing surface, which may lead to a dense coalescence of GaP on the Si substrate as in GaAs growth on Si by MBE[8]. A streak pattern with twofold superstructure along the [110] azimuth in RHEED was observed during the growth of a GaAsP epilayer with a thickness above 1μm[7]. The streak pattern was not observed in the direct growth on Si. The streak pattern indicates smoothness of the surface in the growth with the GaP buffer layer.

PROPERTIES OF GaAsP ON Si

Based on a cross-sectional image of transmission electron microscope (TEM) for GaAsP
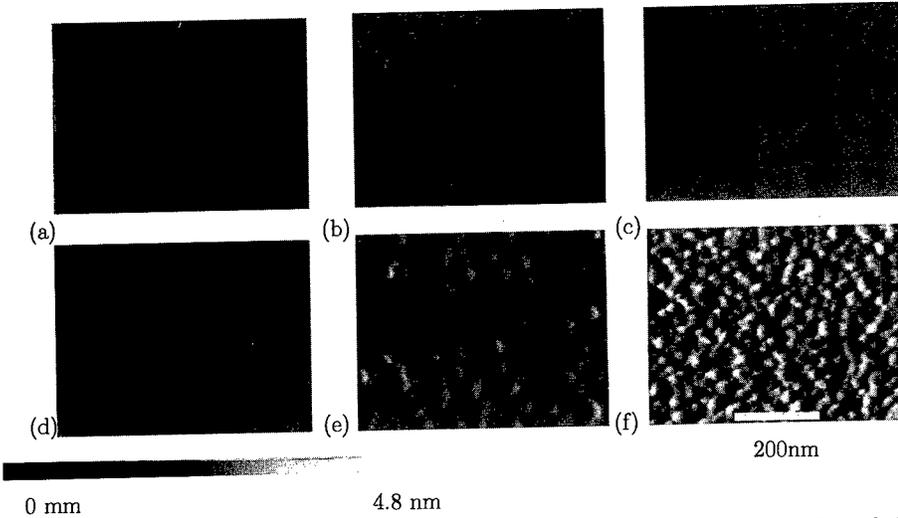
Figure 2: Atomic force microscopy observation of an initial stage of GaAsP. GaAsP on GaP: (a) GaP substrate. (b) after 30 sec, (c) after 120 sec TEGa irradiation. GaAsP on Si: (d) Si substrate. (e) after 10 sec, (f) after 30 sec TEGa irradiation. $PH_3/tBAs=1$.

Si as shown in Fig.3(a), the number of dislocation lines (N_{DL}) per unit length parallel to the growing surface was counted as shown in the inset of Fig. 3(b). The values of N_{DL} for both GaAsP grown directly on Si and GaAsP/Si with the GaP buffer layer are in proportion to the reverse of the thickness of GaAsP as shown in Fig. 3(b).

In a report[9] regarding the heteroepitaxial layers of InAs/GaAs, GaAs/Si, GaAs/InP, and InAs/InP with a thickness between 0.5 and 6 μm, the dislocation density, D_{DL}, in a range $\sim 10^7 - 10^9$ cm^{-2} was on the same curve expressed by the following experimental equation.

$$D_{DL}[\text{cm}^{-2}] = \frac{1.2 \times 10^9}{d[\mu\text{m}]} \tag{1}$$

Here, d is the thickness of the heteroepitaxial layer. In another report on GaAs/Si[10], D_{DL} was also in proportion to the inverse of d. This scaling law for the reduction of the dislocation density has been quantitatively analysed in terms of annihilation or fuse of dislocation by glide or climb[11]. By assuming that the thickness of the milled GaAsP for the cross-sectional TEM observation is 0.3 μm, D_{DL} predicted by eq.(1) can be transformed into the dotted line in Fig.3(b) by the following equation.

$$N_{DL}[\mu\text{m}^{-1}] = D_{DL}[\text{cm}^{-2}] \times 10^{-4} \times 0.3 \times 10^{-4} \tag{2}$$

Since the TEM observation was carried out using a TEM equipment with an acceleration voltage of 200 kV for the electron beam, the value of 0.3μm is in the reasonable range for the electron beam penetration.

The dependence of $N_{DL} \propto 1/d$ in Fig. 3(b) probably shows the same behavior of the dislocation density in GaAsP as in the above-mentioned epitaxial films. Although the difficulty in estimating D_{DL} from the cross-sectional TEM image has been pointed out due to
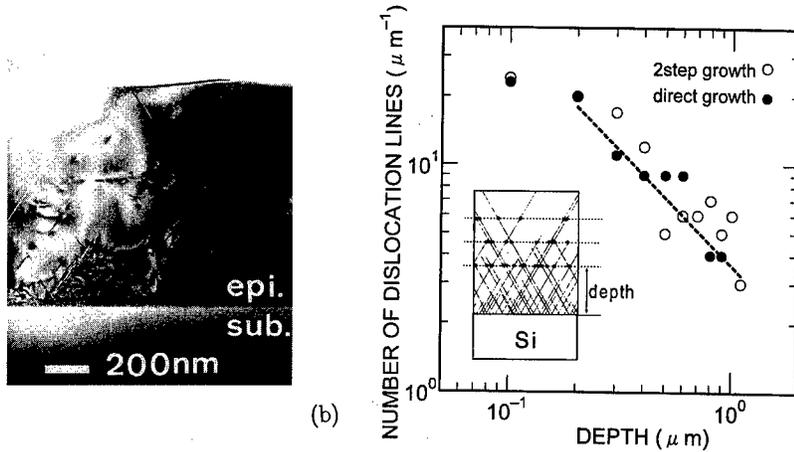
Figure 3: (a) TEM image of GaAsP/Si. (b) Depth profile of the number of dislocation, N_{DL}, per unit length parallel to the growing surface in TEM image. The dotted line is estimated on eq.(1) and (2). Inset: method for counting N_{DL}.

the difficulty in estimation of the thickness[9], the value of D_{DL} for 1 μm-thick GaAsP in this study is possibly on a range of 10^9 cm^{-2} based on eq.(1). Note that reduction of the dislocation density of GaAs/Si down to 1×10^6 cm^{-2} was achieved in the GaAs epilayers with a thickness around 100 μm[10].

PL was observed from a GaAsP epilayer on Si with a GaP buffer layer. The PL peak energy increases from 1.75 to 1.98 eV with increasing P composition from 0.23 to 0.54[7]. The PL indicates that the number of defects of nonradiative centers significantly decreases by inserting the GaP buffer layer. No difference in N_{DL} is observed between GaAsP grown directly on Si and GaAsP on Si with the GaP buffer layer. Defects related nonradiative recombination centers may become low in GaAsP on Si with the GaP buffer layer. The nonradiative centers are ascribed to point defects or fine structures of the dislocation.

Undoped GaAsP epilayers on Si showed p-type conduction, confirmed by a thermo-probe method, with a resistivity in an order of 10^6 Ωcm, based on a two-terminal current(I)-voltage(V) measurement. P-type and n-type doping were achieved with diethylzinc (DEZn) and tetraethyltin (TESn), respectively. For n-type doping, the carrier density of doped epilayers was changed between 6×10^{16} cm^{-3} with a mobility of 1200 cm^2/Vs and 1×10^{18} cm^{-3} with a mobility of 700 cm^2/Vs by changing the TESn supply. The mobility of 1200 cm^2/Vs at 300 K is comparable to the reported value of 1000 cm^2/Vs for GaAsP grown on GaAs by chemical vapor deposition[12]. For p-type doping, the carrier density of doped epilayers reached 5×10^{17} cm^{-3}. A GaAs$_{0.72}$P$_{0.28}$ pn junction grown on GaP showed rectifying characteristics and a visible light emission ($\sim$ 1.86 eV) at room temperature.

A preliminary GaAsP pn junction was fabricated on a Si substrate in the structure of n-type GaAs$_{0.88}$P$_{0.12}$ /p-type (undoped) GaAs$_{0.88}$P$_{0.12}$ /p$^+$-type Si. The pn junction showed rectifying characteristics with one order of magnitude. The high resistivity of p-type GaAsP without intentionally doping may degrade the pn characteristics. The structure showed an infrared-light emission under pulse operation at room temperature, in accordance with its band gap.

SUMMARY

GaAs$_{1-x}$P$_x$ ($0.2 < x < 0.7$) was grown by metalorganic molecular beam epitaxy with a GaP buffer layer on Si for visible light-emitting devices. Insertion of GaP buffer layer resulted in a bright photoluminescence of the GaAsP epilayer. A chemical oxide left on Si is effective to avoid formation of SiC on Si during the thermal flush, which leads to an improvement in the crystallinity of GaAsP on Si. Optimal growth conditions of the substrate temperature and the V/III ratio for the GaP buffer layer were determined based on the results of AFM, RHEED and X-ray diffraction. The dislocations in GaAsP presumably annihilate in proportion to the inverse of the thickness as in heteroepitaxial films of InAs and GaAs with a large lattice mismatch. P- and n-type doping were achieved for GaAsP, and GaAsP pn junction emitting visible light was fabricated on GaP. A preliminary fabricated GaAsP pn diode on Si emitted infrared light.

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SINGLE CRYSTAL Gd$_2$O$_3$ FILMS EPITAXIALLY GROWN ON GaAs
- A NEW DIELECTRIC FOR GaAs PASSIVATION

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ABSTRACT

Single crystal Gd$_2$O$_3$ dielectric thin films were epitaxially grown on GaAs. The Gd$_2$O$_3$ film has a cubic structure isomorphic to Mn$_2$O$_3$, and is (110) oriented in single domain on the (100) GaAs surface. The oxide film has low leakage current densities $\sim 10^{-9}$ - 10^{-10} A/cm^2 at zero bias. Typical breakdown field is 4 MV/cm for an oxide film 185 Å thick, and >10 MV/cm for an oxide less than 50 Å thick. Both accumulation and inversion layers were observed in the Gd$_2$O$_3$-GaAs metal oxide semiconductor (MOS) diodes using capacitance-voltage (C-V) measurements, with an interfacial density of states around 10^{11} cm^{-2} eV^{-1}.

INTRODUCTION

Deposition of (Ga,Gd)$_2$O$_3$ dielectric film on GaAs surfaces by electron beam evaporation from single crystal Ga$_5$Gd$_3$O$_{12}$ has produced MOS diode structures with a low interfacial density of states (D$_{it}$)[1,2]. Employment of this novel oxide as a gate dielectric along with a conventional ion implantation process has led to the first demonstration of the enhancement-mode GaAs MOSFETs with inversion on semi-insulating GaAs substrates in both n- and p- channel configurations[3]. The same technique using the oxide and the processing method has also been extended to fabricate the n-channel enhancement-mode InGaAs MOSFETs with inversion on InP semi-insulating substrates[4]. More recently, we have improved depletion-mode GaAs MOSFET's with negligible drain current drift and hysteresis[5], an important technological advance toward the manufacturing of this class of devices.

At the same time, material aspects on this novel oxide and the oxide/GaAs interfaces were studied[6,7] using high-resolution transmission electron microscopy (HRTEM), x-ray reflectivity, Auger analysis, Rutherford backscattering spectrometry (RBS), and other analytical tools. Electrical properties of the oxide/GaAs heterostructures were characterized using current-voltage (I-V) and capacitance-voltage (C-V) measurements. An interfacial roughness as small as 3 Å (roughly equivalent to one atomic layer of GaAs) was observed using x-ray reflectivity. The HRTEM and x-ray reflectivity measurements are in fair agreement, with HRTEM suggesting a larger rms variation of 10 Å. The (Ga,Gd)$_2$O$_3$ films are not entirely amorphous and show short range ordering containing nanometer sized microcrystallites. Nevertheless, the films are very dense, pinhole-free, and smooth. This is consistent with the (I-V) electrical measurements, which show a very low leakage current density (10^{-9} A/cm^2) at low bias.

The fundamental cause responsible for such a remarkably low interfacial state density (D$_{it}$) near the (Ga,Gd)$_2$O$_3$/GaAs interface is not clear. Low D$_{it}$'s were not obtained in other oxide/GaAs systems, such as MgO, SiO$_2$, Al$_2$O$_3$, and pure gallium oxide (Ga$_2$O$_{3-x}$) by a similar

approach[1,8]. As in reference 9, it was assumed that e-beam evaporation from single crystal $Ga_5Gd_3O_{12}$ may result in a deposited film consisting essentially of pure Ga_2O_3, with only a small amount (e.g., 0.1 at %) Gd present. Furthermore, it was believed that the Gd is undesirable, and that ideally the film should be pure Ga oxide. However; according our recent studies[7], the systematic dependence of the dielectric properties of $(Ga,Gd)_2O_3$ on the content of Gd clearly indicated that Gd_2O_3 is a necessary component to stabilize the gallium oxide in the 3^+ fully oxidized state due to the electropositive nature of Gd^{+3}. Moreover, the Gd content of the $(Ga,Gd)_2O_3$ films which yielded low leakage current and low D_{it}, is at least 20 at %. Contrary to the earlier assumption[9], our findings strongly suggest the necessity of Gd_2O_3.

In this paper, we report growth of a new dielectric oxide, Gd_2O_3 to passivate GaAs surface. Contrary to the $(Ga,Gd)_2O_3$ films being predominantly amorphous, the e-beam evaporated Gd_2O_3 film is a single crystal epitaxially grown in (110) orientation on the GaAs (100) surface. Our structural studies indicated the epitaxy takes place in single domain growth over an oxide thickness from 25 Å to at least 250 Å. The electrical measurements showed that Gd_2O_3 is an excellent dielectric with a dielectric constant of ~10. Typical electrical leakage current density J_L is less than $10^{-9} A/cm^2$ at zero bias, and the breakdown strength is 4-5 MV/cm for a film 100 Å thick (a higher breakdown field for thinner films). Furthermore, both inversion and accumulation layers were observed in the Gd_2O_3/GaAs MOS diodes.

EXPERIMENT

Growth of Gd_2O_3/GaAs samples was performed in a multi-chamber ultrahigh vacuum (UHV) system under conditions similar to our previous work[1] on $(Ga,Gd)_2O_3$. Fresh GaAs epi-layers were grown in the III-V molecular beam epitaxy (MBE) chamber. The films were then in-situ transferred to the oxide chamber. Either an As-stabilized (2x4) or a Ga-stabilized (4x6) reconstructed surface was obtained prior to the oxide deposition. A powder packed Gd_2O_3 source was used for e-beam evaporation. The substrate temperature is held at ~200-550°C. In-situ reflection high-energy electron diffraction (RHEED) was used to monitor the growth process. Oxide film thickness was determined by ellipsometry and x-ray reflectivity[6]. The structural properties were characterized by x-ray diffraction using a rotating anode source equipped with a triple-crystal four-circle diffractometer[10]. The I-V and C-V measurements were taken by the standard methods. Au/Pt dots of 75, 100, and 150 µm in diameter were evaporated using a shadow mask to the oxide surface for electrical contacts. The other probe was placed to the back of GaAs substrate.

RESULTS AND DISSCUSION

In-situ RHEED studies indicated that deposition of a Gd_2O_3 film 25 Å thick on an As stabilized (2 x 4) reconstructed GaAs surface resulted in streaky diffraction patterns of two-fold symmetry as reported earlier[11]. The quality of the RHEED patterns improved for thicker films of 250 Å, suggesting the epitaxial growth continues, but is not limited to an oxide film thickness of 250 Å. We also notice surface reconstruction occurring on the Gd_2O_3 films. Analysis of the diffraction patterns indicates that the Gd_2O_3 film is (110) oriented and grown in single domain. The in-plane epitaxial relationship between (100) GaAs substrate and (110) Gd_2O_3 film is $[001]_{Gd2O3}$ // $[011]_{GaAs}$ and $[\bar{1}10]_{Gd2O3}$ // $[01\bar{1}]_{GaAs}$.

X-ray diffraction studies of the Gd_2O_3 films of 185 Å, 45Å, and 25Å, respectively, showed that these oxide films are indeed single crystals[11]. The crystallographic orientation relationship between Gd_2O_3 and GaAs determined from x-ray diffraction is in agreement with the RHEED analysis. Additional single crystal scans made on the samples confirmed the bulk structure as Mn_2O_3 archived in powder diffraction file data bank[12]. The rocking scans show substantial broadening over the instrument resolution of 0.25°, indicating that films have a mosaic spread[11]. The film 25 Å thick, however, shows a very sharp component in the rocking scan, meaning that the epitaxial film at such a fine thickness elastically distorts its unit cell in order to conform to the in-plane perfect epitaxial condition. As the film grows thicker, it is energetically favorable to relax the strain possibly by generating misfit dislocations. HRTEM is now being used to examine the details of film microstructures.

Additional x-ray scans were taken to ascertain that Gd_2O_3 film is indeed of single domain. This was done by fixing the detector to the lattice spacing of the (222) reflection of the oxide, and then rotating the sample (ϕ angle) 360° on a cone centered to the surface normal. Observed reflections of two-fold symmetry unequivocally suggest a nearly perfect epitaxial growth of a single-domain, single crystal Gd_2O_3 film on GaAs (100), as shown in Fig. 1. This is unusual considering the two-fold degeneracy of aligning the (110) Gd_2O_3 plane of a rectangular symmetry onto the square symmetric (100) GaAs surface. The attainment of single domain is attributed to the (2x4) reconstruction occurring on the GaAs surface that removes the two-fold degeneracy, thus favors the single variant growth. We also found that Gd_2O_3 film grows in single domain on a Ga-stabilized (4x6) reconstructed GaAs surface.
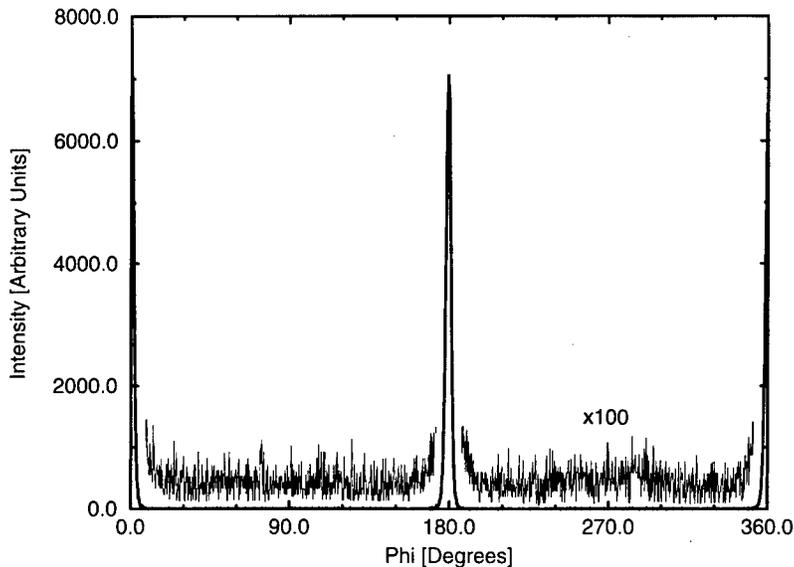
Fig. 1 X-ray diffraction ϕ scan of the (222) reflection of the oxide. The intensity of the background has been magnified 100 times to show that the second domain was not detected.

Shown in Fig. 2 is a schematic of Gd_2O_3 crystalline structure in alignment with that of GaAs. Along [011] direction of GaAs, we find a super-cell lattice match, i.e. the spacing of three Gd_2O_3 [100] lattices matched to that of four GaAs [011] lattices. The lattice constant mismatch is 1.9%. As for the perpendicular direction along [0 1 $\bar{1}$] of GaAs, the super-cell lattice match is one Gd_2O_3 [$\bar{1}$10] lattice spacing matched to that of two GaAs [0 1 $\bar{1}$] lattices. The lattice mismatch is -3.9%.
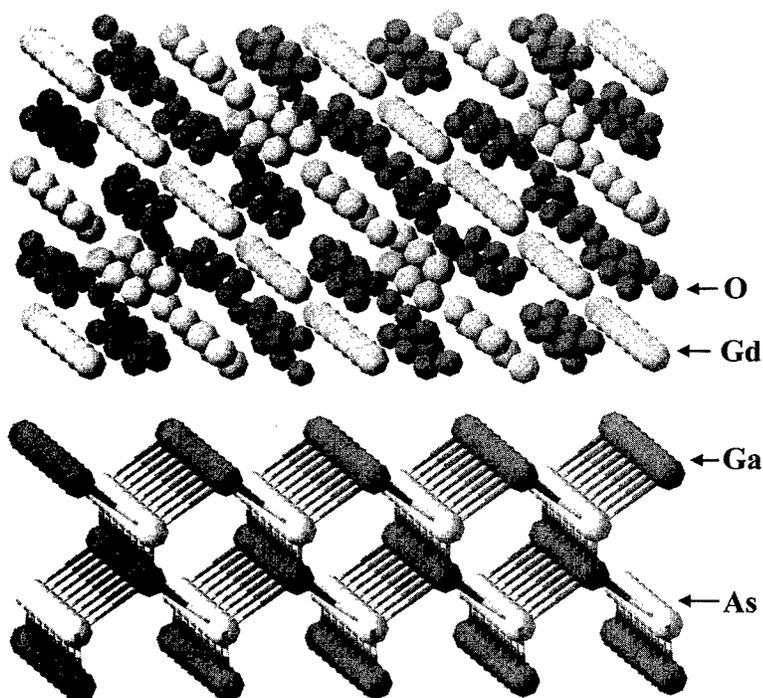
Fig. 2 A schematic of (110) Gd_2O_3 crystalline structure (upper lattice) aligned with that of (100) GaAs (lower lattice).

The Gd_2O_3 dielectric films are highly electrically insulating, showing very low leakage current densities $\sim 10^{-9}$-10^{-10} A/cm^2 at zero bias. Fig. 3 shows the dependence of leakage current density (J_L) on the applied voltage (V) for a set of Gd_2O_3 samples with the oxide thickness (t_{ox}) systematically reduced from 260 Å to 25 Å. The positive bias means that the metal electrode is positive with respective to GaAs. As t_{ox} is decreased from 260 Å to 45 Å, the respective breakdown field E_{br} increases systematically from 3 to 10 MV/cm, yet J_L at a fixed field of 1.5 MV/cm increases merely by one order of magnitude. The fact that the low electrical leakage remains intact even for films as thin as 25 Å suggests that a high degree of structural integrity is sustained through epitaxy.
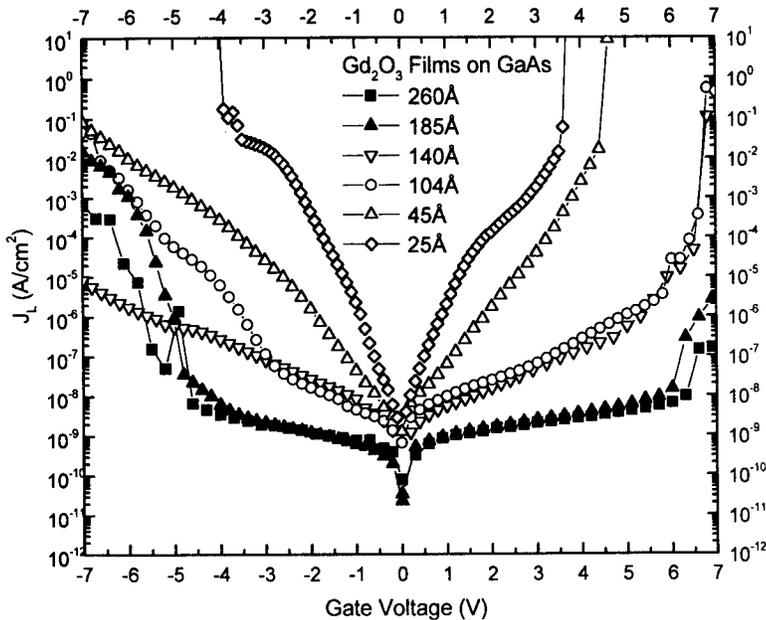
Fig. 3 Leakage current density J_L vs applied voltage V for Gd_2O_3 films with decreasing thickness of 260, 185, 140, 104, 45, and 25 Å.

Figure 4 shows the capacitance-voltage (C-V) traces of a MOS diode made of the Gd_2O_3 185Å thick. A transition from accumulation to depletion modes occurs at ~2V. The inversion carriers (holes) follow the a.c. signal up to a frequency of 10 kHz, and do not respond to frequencies greater than 100 kHz. Typical dielectric constant of the Gd_2O_3 film is about 10. The C-V characteristics can be understood by taking the conductance (G) into account[13]. The finite value of G, mainly arising from the tunneling current through the ultra-thin oxide layer, is in parallel with the oxide capacitance (C_{ox}). This simple equivalent circuit model explains that the total capacitance increases as the modulation frequency decreases. After re-plotting the C-V curves by subtracting the contributions from G and C_{ox}, the interface density of states (D_{it}), which responses only to the low-frequency measurements, is then deduced from the high- and low-frequency curves. This analysis gives a D_{it} at the midgap is about ~ 10^{11} cm^{-2} eV^{-1}, which is comparable to that of $(Ga,Gd)_2O_3$/GaAs interface, and slightly higher than those of the best SiO_2/Si interfaces.

The single-crystal Gd_2O_3 films and their interfaces to GaAs are thermodynamically stable when subject to rapid thermal annealing (RTA) to 850°C for post growth processing. The I-V data for the annealed samples after RTA showed little change, and the C-V measurements still showed accumulation and inversion, indicating the intact of the oxides and the interfaces under such severe thermal stress.
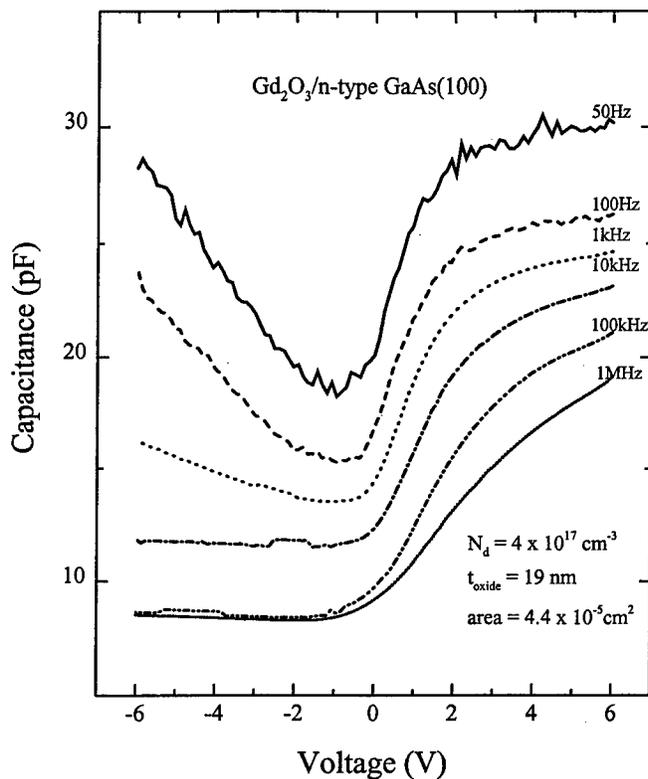
Fig. 4 C-V traces for a MOS diode made of a 185 Å Gd_2O_3 film[11].

The result of Gd_2O_3/GaAs presented in this paper is not the first demonstration of an epitaxial oxide on GaAs. Earlier work has reported epitaxial growth of MgO film on GaAs[14]. However, in the MgO/GaAs heterostructures,[1,15] the Fermi level was pinned, and it is unclear whether low leakage currents were achieved for MgO films thinner than 200 Å. Moreover, MgO films, even in the single-crystal form, are known to be unstable when exposed to room air. In comparison, we have shown that Gd_2O_3 films epitaxially grown on GaAs give low D_{it} and are thermodynamically stable in room air, and are robust withstanding RTA to high temperatures ~850°C.

CONCLUSION

We have demonstrated the epitaxial growth of single crystal Gd_2O_3 films on GaAs achieving a low interfacial density of states. The atomically smooth interface and single domain structure of Gd_2O_3 ensure excellent dielectric properties with low leakage conduction and high breakdown strength even for films of only 25 Å thick. The robustness of the epitaxial dielectric against post high temperature annealing adds another attractive feature for device application. We expect that

epitaxial growth of the Mn_2O_3 structure can be extended to other rare earth oxides, and to other semiconductor substrates like Si. Our findings from this work thus suggest new opportunities of producing high ε gate dielectrics for Si and GaAs based MOSFETs.

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FABRICATION OF INTEGRATED FERRITE/SEMICONDUCTOR CIRCULATORS

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ABSTRACT

Integrated planar circulator circuits operating at frequencies near 10 GHz have been
fabricated using transferred film techniques. A 100 micrometer thick film of single-crystal yttrium
iron garnet was transferred onto a metallized silicon die using a bond and lap-back process. The
alloy bond layer was formed through a low-temperature solid-liquid interdiffusion process using
films of indium and gold. This bond layer proved of sufficient strength to permit removal of the
gadolinium gallium garnet substrate through grinding, but chemical analysis of the bond shows
that interdiffusion occurs between the bond and metallization layers. These integrated
garnet/silicon circulator circuits show good device performance.

INTRODUCTION

The successful integration of insulating magnetic oxides, or ferrites, into planar thin film
monolithic microwave integrated circuits such as circulators may allow for decreases in size and
weight and increases in performance over present devices. However, this goal has proven to be
very difficult to attain because of the dissimilarities in properties between ferrites and
semiconductors. These include substantially different coefficients of thermal expansion, which
when combined with the high growth temperatures (>700°C) and oxidizing atmospheres needed
to deposit high quality ferrite films, provide for great difficulties in developing film deposition and
fabrication processes [1]. Moreover, the ferrite films needed for planar devices are very thick by
typical film deposition standards, ranging from 40 micrometers to greater than 100 micrometers
depending upon the frequency band of the device being fabricated, and in addition they must also
be underlaid by a highly conductive metallic ground plane for incorporation into traditional
microstripline circuits.

Recently, we have used film transfer techniques to fabricate and test integrated planar
circulators on silicon substrates operating at microwave frequencies [2]. These techniques were
developed to avoid some of the obstacles involved in directly depositing ferrite films on metallized
semiconductor substrates. The general procedure used in the fabrication of integrated
ferrite/silicon devices by film transfer is shown in Figure 1, which is broken down into three steps.
The first step entails obtaining high quality ferrite films, which for the case where film transfer is
being used means that the films can be grown under optimal conditions onto the most appropriate
substrate. The film quality required will depend upon the device requirements, although given the
effort involved in making these devices it is probable that only the highest quality films will be
used. Continuing in Figure 1, the second step entails bonding the film/growth substrate onto a
metallized silicon wafer, which is then followed by the third step where the growth substrate is
removed prior to final device fabrication. It should be noted that the process shown in Figure 1 is
not the most efficient as the entire growth substrate is wasted during the third step. Thus, we have
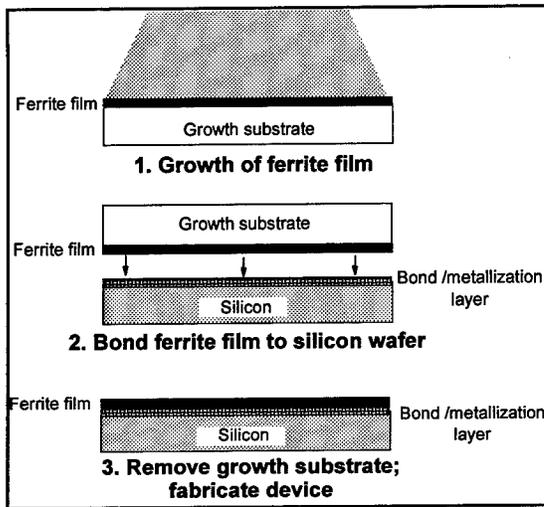
Figure 1. Fabrication steps for the integrated ferrite / silicon circulators.

replaced the bond and lap-back process shown in Figure 1 with a film lift-off process using a weak adhesion layer at the film - growth substrate interface. Regardless of the exact process used, the foremost advantage of the film transfer method is the separation of initial film growth from final device integration and fabrication.

Here, we report on the fabrication and testing of planar single-crystal garnet circulators integrated onto silicon substrates that were fabricated using the film transfer process shown in Figure 1. The choice of yttrium iron garnet (YIG) as the ferrite film was made because YIG has the best microwave magnetic properties of any ferrite, and a limited number of thick single-crystal YIG films are available commercially.

EXPERIMENT

The integrated circulator circuits reported on here were fabricated using the bond and lap-back technique procedure shown in Figure 1. The ferrite film consisted of 100 micrometer thick film of single-crystal yttrium iron garnet grown onto a lattice-matched gadolinium gallium garnet (GGG) substrate by liquid phase epitaxy (LPE) techniques. This ferrite film was procured from the Airtron Corporation in the form of a two-inch wafer having a LPE YIG film on both sides of the 0.5 mm thick GGG substrate. These films are known to have excellent crystallographic, magnetic and microwave magnetic properties [3]. The semiconductor used as the transfer substrate was a three inch diameter metallized silicon wafer obtained from M/A-COM, Inc., which had as a top surface a standard microwave ground plane consisting of 2 microns of silver plus barrier layers. Both wafers were diced to yield die having dimensions of 0.5 in. x 0.4 in. to fit the microwave testing assembly.

In order to minimize stresses at the interface that will arise because of the thickness of the YIG film and the difference in thermal expansion coefficient between YIG (α=13 x 10^{-6} °K^{-1})and

silicon (α=4-5 x 10^{-6} °K^{-1}), a low temperature alloy bonding process was used. In particular, an In-rich In-Au binary alloy was chosen because of the low melting temperature of indium (156°C), and also to provide a bond layer that was very compliant to stress. The bond layer was formed by depositing films of elemental gold (100 nm) and then indium (2500 nm) onto an adhesion layer of TiW that was deposited onto the mating face of each die. The two die were then mated and placed into a graphite strip oven for thermal processing under vacuum. Each bonded die was then heated at 195°C for 20 minutes, and was allowed to slowly cool to room temperature in flowing nitrogen gas. The resulting In-Au alloy bond has a composition near 12 wt.% Au, which was a much lower percentage of gold than bonds tested previously [4][5].

The topmost YIG film and the GGG substrate were removed from the bonded die by mechanical grinding and polishing using diamond pastes in a commercial grinding unit following standard methods. A final polish of the exposed YIG surface was done through a chemical-mechanical planarization using an alkaline silica-based solution. The resulting surface had a mirror finish, and profilometer measurements indicated a mean surface roughness of 12 nm. Each die also showed a beveled edge where an additional 10 micrometers of YIG was removed. After polishing the top surface was metallized by depositing 2.5 micrometers of copper onto a TiW adhesion layer.

The circulator circuits were fabricated through standard photolithography and wet-etching processes for the copper metallization. There was no circulator design base available for these planar integrated devices, because of the use of a 100 micrometer single-crystal YIG film compared to standard bulk ceramic circulators. However, the Y-junction circulator and microwave impedance matching circuits were designed by extrapolating the standard circulator model into the thin-film region. The circuits were tested using a microwave vector analyzer, where external magnets were provided to bias the circulator to the operating frequency.
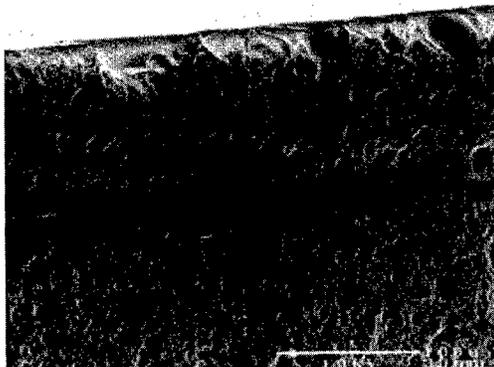
Figure 2 Cross section of a diced YIG/silicon circulator circuit showing the bond/ground plane.

RESULTS

The process chosen to fabricate the integrated YIG/Si circulator circuits was found to perform adequately in the device fabrication, especially in mitigating damage to the YIG film while 85% of the garnet wafer was removed during the grinding and polishing procedures. Figure

2 shows an electron micrograph of a cross section of a die after dicing, where the top layer metallization has been previously removed by etching. Here the combined bond and ground plane metallic layers are apparent between the YIG film (top) and the silicon wafer. The smoothness of the YIG top surface is also apparent in this image.

Although the In-Au alloy bond layer successfully resisted the shear stresses present during grinding and polishing, this layer failed under tensile stress, exposing the bonding interface. The
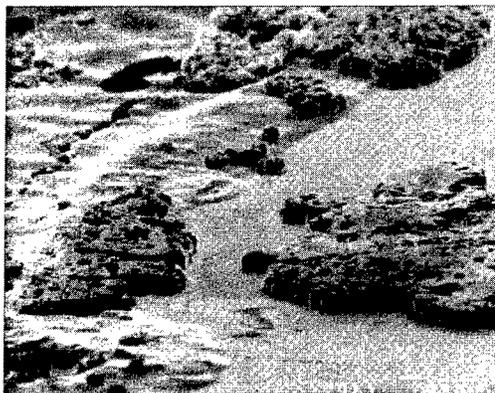
Figure 3 Micrograph of the exposed surface of the metallized silicon after breaking the bonding layer.

exposed surface of the metallized silicon is shown in Figure 3, where a number of terraces are apparent on a smoother metallic layer. Coincidentally, the exposed mating face of YIG also shows a pattern of terraces, presumably having an opposite relief. The composition of the exposed features was determined by energy dispersive x-ray spectroscopy measurements. First, the chemical constituents of the smooth film underlying the terraces were found to match those of the silver ground plane, barrier layers, and also the TiW adhesion layer. The corresponding TiW layer was also found on the surface of the YIG film, indicating that the failure of the bond layer occurred at the TiW/bond interface. Additional tests of In-rich In-Au alloys on TiW layers deposited directly onto silicon repeated this failure mechanism, and also indicated that elemental In films poorly wet TiW. The second finding was that the blocky terraces contained a significant amount of silver in addition to indium and gold. This result is presumably caused by the diffusion of silver from the ground plane into the indium rich layer, which would occur where the silver layer is exposed, such as at the tear on the left hand side of Figure 3. What is unclear is whether this diffusion occurs only at defects in the barrier layers, or is provoked when the indium is in the liquid phase during the anneal.

Test results taken on the integrated circulator shown in Figures 2 and 3 before it was diced are given in Figure 4, which gives the scattering parameters corresponding to power transmitted in the forward direction (S_{21}) and reverse direction (S_{12}) through the circuit as a function of frequency, where the third circulator port has been terminated in a broad band load. Here the value 0 dBm corresponds to a transmitted power of 1 mW at the measured frequency. The difference in power transmitted for the two opposite directions is indicative of the nonreciprocal behavior of the circulator, which in this case is acting as an isolator with the amount of isolation in the reverse direction approaching 20 dBm over a 2 GHz bandwidth centered about 9 GHz.
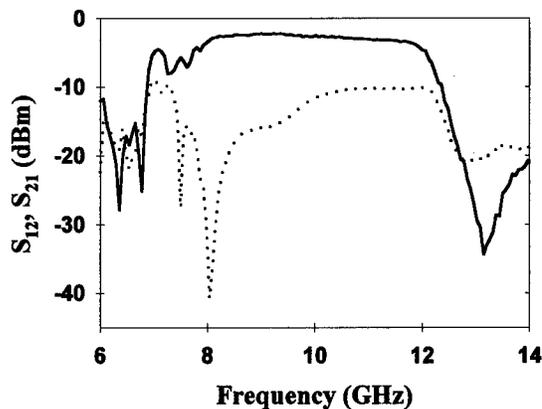
Figure 4. Power transmission in the forward (solid line) and reverse
(dotted line) directions for the integrated YIG/silicon circulator
circuit as a function of frequency.

The overall performance of the integrated YIG/silicon circulator circuit shown in Figure 4
is good compared to the standard bulk circulators made from thick (~5 mm) ceramics, where the
latter are incompatible with integrated microwave integrated circuits. The microwave loss in the
forward direction has been determined to be dominated by conductivity losses [6]. Thus, the
conductivity of the ground plane becomes an important determining factor in the overall device
performance, as does the conductivity of the bond layer for the device fabrication process
described here. In order to further improve the device performance, the fabrication process shown
in Figure 1 was modified by the addition of an additional step where the top surface of the YIG
film was metallized by depositing a 2.5 micrometer thick copper film onto a TiW adhesion layer.
Circulators made using this modified process were found to have significantly less loss, and better
isolation, than that shown in Figure 4 [2]. However, it is probable that diffusion between the In-
Au bond layer and the copper film has also degraded the conductivity of the copper ground plane.
Ongoing research is examining barrier layers to protect the ground plane from interdiffusion with
the bond layer.

CONCLUSIONS

The bond and lap-back film transfer method described here has been used to fabricate
planar integrated YIG/silicon circulator circuits. The performance of these first-of-their-kind
devices has been more than adequate to show the usefulness of applying transferred film
techniques to microwave integrated circuits. In particular, the conductivity of the ground plane
greatly effects the overall device performance, and it will thus be necessary to develop methods to
protect the ground plane. Finally, the replacement of the bond and lap-back method with a ferrite
film lift-off method that provides for reuse of the growth substrate will provide additional benefits.

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EFFECT OF MICROSTRUCTURE AND CHEMICAL BONDING ON THE ADHESION STRENGTH OF A SILICON/POLYMER INTERFACE FOR MICROELECTRONIC PACKAGING APPLICATIONS

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ABSTRACT

Interface reinforcement brought about by addition of a γ-amino-propyl-triethoxy-silane (γ-APS) adhesion promoter layer between a silicon wafer and a spun-on benzocyclobutene polymer (BCB) is investigated. Combining cross-sectional TEM and XPS, crack growth is shown to occur along the γ-APS/BCB interface. Ion etching and in-situ XPS are further employed to study chain orientation and chemical bonding variations through the silane layer. A tendency of the amide group to orient away from the wafer is documented and Si-O-Si siloxane bonding at the γ-APS/SiO$_2$ interface is hypothesized as an important mechanism for adhesion strength enhancement.

INTRODUCTION

Silicon/polymer interfaces are encountered in a variety of microelectronic packaging applications[1], such as direct chip attach, flip chip structures, and back end chip passivation. An SiO$_2$/polymer interface is more specifically involved in the latter, with BCB being an important candidate for this application[2]. Oxide/polymer interfaces however, exhibit relatively poor adhesion strength and thus silane coupling agents, such as γ-APS, are often employed as strengtheners[3-4]. Silane coupling agents have been extensively studied and several models have been proposed to interpret their capability to promote adhesion between organic and inorganic materials[5-6]. However, key issues, such as the effect of processing steps on chain configuration and cross-linking and the exact nature of bonding mechanisms at both the silane/organic and silane/inorganic interface have yet to be fully explained and experimentally tested. We studied a Si/SiO$_2$/γ-APS/BCB structure, for samples prepared following standard manufacturing procedures. Using high resolution, cross-sectional TEM and XPS analyses of surfaces exposed after fracture, the weakest path through the structure was identified. Ion etching in combination with in-situ, high energy resolution XPS (0.1 eV) was used to investigate chain alignment and chemical environment variations with depth in the silane layer and to provide information about the adhesion promoting mechanisms. The results of our analyses were directly correlated with reliable quantification of the actual interface adhesion strength enhancement.

EXPERIMENT

Samples with a BCB film constrained between two silicon wafers to be used for measurement of the interface debond energy G were fabricated by Dow Chem. Co. First, a γ-APS layer (Du-Pont VM 651) was deposited on oxide passivated silicon wafers. 3 ml of 0.1% silane solution in glycol ether (Dowanol PM) was spun-on the wafers and dynamically dispersed at

500 rpm spin rate. This was followed by 30 sec spinning at 3000 rpm which removed most of the solvent. The thickness of the resulting silane film was 2.5-3 nm as revealed by cross-sectional TEM. Next, a 1.5 nm thick film of BCB-type polymer (Cyclotene^{TM} 5021, Dow Chem. Co.) was spun-on the wafers. Two such wafers were placed face-to-face with each other and hard cured at 300 °C for 1 hr in a high purity N_2 atmosphere. This resulted in Si/SiO$_2$/γ-APS/BCB/γ-APS/ SiO$_2$/Si sandwich structures. Si/SiO$_2$/BCB/SiO$_2$/Si structures without the γ-APS were also fabricated following a similar procedure.

After bonding, samples of both types were cut into fracture test bars with appropriate dimensions, with a notch introduced between the SiO$_2$ and the BCB layers to initiate crack growth. The adhesion strength G was measured using a four-point bend configuration. The details of the experimental set-up and the theoretical background allowing reliable determination of interface G have been described elsewhere[7]. In-situ optical microscopy was used to monitor the crack growth during the testing.

Each completed fracture test resulted in two debonded sides, each terminated by the corresponding surface that was gradually created as the crack front propagated through the initial structure. Since the crack was initiated at one of the two oxide/BCB interfaces of the sandwich structure, the exposed surfaces will for clarity reasons be referred to as wafer side and polymer side fracture surface respectively. Because of its nanometer scale thickness, detection of the γ-APS layer, and thereby determination of the exact debond path with respect to it, necessitated use of a high resolution imaging technique, such as TEM.

Standard sample preparation procedures for cross-sectional TEM involve using an epoxy adhesive to embed the multilayer of interest in a stiff, supporting structure, so that the studied interfaces will remain intact during the multiple thinning steps. To avoid confusion as to the exact position of the fracture surface caused by the epoxy adhesive in cross-sectional TEM micrographs, a 10 nm thick Au layer was deposited via standard DC sputtering on the fracture surface before embedding the sample within the supporting structure. Since Au has a high atomic number more electrons are scattered by it than by the adjacent carbonaceous polymers or the silicon wafer. Therefore the Au film appears as a dark line in TEM pictures, outlining the terminating surface of the debonded sample. TEM micrographs were taken with a Philips EM-430 ST microscope operating at 300 keV.

Chemical analysis of the fracture surfaces was performed with an X-ray photoelectron spectrometer (S-probe, Surface Science Instruments) using monochromatic Al K$_a$ radiation and a spherical capacitor type analyzer. The X-ray beam had an incidence angle of 35° relative to the analyzed surface and a spot size of 150x1000 μm^2. A low-energy electron flood gun was used to minimize sample charging during analysis. Survey scans for element detection and semi-quantitative compositional analysis were taken at 1 eV energy resolution. To determine peak binding energy accurately or to identify peak splitting into sub-peaks representative of a specific chemical environment, high energy resolution spectra (0.1 eV) were taken around several peaks of interest. Compositional analysis, peak positioning and composite peak fitting was performed by specialized software. The compositional analysis was based on relative sensitivity factor calculations, introducing a 10%-20% error. In-situ ion etching was performed using Ar as the working gas (5000 eV Ar ions), with the sputter area being approximately 2x2 mm^2. The average etch rate calculated for these experimental conditions using Si/SiO$_2$ standards was ≈ 1.5 nm min^{-1}.

RESULTS

Addition of the γ–APS layer significantly enhances the adhesion strength of the structure. The results of debond energy measurement using a four-point bend experimental configuration are shown in Fig. 1[7]. The average measured fracture toughness of the silane reinforced interface was ≈48 J/m^2, whereas the corresponding value for the samples without the coupling agent was ≈18 J/m^2. Fig. 2[7] shows an optical micrograph taken during testing one of the reinforced samples and indicating exclusivey adhesive failure at the wafer/BCB interface. The γ–APS layer is not detectable in this picture.
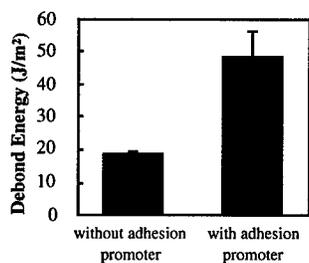
Figure 1: Measured debond energy values for the two tested types of samples
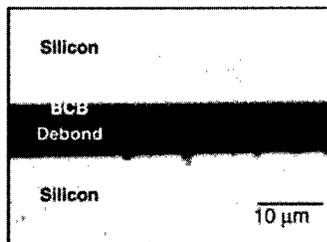
Figure 2: Optical micrograph showing adhesive failure at the SiO$_2$/BCB interface

The exact crack path with respect to the coupling agent film has been determined via chemical analysis of the exposed fracture surfaces. Fig. 3 shows a survey scan XPS spectrum of the wafer side fracture surface. The strong C(1s) peak indicates the existence of a carbonaceous film left on top of the oxide, whereas the N(1s) peak identifies this film as the silane adhesion promoter, since N is only contained in the γ-APS molecules. In Fig. 4 the corresponding spectrum of the BCB side fracture surface is shown. No N signal is detected and the chemical composition is as expected for Cyclotene^{TM} polymers[2]. These spectra indicate adhesive failure at the γ-APS/BCB interface.
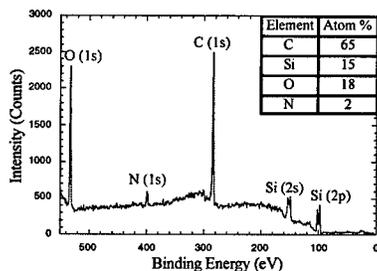
Figure 3: XPS spectrum of the wafer side fracture surface
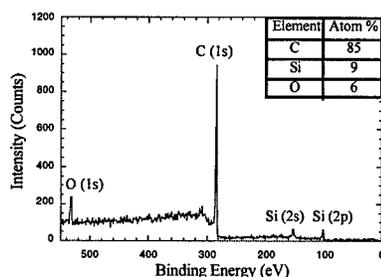
Figure 4: XPS spectrum of the polymer side fracture surface

To confirm the above crack path selection model and obtain information on the interface microstructure, high resolution cross-sectional transmission electron microscopy was employed. Fig. 5 shows a TEM micrograph of the wafer fracture side. Individual atom rows of the silicon crystal are clearly shown, with the amorphous oxide layer on top. The amorphous silane film appears as a light zone 2.5-3 nm thick on the SiO_2 surface, with the contrast coming from the fact that C has lower atomic number Z than Si. The deposited Au film outlining the precise fracture surface topography is the dark band at the top part of the micrograph. Thus the combined investigations of the fracture surface with TEM and XPS identify the γ-APS/BCB interface as the weakest microstructural path selected by the propagating crack.
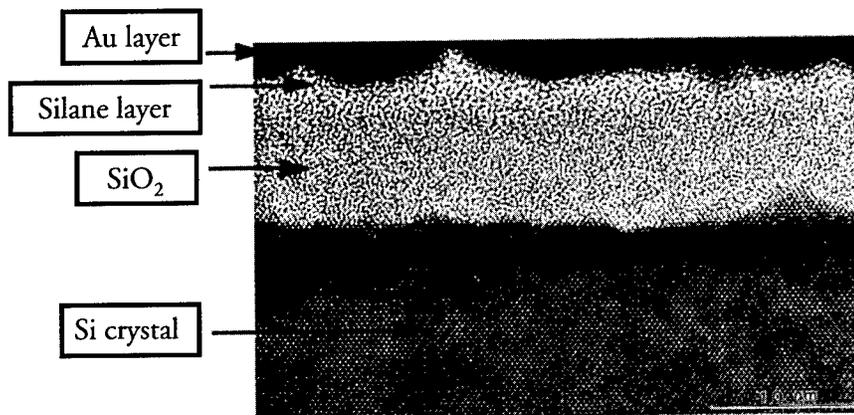
Figure 5: High resolution, cross-sectional TEM micrograph
of the wafer fracture side

This is not surprising, considering the chemical reactions that govern the deposition of silanes on silica[8]. Aminosilane molecules are of the general structure X_3Si-R-NH_2, with X being a hydrolyzable group that forms silanol groups (Si-OH) in solution. In the case of γ-APS the hydrolysis reaction can be described by the following chemical equation:

$$NH_2[CH_2]_3Si[OCH_2CH_3]_3 \rightarrow NH_2[CH_2]_3Si[OH]_3 \qquad (1)$$

At a subsequent step these hydrolyzed molecules undergo a condensation reaction described by the following chemical equation:

$$2\,NH_2[CH_2]_3SiOH \rightarrow NH_2[CH_2]_3SiOSi[CH_2]_3\,NH_2 + H_2O \qquad (2)$$

As a result, a cross-linked silane layer forms on top of the silica with the condensed monomers bonded to each other via siloxane bonds (Si-O-Si). Condensation also involves formation of siloxane bonds between the silane molecules and hydroxylated sites on the silica surface. This type of covalent bonding generally provides for a strong SiO_2/γ-APS interface and makes it energetically favorable for the crack to grow along the relatively weaker γ-APS/BCB interface. As

indicated by our results this has indeed been the case in the samples that we studied. It was the adhesion strength of the interface between the silane and the overlying BCB polymer that ultimately determined the measured fracture toughness of the overall structure.

To further investigate the mechanisms of adhesion strength enhancement and study the chain orientation and variations of chemical bonding in the silane layer, we performed ion etching combined with in-situ XPS analysis of the wafer side fracture surface. The XPS spectrum of this surface after removing 1.5-2 nm is shown in Fig. 6. The N (1s) peak has completely disappeared indicating a tendency for chain alignment with the (NH$_2$-) groups orienting away from the SiO$_2$ surface.

Element	Atom %
C	38
Si	44
O	18
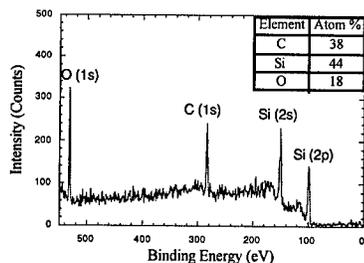
Figure 6: XPS spectrum of the wafer side fracture surface
after removing 1.5-2 nm via ion-etching

Furthermore, a higher energy resolution spectrum taken around the C (1s) peak and shown in Fig. 7 reveals that the C (1s) peak is composed of two sub-peaks corresponding to C-C and C-Si types of chemical bonding. The C-Si sub-peak was not detectable before ion etching, because the C atoms bonded to Si at the silane chain end closer to the wafer were initially buried under 1.5-2 nm of material containing mostly CH$_2$ groups (C-C type of bonding). The table on top of Fig. 7 contains information on sub-peak binding energy and FWHM, as calculated by fitting the experimental data using the software provided with the photoelectron spectrometer.

Bonding type	Peak position (eV)	FWHM (eV)
C-C	283.42	1.58
C-Si	281.83	1.69
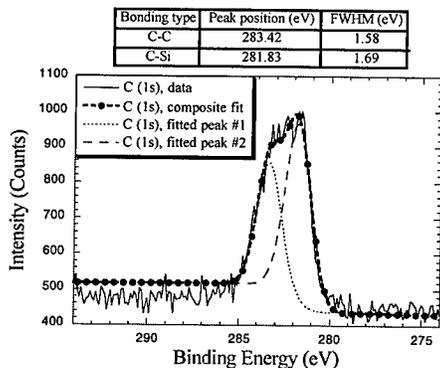
Figure 7: High energy resolution XPS spectrum taken around the C (1s) peak
after removing 1.5-2 nm via ion-etching

169

Silane chain orientation phenomena, generally termed electro-kinetic effects, have been observed and reported by other researchers as well. Plueddemann[9] investigated the effect of solution pH on γ-APS molecule alignment on a silica surface and reported that for pH higher than the SiO_2 IsoElectric Point of Surface (IEPS) the cationic (NH_2-) group was attracted by the surface and orienting towards it, and vice versa. We intend to study the processing parameters causing such chain orientation phenomena and their effect on interface adhesion in future work.

CONCLUSIONS

Addition of a γ-APS film at an SiO_2/BCB interface results in a 2.5x stronger structure. The weakest path through the reinforced structure is the γ-APS/BCB interface. The measured fracture toughness value G=48 J/m^2 is the debond energy of this interface. A preference for silane chain orientation with the amide group away from the wafer is documented. The process related mechanisms causing the above preferred orientation and their effect on the adhesion strength of the SiO_2/γ-APS/BCB interface structure will be investigated in future work.

ACKNOWLEDGEMENTS

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FE-MODELING AND PHYSICAL TESTING OF IGBTs FOR PRESS-PACKAGING

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ABSTRACT

The reliability of press-packed IGBTs strongly depends on the solutions adopted in terms of heat dissipation and thermo-mechanical stress management so as to guarantee satisfactory electrical and thermal contact conditions throughout the service life. In this paper, two aspects concerning the design process of a single-chip press-pack IGBT are outlined: i) cyclic stresses and strains occurring in the package and in the chip are discussed on the basis of finite element (FE) simulations, ii) a testing rig developed for accelerated testing of single IGBT chips under controlled contact pressure conditions is presented.

INTRODUCTION

The rapid evolution of semiconductor technology and the ever-increasing effort to reduce costs and development cycle time of high power, high voltage insulated gate bipolar transistor (IGBT) devices require the mechanical analysis for design/performance optimization and the reliability prediction of a new product to be carried out at the conceptual design stage. The press-packaging technology for IGBT assembly is based on the classical thyristor packaging technology: the IGBT and the diode chips are placed between two copper electrodes and pressure is used to obtain good electrical and thermal contact. As the power density of high power IGBT packages is more than one order of magnitude higher than in microprocessor packages, heat management and thermo-mechanical stresses become key reliability issues, especially when paired with demanding lifetime requirements of traction application, [1]. In order to mitigate the thermal expansion difference between the Si chip and the Cu electrode, an intermediate layered structure has to be devised with material selection based on electrical conductivity, coefficient of thermal expansion, thermal conductivity, stiffness and low cost, [1].

Previous finite element (FE) analyses [2, 3], recently corroborated by the work of [4], showed that non-uniform stresses develop on and inside the IGBT chip due to the assembly and the following thermal cycling. Locations potentially sensitive to thermo-mechanical fatigue and fretting conditions due to thermal cycling were identified. In this paper, a testing rig developed for accelerated testing of a single IGBT chip under controlled contact pressure conditions is presented. Pressure uniformity over the chip, one of the design requirements, is experimentally verified. A combined physical testing-FE analysis procedure has been used to assess the state of stress in the chip under power cycling.

SINGLE-CHIP DEVICE PRELIMINARY ANALYSIS

A 1700V-75A IGBT chip is the subject of this study. A schematic cross-section of the assembly is presented in Fig. 1. The emitter pole, washer and foil are made of nickel-plated copper, molibdenum and silver, respectively. The IGBT chip contains a 4 x 2 array of contact pads, Fig. 2. The soft contact foil with the corresponding array of contact pads is placed on the upper side of the chip so as to ensure a proper electrical contact and minimize pressure

distribution non-uniformity. A centering frame is used to prevent chip-housing misalignments. The clamping pressure is applied by a suitable loading system.
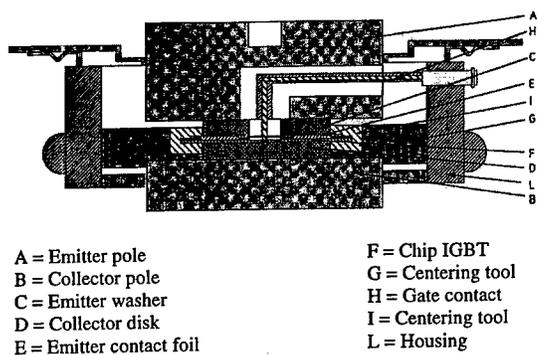
A = Emitter pole
B = Collector pole
C = Emitter washer
D = Collector disk
E = Emitter contact foil

F = Chip IGBT
G = Centering tool
H = Gate contact
I = Centering tool
L = Housing
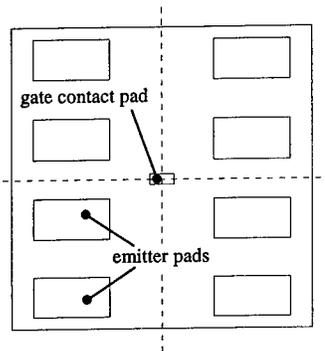
Fig. 1: cross-section of the single-chip IGBT assembly.

Fig.2: IGBT chip.

The finite element approach has been previously adopted to investigate the thermo-mechanical stresses in the module during thermal cycling and possible contact deterioration conditions during service life. Both simplified 2D and refined 3D FE models were used in the calculations. Details of the simulations can be found in [2, 3]. The results showed a contact pressure evolution, with relative slidings at the external edge of the chip-foil contact area that may lead to fretting, while cyclic stresses and strains in the chip and in the foil are high enough to generate thermomechanical fatigue.

SINGLE-CHIP TESTING RIG DEVELOPMENT

As the result summarized in the previous part indicated that deterioration of the chip and of the contact may occur, an accelerated testing procedure to assess the durability of the chip or its satisfactory performance with respect to the design requirements needs to be developed. The necessity to evaluate different solutions for geometries, materials and loading conditions called for the development of a flexible and dedicated testing rig. The basic design requirements were: i) nominal pressure on the chip pads up to five times the standard pressure level for IGBT devices; ii) contact pressure uniformity over the chip; iii) suitable connections for the electrical testing of the chip; iv) controlled heating of the chip to determine the V_{ce}-T_j relationship. The testing rig is shown in Fig. 3.

The contact force was applied with a 3 kN pneumatic actuator and the supporting frame was designed according to typical guidelines for press machines. Great attention was paid to contact probe geometrical design as it affects contact pressure uniformity. FE analysis of the chip-probe assembly guided the selection of the optimal diameter-to-height ratio, d/h in Fig. 4, of the contact probe. A spherical joint below the lower probe and a laterally flexible spring above the upper probe were introduced to compensate flatness tolerances. Also, a centering die holding the chip was required, Fig. 4.

During assembly of the rig, the actual uniformity of the contact pressure distribution was investigated using a pressure-sensitive film (Fuji Press-scale) placed between chip and contact foil. These polymeric films respond to an applied pressure with a change in color intensity. Therefore, to determine the pressure distribution over the chip-pad contact, the color distribution

of the film was digitized and converted via software to a pressure distribution according to the calibration curves supplied by the film manufacturer, [5]. A typical plot of the pressure distribution, p, is shown in Fig. 5.
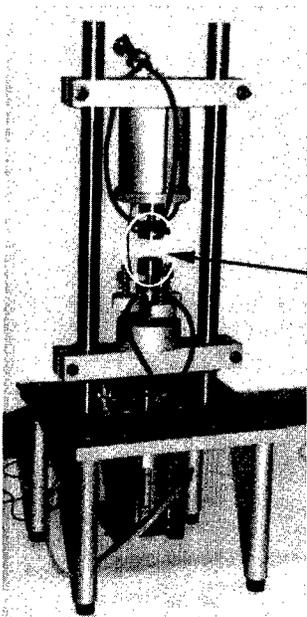
Fig. 3: single chip IGBT testing rig.
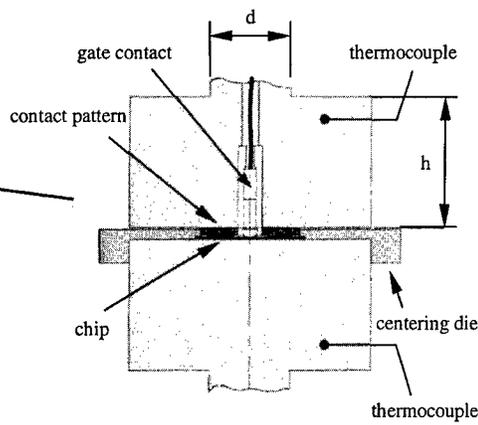
Fig. 4: detail of the contact probes.
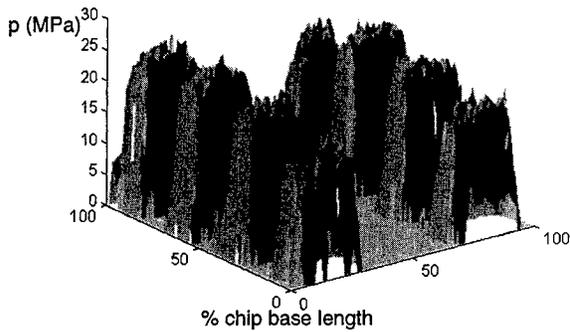
Fig. 5: pressure distribution on the IGBT chip.

COMBINED PHYSICAL TESTING AND FE MODELING

The testing rig has been developed with the aim of replicating the mechanical damage phenomena on the single chip subjected to the press-pack loading and to accelerated testing conditions such as in power cycling. For this reason, it is necessary to determine the state of stress in the chip under test. An uncoupled thermo-mechanical FE analysis of the testing rig in

operation was developed. The 2-D axysymmetric FE model of Fig. 6 reproduces the two probes with the chip and the related contact pattern in between. Physical properties for bulk materials taken from literature were used.

distributed load

convective heat exchange

upper temperature
control point (T_h)

heat generation, T_j

lower temperature
control point (T_l)

convective heat exchange

vertical restraints

symmetry axis
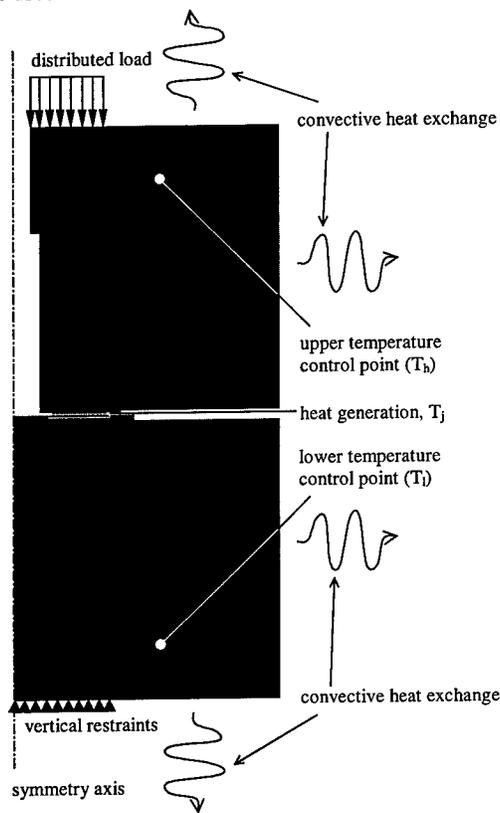
Fig. 6: thermal-mechanical FE model of the testing rig.

Critical was the definition of the boundary conditions. The electrically dissipated power within the chip was applied to the model as a constant heat generation rate attached to the elements corresponding to the semiconductor junction. Besides, the junction temperature T_j, measured by means of the V_{ce}-T_j relationship, has been introduced on the nodes at the junction. The temperatures T_h and T_l actually measured during physical testing at two points on the upper and lower probes, respectively, were used as reference data to tune the convective heat transfer coefficients applied to the external surfaces. Since the chip is not axysymmetric, those temperatures were also used to assess any angular orientation effect. It was found that away from the chip, the temperature field is axysymmetric.

The linear V_{ce}-T_j relationship at low current level (eg. 100 mA) was determined according to the procedure outlined in [6]. In this case, the chip was heated by an external source at temperatures ranging from 20 to 120 °C. In the power cycling, the collector current I_c during the off phase has been set to the same value (100 mA) used in the calibration, which gave directly

the value of T_j. Instead, during the heating phase short negative pulses have been superimposed every 5 s to I_c in order to reach the level of 100 mA at which to acquire V_{ce}. The temperature transient measured with this technique is shown in Fig. 7 along with the related V_{ce}-T_j calibration curve. The instrumentation consisted of a HP6684A programmable current supply for I_c and a LeCroy 9361 digital osilloscope for V_{ce} acquisition and current checking. The temperatures T_h and T_l in the two check points on the upper and lower probe, respectively, are measured by two k thermocouples.
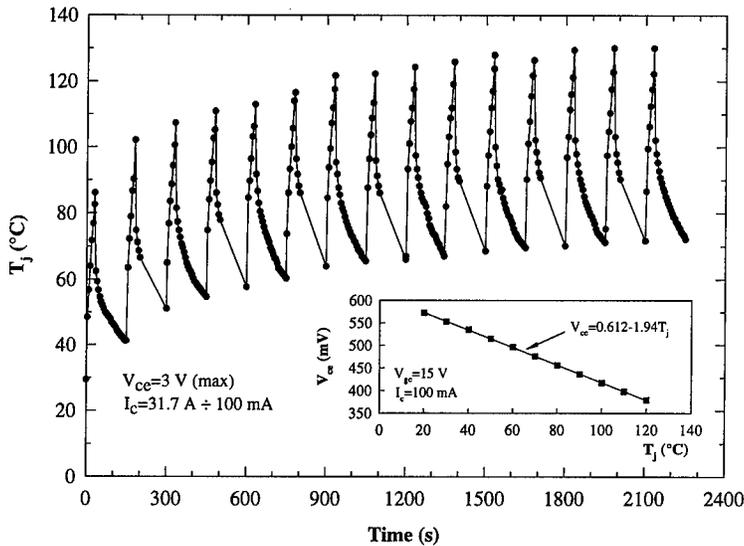
Fig. 7: T_j during power cycling measured by means of the V_{ce}-T_j relationship (see box).

Since stresses and displacements transmitted between contacting bodies are history-dependent, the whole transient of Fig. 7 had to be simulated to get the steady-state cyclic variation. To reduce the computational burden while retaining enough information on the stress/strain evolution, the first two cycles have been simulated. The heat exchange coefficients were tuned so that the values of T_h and T_l differed by less than 3% from the experiments (see Fig. 8). For the subsequent mechanical analysis suitable contact conditions were specified, see [2, 3]. After a first step where the effect of the assembly pre-loading (i.e. a nominal uniform pressure of 15 MPa) were determined, the computed transient temperature field associated to the two power cycles was applied to the FE model. The resulting contact pressure evolution is shown in Fig. 9. A strongly non-uniform distribution develops so that the points on the outer edge are no longer in contact in accordance with the trend found in [7] for a thermal cycling simulation. It is worth to remark that in the power cycling simulation the whole region encompassing the chip, the contact foil and the probe surfaces was practically at a constant temperature, thus it is actually undergoing a thermal cycling. At this stage of the work, it is important to underscore that the temperature fields in the rig and the related mechanical stresses can be predicted with the procedure presented and that the calculated trends agree with those obtained in the FE simulation of [2, 3, 7]: the damage mechanisms in the module can be replicated in the rig. Future computational developments will attempt to predict the influence of the contact pressure, material properties and power cycling parameters on chip degradation mechanisms.
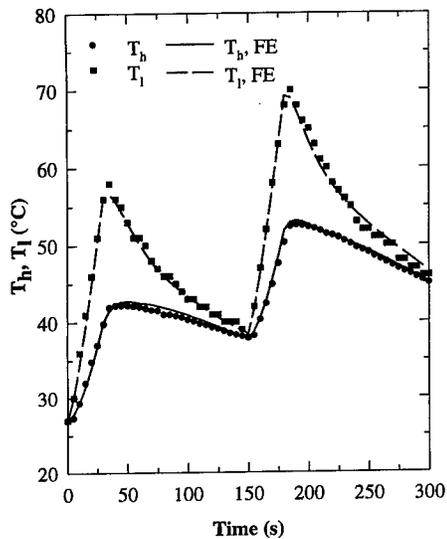
Fig. 8: experimental and computed temperatures during the first two cycles.
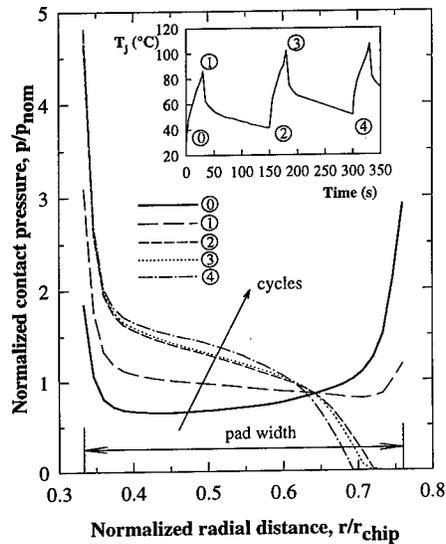
Fig. 9: evolution of contact pressure during the first two cycles.

CONCLUSIONS

Experimental and computational activities aimed at supporting press-pack IGBT design and development have been reported in this paper. A testing rig for accelerated testing of single IGBT chips under controlled thermal-electrical-mechanical conditions has been developed. A parallel modeling effort demonstrated that the thermomechanical stresses resembles those in the device: contact deterioration can be replicated in the rig.

ACKNOWLEDGMENTS

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Part V

III-V Processing and Growth

DYNAMICS OF WET OXIDATION OF HIGH-AL-CONTENT III-V MATERIALS

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ABSTRACT

Oxidation of layers of high-Al-content III-V materials by water vapor has become the enabling process for high-efficiency vertical cavity surface emitting lasers (VCSELs) and has potential applications for reducing substrate current leakage in GaAs-on-insulator (GOI) MESFETs. Because of the established importance of wet oxidation in optoelectronic devices and its potential applications in electronic devices, it has become increasingly important to understand the mechanism of wet oxidation and how it might be expected to affect both the fabrication and subsequent operation of devices that have been made using this technique. The mechanism of wet oxidation and the consequence of this mechanism for heterostructure design and ultimate device operation are discussed here.

INTRODUCTION

The rapid oxidation of AlGaAs with high aluminum mole fraction (>85% Al) using flowing H_2O/N_2 gas mixtures [1] is an enabling technology for high-efficiency vertical cavity surface emitting lasers (VCSELs). Threshold currents below 10 μA and threshold voltages only 50 meV above the emitted photon energy have been obtained [2] Wet-oxide-based VCSELs have even demonstrated greater than 50% wall-plug efficiency [3]. The wet oxidation process is also being studied for electronic applications such as gallium-arsenide-on-insulator (GOI) metel semiconductor field effect transistors (MESFETs) [4] and metal-insulator-semiconductor field effect transistors (MISFETs) [5]. If such devices are to go beyond laboratory demonstration to widespread commercial availability, it is imperative to understand the many factors that influence the extent of oxidation in a particular device and the influence of wet oxidation on relevant device properties. To first order, oxidation rates are determined by Al mole fraction. However, additional effects related to layer thickness and the nature of the adjacent layers in a device can dominate over mole-fraction effects. Alteration of adjacent unoxidized layers due to the generation of elemental As during the oxidation process can change important optical and electronic properties of a device. A mechanism for wet oxidation and the consequence of this mechanism for heterostructure design and ultimate device operation are discussed here.

EXPERIMENT

Prior to lateral wet oxidation of Al-III-V heterostructures, the Al-containing layer is exposed by etching a mesa structure to expose the layer to be oxidized. Wet oxidation is usually performed between 375 and 500 °C in a tube furnace with a water-saturated nitrogen stream passing over the sample to be oxidized [6]. Oxidation begins at the exposed edges and proceeds inward. Because of the strong temperature dependence of the oxidation, a three-zone furnace is especially desirable for well-controlled oxidation profiles. Water temperature and gas flow can be varied to control the supply of H_2O reactant to the exposed layer edges. Typically, water temperatures between 75 and 95 °C are employed. The oxidized length can be determined either optically (for sufficiently deep oxidations) or using scanning electron microscopy (SEM). Lateral

oxidation results presented here were obtained with 80 ±0.5 °C water and a flow rate of 3.0 slm through a 4"-diam. 3-zone tube furnace.

The Raman spectra presented here employed planar 2-μm-thick $Al_{0.98}Ga_{0.02}As$ layers on GaAs that were oxidized from the surface down rather than laterally from an exposed edge [7]. Prior to wet oxidation, a 300-Å GaAs cap was selectively removed using a citric acid/peroxide mix [5:1 of (1g citric monohydrate/1g H_2O):30% H_2O_2]. Samples were heated to the reaction temperature (400<T<455 °C) in dry nitrogen. The nitrogen flow (0.4 slm, 2-in. diam. tube) was then switched to bubble through 80 ± 1 °C water. The reaction was terminated by switching to a dry nitrogen flow. Raman spectra were measured in the x(y',y'+z')x̄ backscattering configuration (y' and z' parallel to (110) planes) using 514.5-nm light at < 85 W/cm^2.

RESULTS AND DISCUSSION

To first order, oxidation rates are determined by the Al mole fraction in the oxidizing layer. (Fig. 1). However, the time dependence of the reaction rate for samples with identical Al mole fraction has been observed to vary depending on individual processing conditions. Many workers operate in a reaction-rate-limited regime (linear time dependence) to facilitate more precise control of oxidized depth in device structures and others report diffusion-limited behavior (parabolic time dependence). Extrapolations of oxidized depth vs. time curves often fail to pass through the origin, with deviations in both directions having been reported. This complicates mechanistic interpretations. However, sufficient information is available about the temperature and composition dependence of wet oxidation rates to support the following understanding of the important dynamic characteristics that determine the time dependence.
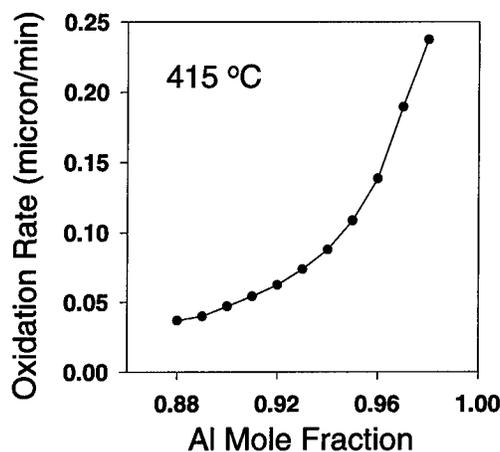
Fig 1. Composition dependence of wet oxidation

The Deal and Grove model for oxidation [8] describes the temporal dependence of an oxidation process as the sum of a linear and a parabolic term,

$$\frac{d^2}{k_{diff}} + \frac{d}{k_{rxn}} = t \qquad (4),$$

where the linear term dominates when the oxidation rate is reaction-rate limited and the parabolic term dominates when the rate is diffusion limited. A range of dependences on time have been reported for wet oxidation of AlGaAs. The oxidation of the most preferred device composition of $Al_{0.98}Ga_{0.02}As$ is generally reported to be linear from 380 to 440 °C [6], while the oxidation of AlAs has been reported to have a parabolic dependence from 370 to 450 °C [9]. Another study of AlAs has reported a linear time dependence at 356 °C , a parabolic depencence at 516 °C, and a mixed linear/parabolic dependence at intermediate temperatures [10]. Yet another study of AlAs has shown linear dependence at T ≤ 350 °C and parabolic behavior at T ≥ 375 °C [11].

To explain why a shift occurs between reaction-rate-limited and diffusion-limited regimes, it is necessary to have an understanding of the chemical nature of the reaction. Raman studies of partially oxidized planar AlGaAs structures always show the presence of a significant amount of elemental As that has been liberated during the oxidation process. Raman spectra of partially oxidized films are dominated by crystalline elemental As peaks at 198 and 257 cm^{-1} and a broad feature between 200 and 250 cm^{-1} peaking near 227 cm^{-1} due to amorphous As [12]. At higher reaction temperatures, significant amounts of As_2O_3 are also detected. The broad feature centered at 475 cm^{-1} is due to amorphous As_2O_3 [13]. This species, if present, is below the Raman detection level for oxidations performed at 400 and 425 °C, but it is observed at relatively constant levels throughout the oxidation at 450 °C (Fig 2). As the oxidation front advances into AlAs or AlGaAs films, one observes a relatively constant Raman signal from As and $a-As_2O_3$ while the intensity of the AlAs-like phonon steadily decreases as the AlGaAs is converted to oxide [14].
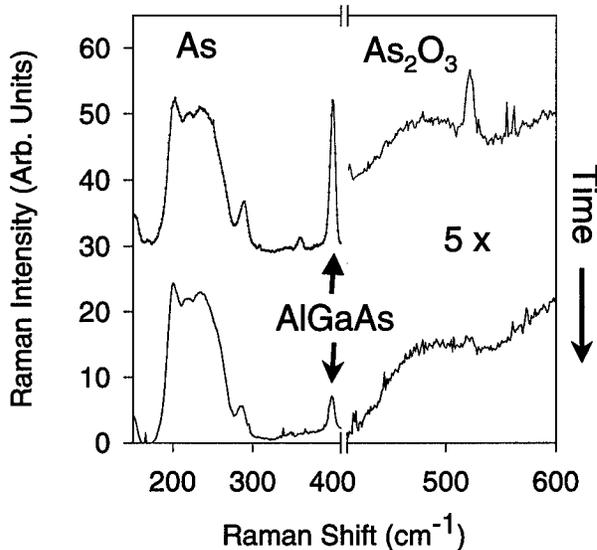
Fig. 2. Time evolution of Raman spectra of 2 μm layer of $Al_{0.98}Ga_{0.02}As$ oxidizing at 450 °C.

181

Due to the strong ability of low-oxidation state Al to donate electrons to other atoms, H^+ from water can serve as the oxidizing agent for the reaction. In the process, H^+ becomes zero-valent H^0 and can serve as a reducing agent for another species. Both As_2O_3 and As are present as intermediates in the wet oxidation process. Their presence can be explained as follows.

Water has been shown to adsorb dissociatively on AlAs at 100 K under UHV conditions to produce Al-O, Al-OH, and As-H type species on the AlAs surface [15] Since literature values for the thermodynamic quantities of these surface species are unavailable, we have chosen to employ the molecular analogs [16], leading to Eqns. 1 and 2 at a reaction temperature of 425 °C.

$$2\ AlAs + 6\ H_2O_{(g)} = Al_2O_3 + As_2O_{3(l)} + 6\ H_2 \qquad \Delta G^{698} = \text{-473 kJ/mol} \qquad (1)$$

$$2\ AlAs + 6\ H_2O_{(g)} = Al_2O_3 + 2\ AsH_3 \qquad \Delta G^{698} = \text{-451 kJ/mol} \qquad (2)$$
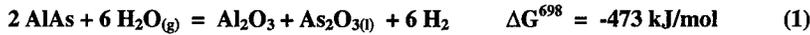
Under these typical wet oxidation conditions, one would expect both reactions to proceed readily. At 425°C, further reaction of As-H can decompose to give As and H_2, as suggested by the Raman spectra (Eqn 3). It can also react with water to produce As_2O_3, but the free energy change is quite small (Eqn. 4). Given the low-temperature UHV results, it is likely that the As_2O_3 observed results from the combination of reactions like Eqn 2 and 4. Both AsH_3 and As_2O_3 can be readily converted to elemental As (Eqns. 3 and 5).

$$2\ AsH_3 = 2\ As + 3\ H_2 \qquad \Delta G^{698} = \text{-253 kJ/mol} \qquad (3)$$

$$2\ AsH_3 + 3\ H_2O = As_2O_3 + 6\ H_2 \qquad \Delta G^{698} = \text{-22 kJ/mol} \qquad (4)$$

$$As_2O_{3(l)} + 3\ H_2 = 2\ As + 3\ H_2O_{(g)} \qquad \Delta G^{698} = \text{-131 kJ/mol} \qquad (5)$$

The transition from reaction-limited (linear) to diffusion-limited (parabolic) behavior for a particular AlGaAs composition will depend on the relative temperature dependences of Eqn. 1-5 as Ga is substituted for Al. Experimental results to date suggest that Eqn. 1 becomes increasingly important for higher Al contents and higher reaction temperatures.

Fig. 3. Schematic of effect of increase in rate of As_2O_3 formation relative to its reduction to As for removal to leave behind a porous As_2O_3 film.

The relationship between the rate of formation and conversion of As_2O_3 to As (Eqn.1,4, and 5) and the rate of loss of As from the oxidized layer to leave behind a relatively As-free, porous AlO_x matrix will determine the time dependence of the oxidation rate (Fig. 3). The existence of a thin, dense, amorphous region of a few nanometers thickness has been observed at the oxidation front by transmission electron microscopy (TEM) [17]. Behind this dense region is a less dense region of amorphous $(Al,Ga)_2O_3$ that extends back to the exposed mesa edge. The time-evolution of the thickness of the dense region will determine whether linear or parabolic behavior dominates. When the removal of As is sufficiently fast to balance the rate of formation of As_2O_3, a relatively constant thickness of dense oxide consisting of Al_2O_3 and As_2O_3 will be found near the oxidation fronts it moves deeper into the layer; this will produce the relatively constant As_2O_3 Raman intensity observed in films that were partially oxidized at 450 °C. Under these conditions, a linear time dependence will appear because the diffusional contribution to the reaction rate does not increase significantly as the front moves deeper into the layer for typical reaction times. For long reaction times, the deviation from linearity will become increasingly apparent. If reaction conditions are changed to preferentially increase the formation of As_2O_3 relative to As loss, a steadily increasing thickness of the dense, As_2O_3-containing layer will form and the diffusion-limited parabolic time dependence will become dominant.

The transition from linear to parabolic behavior should be favored by conditions that increase the rate of Eqn. 1 relative to that of Eqn. 5. The greater amounts of As_2O_3 seen in the Raman spectra for oxidation at 450 °C vs. 425 °C and the relatively constant As signal under the two conditions (Fig. 4) suggest that higher temperatures preferentially enhance Eqn. 1 vs. Eqn. 5 for $Al_{0.98}Ga_{0.02}As$. The transition from predominantly linear to predominantly parabolic with increasing temperature has been previously been reported for AlAs [9-11].
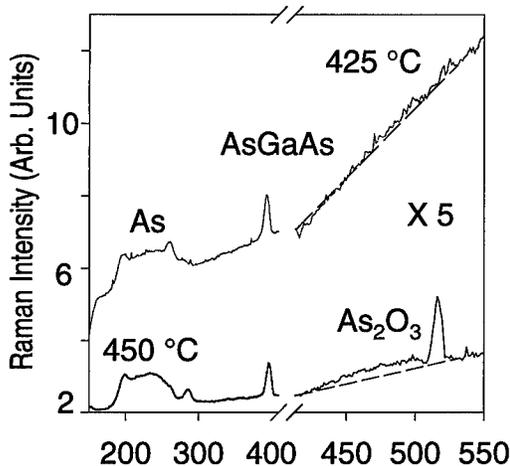
Figure 4. Temperature dependence of Raman spectra a 2 μm layer of $Al_{0.98}Ga_{0.02}As$.

Replacing Al with Ga in $Al_xGa_{1-x}As$ will affect the favorability of Eqn. 1 and 2, since ΔG^{698} for Eqns. 1 and 2 for GaAs are respectively +10 kJ/mol and +32 kJ/mol, and may thereby retard wet oxidation as Ga content increases. In contrast, Eqns. 3-5 do not explicitly include either Al or Ga. Consequently, the reduction of As_2O_3 to As should be relatively independent of the Al/Ga ratio. One would, therefore, expect that there might be a change in the time dependence of the total wet oxidation reaction when the rates for Eqn. 1-2 are increased or decreased faster than the rates for Eqn. 3-5. For example, the slower rate of Eqn. 1 for higher Ga-content AlGaAs could produce linear behavior under some conditions that produce parabolic behavior for higher Al-content material. This has, in fact, been observed during oxidation of a structure containing 45-nm layers of both 98% and 94% AlGaAs oxidized at 440 °C (Fig. 5). In contrast, the slower rates of formation of As_2O_3 from both compositions at 400 °C permits the reduction and loss of As to keep pace with the oxidation process, and linear behavior is observed for both compositions. The transition from reaction-limited to diffusion limited for these samples lies between 0.2 and 1.3 μm/min oxidation rates for the H_2O temperature and flow rate employed (3.0 slm in a 4"-diam. furnace, 80 ± 0.5 °C H_2O).
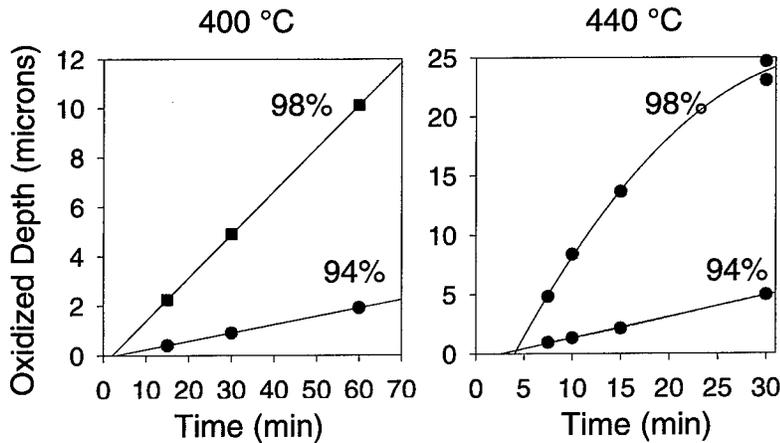
Fig. 5. Temperature dependece of the oxidation of 450-Å layers of $Al_{0.09}Ga_{0.02}As$ and $Al_{0.94}Ga_{0.06}As$ within the same sample.

Two additional device design characteristics can have a profound effect on the oxidation rate of a specific layer of AlGaAs as its Al mole fraction. These are the thickness of the layer to be oxidized and the close proximity of a more rapidly oxidizing layer. Under some conditions, both can prove more important than Al mole fraction in detemining the relative oxidation rates of different layers in the same structure.

The dependence of oxidation rate on layer thickness is illustrated in Fig. 6 for $Al_{0.98}Ga_{0.02}As$ and $Al_{0.94}Ga_{0.06}As$ oxidized at 425 °C under conditions that yield a linear time dependence for thick layers. For layers thicker than 75 nm, there is very little dependence on layer thickness. In contrast, there is a rapid drop-off of the oxidation rate as the layer thickness decreases below 75 nm. The decrease in oxidation rate as the layers become thinner is sufficient to invert the relative oxidation rates for higher and lower Al-mole-fraction materials when a relatively thick layer of lower Al content is compared to a thin layer of higher Al content. The

184

mechanism of this decrease in rate has not been definitely identified. It has been suggested that
the decrease in very narrow channels is related to the vapor transport coefficient at the gas-oxide
interface [18]. An alternative modal has been proposed based on the surface energy of the
curvature observed at the oxide tip [19]. The latter model assumes identical contact angles at the
top and bottom interfaces; however, a pronounced asymmetry is generally observed, with the
contact angle generally being greater at the top interface [17]. In addition, the activation energies
so derived are unusually large compared to other literature values. Hence, the gas transport
model, though not quantitatively evaluated, appears preferable at this time.
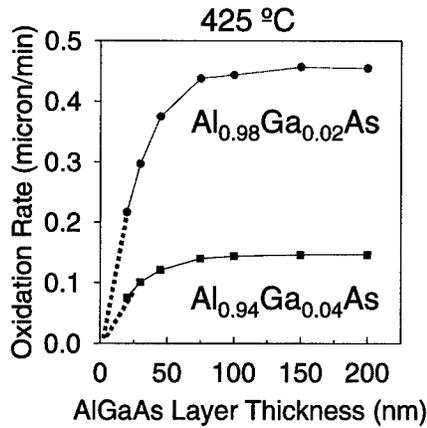
Fig. 6. Thickness dependence of the wet oxidation rate of AlGaAs.
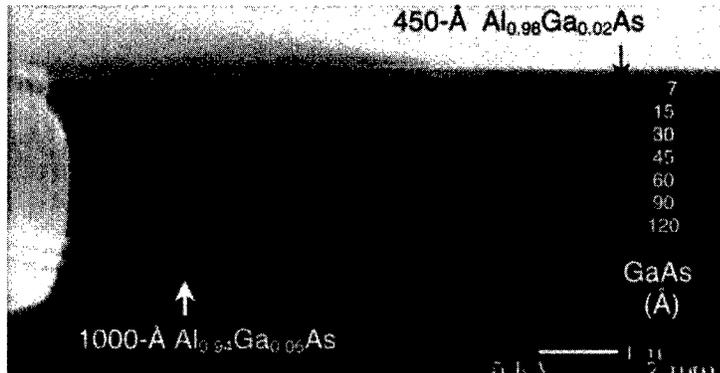
Fig 7. Cross sectional SEM of a partially oxidized (400 °C, 90 min) sample of alternating 450
Å layers of $Al_{0.98}Ga_{0.02}As$ and $Al_{0.94}Ga_{0.06}As$ seperated by GaAs barriers with thicknesses
varying from 120 Å near the substrate to 7 Å near the surface. Dark regions are oxide, light
regions are unoxidized.

The oxidation rate of a lower-Al-content layer can be appreciably increased when it is in close proximity to a faster-oxidizing layer. The effect of such close-proximity faster-oxidizing layers [14] is shown in Fig. 7 for 45-nm layers of undoped $Al_{0.94}Ga_{0.06}As$ separated from 45-nm layers of undoped $Al_{0.98}Ga_{0.02}As$ by thin layers of undoped GaAs (0.7, 1.5, 3, 6, 9, and 12 nm) oxidized at 400 °C for 90 min. Although no enhancement of the reaction of the $Al_{0.94}Ga_{0.4}As$ layer is observed after this reaction time with 9 and 12 nm barriers, there are progressively greater enhancements of the oxidation of the $Al_{0.94}Ga_{0.06}As$ layers that are separated for the already oxidized $Al_{0.98}Ga_{0.02}As$ by 6, 3, 1.5, and 0.7 nm GaAs layers. All $Al_{0.94}Ga_{0.06}As$ layers exhibit rate enhancements at longer reaction times. The oxidation of the $Al_{0.94}Ga_{0.06}As$ layers can be modeled as the sum of the unenhanced rate plus a contribution derived from the diffusion of something into the layer from the already oxidized adjacent layers [20]. The close-proximity enhancement is not significant only in the presence of barriers. Structures with graded compositions result in profiles that show appreciably deeper oxidation than expected from compositional effects alone [21]. This proximity enhancement is especially important since compositional grading is used to fabricate tapered oxide current aperatures for optimum VCSEL performance [6,22] and to minimize stresses in the oxidized devices.

Because elemental As is a major product in wet oxidation, it is necessary to consider its influence on important device properties. The presence of large amounts of elemental As at the oxide/semiconductor interface will result in the injection of As interstitials, As_i, into the adjacent unoxidized semiconductor. It will also lead to the generation of additional types of point defects [23]:

$$As^0 \leftrightarrow As_i$$
$$As^0 \leftrightarrow GaAs + V_{Ga}$$
$$As_i + Ga_{Ga} \leftrightarrow As_{Ga} + Ga_i$$
$$As_i + V_{Ga} \leftrightarrow As_{Ga}$$
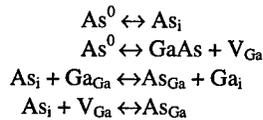
Reaction of As with the surface GaAs can lead to the generation of Ga vacancies, V_{Ga}. Interstitial As can diffuse into the material and generate Ga interstitials by displacement to form As antisite defects, As_{Ga}. Antisite As_{Ga} can also form by reaction with Ga vacancies. The increased concentrations of these point defects can be quite deleterious for devices made using wet oxidation.

The most gross evidence for the large quantities of point defects that are produced during wet oxidation is the appearance of As precipitates quite remote from the original oxidation. Such As precipitates have been observed widely dispersed through the adjoining layers and even segregated at the GaAs surface of a wet-oxidized sample [24]. Precipitates have also been reported in the InGaAs channel of a GOI MESFET that had a 10 nm $Al_{0.25}Ga_{0.75}As$ layer interposed between the channel and the oxidized layer [25].

The photoluminescence from quantum wells that are near wet-oxidized regions exhibits changes that are typically seen in the presence of excessive numbers of point defects. The photoluminescence is decreased for quantum wells (QWs) situated 20 and 40 nm from oxidized

AlAs [26]. The time and temperature dependence of this degradation is consistent with the presence of oxidation-generated point defects that have diffusivity comparable to As in GaAs. Post-oxidation hydrogen treatment partially restores the photoluminescence intensity from GaAs quantum wells separated from the oxidized layer by 25-nm AlGaAs spacers. [27] While oxidation reduces the PL intensity to 6% of the original intensity, post-oxidation H-annealing restores the intensity to 67% of its original level. Such PL restoration is to be expected from hydrogen passivation of As-associated deep levels, e.g., As_{Ga}, that were formed during oxidation by indiffusion of excess As.

Intermixing at quantum well interfaces by heating is seen to be greater near oxidized AlGaAs regions than near unoxidized regions of the same device. However, even the QW emission from the regions that are not immediately above or below oxidized material exhibit a blue-shift. Such behavior is expected if there is increased mobility of column III atoms in the presence of excess As [28]

In addition to the observation of As precipitates in the InGaAs channel of a GOI MESFET, a deterioration of both the mobility and the free carrier concentration is obtained following oxidation . This deterioration was minimized by decreasing oxidation temperature and/or oxidation time [25]. Both process alterations would reduce the diffusion of As-derived defects into the device, thereby minimizing device degradation.

SUMMARY

Wet oxidation of high-Al-content AlGaAs produces both elemental As and As_2O_3 as important products that can remain near the reaction front. The thickness of the As_2O_3-containing region at the oxide/semiconductor interface will determine the time-dependence of the process. A shift from reaction-rate-limited (linear) to diffusion-limited (parabolic) time dependence is favored by increasing temperature or increasing Al mole fraction. The elemental As that is produced in the reaction acts as a source of defects that can affect important chemical and electrical properties of devices. Free As is an inherent part of the wet oxidation process that cannot be totally avoided so applications of these oxides must either not depend strongly on concentrations of point defects in the material or attempts must be made to design around the endemic As problem.

ACKNOWLEDGMENTS

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IN SITU MONITORING OF III-V PROCESSING

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ABSTRACT

Fabrication of high performance III-V devices and integrated circuits depends on careful control of layer thicknesses and compositions in the as-grown epitaxial layers and in the etching of these layers. The relatively high value of compound semiconductor devices (compared with high-volume Si devices) makes the use of advanced process control (with expensive *in situ* sensors) potentially advantageous. Considerable attention has been given to the problems of real-time feedback control of MBE growth systems. In this paper, I will discuss experiences with use of both *in situ* and *ex situ* monitors for controlling reactive ion etching (RIE) of III-V materials. Specific examples from an electron cyclotron resonance (ECR) RIE base contact etch from an AlInAs/GaInAs HBT process will be given. The relative merits of reflection-based wafer sensors vs. process state sensors (optical emission spectroscopy and mass spectroscopy) will be discussed. The unique opportunities and problems associated with the III-V materials and required etch processes will be contrasted to implementation of advanced wafer state endpoint detection schemes in Si and flat panel display processes. Specific problems and solutions from our research which I will discuss include chamber seasoning effects on the drift of optical emission based endpoint detection schemes and signal processing techniques for accounting for this drift, modeling of the optical dielectric function of the compounds of interest vs. composition, and the effects of surface roughness on optical thickness measurements.

INTRODUCTION

Advanced process control (APC) based on in situ and in line monitors (sensors) is being pursued by researchers in all aspects of thin-film technology (Si VLSI, compound semiconductor devices, flat panel displays, advanced optical coatings, etc.) to improve process margins with the coupled goals of improving the manufacturability of leading-edge devices and reducing costs. In compound semiconductor fabrication, in situ monitors and real-time feedback control have been relatively aggressively applied to epitaxial growth control for both MBE and OMCVD reactors.[1,2,3,4,5] This is a very sensible starting point, as the quality of the epitaxial layers is certainly the most critical factor in the manufacture of high performance compound semiconductor devices. However, many of these device structures also require careful control of either dry or wet chemical etches to expose layers for application of ohmic contacts and Schottky gates. Less attention has been paid to the problems of etch control in III-V compound materials. In this paper, I will address some of the issues and possible solutions for high-accuracy etch endpoint detection.

To effectively implement in situ sensor-based APC schemes, it is, of course, necessary to have the in situ sensors and related equipment controller hardware and software. Also, it is important to have available effective ex situ, in-line measurement systems. These systems are needed both to verify the effectiveness of the in situ based systems and to provide

complementary measurements which cannot be performed in situ. In Si VLSI fabrication, rapid, nondestructive, in-line measurements are commonly used to monitor film thicknesses and linewidths on sampled product lots as part of routine statistical process control (SPC) schemes. In research and development, the Si VLSI industry is moving toward implementation of batch-to-batch and wafer-to-wafer control (two variations of run-to-run control) by increasing the use of in-line metrology. In III-V device fabrication, the most common process control approach is to develop individual unit process using relatively simple test structures and to evaluate the processes using relatively sophisticated measurements including high resolution X-ray diffraction (rocking curves), photoluminescence, photoreflectance, etc; however, relatively few in-process measurements are typically performed on device wafer prior to electrical test. As one of the results of our process control efforts, I will illustrate the use of a common Si in-line metrology tool, the microscope-based spectral reflectometer, for use in compound semiconductor process monitoring.
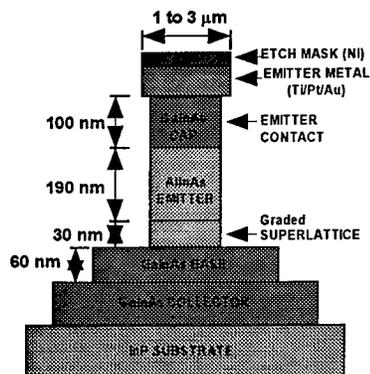
Figure 1 Schematic cross section of the HBT device which was the subject of this process control project.

The experimental results which I will discuss in this paper were primarily the result of an effort to control the dry etching of a self-aligned base contact etch in a Hughes Research Laboratories (HRL, Malibu, Ca.) InP-based heterojunction bipolar transistor process.[6] The device cross-section is shown in Figure 1. The critical requirements for this process were to etch through the GaInAs cap, AlInAs emitter, the graded GaInAs/AlInAs superlattice (SL), and finally to stop in the GaInAs base with no more than 5nm of over-etch. The accuracy with which this goal could be achieved would determine the minimum allowed base width and, thus, would be a major determining factor in the high frequency performance of the HBT. Also, since the base contact metallization was to be applied in a self-aligned approach, a controlled undercut of the emitter contact metal was also needed. Finally, the dry etch need to be performed in a low damage mode. The electron cyclotron resonance (ECR) dry etch process developed at the University of Michigan to address this problem has been documented elsewhere.[7] In this paper, I will restrict the discussion to the successes and failures of the in situ and in-line sensors employed in the process control effort, and to a discussion of possible improved solutions for problems of this type.

EXPERIMENT

The ECR-based dry etch system with the in situ monitors which we employed is illustrated schematically in Figure 2. The etch system was built by PlasmaTherm, Inc. and incorporate a 2.45 GHz ECR source from Wavemat, Inc. The wafer chuck was mechanically-clamped and He-backside cooled, and could be raised and lowered via a bellows arrangement to enable optimization of the wafer position relative to the ECR source. The wafer could be separately biased with a 13.56 MHz RF source. The process used for all of the etch experiments described in this work used an Cl_2/Ar chemistry.[7]

IN SITU MONITORS

To perform automated endpoint detection for the base contact etch, we installed three in situ monitoring devices
1. A differentially-pumped quadrupole mass spectrometer (QMS);
2. A monochromator-based optical emission spectrometer (OES);
3. A dual-λ reflectometer.

These systems are illustrated in Figure 2. The QMS was a MKS PPT system which uses an open source ionizer, 6.3mm quadrupole rods, and an electron multiplier detector. Process gas was sampled into the QMS through a small port in the chamber near the typical level of the wafer. Due to the variable vertical position of the wafer chuck, it was not easily possible to place a sampling port for the QMS very close to the wafer itself during the etch.

The OES system was constructed using a Spex 500M 0.5 meter Czerny-Turner monochromator, a room temperature Hammamatsu R636 GaAs-photocathode photomultiplier tube (PMT), and a Stanford Research 570 low noise current preamplifier. A multi-stranded quartz optical fiber was used to bring light to the monochromator. The fiber bundle was arranged in vertical line and focused onto the entrance slit of the monochromator to maximize the signal strength. This arrangement was used (rather than a multi-wavelength array detector) to provide the maximum possible signal to noise ratio for a single emission species.

The reflectometer system (illustrated in Figure 3) was designed and constructed using a polarizer-photoelastic modulator (PEM)-polarizer system to provide high-frequency (100KHz) amplitude modulation of the probe beam and the reflected beam was demodulated using a pair of SR850 lockin amplifiers. This arrangement gave good signal to noise ratios using a 75W Xe lamp source with the sample approximately 1 m from the beam-splitter. A lamp source was used rather than lasers to permit optimization of the probe wavelengths to the regions of maximum index differences between the layers of interest. There are relatively large differences in the refractive indices of AlInAs and GaInAs at Hg emission lines; therefore, we intended to perform the base endpoint experiment using a Hg lamp. The experimental performance of this system on a polycrystalline Si test sample and the theoretical performance on the HBT are shown in Figure 4. Two wavelengths were employed rather than the more common single wavelength arrangement (typically HeNe laser-632.8 nm) to improve the sensitivity. As in the case of the OES system, discrete PMT detection was used to maximum the SNR at the expense of the additional information available from spectral measurements. The reflectometry system was deployed in a normal-incidence configuration due to the vertical movement of the wafer stage

191

(which precluded the use of a pair of off-normal "ellipsometry" ports for specular reflection measurements).

The basic rational was that the QMS and OES systems would provide chemical process state information on the plasma environment and that the dual-λ reflectometer would provide real-time information on the remaining film thickness during the etch. In principle, any one of the in situ monitors should have been able to detect the transition from the AlInAs layer to the GaInAs layer by sensing either the presence of Ga (for the two chemical process state sensors) or the change in the reflection (for the reflectometer). The apparent challenges for all three monitors lay in the speed and accuracy, and the problem of detecting the non-abrupt transition from the graded AlInAs/GaInAs SL into the GaInAs base layer.
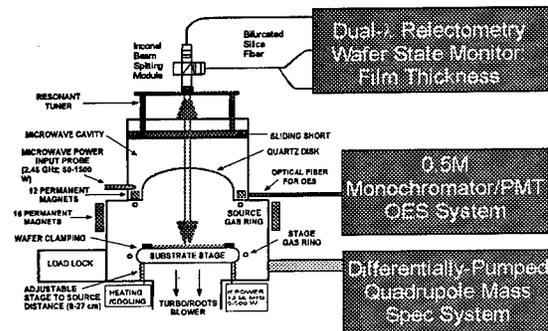
Figure 2 Illustration of ECR etch system used in the HBT control project and in situ monitors employed.
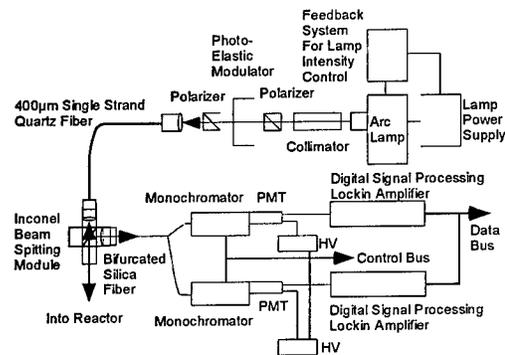
Figure 3 Cross-polarizer/PEM dual-λ reflectometer for in situ film thickness monitoring.

IN-LINE MONITORS

To provide routine film thickness measurements for evaluation the endpoint detect schemes, we modified the software of a commercial microscope-based spectral reflectometer system (a Leitz MPV-SP). The software was modified to allow arbitrary layer structures to be input into the optical modeling routines. The hardware itself was not modified. The system provided measurements of the sample reflectance vs. wavelength over the 400-800nm spectral range using a scanning monochromator-PMT arrangement. We also added a computer controlled scanning stage for late in this work. The measurement spot size could be varied from as small as 1x1μm (using a 100X objective) to larger sizes. We typically used a 100x100 μm spot size delivered through a 10X objective. Newer systems from a variety of manufactures (KLA-Tencor, Nanometrics, Leica, and others) offer these capabilities without modification, but are not yet commonly used in compound semiconductor efforts. The use of a microscope-based reflectometer for ex situ film thickness measurement is advantageous both for mapping of sample uniformity over a wafer and for performing measurements in nominally uniform regions (away from contacts or other topography). Also, these measurements could be made at a time of only a few seconds per measurement spot.
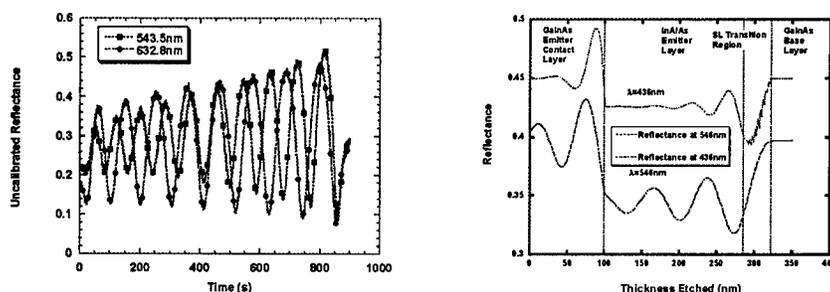
Figure 4 Experimentally measured response of dual-λ reflectometer on a poly Si/SiO₂/Si test sample etch in a Cl₂ environment in the ECR (left) and the theoretical response of the reflectometer for the AlInAs/GaInAs HBT structure. The experimental data was collected through the quartz dome in the ECR system with the sample approximately 1 m from the beam splitter. The data was collected at a 0.1s sampling time. A 75W Xe lamp was used as the light source.

To provide the reference data on the optical dielectric functions needed for operation of both the in situ reflectometer and the in-line spectral reflectometer, we characterized our materials and samples using ex situ spectroscopic ellipsometry using both a Rudolph S2000 system and a Sopra GESP-5 system.

RESULTS

MASS SPECTROSCOPY

In our test experiments on GaAs wafers, the QMS did not show any Ga-containing species[8,7] and was therefore not used in attempting to endpoint the HBT etch. At least one group has been successful on a similar attempt using a similar quadrupole system but with a sampling tube located near the wafer being etched.[9] In our configuration, it is possible that the Ga-containing species were being removed by deposition reaction on the plumbing prior to the quadrupole mass filter itself or in the ionizer. In addition to the problem of the movable sample stage discussed earlier, we chose not to invest further effort into this sensor for two reasons. First, placing a sampling tube near the wafer (an thus with exposure to the plasma) introduces the possibility of significant wafer contamination. Also, due to the well-known problem of process gas induced gain shifts when using thoriated iridium filaments, we had attempted to use tungsten filaments in the ionizer. However, due to the Cl_2 in our etch gas, the lifetime of the W filaments was too short for practical use. Thus, while the QMS initially seemed to be a straightforward solution, our conclusion was that it is not a practical solution for even limited lot production applications.

OPTICAL EMISSION SPECTROSCOPY

The OES system provided a usable endpoint signal from the Ga emission line at 417.2 nm. At typical test run is illustrated in Figure 5. As can be seen in this figure, the major regions of the sample can be resolved and the approximate etch rates of each material can be estimated. However, high accuracy endpointing of the etch required a more sophisticated procedure than simply detect the presence of Ga at some predefined OES signal threshold The problem is that the chamber becomes seasoned with Ga-containing compounds after only a few runs, and, thus, there is a time-varying Ga OES signal present even while etching the AlInAs. By using a more sophisticated signal processing approach, we were able to demonstrate acceptably high accuracy endpoint detection on simple test samples with abrupt layers of AlInAs on GaInAs on InP.[10] The maximum-likelihood estimator method described in this reference could be readily adapted to the grade SL case, but was not used due to limitations in available samples. The basic problem is that some level of experimental "training" of the algorithm was required for each type of sample and also this effort must be repeated on a roughly daily basis to correct for major etch system drifts. In production applications with repeated runs of the same type of product through an etch system, the combination of the OES method (interpreted through a drift correcting algorithm) and ex situ in-line metrology would provide a reliable solution. Without this repetition, the requirement for calibration runs would probably make this technique to expensive to implement.

DUAL-λ REFLECTOMETRY

Although it was test successfully on Si test samples (see Figure 4), the dual-λ reflectometer was not used successfully for endpointing the HBT etch due to rapid clouding of the ECR quartz dome. This system was successfully test in a poly Si endpoint experiment on a parallel plate RIE. The reflectometer signal was initially calibrated using a bare Si wafer in the chamber prior to the etch run. The signal was then calibrated for window changes and alignment errors by fitting the

measured data to the theoretical reflectance a the last peak and valley of the reflectance oscillations to provide a gain and offset correction. The endpoint was then triggered when either wavelength signal reached the desired theoretical reflectance. A series of poly Si/SiO$_2$/Si runs resulted in an oxide over-etch of 3.6 nm with a standard deviation of only 0.87 nm. The over-etch could have easily been reduced by adjusting the target reflection value.

In related work on flat panel displays, we have shown that dual-λ reflectometry coupled with advanced signal processing (Extended Kalman Filtering) can etch to desired target remaining film thicknesses to an accuracy of 1.5 nm (3σ limit).[11] In these experiments, films of a-Si/SiNx/Ta/1737f display glass were etched to a target remaining film a-Si thickness of 50nm. Other target thicknesses could have been chosen. The remaining a-Si film thickness had average film thickness of 48.4 nm with an extreme spread in all experiments of 1.4nm (as measured by ex situ spectroscopic ellipsometry).
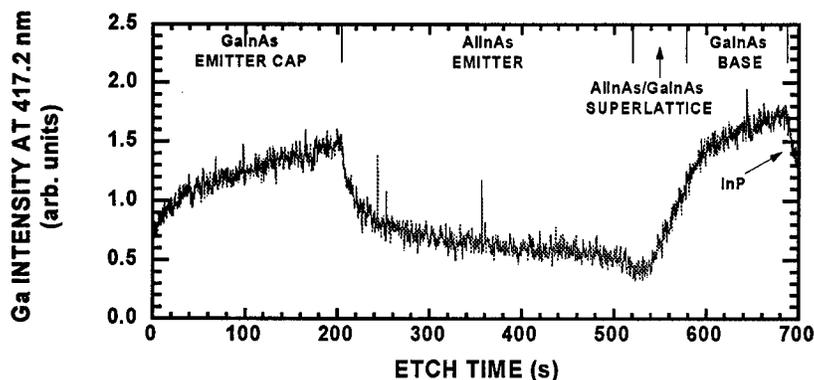
Figure 5 Typical OES signal (417.2nm) while etching completely through a test structure. The approximate positions of the layers on this signal are indicated. The conditions of this run were: 50W microwave power, 100W RF power, 3sccm Cl$_2$, 27 sccm Ar, 2 mTorr pressure.

IN LINE MONITORS

We characterized the optical properties of the materials in the HBT structure using ex situ spectroscopic ellipsometry. Most the effort required was in the characterization of the AlInAs, a material which previously had not been extensively studied for optical properties in the UV-Vis-NIR range.[12] This data was then used in our ex situ film thickness monitoring efforts. A spectroscopic ellipsometry (SE) measurement of an HBT test sample is shown in Figure 6 and a microscope-based spectral reflectometry (SR) measurement of the same sample is shown in Figure 7. As can be seen in the figures, the agreement between the two methods is good. As expected, the SE result has better statistical confidence limits due to the inherently higher accuracy of this optical measurement; however, the SR measurement were sufficiently accurate for our process monitoring applications and could be made in much smaller areas.

Figure 6 Ex situ spectroscopic ellipsometry measurements of HBT test structure.

Growth Target	SE Analysis
	1.88±0.03nm Oxide
100nm InGaAs	94.41±0.16nm InGaAs
190nm InAlAs	171.81±0.29nm InAlAs
9 Period InAlAs/InGaAs Super Lattice Period 3.33nm	Simulated Using Growth Targets
60nm InGaAs	61.64±0.40nm InGaAs
InP Substrate	

Figure 7 Microscope-based spectral reflectometry measurements of same test structure wafer as in Figure 7.

Growth Target	SE Analysis
	0.93±0.99nm Oxide
100nm InGaAs	96.97±1.16nm InGaAs
190nm InAlAs	176.12±0.98nm InAlAs
9 Period InAlAs/InGaAs Super Lattice Period 3.33nm	Simulated Using Growth Targets
60nm InGaAs	60.22±2.87nm InGaAs
InP Substrate	

The relatively rapid SR measurement were used to quantify the accuracy of our OES based endpoint experiments. A before- and after-etch pair of measurements from a test sample are shown in Figure 8. However, two significant complications were noted. First, the apparent roughness layer on the sample was reduced following a DI H_2O rinse of the sample. XPS results indicated that this rinse removed a Cl-containing film from the surface.[7] Second, because diffuse scattering from surface rough layers has a more serious effect on SR measurements (which use absolute intensity) than SE measurements, we employed an algorithm adapted from Beckmann-Kirchoff scattering theory to model of the surface roughness layer. [13]

We also used the SR method to test the uniformity of the samples used in our endpoint experiments. We typically tested only 5 points per sample unless significant nonuniformities were detected. However, as an illustration of the results that are possible from a large number of measurements using an automated stage, a relatively nonuniform epi test sample is shown in Figure 9.
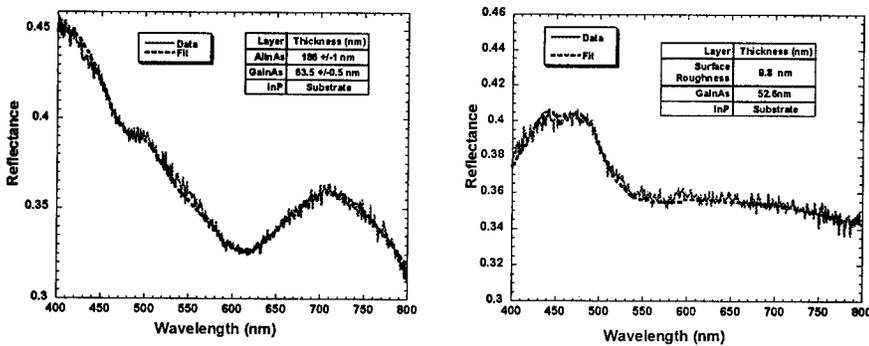
Figure 8 An abrupt interface AlInAs/GaInAs/InP test sample measured before and after etch using the microscope based SR method.

While the SE and SR characterization methods were successfully applied to ex situ sample measurements, we did identify a measurement problem which remains unsolved and presents a serious limitation to the wide-spread application reflectance measurement for monitoring of product (device) wafers. The problem is the accurate modeling of superlattices with very thin layers. As an example, a measurement and modeled SE response for the graded SL of the HBT structure is shown in Figure 10. We were unsuccessful in the fitting this structure with any of the models which we tried, including treating each layer as "bulk" materials (as in the figure), effective media approximations, quaternary alloy approximations (using harmonic oscillator interpolations), and others. In some respects this failure is not surprising as there is (intentionally) a significant amount of electron transfer between the layers in this type of structure. It might be expected that this sort of material would act as an anisotropic layer with unique optical properties.

CONCLUSIONS

While our attempts to accurately endpoint the targeted HBT fabrication step were not fully successful, I would like to offer the following conclusions and conjectures.

First, reflectance based techniques are capable of achieving few-monolayer level accuracies provided: (1) that there is an adequate optically clear view of the wafer surface; (2) that the optical properties of the materials are well characterized. Optical access to the wafer can be maintained in high density plasma systems if the sample positioning is fixed and off-normal ports are installed outside of the plasma discharge area. We are currently operating an in situ spectroscopic ellipsometry system on a high density, inductively coupled plasma tool (a Lam 9400 TCP) using Cl_2/HBr etch chemistries. While the quartz plate below the TCP coil is heavily clouded by ion bombardment, chemical etching, and coating by etch byproducts, the ellipsometry ports have not shown any clouding or etching. Thus, this annoying problem can be
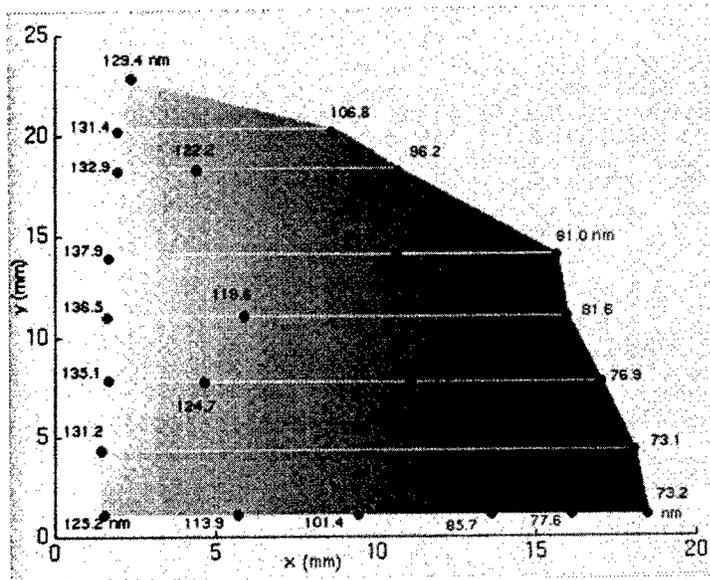
Figure 9 An SR measurement of the thickness uniformity of a $Al_{0.44}In_{0.56}As/InP$ test sample.
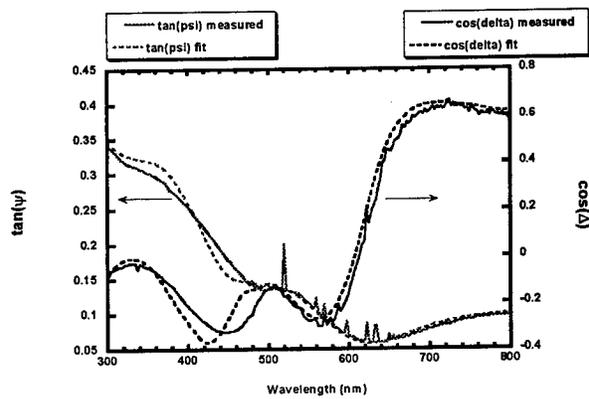
Figure 10 SE measurement (right) of a graded superlattice test structure (left) and the modeled result from the growth target layer thicknesses.

readily solved once the geometry of the etch system is held fixed. In most cases, the optical properties of the materials of interest can be obtained by ex situ spectroscopic ellipsometry. Preparing and characterizing the specialized test samples required, however, often proves to be outside the financial scope of many projects. Our efforts to characterize AlInAs, while sufficient for this effort, were not complete. Significant effort is needed in the optical characterization and modeling of superlattice materials. This continues to be a limiting issue in the use of SE, SR, and related methods in both in situ and ex situ process monitoring efforts. Also, additional effort needs to be made in the optical modeling of process-induced damaged layer and etch byproduct layers. For all of these optical modeling complications, individual process endpoint solutions could be found by empirically matching the raw optical data to a known good shape; however, this type of solution is not robust against changes in sample layers structures or to changes in process-induced surface layers.

Second, process state measurements are well suited to control of repeated processes with significant product flow. However, for small lot applications, the effort and samples required in calibration and training of algorithms tends to offset their advantages. In these applications, SPC and run-to-run control methods using in-line monitoring tools may be more cost-effective. If run-to-run variations in the process are too severe to allow effective adjustments using ex situ, in-line methods, then properly installed in situ optical metrology should prove effective.

Third, even if in situ monitors are available and effective, the use of microscope-based SR (a widely used tool in the Si industry) can be effectively employed for compound semiconductor applications. In particular, mapping of the thicknesses and uniformity of epitaxial layers would be useful in both not processing improperly grown wafers and in planning subsequent processing to account for variations in usable wafers. Depending on the layer thicknesses and absorption lengths, accurate estimates for the top two to four layers should be possible.

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IN SITU CONTROL OF WET ETCHING USING
SPECTROSCOPIC ELLIPSOMETRY

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ABSTRACT

Etching of a GaAs/$Al_{0.3}Ga_{0.7}$As/GaAs heterostructure in a nonselective etch solution of
25:1:75 (citric acid :H_2O_2:H_2O) was studied in-situ using real time spectroscopic ellipsometry
(RTSE). Etch rates for GaAs and AlGaAs of 15.3 nm/min and 17.6 nm/min, respectively, were
determined by numerically fitting RTSE data. RTSE was successfully used to stop the etch
after removal of the thin GaAs cap, while removing very little of the underlying AlGaAs layer.
In addition, etch depth into the AlGaAs layer was accurately controlled, using RTSE to stop the
etch with 100 nm remaining. Finally, RTSE data for wet etching of a patterned sample (75%
coverage with photoresist) showed similar behavior to that for the unpatterned sample.

INTRODUCTION

Selective wet chemical etching is an important processing step in fabrication of high
speed electronic devices such as heterojunction bipolar transistors (HBTs)[1] and high electron
mobility transistors (HEMTs).[2] Selective wet chemical etching using a citric acid/hydrogen
peroxide solution in AlGaAs/GaAs heterostructure has been widely used for mesa isolation and
gate recess in device fabrication due to its high selectivity. Selectivities, etch rates, and other
properties have been reported.[3,4] A high selectivity is usually associated with a very high GaAs
etch rate. However, a high GaAs etch rate makes it difficult to control the etch depth without
using an etch stop layer. If an etch stop layer is employed, a high etch rate process can cause
excessive undercutting.

Using a nonselective etch[2] with low etch rates, and monitoring with in-situ RTSE can
potentially solve these problems. Real time monitoring of wet chemical etching using RTSE
can be used to determine etch rates of GaAs and AlGaAs, as well as for end point detection,
and to control etch depth accurately.

EXPERIMENTAL

$Al_{0.3}Ga_{0.7}$As with a thin GaAs cap was grown on semi-insulating (100) oriented GaAs
substrates using metal organic chemical vapor deposition (MOCVD). The wafers were cut into
1cm by 1 cm pieces. All etching experiments were performed at room temperature. Anhydrous
citric acid crystals were dissolved in deionized water (D.I. H_2O) in a 1:1 by weight ratio to form
the citric acid. The etch solution was then prepared by adding 30 % hydrogen peroxide (H_2O_2)
and D.I. H_2O in the appropriate ratios. Some samples were cleaned in 60°C trichloroethane
(TCA), acetone, and methyl alcohol for 10 minutes each then rinsed in flowing D.I. H_2O and
blown dry; others were not cleaned.

A real time spectroscopic ellipsometer measuring at 88 wavelengths ranging from 1.63-
4.43 eV (760-280 nm) was used for all in-situ measurements. The sample cell was made of

teflon with two quartz windows positioned for an angle of incidence of 75°. A rotary stage and tilt platform were used to align the cell in order to make the beam normally incident on the windows. After the sample and cell were aligned and RTSE measurements were started, the etch solution was poured into the top of the cell.

To confirm thicknesses and surface conditions before and after etching, ex-situ SE measurements were made in air using a variable angle spectroscopic ellipsometer over the spectral range 1.5-5.5 eV (827-225 nm) in 0.025eV increments at an incidence angle of 75°.

VASE analysis

Ellipsometry measures a complex quantity ρ which is related to the complex ratio of reflection coefficients:

$$\rho \equiv \tan(\psi)\, e^{i\Delta} = \frac{R_p}{R_s} \tag{1}$$

where R_p and R_s are the complex reflection coefficients for light polarized parallel and perpendicular to the plane of incidence, respectively. The pseudodielectric function $<\varepsilon(E)>$ is derived from ρ as follows :

$$<\varepsilon> = <\varepsilon_1> + i <\varepsilon_2>$$
$$= \varepsilon_a \sin^2 \Phi \left[\left(\frac{1-\rho}{1+\rho} \right)^2 \tan^2 \Phi + 1 \right] \tag{2}$$

where Φ is the external angle of incidence.[5] This is what the dielectric function of the sample would be if there were no overlayers.

In order to analyze the measured ρ data they must be numerically fitted with a multilayer model. R_p and R_s for the overall structure are calculated and compared to the experimental data, as described further below. For analysis of in-situ data the optical constants of the liquid ambient (etch solution) must also be included in the model. To obtain these each liquid was measured separately by ex-situ SE, and these data were fitted with a Cauchy model for the optical constants :

$$n = A_n + \frac{B_n}{\lambda^2} \tag{3}$$

$$k = A_k \exp\left(B_k \frac{1.24}{\lambda} \right) \tag{4}$$

where $(n+ik)^2 = \varepsilon_1 + i\varepsilon_2$ and λ is the wavelength in microns.

In cases were microscopic roughening occurs, the Bruggeman effective medium approximation (BEMA) can be used to model the optical constants of the roughness overlayer or interface. (This model only applies to roughness whose spatial wavelength is much less than the wavelength of light.) The BEMA gives the effective dielectric function ε of a microscopic mixture of two materials with known dielectric functions ε_a and ε_b, and volume fractions f_a and f_b ($f_a + f_b = 1$).[6]

Multilayer model parameters (thicknesses, volume fractions, etc.) are adjusted to fit the model-generated to the experimental ρ values. This is done using the Levenberg-Marquardt algorithm to minimize a biased fitting function, defined as[7]

202

$$MSE = \frac{1}{2N-M}\sum_i \left[\left(\frac{\psi_i^{mod} - \psi_i^{exp}}{\sigma_{\psi,i}} \right)^2 + \left(\frac{\Delta_i^{mod} - \Delta_i^{exp}}{\sigma_{\Delta,i}} \right)^2 \right] \qquad (5)$$

The sum is over all photon energies and incidence angles (a total of N measurements); $\sigma_{\psi,i}$ and $\sigma_{\Delta,i}$ are the experimentally determined standard deviations in ψ_i^{exp} and Δ_i^{exp} , and M is the number of variable parameters in the model.

RESULTS AND DISCUSSION

Figure 1 shows simulated $<\varepsilon_2>$ spectra generated from the inset model. Interference oscillations below 2.5 eV are due to the relatively thick AlGaAs layer, making this spectral region highly sensitive to that layer thickness. At higher photon energies the light is absorbed within the AlGaAs layer, so this spectral region is sensitive only to the top oxide and GaAs cap layer thicknesses. The series of spectra shows that as the cap layer thickness is reduced from 16 to 0 nm the spectral structure near 3 eV (E_1 peak) changes markedly. The apparent E_1 peak starts out near that for bulk GaAs (2.9 eV), and gradually shifts to that for the AlGaAs (3.2 eV). Monitoring in real time at 2.9 eV, therefore, will be very sensitive to cap removal. After cap removal, the region below 2.5 eV is useful for monitoring AlGaAs thickness until it becomes thin enough (≤ 150 nm) for the E_1 region to again become sensitive to it.

Figure 2 shows RTSE data at 2.9 eV obtained during etching of a 17 nm-GaAs/450 nm-$Al_{0.3}Ga_{0.7}As$/GaAs heterostructure in a 25 citric acid : 1 H_2O_2 : 75 H_2O solution. This is a nonselective etching solution, with etch rates roughly equal for GaAs and AlGaAs. Data-taking was initiated before the solution was poured into the cell, at about 1.2 min. The thin GaAs cap etched away in a little over a minute. Afterwards $<\varepsilon_2>$ at 2.9 eV remained stable as the AlGaAs etched, until about 18 min. Then interference oscillations began and grew until the AlGaAs was completely removed (~27.5 min). The inset is an expanded view of the first two minutes, when the cap was removed. The delay before the onset of GaAs etching, ~0.3-0.5 min here, is probably related to the presence of organic material on the surface. Thorough cleaning minimized the delay, while delays of up to 1.5 min were seen for uncleaned samples.
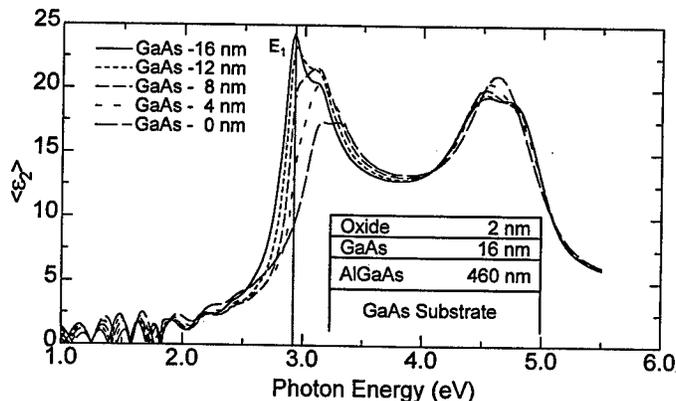
Figure 1. $<\varepsilon_2>$ generated using the inset model, with GaAs cap thickness decreasing from 16 to 0 nm
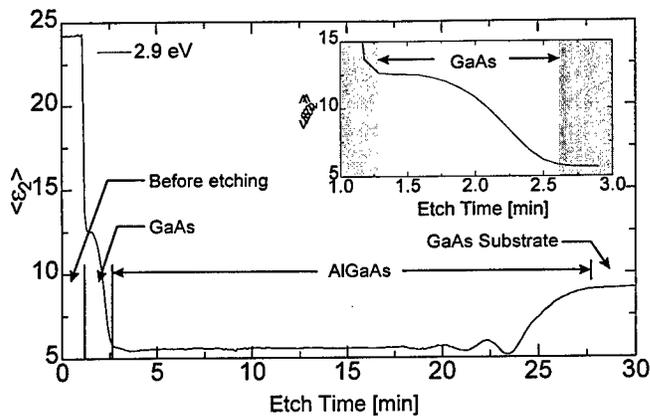
Figure 2. $<\varepsilon_2>$ measured at 2.9 eV while etching a GaAs/AlGaAs/GaAs heterostructure.

(a)   (b)
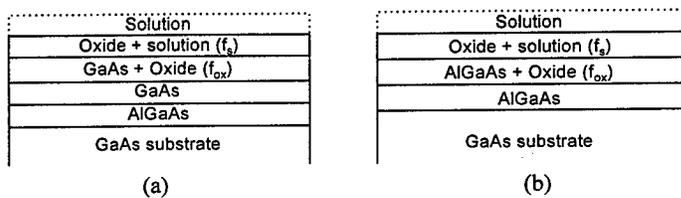
Figure 3. Models used to analyze RTSE data for (a) GaAs cap removal detection and
(b) AlGaAs etch depth control

Etch rates were determined by numerically fitting the layer thicknesses to data at each point in time. In addition to the AlGaAs[8] and cap layers, the fitting model contained an interfacial layer consisting of a mixture of GaAs[9] and its oxide[10] modeled with the BEMA, and a porous oxide layer also modeled with the BEMA as a mixture of oxide and citric acid solution (figure 3). The interfacial layer may represent microscopic roughening of the surface. The etch rates of GaAs and $Al_{0.3}Ga_{0.7}As$ in the 25:1:75 (citric acid : H_2O_2 : H_2O) solution obtained from fitting were 15.3 nm/min and 17.6 nm/min, respectively. The ratio, 0.87, is in good agreement with that given by Mao et al.[2]

An objective was to use RTSE to stop the etch after the cap was removed, removing as little of the underlying AlGaAs as possible. This objective was made more difficult by the reverse selectivity of this solution, with the AlGaAs etching a little faster than the GaAs. The model of figure 3(a) was used to fit for the GaAs thickness in real time. When the fitted thickness became zero the sample was taken from the solution, rinsed in flowing D.I. H_2O and blown dry. Then ex-situ SE data were measured to verify the AlGaAs thickness. The model in figure 3(b), with void replacing solution in the ambient and oxide, was used to fit the data. Fitted thickness and volume fraction values from ex-situ analysis before and after etching are given in Table I. These results show that the cap was removed but little of the AlGaAs was etched, though an interfacial layer of some kind (perhaps roughness) remained.

Table I. Fitted model parameter values before and after GaAs cap removal.
90 % confidence limits are given in parentheses.

Before Etching		After Etching	
Layer	Thickness[nm]	Layer	Thickness [nm]
Oxide	2.1 (0.03)	Oxide + Void (35%)	7.1 (0.3)
GaAs	17.2 (0.20)	AlGaAs + Oxide (30%)	7.3 (0.9)
$Al_xGa_{1-x}As$*	448.8 (0.40)	$Al_xGa_{1-x}As$*	448.2 (1.4)
MSE	4.3	MSE	7.0

* Mole fraction of aluminum, x, was fixed at 0.31
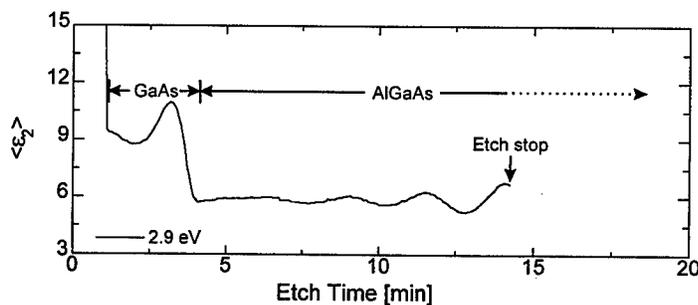
Figure 4. RTSE data used for AlGaAs etch depth control.

A second objective was to control the depth of etching into the AlGaAs layer. The AlGaAs thickness was fitted in real time using the model of figure 3(b). Etching was stopped at about 14 minutes as shown in figure 4, when the fitted thickness reached 100 nm. Ex-situ SE measurements were then made and fitted with the same model replacing solution with void, keeping the mole fraction of aluminum fixed to 0.35. The fitted AlGaAs thickness was 98 (±1.4) nm, with just under 5 nm of roughness modeled by the interfacial layer and 6 nm of porous oxide. The fit here was not as good as before (MSE=15.9). Further modeling indicated that the AlGaAs layer may have been nonuniform in thickness after etching. A scanning electron micrograph (SEM) of a small cross section prepared by focused ion beam (FIB) milling indicated an AlGaAs thickness of 104 nm in good agreement with the sum of the AlGaAs and interface thickness given above.

Finally, RTSE was used to observe etching of a patterned sample. A photoresist layer was spun on to the heterostructure (50 nm GaAs cap, 300 nm AlGaAs) and developed into a rectangular bar pattern(~75% coverage) The real time data at 2.9 eV (figure 5) is very similar to that for the unpatterned sample. The primary difference is a lower (but still adequate) signal to noise ratio, due to the effective reduction in sample area caused by patterning. This preliminary result indicates that RTSE will also be useful for controlling etches of patterned surfaces.

CONCLUSIONS

The etching of GaAs/AlGaAs/GaAs heterostructures in a citric acid :H_2O_2:D.I. H_2O solution was studied by ex-situ SE and in-situ RTSE. A volume ratio of 25 : 1 : 75 produced relatively low etch rates of 15.3 nm/min and 17.6 nm/min for GaAs and AlGaAs, respectively.
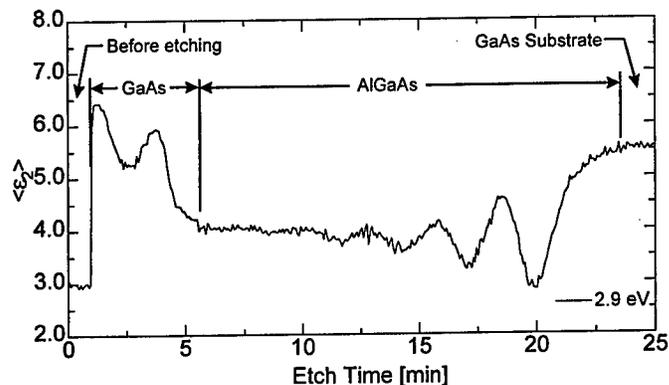
Figure 5. RTSE data at 2.9 eV while etching a patterned GaAs/AlGaAs/GaAs sample.

Despite the lack of selectivity, the etch could be accurately stopped after the cap removal using RTSE monitoring. Etch depth into the AlGaAs layer was also controlled using RTSE . Finally, etching of a patterned heterostructure sample showed good sensitivity to cap and AlGaAs layer removal, despite the large (75%) area coverage by photoresist.

ACKNOWLEDGMENTS

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MOCVD-PREPARATION AND IN-SITU / UHV-ANALYSIS OF EPITAXIAL INP-FILMS

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ABSTRACT

Surface science analysis can be utilized for improving the preparation of hetero-interfaces. Epitaxial InP(100)-films were prepared with TBP (tertiarybutylphosphine) and TMIn (trimethyl-indium) as precursors in a commercial MOCVD apparatus. With a new type of transfer system the sample is shifted from the MOCVD apparatus to a UHV chamber within 20 s. A description of the new transfer system is given. RAS (reflection anisotropy spectroscopy) is carried out in the MOCVD and UHV environments. It shows whether the InP(100) surface corresponds to the (2x1) or (2x4) reconstruction or whether it is oxidized. For the first time contamination-free transfer of the (2x1) reconstructed, P-rich InP(100) surface is achieved.

INTRODUCTION

For device applications of III-V semiconductors and also for basic research it is advantageous to utilize the many extremely powerful UHV based characterization methods. Several research groups were engaged in preparing clean surfaces of III-V semiconductors [1-4]. Hitherto, different UHV based preparation methods were applied, e.g. sputtering/annealing cycles [5], deposition and desorption of MBE-grown caps [6], etching [3], and direct MBE transfer [7]. In the case of InP only In-rich, but not P-rich surface stochiometries could be studied without encountering severe surface contamination. MOCVD is the preferred method for InP-based devices. Therefore, it is highly desirable to be able to employ an MOCVD/UHV transfer mode with the following properties. It should retain the chemical composition and detailed morphology of the surface prepared via MOCVD, and it should avoid any contamination of the sample surface in the transfer process.

In this paper experimental results are presented that show for the first time contamination free transfer of a P-rich InP surface from an MOCVD environment, where it was grown epitaxially and characterized using RAS, to a UHV apparatus, where the same RA spectrum was obtained and confirmed by a corresponding Auger-electron-spectrum. Contamination free transfer of the P-rich InP surface was obtained in a transfer apparatus with a newly designed combination of purging, valve operations, and pumping sequences that allow the transition from the MOCVD environment to UHV (down to the 10^{-9} mbar range) in 20 seconds.

EXPERIMENT

Epitaxial growth of InP films was performed in a commercial horizontal AIX 200 reactor (AIXTRON AG) that was equipped with an optical window for in-situ measurement of RA spectra. The precursor sources were TBP (tertiarybutylphosphine) and TMIn (trimethylindium). The growth rate was 1.8 μm/h. Either H_2, purified in a palladium cell, or N_2, purified in a getter column, were applied as carrier gases. All growth experiments were performed at a pressure of 100 mbar and at a total gas flow rate of 5.5 l/min. The samples were grown either at 838 K or at

873 K. Calibration of the sample temperature reading was obtained at the eutectic point of an Al-Si alloy (850 K). S-doped (3×10^{18} cm^{-3}) InP(100) wafers or semi-insulating wafers (Fe-doped) were used as substrate materials. After standard wet-chemical substrate preparation the samples were dried in a stream of N_2 and attached by clamping to a molybdenum sample holder which was placed in the center of the modified graphite susceptor inside the MOCVD reactor.

The transfer system attached to the MOCVD reactor (compare Fig.1) consists of an interim chamber, where a total pressure $< 10^{-8}$ mbar is reached in less than 20 seconds, a basic UHV chamber, where MBE could be performed, and the mobile UHV transport chamber. The latter is equipped with an optional battery driven ion getter pump supplying $< 3 \times 10^{-10}$ mbar. All the chambers and the MOCVD reactor are separated by UHV-valves. After epitaxial growth of the InP film the TBP flow was maintained in the reactor until 563 K or 613 K were reached to prevent P-desorption from the surface. At that temperature the flow of TBP was switched off, the purge gas was changed to nitrogen, and the reactor-pressure was reduced to about 1 mbar. Next, the UHV-valve V1 separating the MOCVD-reactor from the interim chamber was opened and the hot sample ($T_{sample} < 623$ K) along with the molybdenum holder were transferred within a few
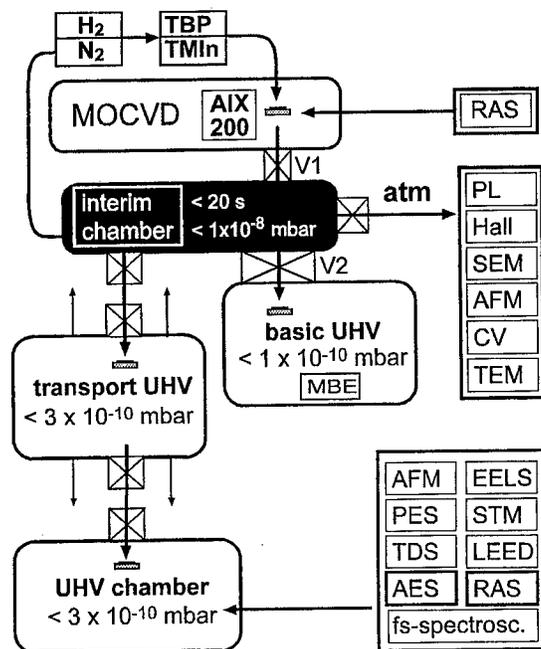

Fig.1 Scheme illustrating the preparation of the InP sample with MOCVD and its transfer to UHV. For sample transfer a carrier gas purged interim chamber is employed. The sample is placed in a mobile UHV chamber. Docking the latter to any suitable UHV chamber facilitates the characterization of the sample with all the available UHV-based surface science tools.

seconds into the interim chamber. The latter was purged with the carrier gas. Next, the valve V1 was closed and the valve V2 to the UHV basis chamber was opened. Less than 20 seconds later a pressure in the 10^{-9} mbar range was reached. After 5 min the pressure was $< 1 \times 10^{-9}$ mbar, and 10 min later the pressure was below 3×10^{-10} mbar. Now the sample could be transferred into the UHV transport-chamber and, maintaining UHV conditions, to any other UHV system that is equipped with an appropriate UHV load-lock system. AES for chemical analysis was performed with a hemispherical mirror analyzer (HSA 100, Co. VSI) and an electron gun for primary excitation of the sample. For AES measurements 3 keV-electrons were directed onto the sample. The equipment for the RAS measurements was described already in the literature [8]. RAS measurements were performed through an almost strain-free optical window in the MOCVD apparatus with the light beam passing through the window at nearly normal incidence. After transfer of the sample to UHV the same RAS set-up was employed. Corrections for the influence of strain in the window of the UHV system on the RAS signal were made by correcting against the signal from an isotropic sample (Si(100)-wafer). The corrections were not completely successful over the whole spectral range.

RESULTS

Bulk properties of MOCVD-grown InP layers

Ex-situ 2 K photoluminescence spectra showed a high bulk quality of epitaxial MOCVD grown InP films (not shown here). A strong peak due to free exciton luminescence appeared at 1.4188 eV. The height of this peak is a sensitive probe for structural perfection, chemical purity, and dopant concentration [9,10]. The rotational structure and heavy hole-light hole splitting of the donor-bound exciton between 1.4170 eV and 1.4184 were resolved and showed that there was hardly any strain in the layer [9]. The free exciton peak showed that the dopant concentration was $< 1 \times 10^{15}$ cm^{-3}. The often encountered donor-acceptor pair luminescence at around 1.375 eV was very weak in this sample.

Scannning electron microscopy (SEM) and atomic force microscopy (AFM) (compare Fig.1) were employed to check on the smoothness of the surface. The sample surface was found to be smooth with only terraces of monolayer height at suitable V/III ratios, e. g. 12. Details of the STM surface structure will be described elsewhere.

In summary, modifying the commercial MOCVD reactor in order to facilitate MOCVD/UHV transfer did not introduce any negative effect.

RA spectra of InP(100) surfaces measured in the MOCVD apparatus and in UHV

It is well known that the (2x1) reconstructed surface of InP is difficult to prepare in UHV. Hitherto one has not been able to preserve this surface structure if it was prepared in an MOCVD apparatus and transferred afterwards to a UHV chamber. Therefore, it was selected as the test case for the new MOCVD/UHV transfer system. An about 1 μm thick InP layer was grown in the MOCVD apparatus at V/III ratio = 12 and T_G = 838 K and transferred to the transport chamber (Fig.1) according to the procedure described in the experimental section. The transport chamber was docked to an UHV apparatus and the sample was investigated again with RAS in UHV ('after transfer' in Fig.2). The corresponding RA spectrum measured in the MOCVD reactor before transfer to UHV is labeled 'before transfer' in Fig.2. All the essential features of the P-rich
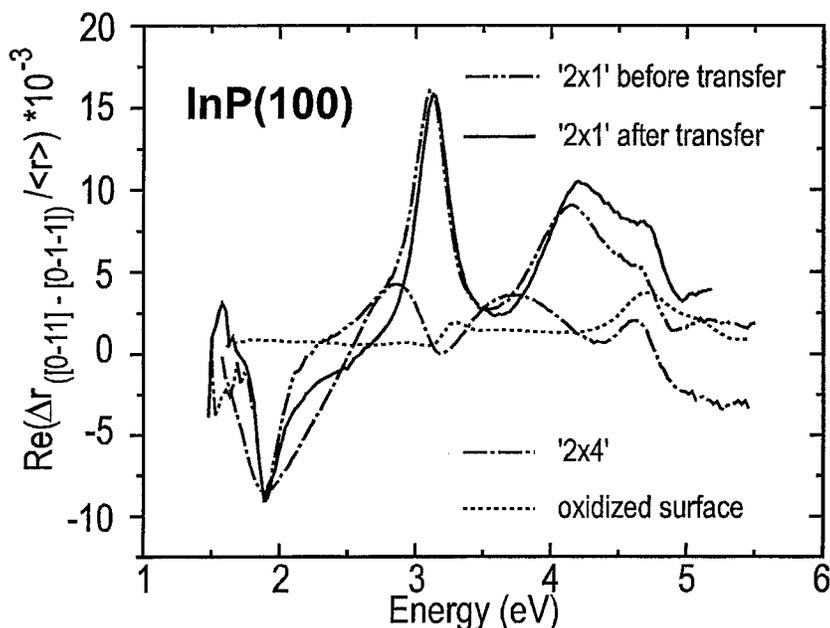
Fig.2 RA-spectra: (2x1)-like InP(100) surface taken in the MOCVD apparatus before and in the UHV chamber after transfer, (2x4) reconstructed surface, oxidized surface.

(2x1) surface reconstruction in the RA spectra [11] are retained after transfer. They are very different from those associated with the In-rich (2x4) surface reconstruction (Fig.2). Thus, Fig.2 shows that the (2x1) surface reconstruction was not affected by the MOCVD/UHV transfer. The small difference between the two '(2x1)-like' RA spectra in Fig.2 is attributed to the strain in the window of the UHV chamber whose influence could not be completely eliminated by the correction method described in the experimental section. The P-rich surface can be transformed into an In-rich surface simply by heating the sample above 650 K [12,13]. The RA spectrum of an oxidized InP(100) surface is featureless and thus completely different from the RA spectrum of the (2x1) and the (2x4) reconstructed surfaces.

AE spectra of InP(100) surfaces measured in UHV

Fig.3 shows a corresponding Auger electron spectrum in the differential distribution (dN/dE) for the surface whose RA spectrum is shown in Fig.2. The Auger spectrum does not show a trace of contaminants like oxygen or carbon. The respective positions are marked by arrows in Fig.3. The spectrum in Fig.3 can be attributed to the phosphorus-rich (2x1) surface reconstruction that was prepared in the MOCVD reactor by cooling the sample in the TBP flow down to 613 K (compare Fig.3). The corresponding intensity ratio of the Auger peaks P_{LMN}/In_{MNN} = 1.05 measured here for the (2x1) surface reconstruction is clearly higher than values 0.5 to 0.8 reported by another group for annealing experiments on InP wafers [12]. This confirms that the (2x1) reconstructed InP surface is indeed P-rich.
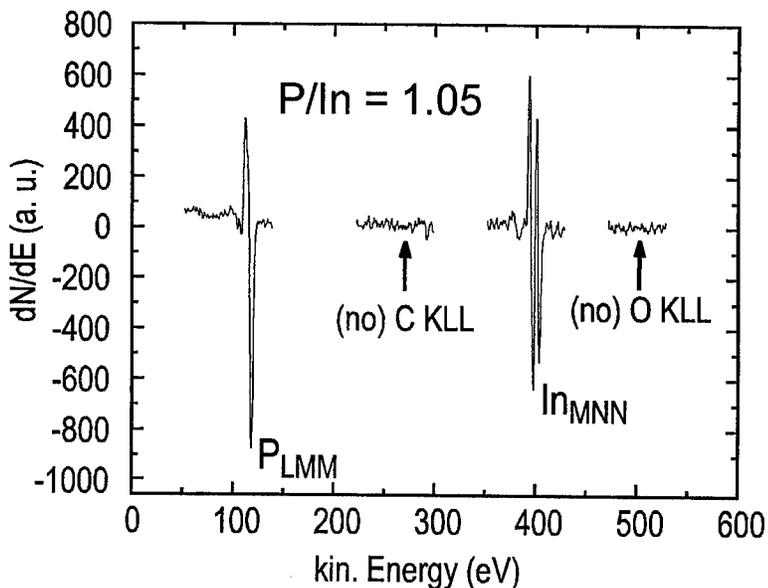
Fig.3 Auger spectrum in the differential distribution of a contamination-free (2x1)-like InP(100) surface in UHV.

Other preparation procedures for InP-surfaces, i. e. annealing and/or sputtering, resulted in the preferential removal of phosphorus from the surface [12,15]. With earlier transfer modes only the In-rich (2x4) reconstructed surface could be recovered contamination-free in UHV [2].

CONCLUSION

The standard MOCVD preparation conditions for InP layers grown with TBP as precursor yields RA spectra that can be associated with the (2x1)- reconstruction of the InP(100) surface [11]. The most important new result reported in this work is the successful contamination-free transfer of P-rich surfaces of InP from the MOCVD apparatus to a UHV chamber. The successful sample transfer was demonstrated by measuring the same essential features in both the RA spectra indicating the (2x1) surface reconstruction in the MOCVD apparatus before transfer and in the UHV chamber after transfer. The P/In Auger peak ratio P/In = 1.05 was correlated with the (2x1), based on assignments of this peak ratio given in the literature. The new MOCVD/UHV transfer mode employed in this work opens the way to investigating delicate surfaces prepared with MOCVD with all the experimental surface science tools that can be employed in UHV.

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GROWTH AND CHARACTERIZATION OF AMORPHOUS AlN THIN FILMS BY REACTIVE MAGNETRON SPUTTERING AT LOW TEMPERATURE

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ABSTRACT

We present the first report of the preparation and characterization of α-AlN films using reactive magnetron sputtering at cryogenic temperature. By comparison, analogous films grown at room temperature were polycrystalline. The films were characterized using X-ray Diffraction (XRD), Scanning Electron Microscopy (SEM), Rutherford Backscattering Spectrometry (RBS), Infrared (IR) Spectroscopy and optical transmission. XRD studies on films grown at room temperature showed diffraction peaks corresponding to (100), (101), (102) and (210) planes. In contrast, no peaks were observed for AlN films formed at liquid nitrogen temperature confirming the amorphous nature of the films. Composition analysis using RBS showed the presence of Al and N in ~1:1 stoichiometry. The films were highly transparent and the computed bandgaps of α- and c-AlN films were 5.90 and 5.89 eV respectively. We also consider the possibilities of wet etching the AlN films in diluted KOH solution and the results are discussed.

INTRODUCTION

Aluminum nitride (AlN) is one among the group of III-V nitride semiconductors with a direct, broad bandgap of 6 eV and hexagonal Wurtzite structure. The other attractive material properties of AlN are high thermal conductivity, chemical stability, electrical resistivity, and large piezoelectric constant. These properties make them viable for device applications like surface acoustic wave (SAW) sensors [1], and encapsulating layer for high temperature annealing of GaN and SiC [2-3]. AlN together with GaN and InN can be tailored to fabricate light emitting diodes (LED) with wavelengths varying from red to vacuum ultraviolet (UV) region [4].

There have been a number of studies on the preparation of epitaxial and polycrystalline aluminum nitride (c-AlN) films by sputtering [5-6], molecular beam epitaxy (MBE) [7] and metal organic chemical vapor deposition (MOCVD) [8], and laser ablation [9]. Thus, most of the work on AlN film growth to date has been focused mainly on controlling the orientation of the crystalline thin films. Moreover, the growth has been carried out at high substrate temperatures (300 - 1200°C) leading to the intrinsic stress formation and complicates application of these films for devices. Recently, there has been renewed research interest on the growth and applications of amorphous gallium nitride (α-GaN) films [10-11] because of their potential structural flexibility leading to large-area device applications, reduction of dislocation density, and the absence of grain boundaries and deep gap states which greatly influence the device performance. The device processing can also be made much easier. For example, cost-effective wet etching technology might be used instead of expensive dry etching technology.

No detailed and systematic investigations on amorphous aluminum nitride (α-AlN) semiconductors have been reported in the literature. While some previous studies report 'amorphous' AlN or GaN deposition in the temperature range 0-500 °C, we believe such films are actually polycrystalline. Indeed, we show here that films deposited at room temperature by

sputter deposition result in c-AlN. By comparison, we report for the first time the growth of α-AlN by dc reactive magnetron sputter deposition at cryogenic temperature. Films grown at low temperature may have certain advantages like the reduction of film stress, dislocation density etc. The reason for selecting sputtering for the AlN growth among the various techniques is because it offers large-area device quality coatings, low deposition temperature, higher growth rate, cost effectiveness and also competitive to MBE and MOCVD.

EXPERIMENTAL

AlN films were grown onto glass, quartz, Si (100) and carbon substrates by DC reactive magnetron sputtering. The deposition system had a base pressure of 5×10^{-10} mTorr. The films were prepared both at liquid nitrogen and room temperatures using an Al target of 99.999% purity in a gas mixture of Ar and N_2 (1:1). The deposition pressure and the sputtering power during the growth were maintained as 5 mTorr and 150 Watts respectively. The growth rate was 200 nm/hr and the thickness of the films was varied from 100 to 400 nm.

The X-ray diffraction profile was recorded using RIGAKU X-ray diffractometer. The surface analysis was made using a JEOL (Model JSM-5300) scanning electron microscope. The infrared (IR) reflectance spectrum was collected with a Perkin Elmer Spectrum 2000 spectrometer using unpolarized light with a reflectance angle of 20° from the normal. The optical transmittance (T%) data was recorded using a UV-VIS spectrophotometer in the wavelength range 190 to 820 nm. The elemental analysis of the films was analyzed by Rutherford backscattering spectrometry (RBS). A 3 MV Tandem Pelletron Accelerator with beam energy of 2.201 MeV and scattering angle of 168° have been used for the RBS analysis. Wet etching of the samples was carried out using diluted potassium hydroxide ($KOH:H_2O=1:3$) solution.

RESULTS AND DISCUSSION

As many as 10 sets of films were prepared at both liquid nitrogen and room temperatures. One film on Si (100) in each set was examined by SEM and found to have mirror-like surfaces and showed no evidence of pits or voids. Fig. 1 depicts the XRD patterns for AlN thin films of 350 nm thick grown on Si (100) substrate at room temperature. The films are polycrystalline and the observed peaks are indexed as (100), (101), (102), and (210) by using the ASTM data for AlN powder [12]. The films exhibit a preferential growth along the (101) plane. The crystallite size computed from the width of the (101) peak is about 15 nm. A prominent peak from the Si (100) substrate is observed at $2\theta = 69.10°$ in the curve. The other diffracted planes are originated from the diffractometer aluminum sample holder. Fig. 2 displays the XRD curve for AlN films of 320 nm thick on Si deposited at cryogenic temperature. There are two diffracted planes corresponding to Si (200) and Si (400). It is evident that the films are amorphous as no peaks for AlN are seen in the curve.

The IR reflectivity of AlN is used to identify the frequencies at which the vibrational modes (longitudinal and transverse oscillations) for AlN are observed. The IR absorbance spectra for c-AlN and α-AlN films on Si are displayed in Fig. 3. The position of the LO mode is also indicated in the spectra. It is found that the band is broad in α-AlN whereas it is narrow in c-AlN. The LO modes are indexed at around 878 cm^{-1} and 888 cm^{-1} for α-AlN and c-AlN films respectively. For crystalline hexagonal AlN, the LO mode is noticed at 890 cm^{-1} [13]. Our results for c-AlN are in good agreement with this report. However, the results for α-AlN do not agree with the value of 890 cm^{-1}. The shift and broadening of the LO peak are attributed to the

disordering of amorphous AlN, and are typical of the response expected from the amorphous phase [14].

Fig. 4 shows the optical transmittance (T%) spectra of both α- and c-AlN films on quartz.
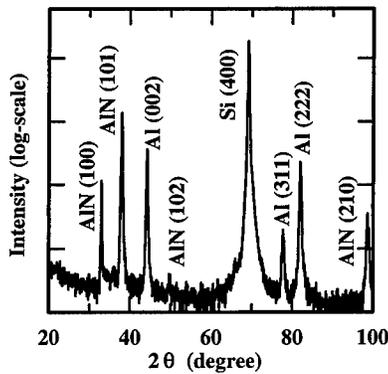
Fig. 1 XRD profile of AlN thin films grown at room temperature.
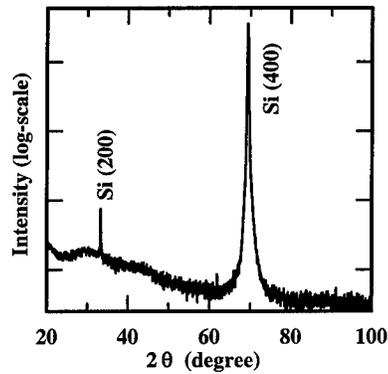
Fig. 2 XRD pattern of AlN thin films deposited at low temperature.

It is found that both c-AlN and α-AlN films are highly transparent in both the visible and ultraviolet regions. Using these spectra, plots of square of the absorption coefficient (α^2) versus
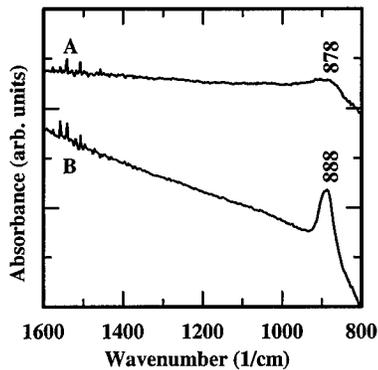
Fig. 3 The IR absorbance spectra of (A)α-AlN and (B) c-AlN films.
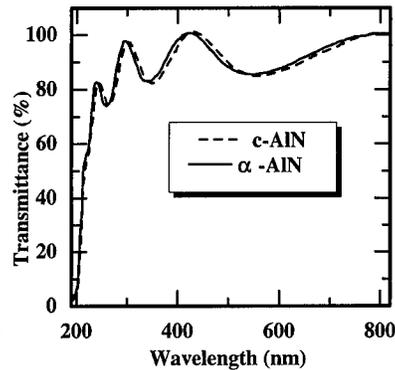
Fig. 4 Optical transmittance spectra of AlN thin films.

the photon energy (hν) are drawn as illustrated in Figs. 5-6. The bandgap (E_g) is obtained by extrapolating the linear portion of the plot to zero absorption. The E_g values are 5.89 and 5.90 eV

for c-AlN and α-AlN films. There is no drastic change in bandgap between c-AlN and α-AlN films. The computed bandgap values closely agree with the reported value of 6 eV [15]. From the transmittance spectra as a function of wavelength, we have computed the refractive index of the films using the method suggested by Swanepoel [16]. The calculated refractive indices of the c-AlN and α-AlN at 480 nm wavelength are 2.27 and 2.26 respectively. These results are in reasonable agreement with the reported value of 2.1 for the bulk material.

Fig. 5 Plot of α²versus h ν for c-AlN thin films.

Fig. 6 Plot of α²versus h ν for for amorphous AlN thin films.

Fig. 7 represents the RBS spectra of c-and α-AlN thin films. The composition estimated for c-AlN in number of atoms/cm² is N:1.05 x 10¹⁸, Al:1.16 x 10¹⁸, O:1.05 x 10¹⁷ and Ga:4.2 x 10¹⁶. The presence of a small amount of Ga is due to the splashing of Ga target onto the Al target

Fig. 7 RBS spectra of c-AlN (left) and α - AlN (right) thin films.

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Fig. 5 Plot of α^2 versus $h\nu$ for c-AlN thin films.
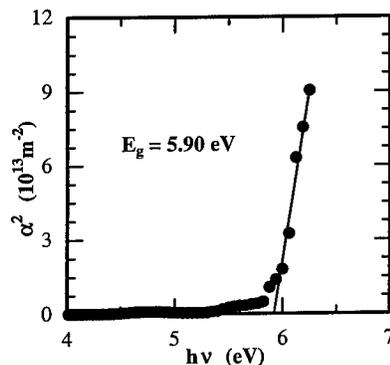
Fig. 6 Plot of α^2 versus $h\nu$ for for amorphous AlN thin films.

Fig. 7 represents the RBS spectra of c-and α-AlN thin films. The composition estimated for c-AlN in number of atoms/cm^2 is N:1.05 x 10^{18}, Al:1.16 x 10^{18}, O:1.05 x 10^{17} and Ga:4.2 x 10^{16}. The presence of a small amount of Ga is due to the splashing of Ga target onto the Al target
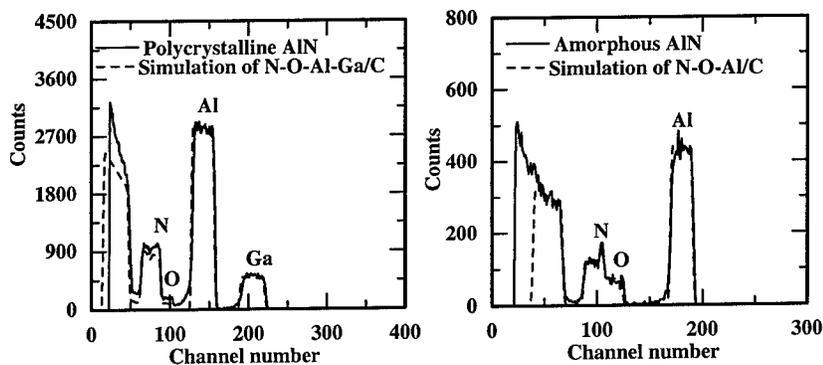
Fig. 7 RBS spectra of c-AlN (left) and α - AlN (right) thin films.

during the GaN growth in the system. The composition of α-AlN has been computed as N:8.1 x 10^{17}, Al:8.1 x 10^{17} and O:3.7 x 10^{17} in units of atoms/cm^2.

AlN controlled etching can be performed in various mineral acids such as HF/H$_2$O [17], HNO$_3$/HF [18] and aqueous NaOH [19] solutions. However, these etchants require high temperature and permit only very low etching rates. For example, Mileham et al [20] have systematically studied the room temperature wet chemical etching of single-crystal AlN films using pure and diluted AZ400K developer whose active ingredient is KOH. From the time dependence of etch depth of a polycrystalline AlN sample in diluted AZ400K developer, the etch rate was found to be about 2.4 nm/s. Pauleau [21] have reported wet etching of plasma-assisted chemical vapor deposition of AlN in hot phosphoric acid with an etch rate of 50 nm/s. In the present investigation, both c- and α-AlN films were etched with a room temperature diluted KOH solution. The etch rate of c-AlN is found to be only 0.4 nm/s whereas the etch rate for α-AlN is 27 nm/s, a 60 fold enhancement of the etch rate. Thus our results of wet etching of AlN at room temperature are promising.

CONCLUSIONS

We have successfully prepared α-AlN films using DC reactive magnetron sputtering at cryogenic temperature and compared the results for films grown at room temperature. All films grown at room temperature are polycrystalline whereas films formed at low temperature are amorphous as evident from the XRD and IR studies. The optical transmittance studies point out that both polycrystalline and amorphous films are highly transparent and the band edge is observed near 200 nm wavelength. The band gap of ~5.9 eV determined in the present study is fairly in agreement with the reported value for bulk AlN. The composition analysis shows that nearly stoichiometric AlN films can be grown successfully. The etch rate of α-AlN is much faster when compared to that of c-AlN.

## ACKNOWLEDGEMENTS

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FERMI-LEVEL EFFECT AND JUNCTION CARRIER CONCENTRATION EFFECT ON p-TYPE DOPANT DISTRIBUTION IN III-V COMPOUND SUPERLATTICES

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ABSTRACT

The pronounced segregation phenomenon in the distribution of p-type dopants Zn and Be in GaAs and related III-V compound heterostructures has been explained quantitatively by treating simultaneously the processes of dopant atom diffusion, segregation, and the effect of heterojunction carrier concentrations on these two aspects. Segregation of a dopant species between two semiconductor heterostructure layers is described by a model incorporating (i) a *chemical* effect on the neutral species; and (ii) in addition, a *Fermi-level* effect on the ionized species. The process of Zn and Be diffusion in GaAs and related compounds is governed by the doubly-positively-charged group III element self-interstitials (I_{III}^{2+}), whose thermal equilibrium concentration and hence also the Zn and Be diffusivities exhibit also a Fermi-level dependence, i.e., in proportion to p^2. A heterojunction is consisting of a space charge region with an electric field, in which the hole concentration is different from those in the bulk layers. This influences the junction region concentrations of I_{III}^{2+} and of Zn^- or Be^-, which in turn influence the distribution of the ionized acceptor atoms. The overall process involves diffusion and segregation of holes, I_{III}^{2+}, Zn^- or Be^-, and an ionized interstitial acceptor species. The junction electric field also changes with time and position.

INTRODUCTION

In some III-V superlattice (SL) device structures for which the involved acceptor diffusion time is short and/or the diffusion temperature is relatively low, the p-type dopants Zn and Be showed a prominent segregation behavior in the SL layers [1-3]. To account for these dopant distribution processes, we present a quantitative model which treats the dopant atom diffusion and segregation processes simultaneously.

FORMULATION

In experiments, Zn^- or Be^- distribution involves diffusion and segregation of holes, the doubly-positively charged group III self-interstitials I_{III}^{2+}, the ionized shallow acceptor atoms A^-, and an ionized interstitial species of the dopant atoms. Furthermore, the junction region carrier concentration changes with the electric field variations as a function of time and position. Because of the involvement of a large number of species for each of which diffusion and segregation occur simultaneously, the diffusion-segregation equation derived by You et al. [4],

$$\partial C/\partial t = \partial\left[D\left(\partial C/\partial x - (C/C^{eq})\left(\partial C^{eq}/\partial x\right)\right)\right]/\partial x , \qquad (1)$$

is used to formulate the problem. In Eq. (1) C^{eq} denotes the thermal equilibrium concentration or solubility of the considered species at the given temperature. The second term on the right-hand side (RHS) of Eq. (1) accounts for the spatial variations in C^{eq}.

An acceptor species consists of a neutral and an ionized species. The thermal equilibrium concentration of the neutral species is given by

$$C_{A^o}^{eq} = C_o \exp\left(- g_{A^o}^f/k_BT\right) , \qquad (2)$$

where C_o is the crystal lattice site density and $g_{A^o}^f$, the Gibbs free energy of incorporating an A^o onto a lattice site, is a constant determined *chemically*, which is independent of the semiconductor type and doping level. The fractional thermal equilibrium concentration of the ionized acceptors is given by the Fermi-Dirac distribution function $f=C_{A^-}^{eq}/(C_{A^o}^{eq} + C_{A^-}^{eq})=1/\left[1 + g \exp\left((E_a - E_F^{eq})/k_BT\right)\right]$,

where E_a is the shallow acceptor level energy position in the semiconductor bandgap, E_F^{eq} is the Fermi level energy position under thermal equilibrium conditions defined for the coexistence of the crystal and an unique acceptor source material, k_B is Boltzmann's constant, T is the absolute temperature, and g is the acceptor level degeneracy factor of 4. Solving for $C_{A^-}^{eq}$, We obtain

$$C_{A^-}^{eq} = (1/g) C_{A^0}^{eq} \exp\left((E_F^{eq} - E_a)/k_B T\right) . \tag{3}$$

Noting that $E_a \approx E_v$, $n_i = N_v \exp((E_v - E_i)/k_B T)$, and $p^{eq} = N_v \exp\left((E_v - E_F^{eq})/k_B T\right)$, where p^{eq} is the hole concentration under thermal equilibrium conditions, n_i is the intrinsic carrier concentration, E_v and E_i are respectively the valence band edge energy and the intrinsic Fermi level energy, and N_v is the effective density of states of the valence band, Eq. (3) becomes

$$C_{A^-}^{eq} = (1/g) C_{A^0}^{eq} (n_i/p^{eq}) \exp\left((E_i - E_v)/k_B T\right) . \tag{4}$$

In turn, p^{eq} satisfies the charge neutrality condition

$$p^{eq} = \left[C_{A^-}^{eq} + \left((C_{A^-}^{eq})^2 + 4n_i^2\right)^{1/2}\right]/2 . \tag{5}$$

It is seen from Eqs. (4) and (5) that, the thermal equilibrium concentration of the ionized species is dependent upon this concentration itself, since p^{eq} is determined by this concentration. With the exception of p^{eq}, all quantities in Eq. (4) are constants. These constants differ for different SL layers, resulting in different $C_{A^-}^{eq}$ values, which in turn leads to the A$^-$ segregation phenomenon.

The p-type dopants Zn and Be are substitutional-interstitial $(A_s$-$A_i)$ species in GaAs and other III-V compounds. The diffusion of A_s is accomplished by the migration of A_i and its subsequent change-over to become A_s via the kick-out mechanism involving the doubly-positively-charged group III self-interstitials I_{III}^{2+} [5,6]:

$$A_i^+ \Leftrightarrow A_s^- + I_{III}^{2+} , \tag{6}$$

where the interstitial species of the dopant is assumed to be a donor, A_i^+. Assuming that thermal equilibrium conditions hold for I_{III}^{2+}, we have

$$C_I = C_I^{eq} = C_I^{eq}(n_i)(p/n_i)^2, \tag{7}$$

where $C_I^{eq}(n_i)$ is C_I^{eq} under intrinsic conditions which is independent of the crystal Fermi level position or carrier concentrations. For A_i, the use of Eq. (1) in accordance with reaction (6) yields

$$\partial C_i/\partial t = \partial \left[D_i\left(\partial C_i/\partial x - (C_i/C_i^{eq})(\partial C_i^{eq}/\partial x)\right)\right]/\partial x - \partial C_s/\partial t . \tag{8}$$

where D_i are respectively the diffusivities of A_i^+, which is a constant at a given temperature in a given SL layer material. Assuming that *dynamical* equilibrium has reached among the three species A_s^-, A_i^+, and I_{III}^{2+}, the change of C_s is then described by

$$C_i/(C_s C_I) = K \equiv C_i^{eq}/(C_s^{eq} C_I^{eq}) , \tag{9}$$

where C_s^{eq} is the thermal equilibrium concentration of the ionized acceptor atoms A_s^- given by Eq. (4). Using Eqs. (4), and (7)-(9), and noting that $C_s + C_i \approx C_s$ and hence $\partial(C_s + C_i)/\partial x \approx \partial C_s/\partial x$, we obtain

$$\frac{\partial C_s}{\partial t} = \frac{\partial}{\partial x}\left[D_s^{eff}\left(\frac{\partial C_s}{\partial x} + \frac{C_s}{p}\frac{\partial p}{\partial x} - \frac{C_s}{n_i}\frac{\partial n_i}{\partial x} - \frac{C_s}{k_B T}\left(\frac{\partial E_i}{\partial x} - \frac{\partial E_v}{\partial x}\right) - \frac{C_s}{C_s^{eq}}\frac{\partial C_s^{eq}}{\partial x}\right)\right], \tag{10}$$

where D_s^{eff} is the effective A_s^- diffusivity given by

$$D_s^{eff} = K C_I^{eq}(n_i)(p/n_i)^2 D_i . \tag{11}$$

Due to doping and the bandgap discontinuity at a heterojunction, the junction region carrier concentration differs from those in the bulk material layers. At the junction, there is a local depletion of carriers one side and an accumulation of carriers on the other side, resulting in a space charge region associated with a local band bending and electric potential. With this potential included, the thermal equilibrium hole distribution is described by

$$p^{eq} = N_v \exp\left((E_v - E_F^{eq} - q\phi)/k_BT\right), \tag{12}$$

where q is the magnitude of the electron charge (taken to be positive); ϕ is the electrostatic potential throughout the SL structure, which changes rapidly in the heterojunction regions; and E_F^{eq} is the thermal equilibrium E_F position, which is constant throughout the SL structure. The quantities N_v and E_v are constants in each SL layer, but are different in the different SL layers. To account for the distribution of holes, the use of Eqs. (1) and (12) yield

$$\partial p/\partial t = \partial\left[D_p\left(\partial p/\partial x - (p/N_v)(\partial N_v/\partial x) - (p/k_BT)(\partial E_v/\partial x) + (pq/k_BT)(\partial\phi/\partial x)\right)\right]/\partial x, \tag{13}$$

where D_p is the hole diffusivity. The potential ϕ satisfies Poisson's equation

$$\partial^2\phi/\partial x^2 = (q/\varepsilon)[n - p + C_{A^-} - C_{D^+} - 2C_I], \tag{14}$$

where ε is the SL layer dielectric constant, C_{A^-} is the total ionized acceptor density for all acceptor species including A_s^-, and C_{D^+} is the total ionized donor density. Here the quantities C_{A^-} and C_{D^+} are used in Eq. (14) to account also for predoping of the SL layers. In the absence of the electric field, Eq. (14) is just the charge neutrality condition.

ANALYTICAL RESULTS

Using the partial differential equation solver ZOMBIE [7], Eqs. (7) and (9)-(15) were numerically solved to fit the available experimental results [1-3], Figs. 1-3. In obtaining these fits, it is assumed that: (i) the dopant diffusivity value under intrinsic conditions, $D_s^{eff}(n_i)$, which is obtained by letting $p=n_i$ in Eq. (12), is the same for all layers of a given SL structure; (ii) the $C_I^{eq}(n_i)$ value is the same for the different layers of each SL.

Figure 1 shows our calculated fitting curve together with the experimental results of Weber et al. [1] obtained by measuring hole concentrations after diffusing Zn at 550°C for 12 min into an InP/InGaAs/InP/InGaAsP SL. It is seen that the fit is excellent. For this case, our calculated Zn profile (not shown) is nearly identical to that of the holes. In accordance with those used by Zimmermann et al. [8], the used Zn intrinsic diffusivity value $D_s^{eff}(n_i)$ is $3\times10^{-13}cm^2s^{-1}$, and the used intrinsic self-interstitial thermal equilibrium concentration value $C_I^{eq}(n_i)$ is 5×10^9 cm^{-3}. The SL layer predoping conditions, together with the used values of the materials' constants for obtaining the fit are listed in Table 1.

Table 1. SL layer predoping conditions of the experiment of Weber et al. [8], and materials' constants used for obtaining the fit. The values of n_i, E_i, E_v and N_v are those at the experimental temperature of 550°C, referenced to the vacuum level of 0 eV. The listed layer $m_{s,o}^{eq}$ values (defined as the solublity ratio of A^o in two adjacent SL layers) are relative to that of the InP layer of 1.

| layer	predoping-type/ concentration (cm^{-3})	n_i (cm^{-3})	E_i (eV)	E_v (eV)	N_v (cm^{-3})	$m_{s,o}^{eq}$
InGaAs	n$^+$/3x10^{19}	2.2x10^{17}	-4.8	-5.31	8.67x10^{19}	100
InP	n/3x10^{17}	1.5x10^{16}	-5.2	-5.65	2x10^{19}	1
InGaAsP	p/3x10^{17}	3.24x10^{16}	-4.95	-5.43	5.17x10^{19}	35
InP	n/3x10^{17}	1.5x10^{16}	-5.2	-5.65	2x10^{19}	1

Fig. 1. The Webber et al. (ref. 1) hole data (open circles) in an InGaAs/InP/InGaAsP/InP SL structure obtained by Zn indiffusion, together with the calculated fitting curve (solid line).

Figure 2 shows our calculated fitting curve together with the experimental results of Humer-Hager et al. [2] obtained by implanting Be into a GaAs/Al$_{0.3}$Ga$_{0.7}$As structure on a GaAs substrate and annealed at 860°C for 3 s. It is seen from Fig. 2 that the fit is fairly satisfactory. The used Be intrinsic diffusivity value, $D_s^{eff}(n_i)$, is 1×10^{-13} cm^{2}s^{-1}, and the used self-interstitial thermal equilibrium concentration under intrinsic conditions, $C_I^{eq}(n_i)$, is 3.65×10^{11} cm^{-3}. In the experiment [1], the SL layers were pre-doped. For space reasons, the expereimental and fitting conditions correspond to those listed in Table 1 for Fig. 1 are given elsewhere [9].
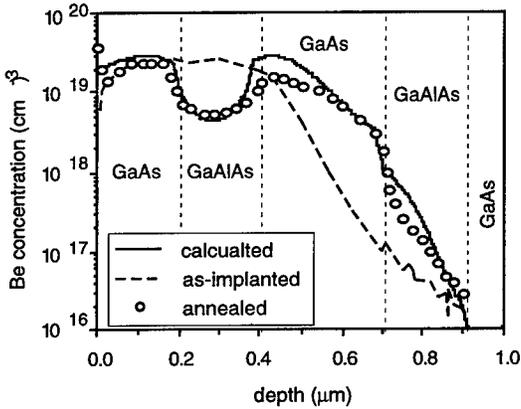
Fig. 2. The Be data of Humor-Haggler et al. (ref. 2) in GaAs/GaAlAs SL obtained by ion implantation, together with the calculated fitting curve. The broken line is the as-implanted Be profile, the symbols are the Be data after annealing, and the solid line is the fitting curve.

Figure 3 shows one example of our fits to the experimental data of Häussler et al. [3], from which it is seen that the fit is excellent. They obtained four sets of results by implanting Be into InP/InGaAs structures and annealing at 850°C for 6 or 26 s, two with the implanted Be peak concentration at the layer interface, and two with the Be peak inside the InGaAs layer. That shown in Fig. 3 is one of the two latter cases. The degree of satisfaction of our fits to all four sets of their data are the same. For these cases [3], the used Be intrinsic diffusivity value $D_s^{eff}(n_i)$ is 2.1×10^{-13} cm^{2}s^{-1} and the intrinsic self-interstitial thermal equilibrium concentration value $C_I^{eq}(n_i)$ is 3.7×10^{11} cm^{-3}. The used values of the materials' constants for obtaining the fits are given elsewhere [9]. The SL layer predoping conditions [3] are not known and we have assumed that they are intrinsic to begin with.

222
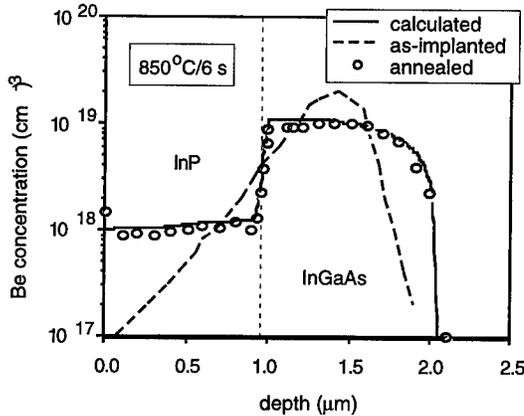
Fig. 3. The Be data of Häussler et al. (ref. 3) with Be implanted into the InGaAs layer and annealed at 850°C for 6s. Dashed lines are the as-implanted data, open circles are those after annealing, and the solid lines are the calculated fitting curves.

DISCUSSIONS

Our fittings to the available experimental dopant distribution data [1-3] are simultaneous descriptions of the acceptor diffusion process and segregation process, with the latter due to the acceptor solubility difference in the SL layers. For the neutral accepor atoms, this solubility difference is determined *chemically*, while for the ionized acceptor atoms, this difference further depends on the SL layer *Fermi-level*. Moreover, the detailed acceptor distribution process is also influenced by the effects of heterojunction space charges on the inoized acceptor concentrations and on the concetrations of I_{III}^{2+} govorning the acceptor diffusion process. The overall dopant distribution process involves diffusion and segregation of holes, I_{III}^{2+}, Zn^- or Be^-, and an ionized interstitial acceptor species. The junction electric field also changes with time and position. In the present study, we have found that the segregation coefficient of the neutral acceptor species A^0, $m_s^{eq\,0}$ determines the order of magnitude of the observed segregation phenomenon. The actually used m_s° values range from ~10 to 100. The Fermi-level effect and the junction carrier concentration effect determine the fine details of the observed acceptor distributions, including the profile shapes and a deviation of the segregation magnitude many times from that described by m_s° alone.

There are three prior attempts in modeling the acceptor diffusion-segregation phenomenon [2,9,10], to various degrees of satisfaction. Weber et al. [1] provided a simulation of their own data by assuming that the solubilities in the layers of the InGaAs/InP/InGaP/InP structure are of different constant values. By diffusing Zn into individual InGaAs and InP materials at 550°C, they found an 80 times Zn solubility difference. Their analysis provided a rough approximation to the complicated situation. Bracht et al. [10] fitted the presently used experimental data by assuming a constant dopant solubility difference in the SL layers due to an *electronic* effect given by exp(-$\delta\epsilon/k_BT$), where $\delta\epsilon$ is the E_v difference of two adjacent SL layers. This means that m_s^{eq} is taken to be 1 among the layers. Their electronic effect is arrived at via a Fermi level stabilization energy (E_{FS}) argument, which bears a resemblance to the presently discussed effect of the Fermi-level. The Fermi level stabilization energy concept is difficult to understand and seemingly illusive. The third attempt concerns with our own preliminary effort [11]. Irrespective of the apparently satisfactory fits obtained, which are very close to the present ones, the report contained errors. First, the segregation effect was attributed to the junction electric field effect alone, which is incorrect. Second, in what should have been the present Eq. (10), the terms concerning the role of n_i and of C_s° were missing. The missing of the n_i term was accidental and in the actual calculation the effect was included. The missing of the C_s° term is due to the use of the assumption $m_s^{eq}=1$. In obtaining the fits, the effect of m_s^{eq} does not equal to 1 was compensated by an adjustment in the E_v value differences among the adjacent layers. This is possible because, in Eq. (10), E_j, E_v and C_s° constitute *similarity* terms in the sense that they are of an identical mathematical form. It is obvious that

the mathematical forms of the E_i and E_v terms in Eq. (10) are identical. By noting that C_s^{eq} is given by Eq. (2), the term $(\partial C_s^{eq}/\partial x)/C_s^{eq}$ in Eq. (10) is equal to $-(\partial g_A^f/\partial x)/k_BT$, which is also of an identical mathematical form of that of the E_i and E_v terms. Thus, since the values of E_i, E_v, g_A° and their differences are all of the order of a couple to a few eV, it is seen that the misuse of the value of one quantity can be readily compensated by using also a wrong value for another quantity. This means that, to solve the problem, we need to know the values of E_i, E_v, and C_s^{eq} accurately, or else a fitting to the experimental data can be obtained by accounting for the effects of these quantities by an arbitrary value for any one of the three or in any combination, which can result in an erroneous interpretation of the physics involved. Under the $m_{s\circ}^{eq}=1$ assumption, our previous fitting parameters for the InGaAs and InP layers of Fig. 2 will lead to unacceptable E_i values which are too close to the E_c values of the appropriate layer materials. Thus, presently, the $m_{s\circ}^{eq}=1$ assumption is abandoned. Since the assumption of Bracht et al. [10] also involves $m_{s\circ}^{eq}=1$, we suppose that the same critique will hold also for their attempt.

CONCLUSIONS

In conclusion, we mention that the observed p-dopant segregation behavior in SL layers in short annealing time and/or low annealing temperature experiments has been satisfactorily explained using a model incorporating three effects. The overall dopant segregation behavior results from the chemical effect on the neutral acceptor species thermal equilibrium concentrations, the Fermi-level effect on ionized acceptor and charged point defect concentrations, and the junction carrier concentration effect on the dopant distribution kinetics in the SL layers. In principle, in SL layers of different chemical compositions the diffusivities of the ionized dopant atoms should be different. The present satisfactory fits of the experimental data means that, quantitatively, the contribution of this factor to the observed dopant segregation phenomenon is fairly small. This Fermi-level effect model has also provided satisfactory fits to available boron distribution profiles in Ge_xSi_{1-x}/Si heterostructures, see the accompanying article [12].

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Peak Voltage Insensitivity to Quantum Well Width in Resonant Interband Tunneling Diodes

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ABSTRACT

We have investigated the peak voltage (V_p) in InAs/AlSb/GaSb/AlSb/InAs double-barrier resonant *interband* tunneling (DBRIT) diodes with various GaSb well widths (L_w). After eliminating the voltage drop resulting from parasitic resistance included in the measured peak voltage (V_p^m), we found that the intrinsic peak voltage (V_p^{int}) was almost insensitive to L_w and had a small, and virtually constant value (~ 60 mV) at L_w, ranging from 10 to 30 monolayers. This insensitivity contrasts with the peak voltage of the conventional resonant tunneling diodes with intraband tunneling, which is sensitive to changes in L_w. This insensitivity can be explained by the fact that V_p^{int} in Sb-based BDRIT diodes is affected by the occupied states in the collector rather than by the resonance level itself in the *interband* tunneling process.

INTRODUCTION

Resonant tunneling diodes (RTDs) with negative differential resistance characteristics have been attracting increasing attention because they make it not only possible to reduce the complexity of circuit configurations [1,2,3,4], but also to increase the speed at which circuits operate [5,6,7]. When these RTDs are employed in practical circuit applications, a peak voltage (V_p) where the resonant tunneling current has a peak value is a crucial parameter for RTD circuits because it determines the operating bias voltage as well as the logic swing. In conventional type-I RTDs, where electrons travel through the resonance level formed in the conduction band of the well, V_p is sensitive to changes in the well width (L_w). This makes it difficult to achieve adequate control over the operating bias voltage and logic swing, which is needed for future RTD-based high-density integrated circuits such as A/D converters employing resonant-tunneling circuits [8,9].

On the other hand, in the InAs/AlSb/GaSb/AlSb/InAs double-barrier resonant *interband* tunneling (DBRIT) diodes, the resonance level is formed in the valence band of the well [10]. This suggests that the mechanism that determines V_p is quite different from that in conventional RTDs. Therefore, it is worthwhile investigating how sensitive V_p in DBRIT diodes is to changes in structural parameters.

The purpose of this paper is to report the dependence of V_p on L_w in InAs/AlSb/GaSb/AlSb/InAs DBRIT diodes and discuss what determines the dependence. We eliminated effects of the parasitic resistance from the measured peak voltage (V_p^m) in order to obtain the intrinsic peak voltage (V_p^{int}). Analyzing the dependence of V_p^{int} on L_w revealed that V_p^{int} was almost insensitive to changes in L_w and had a small and virtually constant value, 60 mV, even at L_w values ranging from 6.1 to
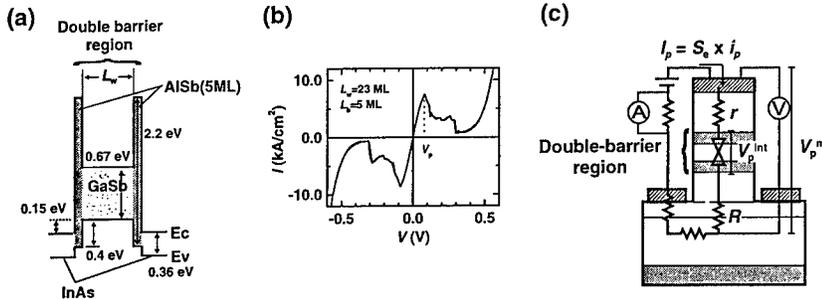
Fig. 1. (a) Schematic band-edge diagram of an InAs/AlSb/GaSb/AlSb/InAs double-barrier resonant interband tunneling (DBRIT) diode. The conduction-band edge and the valence-band edge are indicated by E_c and E_v. The thicknesses of the GaSb well layers (L_w) were 10, 17, 23, and 30 monolayers (ML). The thickness of the AlSb barrier layers was fixed at 5 ML. (b) Current-voltage (I-V) characteristics measured at room temperature for a DBRIT diode with L_w of 23 ML and L_b of 5 ML. The bottom electrode (collector) was grounded. The emitter area was 10 × 10 μm². (c) Schematic equivalent circuit of the measurement system. A peak current (I_p) is written as an emitter area (S_e) × a peak current density (i_p). The intrinsic peak voltage (V_p^{int}) is written as a measured peak voltage (V_p^m) – ($R \times I_p + r \times i_p$). R represents resistance that is independent of S_e. r represents resistance that dependson S_e.

18.3 nm. This insensitivity contrasts with the V_p of the conventional type-I RTDs. The insensitivity in DBRIT diodes can be explained by the fact that V_p^{int} in Sb-based BDRIT diodes with the interband tunneling process is affected by occupied states in the collector rather than the resonance level itself in the *interband* tunneling process.

EXPERIMENT

The heteroepitaxial layers for InAs/AlSb/GaSb/AlSb/InAs DBRIT diodes were grown by molecular beam epitaxy (MBE). The band-edge diagram of the DBRIT diodes and the typical current-voltage (I-V) characteristics are shown in Fig. 1. The double-barrier region of DBRIT diodes consisted of an undoped GaSb quantum well layer sandwiched between AlSb barrier layers. The thicknesses of the AlSb barrier layers (L_b) were fixed at 5 ML. The GaSb well layers ranged from 10 to 30 ML (from 6.1 to 18.3 nm) in thickness: 10, 17, 23, and 30 ML. The growth rate of AlSb was 0.25(±0.01) ML/s, and the growth rate of GaSb was 0.37(±0.02) ML/s. In order to obtain good uniformity in thickness for the AlSb and GaSb layers, the flux switching sequence was carefully controlled [11]. The double-barrier region was separated from Si-doped InAs electrode layers (n = 2×10¹⁷ cm⁻³) by 4.5-nm-thick unintentionally doped InAs spacer layers. The growth temperature of these layers was 460°C. Non-alloyed Ti/Pt/Au electrodes were used for ohmic contacts with the n-InAs emitter and collector layers.

RESULTS

Actually measured peak voltage (V_p^m) includes the additional voltage drop that

226

is caused by two kinds of series resistance (Fig. 1c). One is the resistance that is independent of the emitter area (S_e), whereas the other is the resistance that depends on S_e. The former is indicated by R. Usually the latter, such as the contact resistance between emitter semiconductor and electrode metal, is inversely proportional to S_e and thus can be written as r/S_e, where r is defined to be the resistance per unit area of the emitter. The peak current (I_p) is written as $I_p = S_e \cdot i_p$, where i_p is the peak current density. Thus the intrinsic peak voltage (V_p^{int}) can be defined as follows: $V_p^{int} = V_p^m - (R + r/S_e) \cdot I_p = V_p^m - (R \cdot I_p + r \cdot i_p)$, where $R \cdot I_p + r \cdot i_p$ is the additional voltage drop. In this study, we focused on the V_p^{int}. Current-voltage (I-V) characteristics for all the DBRIT diodes were measured at room temperature and the bottom (collector) electrode was grounded.

Fig. 2. Peak voltages ($V_p(I_p = 0)$ and V_p^{int}) vs. the well width (L_w). Open circles indicate the peak voltage (V_p) extrapolated to emitter area (S_e) of 0, or the peak current (I_p) of 0. The inset shows the peak current density (i_p) vs. the well width (L_w). Solid circles indicate the intrinsic peak voltage (V_p^{int}) from which voltage drop has been eliminated.

The $R \cdot I_p$ term can be eliminated when I_p is zero. Since I_p is proportional to S_e, we measured the peak voltage (V_p^m) for various S_e and extrapolated V_p^m to S_e of 0. The R obtained in this extrapolation ranged from 0.4 to 1.0 ohm. Open circuits in Fig. 2 represent the peak voltage at I_p of 0, which is indicated by $V_p(I_p = 0)$. When L_w increases from 10 to 30 ML (from 6.1 to 18.3 nm), $V_p(I_p = 0)$ decreases from 100 to 80 mV. It should be noted that the resonance level moves up toward the valence-band edge with increases in L_w when the resonance level is formed in the valence band in the well. Thus the decreases in $V_p(I_p = 0)$ are not due to the movement of the resonant level. The decrease in $V_p(I_p = 0)$ agrees rather with the behavior of i_p shown in the inset of Fig. 2. The agreement between $V_p(I_p = 0)$ and i_p implies that $V_p(I_p = 0)$ includes an additional voltage drop due to the $r \cdot i_p$ term. We estimated the relationship between $V_p(I_p = 0)$ and i_p, and eliminated the voltage drop due to $r \cdot i_p$. The r obtained in the relationship was 3.2×10^{-6} ohm·cm². Solid circles in Fig. 2 represent V_0, in which the voltage drop due to $r \cdot i_p$ is eliminated by the relationship. It was found that V_0 is almost insensitive to L_w ranging from 10 to 30 ML and is virtually constant at 60 mV. This insensitivity to L_w was not observed in conventional type I RTDs.

DISCUSSION

In conventional RTDs with *intraband* tunneling, V_p^{int} is the bias voltage that aligns the conduction-band edge of the emitter with the resonance level in the well. Because the resonance level, which is in the conduction band of the well, is sensitive to L_w, V_p^{int} is also sensitive to L_w.

In the following part, the insensitivity in DBRIT diodes with interband tun-

neling is discussed from two points of view: the sensitivity of the resonance level to L_w, and the alignment between band edges and the resonance level.

Because we have clarified that the resonant tunneling current flows mainly through the resonance level in the light-hole band [12], the resonance level itself is sensitive to L_w as it is in the intraband tunneling. Therefore, we have to consider the alignment in DBRIT diodes with interband tunneling, where the resonance level is formed in the valence band of the well. To satisfy the conservation law on total energy, only electrons that have a total energy below the resonance level can tunnel through the well to the collector. This means that the tunneling is affected more by the occupied states below the Fermi level in the collector than it is in conventional RTDs. This is because only electrons with a total energy greater than the resonance level can tunnel through the well in conventional RTDs with intraband tunneling (Fig. 3a). In particular, when the resonance level is low in the DBRIT diodes, the tunneling of the electrons in the emitter, which the conservation law allows to tunnel through the well, is limited more by the occupied states in the collector (Fig. 3b) and the resonance level itself is not crucial for determining V_p.

To understand the effects of the limitation on V_p, we calculated $V_p{}^{cal}$ using a simple model. In this model, the resonant tunneling current is calculated based on the conservation law over a total energy and the wave number parallel to the well layer. Figure 4 shows how $V_p{}^{cal}$ changes with the resonance level, E_z, for a DBRIT diode with interband tunneling. It is found that $V_p{}^{cal}$ decreases while E_z remains large. When E_z is low, $V_p{}^{cal}$ increases with a decrease in E_z. This increase is due to the occupied states in the collector as mentioned previouly, and it

(a) Intraband tunneling

(b) Interband tunneling
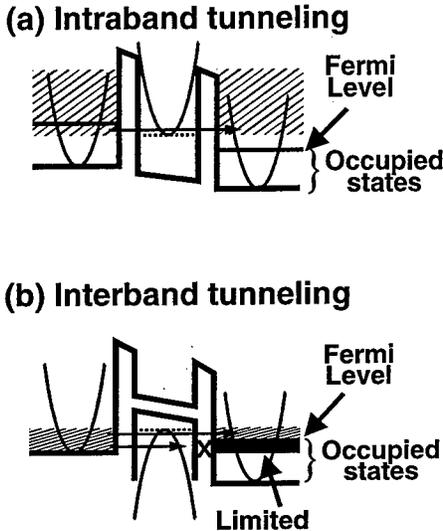
Fig. 3. Schematic band-edge diagrams of (a) an RTD with intraband tunneling and (b) a DBRIT diode with interband tunneling. The shaded portions in the both sides of (a) and (b) represent the energy range of electrons that can tunnel through the well from one side to the other. The solid portion in the right side of (b) represents the energy range where the tunneling is not allowed due to the occupied states in the collector.
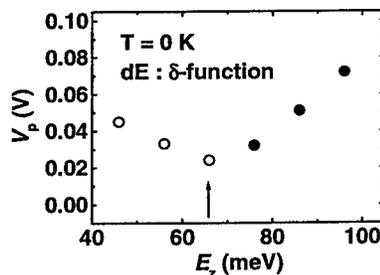
Fig. 4. Calculation result of the peak voltage ($V_p{}^{cal}$) vs. the resonance level in the well (E_z) in a DBRIT diode with interband tunneling. In this calculation, it is assumed that T = 0 K. The DBRIT probability is assumed to be a d-function.

228

makes the range of V_p (Fig. 4a) smaller than for that in the case where there are no effects of the occupied states in the collector (Fig. 4b).

CONCLUSION

In summary, we have investigated V_0 in InAs/AlSb/GaSb/AlSb/InAs DBRIT diodes with various L_w. Analyzing the dependence of V_p^{int} on L_w revealed that V_p^{int} was almost insensitive to L_w and had a virtually constant value, 60 mV. This insensitivity contrasts with the V_p of conventional RTDs with *interband* tunneling. The insensitivity of V_p^{int} to L_w in DBRIT diodes can be explained by the fact that V_p^{int} in Sb-based BDRIT diodes is affected by the occupied states in the collector rather than the resonance level itself in the *interband* tunneling process.

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Thermal Reliability of Pt/Ti/Pt/Au Schottky Contact on InP with a GaInP Schottky Barrier Enhancement Layer

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Abstract

We present the studies of the thermal stability of various metal including Au, Ti, Pt, Pd and Pt/Ti/Pt/Au Schottky contacts on strained $Ga_{0.2}In_{0.8}P/InP$ semiconductors. Auger electron spectroscopy (AES) analysis and cross-sectional TEM of the thermally annealed Schottky diode were performed to investigate the failure mechanism. For Pt/Ti/Pt/Au schottky contacts on strained GaInP/InP, no significant change was found for samples annealed up to 350°C. However, a drastic degradation of the barrier height and the ideality factor was observed in samples annealed at 400°C, which may be caused by the interdiffusion and penetration of metals into the semiconductor. Finally InGaAs/InP doped channel heterojunction FET's (DC-HFET's) with a GaInP Schottky barrier enhancement layer (SBEL) were grown and fabricated. The 0.25 μm gate-length devices showed excellent DC and RF performance, with an f_t of 117 GHz and an f_{max} of 168 GHz.

Introduction

Schottky contacts play an important role in III-V semiconductor devices, such as metal semiconductor field-effect transistors (MESFETs), heterojunction field effect transistors (HFETs), and solar cells. The Schottky barrier height of the gate contact must be large enough to obtain a good rectifying gate contact. However, the low barrier height and the high leakage currents in InP Schottky diodes due to surface Fermi level pinning have made it difficult to realize Schottky contacts on InP [1]. To increase the barrier height, a high bandgap material can be grown on InP to serve as a Schottky barrier enhancement layer (SBEL). In particular, strained GaInP has been investigated [2]. This material presents several advantages over other choices for SBELs (AlInAs or AlInP): 1) GaInP does not contain Al, and therefore may not suffer from Al-related reliability problems and a high deep-level concentrations, 2) GaInP on InP has a conduction band offset ratio ($\Delta E_c/\Delta E_g = 0.8$) that favors carrier confinement [3], 3) selective wet etching of the InGaAs cap layer over GaInP Schottky layer is available, leading to better gate recess control and thus improved threshold voltage uniformity [4]. Because of these advantages, the potential to replace AlInAs and AlInP for SBEL applications.

In this paper, we have systematically investigated the Schottky characteristics on strained $Ga_{0.2}In_{0.8}P/InP$ grown by gas-source molecular beam epitaxy (GSMBE). Different metals including Pt, Ni, Pd, Au, Ti and Pt/Ti/Pt/Au were deposited on $Ga_{0.2}In_{0.8}P/InP$ for these studies. The barrier height, ideality factor, and, thermal stability of these metal/$Ga_{0.2}In_{0.8}P/InP$ diodes were then examined by various methods. Furthermore, in order to study the thermal stability and failure mechanism of the Pt/Ti/Pt/Au Schottky metals on GaInP/InP. Auger electron spectroscopy (AES) analysis and cross-sectional TEM of the thermally annealed Schottky diode were performed. Finally, an InP/InGaAs doped channel HFET structure with a $Ga_{0.2}In_{0.8}P$ SBEL was grown. Both DC and high frequency performance of these devices will be discussed.

Experimental Details

Epitaxial growth of all structures was performed in a modified Perkin-Elmer 430P GSMBE/CBE system. The growth chamber was equipped with a 5000 l/s cryopump and a 2200 l/s turbomolecular pump. Cracked AsH_3 and PH_3 (100%) were used as the group V sources, while elemental solid sources in effusion cells were used for the group III sources. Substrate temperatures (T_s) were measured using a thermocouple which was calibrated by observing the melting point of InSb (525°C). The composition of $Ga_{0.2}In_{0.8}P$ was determined by the gallium and indium beam flux and were examined ex-situ by double crystal X-ray diffraction rocking curve. XTEM measurements made on a Hitachi H800 electron microscope operated at 200kV.

There are three methods to used to determine the barrier heights of the Schottky diodes: the current-voltage (I-V), temperature-dependent current-voltage (I-V-T), and capacitance-voltage (C-V) methods [5-6]. The barrier height determined by these methods are designated as $q\phi_{bn}(I$-$V)$, $q\phi_{bn}(I$-V-$T)$, and $q\phi_{bn}(C$-$V)$, respectively.

According to thermionic emission theory, the forward I-V characteristics of the diode can be described by the following equations:

$$J_s = A^{**}T^2 exp(-q\phi_{bn}/kT), \qquad (1)$$

$$\phi_{bn} = \frac{kT}{q}\ln(\frac{A^{**}T^2}{J_s}), \qquad (2)$$

and

$$n = \frac{q}{kT}(\frac{dV}{d(\ln J)}), \qquad (3)$$

where J_s is the saturation current density obtained by an extrapolation of the log(J) versus V (forward bias) curve to V=0. Other symbols are defined as follows: q is the charge of the electron, V is the applied voltage, n is the ideality factor, k is the Boltzmann constant, T is the measurement temperature, A^{**} is the effective Richardson's constant constant (14 A/cm^{2}K^2 for $Ga_{0.2}In_{0.8}P$), and ϕ_{bn} is the barrier height.

The barrier height determined by the I-V-T method can be given by the equation:

$$\phi_{bn} = -\frac{k}{q}\frac{\Delta(\ln(\frac{J_s}{T^2}))}{\Delta(\frac{1}{T})} \qquad (4)$$

To find the barrier height from the C-V method, an equation for the capacitance of a Schottky diode is needed. Under the abrupt-junction approximation, the capacitance of a Schottky diode is given by the equation:

$$\frac{C}{A} = \sqrt{\frac{q\varepsilon\varepsilon_0|N_d - N_a|}{2(V_{bi} + |V| - kT/q)}} \qquad (5)$$

where V is the reverse-bias voltage, ε is the dielectric constant, ε_0 is the permittivity of free space (=8.854×10^{-14} F/cm), A is the diode area, V_{bi} is the built-in voltage produced by the depletion of electrons at the metal-semiconductor interface, and N_d and N_a are the donor and acceptor concentrations, respectively. The net donor concentration, N_d-N_a, can be obtained from the slope of the $(A/C)^2$ –V plot and V_{bi} can be obtained from the V-axis intercept through the relationship V_i = -V_{bi} + kT/q. The Schottky barrier height ϕ_b in turn is related to V_{bi} by the relationship

$$\phi_{bn} = V_{bi} + V_n \qquad\qquad\qquad (6)$$

where $V_n = (kT/q) \ln(N_C/N_d)$ and N_C is the effective density of states at the conduction band edge. The I-V and C-V characteristics of these Schottky diodes were measured using an HP 4145B semiconductor parameter analyzer and an HP 4275 C-V meter, respectively.

Results and Discussion

(a) Measurements of $Ga_{0.2}In_{0.8}P$ Schottky Barrier Heights

Fig. 1(a) shows the J-V characteristics measured at room temperature for the Au/$Ga_{0.2}In_{0.8}P(150Å)$/InP Schottky junction. The J-V characteristics of the Au/InP Schottky junction are also shown for comparison. On the basis of the equations (1)-(3), $q\phi_{bn}(I$-$V)$ is estimated to be 0.645 and 0.45eV for the $Ga_{0.2}In_{0.8}P$ and InP junctions, respectively. The ideality factors are 1.02 and 1.07 for the $Ga_{0.2}In_{0.8}P$ and InP samples, respectively. The I-V-T measurements were performed in the temperature range 300–400 °K. A Richardson plot of the I-V-T measurement results is given in Fig. 1(b). Using the saturation current obtained for each J-V characteristic and equation (4), $q\phi_{bn}(I$-V-$T)$ is estimated from the slope of the Richardson plot, to be 0.689 and 0.449 eV for the $Ga_{0.2}In_{0.8}P$ and InP Schottky junctions, respectively.
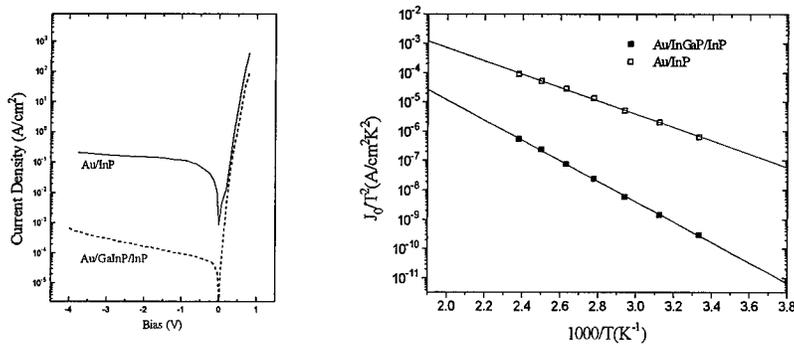

Fig. 1(a) J-V characteristic of Au/InP Schottky diodes with and without GaInP Schottky barrier enhancement layer at room temperature. (b) The Richardson plot of Au/InP Schottky diodes with and without GaInP Schottky barrier enhancement layer

Table 1 Measured barrier height of different metal on $Ga_{0.2}In_{0.8}P$/InP Schottky diodes.

Metal	$q\phi_M$ (eV)	n	$q\phi_{bn}(I$-$V)$ (eV)	$q\phi_{bn}(I$-V-$T)$ (eV)	$q\phi_{bn}(C$-$V)$ (eV)
Pt	5.65	1.04	0.75	0.77	0.8
Ni	5.15	1.03	0.65	0.675	0.71
Pd	5.12	1.02	0.72	0.745	0.78
Au	5.1	1.04	0.645	0.689	0.72
Ti	4.33	1.08	0.6	0.63	0.68

Several metals including Pt, Ni, Pd, Au, and Ti were investigated as the Schottky contacts on strained $Ga_{0.2}In_{0.8}P/InP$. Table. 1   lists the measured $q\phi_{bn}(I\text{-}V)$, $q\phi_{bn}(I\text{-}V\text{-}T)$, and $q\phi_{bn}(C\text{-}V)$ for each different metal contact. Based on the results, $q\phi_{bn}(I\text{-}V)$ and $q\phi_{bn}(I\text{-}V\text{-}T)$ are in good agreement with each other but both of them are smaller than $q\phi_{bn}(C\text{-}V)$. There are several reasons for this disagreement. The equality of the barrier heights for $I\text{-}V$ and $I\text{-}V\text{-}T$ methods occurs because both measure the energy necessary to excite electrons from the metal into the semiconductor and any barrier height lowering is almost equally effective. In the $C\text{-}V$ method the data are extrapolated to $1/C^2 = 0$ corresponding to near flatband conditions in the semiconductor and the barrier height lowering is close to zero [6]. In addition, any damage at the interface affects the $I\text{-}V$ behavior because defects may act as recombination centers or as intermediate states for trap-assisted tunnel currents. Either one of these mechanisms raises n and lowers ϕ_{bn}. $C\text{-}V$ measurements are less prone to such defects. Another novel find is that the barrier height is in the range of 0.6~0.75 eV irrespective of the metal work function (ϕ_M). The ideality factors range from 1.02 to 1.08 depending on the selection of the metals. These observations suggest that Fermi level pinning occurs for Schottky junctions on GaInP similar to the pining for InP Schottky junctions formed by conventional wet etch processes and electron-beam evaporated contacts.

(b) Thermal stability

The thermal stability of the single-layer metal (Pt, Ni, Pd, Au, and Ti) on $Ga_{0.2}In_{0.8}P/InP$ was examined. The Schottky diodes were annealed using a conventional furnace in an N_2 ambient at a temperature ranging from 100°C to 450°C. At each temperature the annealing time was 10 min. The barrier heights and ideality factors under different annealing temperatures are listed in Table 2. The symbol '-' means the rectifying properties vanished. Among single-metal films, the Pt Schottky diode has the best thermal stability since a barrier height as high as 0.68 eV and an ideality factor ~1.08 were maintained after an annealing temperature of 350°C.

Table 2 Barrier height and Ideality factor against annealing temperature for 10 min anneals.

Annealing Temperature	Pt		Ni		Pd		Au		Ti	
	$q\phi_{bn}$ (eV)	n	$q\phi_{bn}$ (eV)	n	$q\phi_{bn}$ (eV)	n	$q\phi_{bn}$ (eV)	n	$q\phi_{bn}$ (eV)	n
As deposited	0.75	1.04	0.65	1.03	0.72	1.02	0.645	1.04	0.6	1.08
T=100°C	0.76	1.04	0.67	1.02	0.73	1.02	0.66	1.03	0.61	1.06
T=200°C	0.76	1.04	0.67	1.02	0.73	1.02	0.66	1.03	0.61	1.06
T=250°C	0.76	1.04	0.66	1.04	0.71	1.04	0.64	1.04	0.6	1.07
T=300°C	0.75	1.05	0.61	1.08	0.7	1.05	0.5	1.12	0.55	1.1
T=350°C	0.68	1.08	0.5	1.2	0.55	1.12	-	-	0.45	1.2
T=400°C	0.64	1.13	-	-	-	-	-	-	-	-

Furthermore, for device applications, the thermal stability and failure mechanism of Pt/Ti/Pt/Au (50/250/500/300Å) Schottky metals on GaInP/InP was studied. Auger electron spectroscopy (AES) analysis and cross-sectional TEM were performed on the thermally annealed Schottky diodes. No significant change was found for samples annealed up to 350°C. However, a drastic degradation of the barrier height and the ideality factor was observed in samples annealed at 400°C ($q\phi_{bn}$ =0.6 eV n=1.2). From AES analysis, it is obvious that there is significant interdiffusion and penetration among chemical elements for the Schottky diode heated at 400°C. Both the interdiffusion and penetration among the Ti, Pt, and GaInP layers were observed. The interdiffusion and penetration between Ti and Pt, and GaInP layer as annealed at 400°C can be

observed by XTEM as shown in Fig. 2. Therefore, the deterioration of the Schottky diode heated at 400°C can be attributed to the penetration of Ti and Pt into the GaInP.

Fig. 2 Cross-sectional TEM Image of Pt/Ti/Pt/Au on GaInP/InP after annealed at 400°C for 10 min. The interdiffusion and penetration between Ti and Pt, and GaInP layer.

Interdiffusion

(c) Device Performance of an InGaAs/InP Doped Channel HFET with a GaInP SBEL

Based on the above studies, the $Ga_{0.2}In_{0.8}P(150Å)/InP/InGaAs/InP$ DC-HFET structure shown in Fig. 3.9 was grown. The process is similar to standard ion-implanted MESFET processes except for the gate recess. The devices were fabricated with mesa isolation and AuGe/NiAu ohmic contacts for the source and drain contacts were alloyed at 400°C for 10min. Mushroom shaped gates were then patterned with a gate length of 0.25 μm using a trilayer resist structure and electron-beam lithography. A selective $H_3PO_4:H_2O_2:H_2O$ (1:1:100) etchant was used for gate recessing. Finally, Pt/Ti/Pt/Au gates were evaporated and lifted-off, completing the FET fabrication process. The device showed both good dc and high frequency properties. The extrinsic dc transconductance is 665 mS/mm and the saturated drain current is 460 mA/mm at V_{ds}= 3V and V_{gs}=0.5V.Using an HP8510C Network Analyzer and an HP4142B DC Source/Monitor, high-frequency S-parameters were measured from 1 to 50 GHz. Fig. 3 shows the high frequency dependence of maximum current gain H_{21} and Mason's invariant, U, at V_{gs}=0.5V V_{ds}=3V. Extrapolations at 20dB/decade from 20 GHz for $|H_{21}|$ and U results in a unity current-gain cutoff frequency (f_T) of 117 GHz and a maximum frequency of oscillation (f_{max}) of 168 GHz. The obtained value of f_T =117 GHz is to our knowledge the highest value for a 0.25 μm gate length InP/InGaAs DC-HFET with GaInP SBEL.

Conclusion

In summary, we have systematically investigated the Schottky characteristics of metal/$Ga_{0.2}In_{0.8}P$/InP. It is found that barrier heights of 0.6~0.7 eV are achieved for Schottky junctions formed on $Ga_{0.2}In_{0.8}P$/InP. Fermi level pinning occurs at the surface of the wet-etched $Ga_{0.2}In_{0.8}P$ prior to metallization. In addition, no degradation in the Schottky characteristics was observed after anneals at temperatures as high as 250°C for 10 min. For Pt/Ti/Pt/Au schottky contacts on GaInP/InP, no significant change in barrier height was found for samples annealed

up to 350°C for 10 min. However, a drastic degradation of the barrier height and ideality factor was observed in samples annealed at 400°C for 10min, which may be caused by the interdiffusion and penetration of metals into the semiconductor The extrinsic DC transconductance of the HFET was 665 mS/mm, and the f_T and f_{max} values were 117 and 168 GHz, respectively. These f_T and f_{max} are also comparable to those of AlInAs/InGaAs HEMTs with the same gate length which suggest that GaInP is a promising material for replacing AlInAs as a SBEL for InP-based HFET applications.
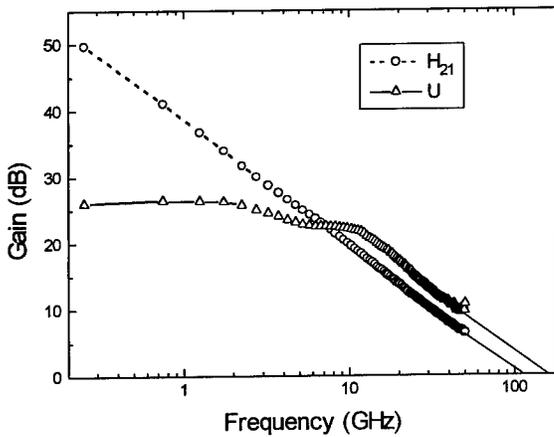

Fig. 3 High frequency dependence of the maximum current gain $|H_{21}|$ and Mason's invariant, U, at V_{gs}=0.5V and V_{ds}=3V.

Acknowledgement

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High Performance Cu-Metallized GaAs HEMTs Processing and Reliability

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Abstract

AlGaAs/GaAs based high electron mobility transistors (HEMTs) with Cu/Ti metallized gates have been fabricated. Copper gates were used to achieve low gate resistance and to minimize the hydrogen induced device degradation. The DC measurement of the processed AlGaAs/GaAs HEMTs with Cu/Ti gates shows comparable performance to similar Au based GaAs HEMTs. The Cu-based HEMTs were also subjected to elevated temperature testing under 5% H_2 –N_2 forming gas up to 250°C and 8 hours and no degradation due to hydrogen effects was found.

INTRODUCTION

GaAs based high electron mobility transistors (HEMTs) have been widely used in opto-electronic and telecommunication applications. However, the reliability of GaAs HEMTs due to hydrogen effects is still a major issue. Hydrogen is a very common impurity in semiconductors. It can be incorporated during the crystal growth and more importantly, it is present virtually at every device processing step of the devices. Hydrogen is found in the chemicals used for wet etching, solvent cleaning, in organic dielectrics and passivation, and in water vapor in vacuum systems. It has been reported that the contamination of hydrogen in a hermetic package can significantly affect the reliability of the HEMTs and cause a pronounced degradation in the electrical performance within a hundred hours at a temperature 175°C [1]. The HEMT degradation is even found within tens minutes under a 4% H_2 forming gas at 270°C [2]. The donor neutralization by hydrogen has been explained as one of possible causes resulting in the degradation of the devices[1-4].

The purpose of the copper metallization in this work is not only to lower the gate resistance but to retard hydrogen penetration into device active region. In this paper we present the results of the DC performance of AlGaAs/GaAs HEMTs with Cu/Ti metallized gates and the reliability issue related to the hydrogen effects.

HYDROGEN EFFECTS ON COPPER

Copper is found to be an endothermic occluder for hydrogen[5], which indicates that the solubility of hydrogen in copper increases with increasing temperature. It has been reported that the ductility of copper can be significantly affected by hydrogen, which has been referred to hydrogen embrittlement of copper[5-7]. However, the mechanism of the hydrogen effect has not been well understood yet. One explanation is that if copper contains an amount of cuprous oxides, the reaction $Cu_2O+H_2->2Cu+H_2O$ could take place, forming water bubbles inside the grains and grain boundaries, which lower the strength of copper[8]. The work by Nakahara, etal[9] shows that the hydrogen effect is due to the development of molecular hydrogen in voids

inside copper and the formation of dislocation loops along the precipitation of the absorbed atomic hydrogen in molecular form. Copper is the only metal to form a hydrite phase among the group IB metals (Cu, Ag, Au). Copper hydrite (CuH) is quite stable at ambient temperatures and the structure of this compound is shown to be hexagonal with lattice parameters a=0.289nm and c=0.461nm[10].

Compared to copper, gold is insensitive to hydrogen and is shown to absorb almost no hydrogen at room temperature[5]. Therefore, the use of copper metallization instead of gold may tie certain amount of hydrogen atoms inside copper metal and minimize the hydrogen penetration into the device active region, and therefore reduce the hydrogen induced device degradation. In addition to the hydrogen concern, other advantages of copper metallization include the lower resistance than even gold and its low cost.

HEMT FABRICATION AND RELIABILITY

The schematic structure of GaAs/AlGaAs HEMTs is shown in Figure 1. The top layer is Si doped n+ GaAs with $2x10^{18}$ cm^{-3} in order to achieve low ohmic contact resistance. The donor layer is n+ AlGaAs with 0.24 Al mole fraction in order to reduce the alloy clustering and DX centers. The channel layer is 50nm undoped GaAs. The buffer layer is a GaAs/AlGaAs superlattice, which is used to build up an additional potential barrier to enhance 2D electron gas confinement and reduce the electron trapping from AlGaAs and the substrate, therefore reducing the leakage current.
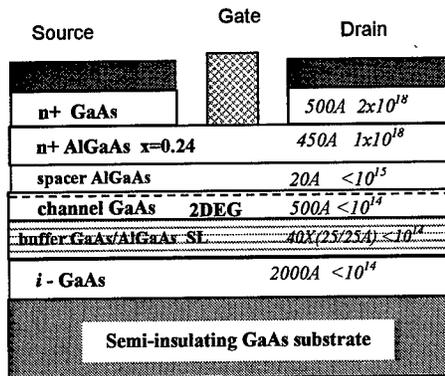

Figure 1. Schematic structure of GaAs/AlGaAs HEMTs.

The main fabrication procedure of the GaAs/AlGaAs HEMTs with Cu/Ti gates is shown in Figure 2. The device process involved mesa etching, ohmic contact formation, a gate recess, and finally gate metallization. Ohmic contacts were formed with AuGe/Ni/Au alloying at 420°C. The gate contact consists of 150nm Ti following by a 150nm copper cap layer deposited by E-beam evaporator. The NH$_4$OH, H$_2$O$_2$ and H$_2$O mixing solution was used to do gate recess. The fabricated GaAs/AlGaAs HEMT with a Cu/Ti gate is shown in Figure 3. The gate width is 250 microns and gate length is 1.5 microns, respectively.

1. Mesa Etching   2. Ohmic Contact Formation

3. Gate Recess   4. Gate Metallization

n^+ GaAs n^+ AlGaAs i - GaAs

SL Buffer   S.I. substrate   Resist
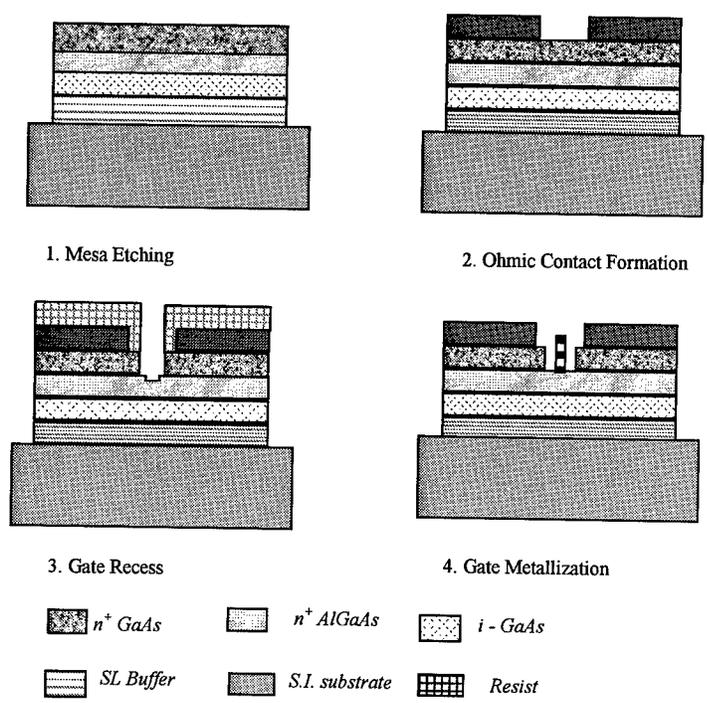
Figure 2. Scheme of fabrication procedures for Cu/Ti gate HEMTs.
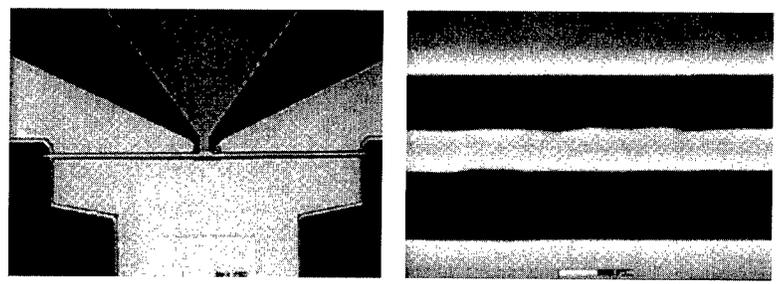
Figure 3. The SEM image of a Cu/Ti gate HEMT.

239

The DC characteristics were measured and are shown in Figure 4. A variational charge control model[11] was used to simulate the DC performance of the GaAs/AlGaAs HEMTs and shows good agreement with experimental results of Figure 4.
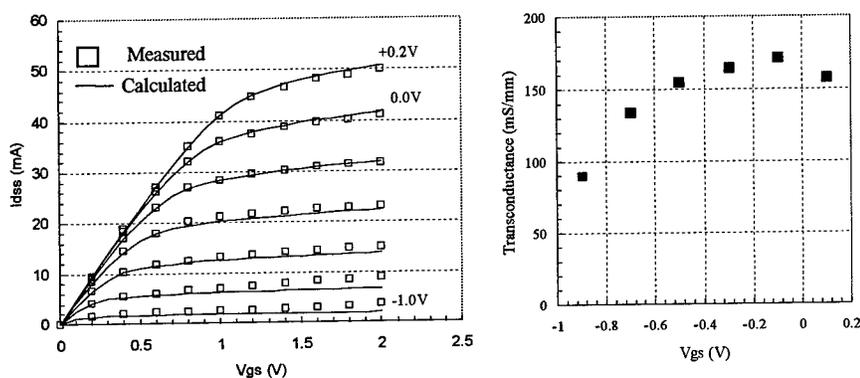

Figure 4. The measured and simulated DC characteristics of Cu/Ti gate HEMTs.

Neutralization of Si donor in n-type GaAs and AlGaAs alloys under hydrogen diffusion has been explained as the formation of hydrogen-silicon complexes[12, 13]. The existence of these complexes has been proved from the observation of local vibrational modes of hydrogen bound to silicon donors[14]. The passivation of donors by hydrogen can reduce the doping level and change the device performance. Figure 5 shows the calculated DC characteristics change by hydrogen passivation from the variational charge control model.
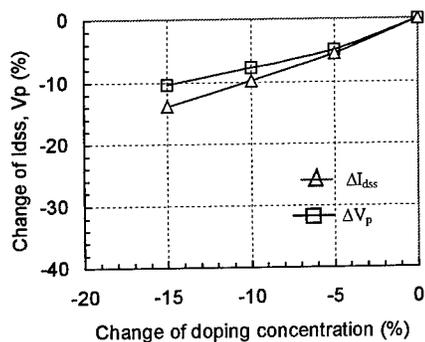

Figure 5. The calculated results show a shift of V_{th} and I_{dss} by the reduction of donor layer doping density, which may result from donor neutralization by hydrogen.

The fabricated Cu/Ti gate GaAs/AlGaAs HEMTs were subjected to temperature testing under 5% H_2-N_2 forming annealing at 250°C for up to 8 hours. The saturation current was

monitored as a parameter for degradation and almost no change was found after the H_2 forming gas anneal. The Fourier transform infrared spectrum(FTIR) was taken for the same HEMT wafer annealed in H_2 forming gas and no Si-H bonds were detected. Unlike the report from Chao[2], since there is no Pt playing a role to dissociate or ionize the molecular hydrogen gas in our case, the hydrogen gas can not diffuse into the device active region and cause the passivation of donors. The device may be more sensitive to the atomic or ionized hydrogen sources, and therefore, investigations with ionized hydrogen sources will be undertaken in the near future.

CONCLUSIONS

AlGaAs/GaAs based high electron mobility transistors (HEMTs) with Cu/Ti metallized gates have been fabricated. The purpose of the copper metallization is not only to achieve a low gate resistance, but also to minimize the hydrogen induced device degradation. The DC measurements of the processed AlGaAs/GaAs HEMTs with Cu/Ti gates show comparable performance to similar Au based GaAs HEMTs. The Cu-based HEMTs were also subjected to elevated temperature testing under 5% H_2 –N_2 forming gas up to 250°C and 8 hours and no degradation due to hydrogen effects was found.

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EFFECTS OF CF$_4$ REACTIVE ION ETCHING ON Si-DOPED Al$_{0.2}$Ga$_{0.8}$As

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ABSTRACT

Effects of CF$_4$ reactive ion etching on electrical characteristics of Si-doped Al$_{0.2}$Ga$_{0.8}$As layers were studied with capacitance-voltage and deep level transient spectroscopy measurements. Plasma exposure for about 30 s drastically degrades the electrical characteristics. Post-annealing at 360 °C for 20 s partially recovers the carrier concentrations. After the post-annealing, some electron traps were observed. Two of the traps show bi-stability. The concentrations of the two traps increase with forward bias temperature annealing and decrease with reverse bias temperature annealing.

1. INTRODUCTION

Reactive ion etching (RIE) has been widely used for fabrication of high-speed devices such as high electron mobility transistors (HEMTs). However, it has been reported that RIE processes introduce plasma damage and contamination.[1-3] Suppression of deep levels induced by RIE is important to obtain excellent device performance.

In this study, we evaluate the effects of CF$_4$ RIE on Si-doped Al$_{0.2}$Ga$_{0.8}$As with capacitance-voltage (C-V) and deep level transient spectroscopy (DLTS) measurements. In the measurements using capacitance, the detectable region is deeper than the depletion edge at 0 V. In order to detect electrical characteristics at near surface region, high carrier concentration samples were used.

2. EXPERIMENTAL PROCEDURE

Figure 1 shows the flow chart of the experimental procedure in this study. The schematic cross section of the sample used is shown in Fig. 2. 130 nm-thick Si-doped (1×10^{18} cm^{-3}) Al$_{0.2}$Ga$_{0.8}$As layers were grown by molecular beam epitaxy on semi-insulating GaAs at a substrate temperature of 600 °C. It included 650 nm-thick undoped GaAs and 260 nm-thick undoped Al$_{0.2}$Ga$_{0.8}$As buffer layers to avoid two-dimensional-electron-gas (2DEG) formation. A 6.5nm Si-doped GaAs cap layer was grown on the Al$_{0.2}$Ga$_{0.8}$As layer. A 150 nm-thick SiN thin film was deposited on the cap layer with plasma-chemical vapor deposition at 250 °C. AuGe/Ni Ohmic contacts were fabricated on the GaAs layer using the SiN mask which was selectively removed by wet etching. Before fabrication of Schottky contacts, the SiN layers were selectively removed by CF$_4$ RIE for 70 s and 100 s with a resist mask. 70 s RIE nearly just etched off the SiN layer under the experimental condition used in this study. Thus, 100 s RIE corresponds to 30 s exposure for the GaAs cap layer. After the 100 s RIE, some samples were annealed at 360 °C for 20 s in a hydrogen ambient. For control samples, the SiN layer was etched off with wet process. In all samples, GaAs cap layers were selectively etched off with wet process using the SiN mask. Au Schottky contacts were made on the Al$_{0.2}$Ga$_{0.8}$As surface with vacuum evaporation. The Schottky contact area was 2.0×10^{-8} m^2. All samples experienced heat treatments at 200 °C for photoresist process.

Electrical characteristics were measured with capacitance-voltage (C-V) method and deep level transient spectroscopy (DLTS) method with bipolar rectangular weighting function.[4,5] In addition to temperature scan DLTS measurements that are usually used, rate-window scan DLTS measurements at constant temperature were applied. The latter method, which we term isothermal constant-voltage capacitance transient spectroscopy (CVCTS) method, is suitable for the study of the heat treatment effect, because it can avoid the annealing effect during temperature scan DLTS

CRYSTAL GROWTH (MBE, Growth Temperature = 600 °C)

SiN THIN LAYER DEPOSITION (plasma chemical vapor deposition, 250 °C)

OHMIC CONTACT FORMATION (AuGe/Ni Alloy)

WET ETCHING   RIE 70 s   RIE 100 s

HEAT TREATMENT
(360 °C, 20 s, H_2)

REMOVAL of GaAs CAP LAYER (wet etching)

SCHOTTKY CONTACT FORMATION (Au, vacuum evaporation)

METALLIZATION

ELECTRICAL MEASUREMENTS (C-V, DLTS measurements)

Fig.1   Flow chart of the experimental procedure

Si-doped region
(10^{18} cm^{-3})

un-doped region

Schottky Contact
Ohmic Contacts

n-GaAs   (6.5 nm)
n-$Al_{0.2}Ga_{0.8}As$ (130 nm)
i-$Al_{0.2}Ga_{0.8}As$ (260 nm)
i-GaAs   (650 nm)
SI-GaAs   (450 μm)
(substrate)
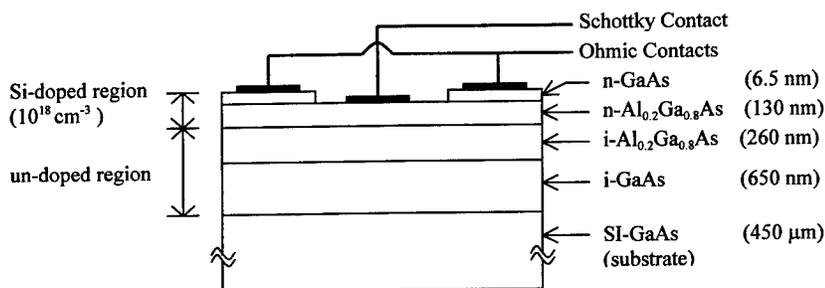
Fig.2   Schematic cross section of the sample

Table I   Capacitance values at 0 [V]

Sample Name	Etching of SiN thin layer	C [pF] at 0 [V]
control	wet etching	53.3
RIE70	RIE 70 s	53.0
RIE100	RIE 100 s	4.2
RIE100A	RIE 100 s + 360 °C annealing	31.9

measurements, and a choice of an appropriate temperature can resolve the spectra of each traps.[6]

3. RESULTS AND DISCUSSIONS

Table I shows the capacitance values measured at 0 V which are related to carrier concentration between the surface and the depletion region edge.   These are averaged values of several samples. The capacitance value of the RIE70 sample is nearly unchanged from that of the control sample, while that of the RIE100 sample drastically decreases.   Post-annealing at 360 °C partially recovers the

capacitance value.   The thickness of the n-AlGaAs layer is 130 nm.   The capacitance value, which corresponds to the 130 nm depletion width, is 16.6 pF.   The observed capacitance value at 0 V in the RIE100 sample is less than this value.   When the carrier concentration uniformly decreases below 6.4×10^{16} cm^{-3} and the built-in potential is 0.8 eV, the depletion layer extends over 130 nm from the semiconductor surface.   The capacitance value of the RIE100A sample suggests that the carrier concentration is about 5×10^{17} cm^{-3} under the assumption of a constant profile of carrier concentration through the post-annealing.

Figure 3 shows the carrier concentration depth profiles of the control, RIE70 and RIE100A samples.   The carrier depth profile of the RIE70 sample is similar to that of the control sample. After RIE for 100 s, the epitaxial layer completely depletes as mentioned above.   Post-annealing partially recovers the carrier concentration.   The carrier concentration is about 6×10^{17} cm^{-3}, which corresponds to about 60 % of the carrier concentration of the control sample.   This carrier concentration is consistent with the estimated carrier concentration value calculated from the
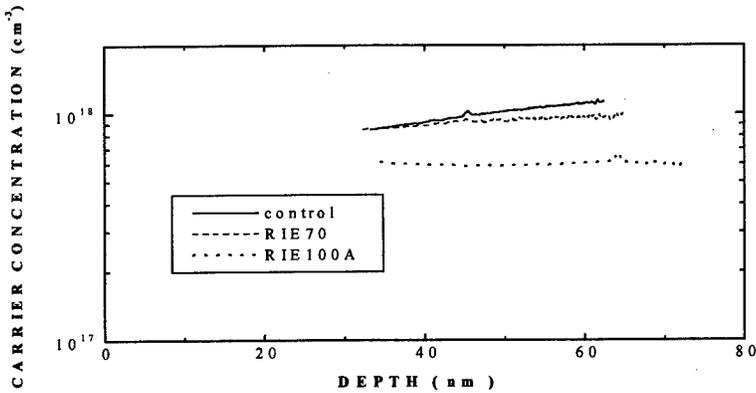

Fig. 3   Carrier concentration depth profiles of the control, RIE70 and RIE100A samples
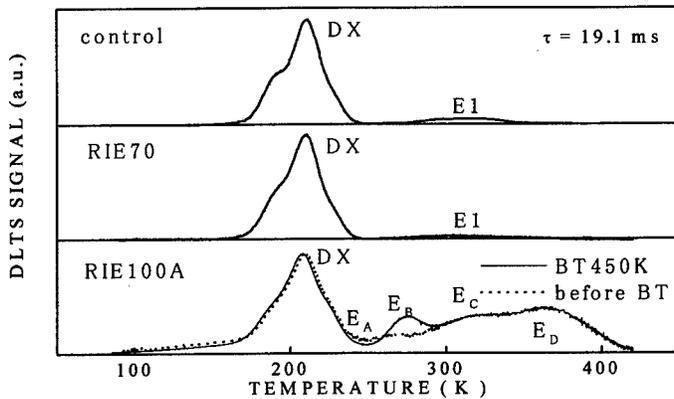

Fig. 4   DLTS spectra of the control, RIE70 and RIE100A samples.   In the RIE100A sample, the spectrum after reverse bias temperature (BT) annealing at 450 K for 30 min is also shown.

245

capacitance value measured at 0 V as mentioned earlier.   Thus, the post-annealing partially recovers the carrier concentration uniformly.

Figure 4 shows the DLTS spectra of the control, RIE70 and RIE100A samples.   In the RIE100A sample, the spectrum after reverse bias (-1.5 V) temperature (BT) annealing at 450 K for 30 min is also shown.   In the control sample, two electron traps were observed.   From measurements of filling pulse width dependence from 1 ms to 50 s, the trap observed around 200 K is identified as a DX center which is usually observed in $Al_xGa_{1-x}As$ (x>0.3) and highly Si-doped $Al_xGa_{1-x}As$(x<0.2).[7] The origin of this trap is reported as Si donor bond breaking and a change in the atomic configuration. It has been reported that the reactivation of Si-donor and DX center concentrations behave similarly in hydrogenated AlGaAs by heat treatments.[8]   The electron trap observed around 310 K, labeled as E1, has a thermal activation energy of 0.52 eV.   The E1 trap corresponds to the ME4 trap which has been observed in MBE grown $n-Al_{0.2}Ga_{0.8}As$ samples.[9,10]

No significant change was observed in the RIE70 sample.   However, the RIE100 sample could not be measured.   These are consistent with the results in Table I and Fig. 3.   After post-annealing, some traps were observed at a temperature range higher than the peak of the DX center in the RIE100A sample.   Precise wave analysis is difficult, because the DLTS peaks of the traps are small and broad.   The thermal activation energies of the E_C and E_D traps are about 0.49 eV and 0.81 eV, respectively.   The trap concentration of the E_C trap is larger than that of E1 trap, although the peak temperature of the E_C trap is similar to that of E_1 trap.   The E_C trap increases with the filling pulse width from 1ms to 10s, while E_1 trap shows no change with that from 1ms to 10s.   These results indicate that the E_C trap was introduced by the RIE process.

The E_B trap increases with the reverse bias temperature annealing (RBTA) at elevated temperatures.   Because all samples experienced heat treatments at 200 °C (473 K) about 2 hours after RIE in device fabrication processes in this study, this increase of the E_B trap is due to the bias temperature (BT) annealing effect.   It seems that the RBTA increases the defect density in the detection region by drift motions of defect origins such as point defects or impurities induced by the RIE process.

It should be noted that the DLTS signal around 250 K decreases, although the DLTS signal of the DX center is similar and that of the E_B trap increases after the RBTA.   This suggests that there exists a negative DLTS peak around 250 K.   A calculated fitting on the observed DLTS spectrum after RBTA needs a minority-carrier-trap-like DLTS signal.   In Fig. 4, we labeled the negative trap as E_A. The BT annealing effect increases the E_A and E_B traps.   The estimated thermal activation
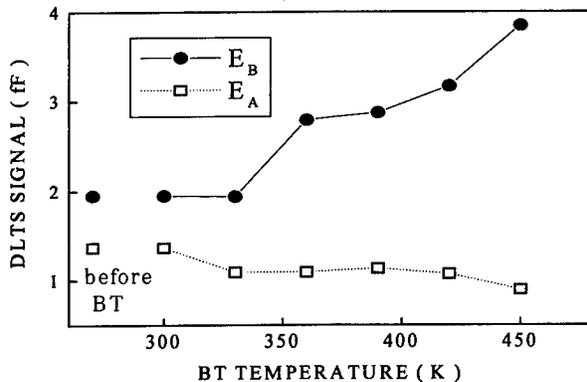

Fig.5   DLTS peak height change with isochronal reverse bias temperature annealing (-1.5 V, 30 min) from 300 K to 450 K.   The values before the BT treatments are also shown.
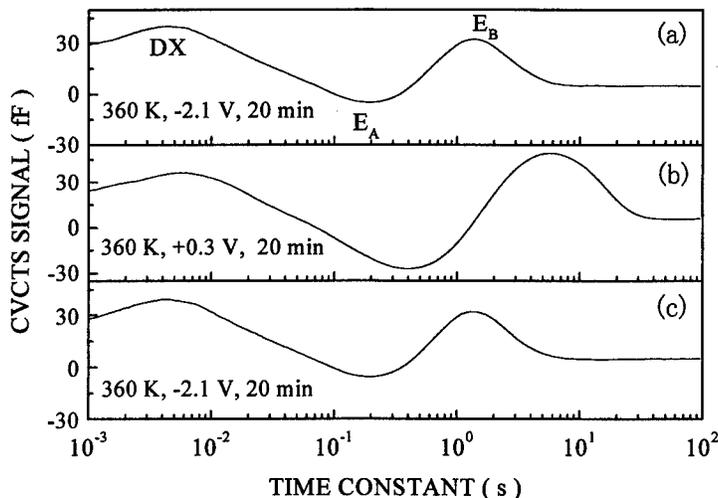
Fig.6 Isothermal CVCTS spectra of an RIE100A sample measured at 220 K. Reverse bias annealing (RBTA) and forward bias annealing (FBTA) were carried out at 360 K.

energies of the E_A and E_B traps are about 0.43 eV and 0.40 eV, respectively.

Figure 5 shows the change of the DLTS peak heights of the E_A and E_B traps by isochronal RBTA (-1.5 V, 30 min) from 300 K to 450 K. The values before the BT treatments are also shown. RBTA above 330 K increases the E_B peak height, while the peak E_A slightly decreases. The observed E_c and E_D traps show no significant change of the peak heights. The amount of the increased E_B peak height is larger than that of the decreased E_A peak height. The relationship between E_A and E_B peaks is discussed later.

Wada et al. have reported that RBTA at 150 °C changes the carrier depth profiles in Ar plasma irradiated GaAs samples.[1] They observed the charge depth profiles that exceed that of the Si donors themselves near the surface after the RBTA. However, in our study, when the DLTS peak height change was observed, no significant change of carrier concentration depth profiles was observed. It seems that the plasma effect depends on plasma species.

Figure 6 shows the isothermal constant voltage capacitance transient spectroscopy (CVCTS) spectra of an RIE100A sample measured at 220 K. Using isothermal CVCTS method enabled us to resolve the spectra of the DX, E_A and E_B traps, which overlap each other in the DLTS spectrum as shown in Fig. 4. Firstly, reverse bias (-2.1 V) temperature annealing (RBTA) at 360 K for 20 min was carried out, and subsequently cooled down to 220 K with application of the reverse bias. After an isothermal CVCTS measurement [Fig. 6 (a)], the sample was raised up to 360K, and forward bias (+0.3 V) temperature annealing (FBTA) was performed for 120 min. Then, it was cooled down to 220 K with forward bias applying, and an isothermal CVCTS measurement was carried out [Fig. 6 (b)]. The peak heights of the E_A and E_B traps increase through the FBTA with an increase of the carrier emission time constants, while those of the DX trap were almost unchanged. The E_A peak clearly shows negative spectrum after FBTA in isothermal CVCTS measurements, although no clear negative peak was detected for overlapping of the spectra in temperature scan DLTS measurements. Again, the sample was raised up and RBTA was performed, isothermal CVCTS spectrum at 220 K [Fig. 6 (c)] was returned to the first CVCTS spectrum with RBTA. Thus, the change of the E_A and E_B

peaks with bias temperature annealing is reversible. This suggests that the reaction of the traps is caused by the charge dependence of the defects at elevated temperatures. When a positive peak height of the E_B trap increases through FBTA, a negative peak height of the E_A trap also increases. The total amounts of the E_A and E_B traps increase through FBTA and decrease through RBTA. This result is consistent with that of the DLTS measurements as shown in Fig. 4. It seems that the E_A and E_B traps transform into other defects. The bi-stable defects corresponding to the E_A and E_B peaks are un-detectable with the DLTS and isothermal CVCTS measurements. It seems that they are transformed to electrical inactive defects or hole traps. However, simultaneous peak height changes suggest that the E_A and E_B traps are complex defects which contain the same defects.

Only majority carrier traps are generally detected with Schottky contacts. They show a positive peak in the measurement system used in this study. It has been reported that a negative peak was observed in Schottky contacts due to the AlGaAs/GaAs hetero-interface.[11,12] However, in the model, all positive traps should accompany a negative peak, whose peak height is lower than that of the positive peak and whose time constant is half of that of the positive peak. In this study, no negative peak was observed at half of the time constant of the DX center. Thus, we can rule out the response of a depletion layer at the hetero-interface.

There may exist a possibility that n-AlGaAs/i-AlGaAs interface affects the CVCTS spectra. We believe that the negative peak is not due to the sample structure, because the negative peak was observed in the region shallower than 60 nm from the surface.

The origin of the negative peak seems to be related to a defect reaction, because its peak height and time constant change with the bias condition at elevated temperatures and only one negative peak was observed. No significant peak height change of the E_A and E_B traps were observed through an RBTA experiment for 4 hr at 220 K. This result suggests that defect reactions of bi-stable states are related to the charge dependent stability and thermally active process.

4. SUMMARY

No significant change was observed in the Si-doped $Al_{0.2}Ga_{0.8}As$ layers through the CF_4 reactive ion etching (RIE) process for 70 s in this study. The RIE for 100 s decreased the capacitance drastically. Post-annealing at 360 °C for 20 s partially recovers the decreased carrier concentration. In the post-annealed RIE 100 s samples, some traps were additionally observed. Two of the traps show bi-stability.

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APPLICATION OF SiO$_2$ FILMS DEPOSITED BY TICS/O$_2$ PECVD TO InSb MISFET

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ABSTRACT

We have fabricated n-channel InSb MISFETs using SiO$_2$ films as gate insulators. The insulator was deposited by PECVD using tetra-isocyanate-silane (TICS) and oxygen (O$_2$) as source gases. Threshold voltage and carrier mobility at 77K were 0.5V and 4200cm^2/Vs, respectively.

INTRODUCTION

High mobility semiconductors are important materials for high speed transistors. Insulating materials are also important for fabricating practical devices because of insulation and passivation. There are many compound semiconductors which have much higher mobility than silicon, and usually such materials require the low temperature processes. It is well known that silicon dioxide is a superior insulator. PECVD SiO$_2$ films can be formed at relatively low temperature and their insulating performance better than films deposited by the other low temperature CVD methods. However, the performance is not as good as thermally grown SiO$_2$. One of the reasons is the hydroxyl bonds and water in the film. A silicon source gas in the conventional CVD process is silane (SiH$_4$) or tetraethyl-orthosilicate (TEOS). Because these source gases include hydrogen atoms, water molecules or hydroxyl bonds will be generated during deposition. The amount of hydroxyl bonds and water increase as the deposition temperature decrease. The deterioration of electrical characteristics becomes serious at low temperature deposition. The best way to eliminate the problem is the use of hydrogen free source gases. We had already proposed the use of tetra-isocyanate-silane[1] (Si(NCO)$_4$:TICS) as the new silicon source gas[2]. We have investigated the characteristics of SiO$_2$ films deposited by PECVD using TICS and O$_2$ at a temperature between 15°C and 300°C[3]. In this report, we have applied the films to indium antimonide (InSb) which has the maximum electron mobility among III-V compound semiconductors and fabricated n-channel InSb MISFETs.

EXPERIMENT

The experimental apparatus was a parallel-plate electrode RF plasma CVD with a working frequency of 13.56MHz as shown in Fig.1. It had two gas lines for TICS and O$_2$. To obtain a sufficient TICS vapor pressure, as well as to maintain a stable gas flow, the TICS cylinder and its gas line were heated up at 110°C. Silicon dioxide films were deposited on Si substrates and un-doped InSb substrates under various deposition condition. Film thickness and refractive index were measured by an ellipsometer. Chemical structure and composition of the films were investigated by Fourier transform infrared (FTIR) spectroscopy. I-V characteristics were measured at a room temperature and C-V characteristics of InSb MIS diodes were measured at
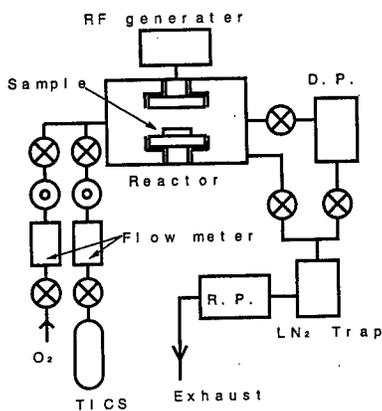
Fig.1 SiO$_2$ PECVD apparatus.
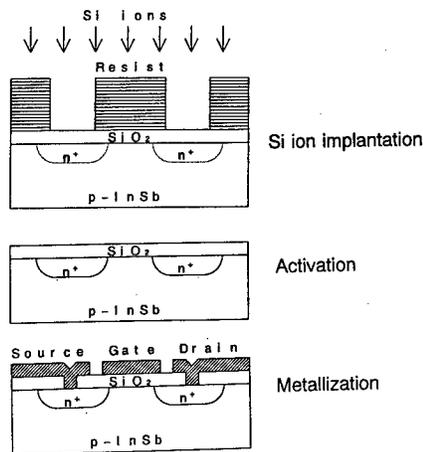
Fig.2 Process steps of InSb MISFET.

77K.

MISFETs were fabricated on Ge doped p-type (111)B InSb wafers. After conventional cleaning, SiO$_2$ film was deposited on a InSb wafer. Using photo-resist as a mask, Si ions were implanted at ion dose of 5×10^{14}cm^{-2} and acceleration voltage of 120kV in order to form source and drain n$^+$ regions. After stripping resist and SiO$_2$ film, SiO$_2$ film was deposited again for a cap layer. The capped samples were annealed in nitrogen at 250°C for 40 minutes for activation. After removing a cap layer, 110nm-thick SiO$_2$ film was deposited at 75°C as gate insulator. Contact hole opening and metallization process were performed. Device channel length and channel width of MISFET were 100μm and 200μm, respectively. Transistor characteristics were measured at 77K.

RESULTS

Figure 3 shows the FTIR spectra of PECVD SiO$_2$ films deposited at various temperatures. The film deposited at 300°C showed no signal which is relating to H$_2$O and -OH. However, low temperature samples were containing water and hydroxyl bonds. This is explained by that deposited film were so porous as to adsorb moisture after unloading. This was recovered by diluting TICS with O$_2$. When TICS was diluted to 5%, water related signals were well suppressed even at a deposition temperature of 100°C as shown in Fig.4.

Figure 5 shows I-V characteristics of SiO$_2$ films deposited on Si substrates at 100°C. As we reduced the TICS content of source gas, lower leakage currents were observed. This seems to be caused by reduction of water content of films. Resistivity of $10^{15}\Omega$cm were observed in films deposited at 100°C.

We applied low temperature films to InSb MIS diodes. Leakage current through SiO$_2$ films on InSb substrate was the same order as that on Si substrate. In order to
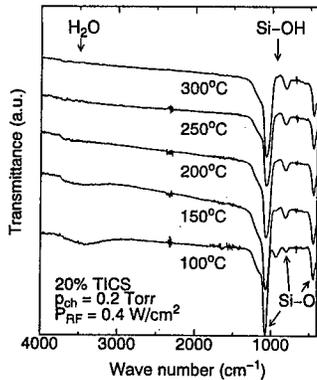
Fig.3 FTIR spectra of SiO_2 films deposited at various temperature.
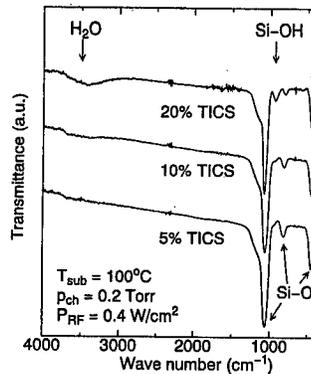
Fig.4 FTIR spectra of SiO_2 films deposited at various gas ratio $TICS/(TICS+O_2)$.
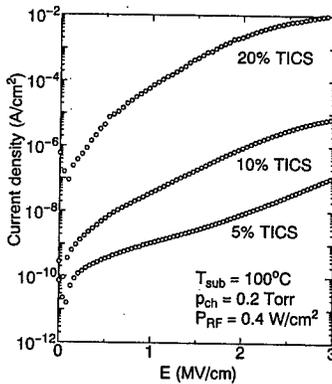
Fig.5 I-V characteristics of SiO_2 films deposited on Si substrates.
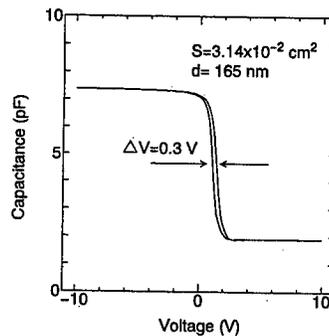

Fig.6 C-V characteristics of InSb MIS diode.

get good C-V characteristics of InSb MIS diode, we needed to reduce deposition temperature down to 75°C. Figure 6 shows best C-V characteristics at 77K. Hysteresis voltage width was 0.3V, interface trap density was $10^{12} cm^{-2} eV^{-1}$. Dielectric constants of the films were 4.4. We examined the dependence of C-V characteristics on post annealing temperature as shown in Fig.7. If annealing temperature was higher than 150°C, C-V curves shifted toward to negative voltages, and became gradual curves. This shows that process temperatures of MISFET should not exceed 150°C after gate insulator formation.

For formation of drain and source of MISFET, we employed Si ion implantation. We had confirmed activation process temperature. As shown in Fig.8, rectifying ratio

251
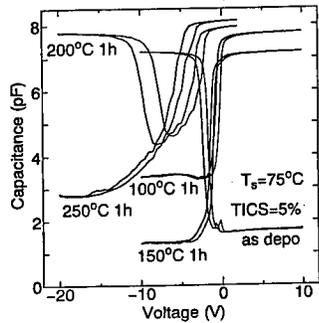
Fig.7 Dependence of C-V characteristics on post annealing temperature.
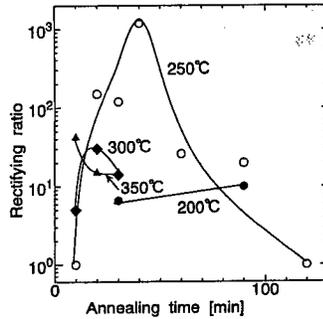
Fig.8 Dependence of rectifying ratio of n^+-p InSb diode on activation process.
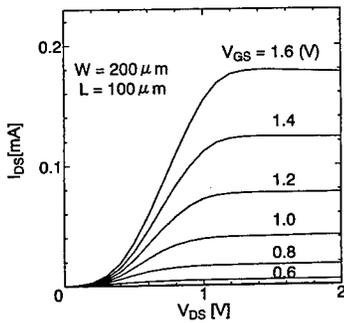
Fig.9 I_{DS}-V_{DS} characteristics of InSb MISFET.

of 10^3 was obtained after 250°C annealing in nitrogen for 40 minutes. As MIS structure is not stable as described above, we formed drain and source before gate. Figure 9 shows the I-V characteristics of InSb MISFET that we fabricated. Good current saturation characteristics were obtained. Threshold voltage was 0.5V. Evaluated electron mobility in a channel was 4200cm^2/Vs. At low drain voltage region, super linear characteristics was observed. This means that large parasitic resistance was exist. We believe that optimization of metallization process will eliminate parasitic resistance and improve mobility.

CONCLUSIONS

We have demonstrated high performance SiO$_2$ by PECVD using TICS and oxygen at a low temperature. Resistivity was $10^{15}\Omega$cm for 100°C deposition. We have applied SiO$_2$ film deposited at 75°C to InSb MIS diode. C-V characteristics of the MIS diode showed that the interface can be controlled by gate voltage between

accumulation and inversion. Interface trap density was $10^{12}cm^{-2}eV^{-1}$. We have fabricated n-channel MISFET using this MIS structure as gate. Electron mobility was $4200cm^2/Vs$, and threshold voltage was 0.5V. I-V characteristics showed that large parasitic resistance was exist. This will be improved by optimization of metallizaion process.

ACKNOWLEDGMENTS

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Part VI

Processing Issues in SiGe/Si and SiC/Si Heterostructures

Si/SiGe and III-V Integrated Circuit Technology for Next Generation High-Speed Systems: Comparisons and Tradeoffs

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ABSTRACT

This paper will summarize the technology tradeoffs that are involved in the implementation of high-speed integrated circuit technology for communications applications. The advantages of Si/SiGe and III-V technology with respect to CMOS and Si bipolar technologies are discussed.

INTRODUCTION

The explosion of interest in integrated circuit technology for communications applications in the last decade has been driven by the expansion of the market for untethered communications in a variety of forms - from pagers and cordless telephones to analog and digital cellular telephones, DBS, and PCS. In addition, the widespread adoption of fiber-optic communications has created a need for high-frequency electronic repeater and switching circuits, whose bandwidth increases on an almost yearly basis. The high-frequency nature of these products typically requires that they contain a mixture of digital, rf and analog functions, operating at the highest possible performance levels.

The consumer/commercial aspect of this market puts a premium on low-cost/low-power/high-volume implementations of functions that were formerly implemented using bulky, expensive, and power-hungry hybrid components. Drawing an analogy to digital integrated circuit technology, it would appear that the optimum technology choice for these applications might follow the same path that purely digital IC implementations followed - towards CMOS - with costs dropping dramatically as the level of integration increases.

However, the technical requirements for the function of a typical high-frequency wireless or fiber-optic device are considerably more multi-dimensional than that of a digital integrated circuit - where power dissipation, speed, and yield are the major performance metrics, and where performance inevitably improves with increasing lithographic sophistication and higher levels of integration. These devices have to contend with issues of noise - both broadband and near carrier - linearity, gain, and efficiency. As a result, the optimum technology choices for high-frequency systems are still evolving CMOS, Si/SiGe, GaAs, InP, SiC and GaN are all vying for differing pieces of this evolving market.

This paper will review the current status of the technologies that are being developed for next generation communications systems, with particular attention paid to those technologies that will have a major impact on next generation systems.

TECHNOLOGY COMPARISONS FOR HIGH-FREQUENCY APPLICATIONS

The optimum technology choice for communications applications is complicated by issues of performance, wafer cost, level of integration, and time-to market, and the temptation to perform "apples-to-oranges" comparisons is nearly overwhelming. The performance issues are very multi-dimensional.

Until recently, GaAs technology was expected to dominate the RF integrated circuit arena, because of its intrinsically higher speed, due to its improved electron mobility and saturated drift velocity. Tables I and II summarize the relative differences of the intrinsic materials properties of silicon, GaAs, InP, and GaN, with particular attention to differences that are key for high-frequency applications.

Properties	Silicon /SiGe	InP /GaInAs	GaN /AlGaN	GaAs /AlGaAs
Breakdown Field (V/cm)	$\approx 3\times 10^5$	$\approx 5\times 10^5$	$\approx 3\times 10^6$	$\approx 4\times 10^5$
RT Electron Mobility (cm^2/V-sec)	≈ 1500	$\approx 10{,}000$	≈ 1500	≈ 8500
Thermal Conductivity at 300°K (watt/cm-°C)	≈ 1.45	≈ 0.7	≈ 1.3	≈ 0.45
Saturated Electron Drift Velocity(@10^5V/cm)	$\approx 10^7$	$\approx 10^7$	$\approx 3\times 10^7$	$\approx 10^7$
1/f Noise Corner Frequency (Hz) BJT/HBT MOSFET/MESFET	 10-10^3 10^3-10^5	 10-10^3 10^6-10^8		 10^4-10^6 10^6-10^8
Substrate Resistivity (typical) (Ω-cm)	$\approx 10^3$	$\approx 10^8$	$\approx 10^8$	$\approx 10^8$

Table I. Comparison of fundamental materials properties of Si/SiGe, InP-based, GaAs-based, and GaN semiconductor technology.

Based on the materials properties alone (low-field electron mobility and breakdown voltage in particular), III-V technology is clearly superior for high-frequency device applications. This is confirmed by the fact that the *highest* performance components of microwave receivers - such as a 0.6 dB noise-figure Ku-Band DBS down-converter LNA's - are inevitably implemented in GaAs MESFET or PHEMT technology [1]; the highest performance transistor mmW devices are invariably InP-based [2]. The highest efficiency commercial cellular power amplifiers are implemented in GaAs technology. However, as Fig. 1 demonstrates, the transistor unity current-gain frequency (f_T) of silicon technology has recently reached the level where it is comparable with GaAs for applications in the 1-10 GHz frequency range [3]. At very short gate lengths and base widths (roughly below 0.2 μm), the saturated drift velocity of the electrons dominates the f_T, and transistors fabricated in silicon and III-V technologies have comparable cutoff frequencies, albeit at higher voltage levels with the silicon-based devices [4].

Material	Eg (eV)	ε_r	E_c (V/cm)
Si	1.12	11.9	3×10^5
GaAs	1.43	12.5	4×10^5
InP	1.34	12.4	4.5×10^5
3C-SiC	2.3	9.7	1.8×10^6
4H-SiC	3.2	10.0	3.5×10^6
6H-SiC	2.86	10.0	3.8×10^6
Diamond	5.6	5.5	5×10^6
GaN	3.4	9.5	2×10^6

Table II. Material Properties for Several Semiconductors.

Despite their roughly comparable production f_T's, GaAs (or InP)-based technologies will continue to maintain a small but significant *absolute* performance advantage compared to silicon due to the higher low-field mobility, which has a major impact on device noise figure [5]. The ohmic resistances leading to the device, which play a major part in determining noise-figure, are dominated by low-field electron mobility, and the metal-gate structure of a typical GaAs MESFET or PHEMT reduces the series gate resistance compared to that of a silicided MOSFET gate. At the same time, the wider bandgap of III-V materials makes them intrinsically higher performing devices for power amplifier applications, due to fundamental Johnson's law speed/breakdown tradeoffs.

However, recent results have demonstrated that a "T-gate" aluminum structure in MOS technology can realize gate resistance values comparable to those of GaAs MESFETs or PHEMTs [6]. This improvement in performance means that silicon technology has comparable - but not equal - performance capabilities to GaAs technology at communications frequencies in the 1-5 GHz range. However, the peak cutoff frequency of the transistor does not paint a complete picture of performance, since the high-frequency performance of the silicon devices is generally achieved at higher power dissipation levels than III-V devices. On the other hand, the higher levels of integration possible with silicon technology may reduce the need for routing high-frequency signals on- and off-chip, compared with GaAs technology, reducing overall *system* power dissipation.
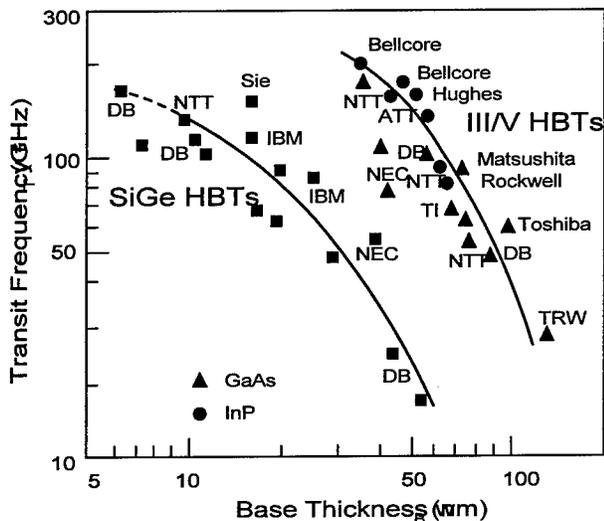
Figure 1. Comparison of HBT f_T as a function of base width for Si/SiGe and III-V technologies [7].

POWER AMPLIFIERS

Power amplifiers form the most challenging of all technological hurdles for a wireless communications system. The circuit must simultaneously satisfy requirements of linearity, gain, output power, and power-added efficiency. In addition, the trend toward lowered power supply voltages for hand-held devices (from 5V to 3V and even lower), has made it difficult to maintain the required output power and efficiency due to impedance matching limitations. Ideally, the power-added efficiency of the amplifier should not degrade significantly as the output power varies from near zero to its maximum value. In addition, there are many "tiers" of applications, running from high-end base station applications - with high output power and linearity, but modest efficiency requirements, - to hand-held portable power amplifiers - with high linearity and efficiency requirements, but relatively modest power requirements.

One of the major dilemmas in wireless systems is that power amplifiers are typically operated in a "backed-off" mode relative to their peak power and power-added efficiency points in order to meet the linearity requirements of the system. The degree of back-off varies depending on the modulation scheme employed - 0 dB for GMSK (GSM and DECT) , 7 dB for Pi/4DQPSK (IS-54 and PHS) , 10 dB for QPSK (IS-95), and 12 dB for 16QAM are typical. In digital communications systems, the linearity of the output power amplifier - which determines the required back-off - is usually specified as an Adjacent Channel Power Ratio (ACPR) in dBc, rather than the more traditional IIP3/IIP5 used in analog communications applications. ACPR is a measure of the spectral "spill-over" due to amplifier non-linearities into an adjacent frequency band by a digitally modulated waveform.

Power amplifiers are typically operated in the Class-AB mode for most RFIC applications in an attempt to achieve a compromise between linearity and power-added efficiency. In this case, the factors of key importance for amplifier performance are transistor f_{MAX} (for high power gain), linearity (for lowest possible adjacent channel interference) and breakdown voltage (BVCEO for bipolar devices or BVGDS for FETs). As it turns out, the breakdown voltage has become less critical for handsets in recent years, due to the reduction of operating voltages in most handheld units. The power-added efficiency of a power amplifier is dependent on the drain/collector efficiency and the power gain of the device. The collector/drain efficiency typically varies from 40 to 75%, which sets an upper limit on power-added efficiency. The finite gain of the device will lower it from that point; since gain is so critical to achieving the best performance, most high-performance power amplifiers in the 2 GHz frequency range have been implemented in GaAs technology to achieve the highest possible power-added efficiency.

At lower frequencies, silicon MOS devices are often employed for power amplifiers because of their low-cost and robust operation, despite their poorer performance compared to GaAs technology. Fig. 2 summarizes a recent comparison of monolithic power amplifier performance for PHS applications at 1900 MHz, where the adjacent channel leakage specification of -55 dBc is specified at 600kHz from the carrier center [8]. The best results are achieved with 0.25μm GaAs PHEMT technology, probably due to its higher f_T and f_{MAX} (50 and 90 GHz respectively) compared with GaAs MESFET technology. The resulting differences are not dramatic however, and the higher current and power gain of the PHEMT device at these frequencies may only translate into modest improvements in power added efficiency at a given output power.
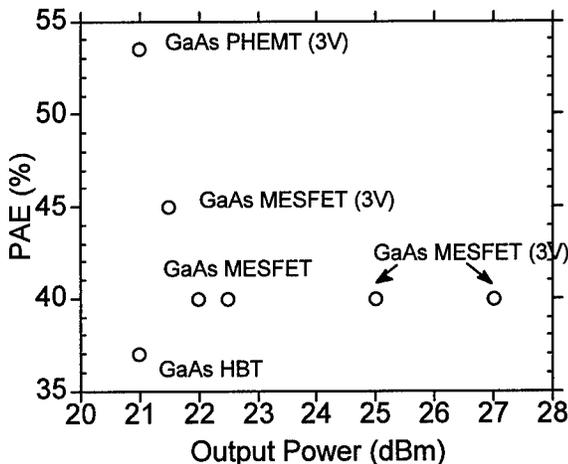

Figure 2. PHS/PACS power amplifier performance for ACP < -55 dBc at 600 kHz offset The best performance is obtained with a GaAs PHEMT.

As with low-noise amplifiers, despite their high f_T, the peak performance of silicon-based devices will lag that of GaAs or InP devices for the foreseeable future, even at lower power supply voltages. The well-known Johnson limit [9] for speed vs. breakdown voltage in semiconductor devices results in significantly higher gain for the GaAs and InP devices, even at the lower operating voltage, due to the higher electron mobility. The higher gain translates into improved power-added efficiency, and potentially linearity, at higher-frequencies of operation. Therefore, the *best* performance is usually obtained with III-V power devices, and this will remain true for the foreseeable future. Care must be taken in the design of power amplifiers in low-voltage technologies, since the peak drain/collector voltage can approach four times the supply voltage under extreme VSWR conditions [10].

SiC- and GaN-based power devices have made dramatic improvements recently in output power *densities* at microwave frequencies, with potential application in the future to high power applications like cellular base stations [11], [12]. The advantage in this case - especially with GaN - is that the high electron mobility, drift velocity and breakdown voltage will translate into high efficiency *and* high output power from a single power cell. These intrinsic advantages are clear from the summaries presented in Tables I and II. This technology is currently limited by material and thermal considerations, which make its absolute performance - power-added efficiency and output power - relatively modest in comparison to existing GaAs, or even silicon, results. Continued improvements in material and processing technology are required to make the technology competitive for microwave applications [13].

Si/SiGe device technology has also moved into the low-voltage power amplifier arena recently, with a number of promising results. Greater than 70% power-added efficiency was obtained at 1.8 GHz with a 33 mW output power, and greater than 60% PAE was observed with over 100 mW output power at 0.9 GHz using a modified "high-breakdown" profile [14]. Although not intrinsically well suited to power applications due to its low breakdown voltage, the high f_T and f_{MAX} of these devices will result in outstanding performance at low voltages and low output powers.

In the III-V area, the demand for low battery voltages favors InP over GaAs, especially with HBT's. The AlInAs/GaInAs/InP HBT has a natural advantage of a base bandgap of 0.75 eV compared to 1.42 eV for GaAs HBTs. InP HBTs also have superior transport characteristics compared to GaAs HBTs, allowing for improved performance at reduced collector bias and current density. A recent result demonstrated a peak PAE of 68% at an output power of 18 dBm, with over 20 dB gain at 1.9 GHz, operating from a 2.7V supply [15].

LOW-NOISE APPLICATIONS

Low-Noise Amplifiers (LNAs) are one of the key performance bottlenecks in a communications system. They are required to contend with a variety of signals coming from the antenna - often of larger amplitude than the desired signal - and so both low-noise and high linearity are simultaneously required. Two measures of these requirements are the amplifier noise-figure, which determines the Minimum Detectable Signal (MDS), and the third-order input intercept point (IIP3), which, together with noise-figure, determines the Spur Free Dynamic Range (SFDR). The SFDR determines the difference between the MDS and the maximum input signal prior to significant distortion [16]. In addition, high-gain and low dc power consumption are other requirements of an LNA.

The noise figure of the amplifier will be improved by employing a technology that operates with as high an f_T and as low a base or gate resistance at a given current as possible. As

a result, technology scaling will have a significant impact on low-noise amplifier performance, but care must be taken to minimize the access resistances ($r_{b/g}$) to the device at the same time the transistor cut-off frequency is raised. It is this later $r_{b/g}$ factor that provides the performance advantage of GaAs-based devices.

Fig. 3 plots amplifier Gain/DC Power Dissipation (in dB/mW) as a function of Noise-Figure (in dB) for a variety of reported low-noise amplifiers in silicon and GaAs technology at 2 GHz. Most of the recently reported LNA results, fabricated in Si CMOS [17], or Si bipolar technologies [18, 19] fall along a Gain/(Pdc•NF) line of approximately 0.4 (1/mW). By comparison, a recent SiGe HBT result [20] demonstrated a fully integrated LNA with 0.95 dB Noise-Figure, 2 mW of power dissipation and 10.5 dB of gain at 2.4 GHz, for a figure of merit of approximately 5.5 (1/mW). The best reported GaAs LNA's have figures of merit of approximately 3.0 (1/mW) [21, 22, 23]. These results demonstrate the potential performance advantage of advanced GaAs or SiGe technologies at these frequencies, if dc power dissipation is a major consideration.
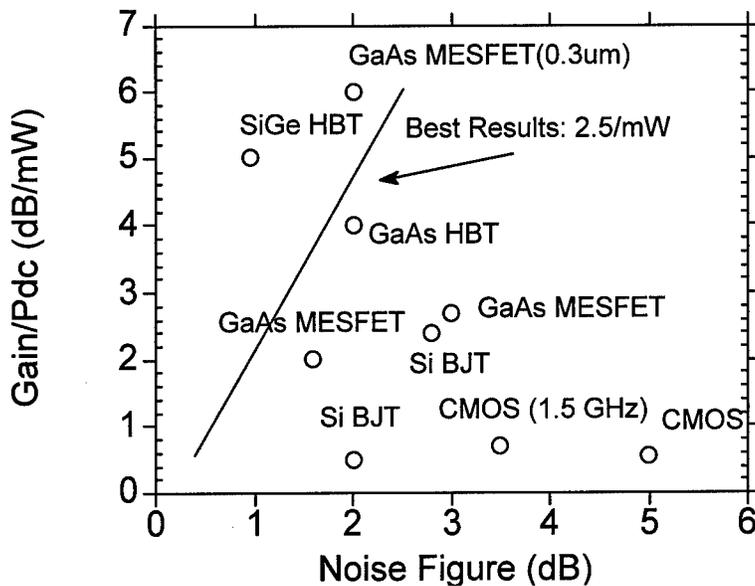
Figure 3. Gain to dc power ratio plotted versus Noise-Figure for state-of-the-art 2 GHz LNA's. The best results have a figure-of-merit of approximately 2.5/mW.

Due to the extreme dynamic range considerations of the low-noise front-end, linearity is an equally important figure of merit for LNAs. In this case, a linearity figure-of-merit is the ratio of the Input Third Order Intercept Point (IP3) to the DC power dissipation. Field-effect transistors (MOSFETs as well as GaAs MESFETs and PHEMTs) generally exhibit improved third order intermodulation distortion compared with bipolar devices, due to their near square-law current vs. voltage behavior. On the other hand, bipolar transistor amplifiers have recently demonstrated outstanding linearity performance as well, apparently due to the partial cancellation of the resistive and capacitive non-linearities in the base-emitter junction at certain frequencies [24].

HIGH FREQUENCY DIGITAL CIRCUITS AND DATA CONVERTERS

The use of compound semiconductor device technology for high density digital and/or data converter applications is complicated by the relatively low yield of these technologies. In these cases, where high yield and high levels of integration are key, the outstanding high-frequency performance of Si/SiGe HBT technology and its silicon VLSI pedigree is key. In many applications, its speed performance advantage can be "traded-off" in a very satisfactory way for dramatically reduced power dissipation. It is at these low power levels where Si/SiGe HBT technology has a distinct advantage compared to Si BJT or CMOS technology. Fig. 4 plots the dramatic improvement achieved recently in Si bipolar performance due to the introduction of epi-base Si/SiGe technology.
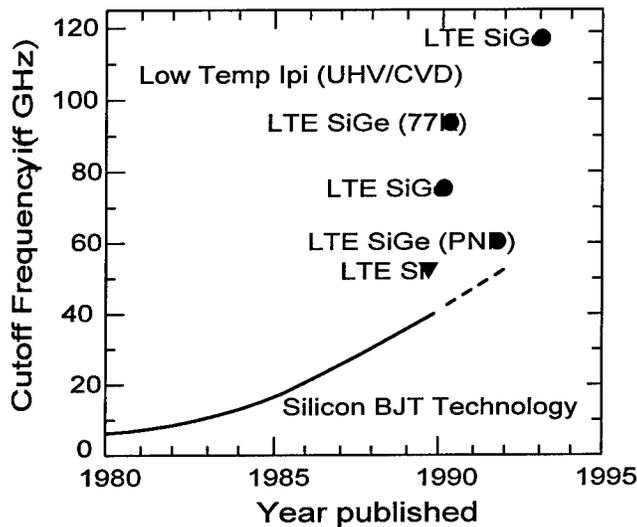
Figure 4. f_T trend chart for silicon-based bipolar transistor performance over the past 15 years [19].

A good example of this improvements can be seen from the transistor data presented in Fig. 5, comparing transistor f_T and as a function of collector current for epi-base SiGe HBTs and

Si BJTs of *comparable base resistance* (approximately 12KΩ/□) [25]. In this case, the peak f_T for the Si BJT and SiGe HBT are 38 and 50 GHz respectively. The epi-base SiGe HBT achieves higher f_T and f_{max} values than the epi-base Si BJT over its entire range of operation. In addition, for a given required f_T or f_{max}, the SiGe HBT requires roughly one-third the collector current of an "equivalent" Si BJT for equivalently sized devices, dramatically lowering the power requirements in those circuits that are required to operate at very high frequencies. Recent research results have demonstrated outstanding performance for Si/SiGe HBT circuits operating at frequencies above 10 GHz. They include frequency dividers operating to 28 GHz [26], Gilbert mixers operating to 12 GHz [27], power amplifiers with over 25 dBM of output power at 1.9 GHz [28], VCOs with, -103 dBc/Hz of phase noise at 7.5 GHz. [29].
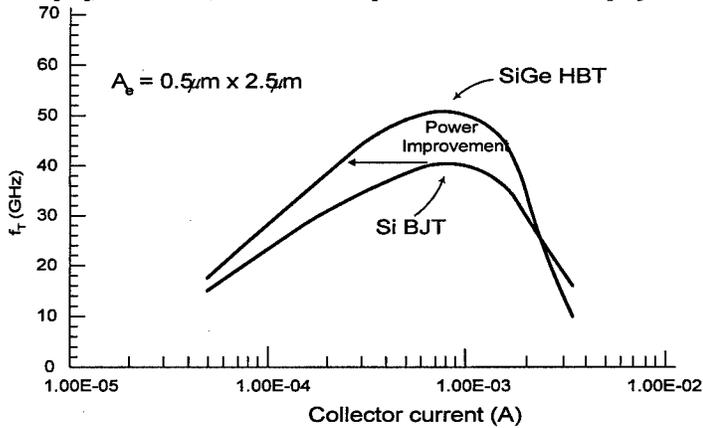
Figure 5. Comparison of epi-base Si/SiGe HBT and Si BJT with comparable base resistivity and geometry (a) f_T vs. collector current [25].

At the highest performance levels, the superior performance of InP-based HBTs has allowed flip-flops to operate at millimeterwave frequencies [30]. In these cases, the highest possible f_T and f_{max} is crucial for high-frequency operation.

CONCLUSIONS

The use of compound semiconductor technology promises dramatic improvements in existing applications in the coming years. Si/SiGe technology will allow high-performance *and* high levels of integration to be achieved, providing for the next performance "jump" in silicon technology. The use of GaN-based power amplifiers promises improved performance at the highest power levels, but improvements are required in materials and processing technology for its performance to achieve a competitive level to GaAs. Low-voltage power amplifiers can be implemented in Si/SiGe, GaAs, or InP technologies. The highest performance circuits will be implemented in InP-based technology, but only at extremely modest levels of integration.

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STUDY OF $Si_{1-x}Ge_x$ / SI / $SI_{1-x}GE_x$ HETEROSTRUCTURES WITH ABRUPT INTERFACES FOR ULTRAHIGH MOBILITY FETS

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ABSTRACT

We grew $Si_{1-x}Ge_x$ / Si / $Si_{1-x}Ge_x$ heterostructures with abrupt interfaces for a high-speed device application. In order to eliminate the interface and the impurity scatterings, a two-step solid-phase epitaxy (SPE) was developed newly. This SPE can obtain an abrupt interface between the upper $Si_{1-x}Ge_x$ and the Si-channel layers as well as a sharp Sb-doping profile in the upper $Si_{1-x}Ge_x$ layer. Single-step SPE growth of the $Si_{1-x}Ge_x$ layer including the Sb-doped layer caused solid-state diffusion of Sb and made the doping-profile difficult to control. A two-step SPE, (that is, two independent SPE processes forming the $Si_{1-x}Ge_x$ and the Sb-doped layers), obtained a sharp Sb depth profile and high electrical activation in the Sb-doped $Si_{1-x}Ge_x$ layer. However, the number of modulation-doped carriers in the Si channel layer was small. Calculation of the carrier distribution between the channel and the doped layer suggests that the carrier density in the channel is low when the Sb-doping profile is extremely sharp; thus, precise control of the modulation-doped-carrier density by optimizing the thickness of the Sb-doped layer is crucial for operating modulation-doped field-effect transistors (MODFETs).

INTRODUCTION

$Si_{1-x}Ge_x$ / Si heteroepitaxy is a key technology for introducing high-speed modulation-doped field-effect transistors (MODFETs) into Si-ULSI devices [1-10]. The mobility of a two-dimensional electron gas confined in the Si layer near the $Si_{1-x}Ge_x$ / Si interface should be potentially high. However, the electron mobilities reported so far have not come close to the ideal value. Reducing any scattering factor is important in order to achieve ultrahigh electron mobility. We consider it is especially crucial to eliminate the interface scattering by growing an abrupt heterointerface and to eliminate impurity scattering by controlling the doping profile. We have thus been developing a new method for growing $Si_{1-x}Ge_x$ / Si / $Si_{1-x}Ge_x$ heterostructures that combines molecular-beam epitaxy (MBE) and solid-phase epitaxy (SPE). This method can produce an atomically flat interface between the $Si_{1-x}Ge_x$ and the Si-channel layers and can control the doping-profile properly. As a result of the smooth interface, we obtained an ultrahigh electron mobility of 8×10^5 cm²/Vs at 15 K [10]. But the carrier concentration could not be properly controlled by simple SPE growth of the $Si_{1-x}Ge_x$ layer including the Sb-doped layer. And the two-step SPE process enabled precise control of Sb-doping profile in $Si_{1-x}Ge_x$ by eliminating the diffusion of Sb atoms.

EXPERIMENTAL

A schematic cross-section of the SiGe heterostructure is shown in Fig. 1. In the heterostructure growth, first, the p-Si (100) substrates were cleaned by chemical etching and introduced into an ultrahigh-vacuum chamber equipped with evaporation sources of Si, Ge, and Sb. A $Si_{1-x}Ge_x$ (0≤x≤0.2) compositionally graded buffer layer (2 μm thick) was then grown at 600°C. Next, a Si-channel layer (20 nm thick) was pseudomorphically grown at 400°C above this layer. Sufficient

269

tensile strain was thus applied to the Si-channel layer. Above the channel layer, a $Si_{0.8}Ge_{0.2}$-spacer layer, an Sb-delta-doped layer and a $Si_{0.8}Ge_{0.2}$-cap layer were formed by two types of SPE processes. In the first process, single-step SPE, each layer was deposited below 100°C then crystallized simultaneously by heating to 600°C in approximately 10 minutes. In the second process, two-step SPE, the $Si_{0.8}Ge_{0.2}$ spacer layer was deposited at below 100°C, crystallized by heating to 600°C, then cooled to below 100°C. In the second step, the Sb delta-doped layer and the $Si_{0.8}Ge_{0.2}$ cap layer were deposited at below 100°C then crystallized by heating to 600°C. Lastly, a Si cap layer was grown on the $Si_{0.8}Ge_{0.2}$ cap layer at 600°C.

The strain and microstructures in the heterostructures were characterized by Raman spectroscopy and transmission electron microscopy. And the transport properties were evaluated by Hall-effect measurement. Quantitative depth-profiles of Sb and Ge were measured by secondary-ion mass spectrometry (SIMS) on a Physical Electronics 6600 spectrometer using 2-keV Cs^+ primary ions.

RESULTS AND DISCUSSION

Single-step SPE grown heterostructures with an abrupt interface

We evaluated the strain in the Si-channel layer of samples with various Ge content ($0 \leq x \leq 0.4$) in the buffer layer (at a top region) by measuring the Raman shifts related to the Si-Si vibration. When the Ge content (x) was 0.2 or more, the value of the tensile strain exceeded 0.4%. This value corresponds to the conduction-band discontinuity of 0.08 eV sufficient for electron confinement in the channel at room temperature. So the Ge content was fixed to 0.2 in our experiments.

A cross-sectional transmission-electron-microscope image at the channel region is shown in Fig. 2. A definite contrast at the heterointerface (A) on top of the channel formed by SPE suggests the interface is atomically flat. In contrast, the interface (B) between the channel and the buffer layer formed by MBE is unclear, indicating interface mixing due to the surface segregation of Ge during the MBE growth of the channel layer.
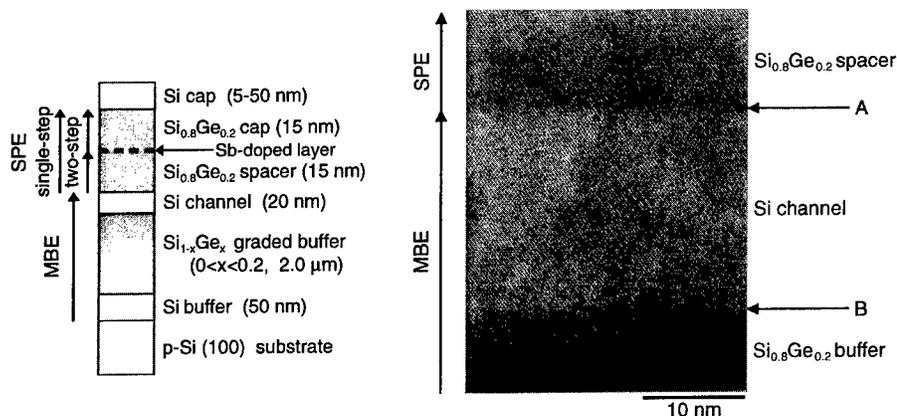
Fig. 1   Schematic cross-section of the SiGe heterostructure.

Fig. 2   Cross-sectional TEM image of the heterostructure at the channel region.

The temperature dependence of electron mobility of our best sample [10] is compared in Fig. 3 with results reported by other groups [1, 5-9]. The electron mobility has a peak of 8×10^5 cm^2/Vs at 15 K, which is the highest value reported to date. However, the mobility below this temperature monotonically decreases, possibly due to ionized impurity scattering. This scattering might be because the carrier density (2×10^9 cm^{-2}) was too low to screen the scattering sufficiently. Another problem in the single-step SPE grown samples was the difficulty in controlling carrier density by changing Sb concentration. To clarify these problems in carrier doping, we measured depth profiles of the Sb dopant concentration.

Sb-doping-profile control by two-step SPE

A SIMS profile obtained from a typical sample grown by single-step SPE is

Fig. 3 Temperature dependences of electron mobility of the heterostructures [1, 5-10].

shown in Fig. 4. There are two peaks in the depth profile of the Sb concentration: one where the Sb is doped (15 nm in depth) and one just above the Si-channel layer (30 nm in depth). These peaks suggest that Sb atoms diffused from the original position during the crystallization of the amorphous $Si_{0.8}Ge_{0.2}$ layer deposited at below 100°C. Because the diffusion coefficient of Sb atoms in the amorphous phase (in the $Si_{0.8}Ge_{0.2}$ layer) is much higher than that in the crystalline phase (in the Si-channel layer), the diffused Sb atoms accumulate on top of the channel layer. This result shows that the Sb profile is difficult to control in single-step SPE growth of these layers.

Fig. 4 SIMS profile of the sample grown by single-step SPE.

Fig. 5 SIMS profile of the sample grown by two-step SPE.

To solve this problem, we developed a two-step SPE process. In this process, Sb atoms are deposited on top of the crystalline phase and are covered by amorphous $Si_{0.8}Ge_{0.2}$ at low temperature, which suppresses the diffusion of the Sb during the crystallization of the covered $Si_{0.8}Ge_{0.2}$. This is because the Sb atoms would be pinned to regular sites on the crystalline phase. The SIMS profile for a sample grown by two-step SPE is shown in Fig. 5. The depth profile of the Sb concentration is sharp and remains at the original position (55 nm in depth). This demonstrates that accurate control of the Sb profile is possible with the two-step SPE technique.

We also investigated the controllability of carrier density by measuring the carrier concentration as a function of the Sb concentration. The sample structure is shown in the inset of Fig. 6. Sb was deposited on the crystalline $Si_{0.8}Ge_{0.2}$ layer, and then a cap layer was formed by SPE. The dependence of the sheet-carrier density on the Sb concentration is shown in Fig. 6. In this figure, the solid line corresponds to the dependence of the carrier density when the doped Sb is fully activated, and the dashed line shows the solubility limit of the delta-doped Sb in Si [11]. The activation coefficient is far lower than unity in the high-concentration region above the 0.01 monolayer (ML). As the Sb concentration decreases, the activation coefficient increases and reaches almost unity at about 0.001 ML. The carrier concentration corresponding to the Sb-concentration range around 0.001 ML is regularly used in the fabrication of MODFETs. Control of impurity concentrations in MODFETs is therefore possible by using the two-step SPE technique.

Evaluation of the modulation-doped-carrier density

We next examined the modulation-doped-carrier density in the channel for a heterostructure grown by the two-step SPE technique. Figure 7 shows the dependence of the carrier density and electron mobility on the gate voltage measured at 290 K on a bar-shaped sample with a gate electrode. The carrier density increases and electron mobility decreases as the gate voltage increases above -10 V. However, if most of the carriers were modulation doped and confined in the Si-channel layer, the electron mobility would have increased with the increasing carrier density. Therefore, most of the carriers must have remained in the Sb-doped $Si_{0.8}Ge_{0.2}$ layer. The decreased
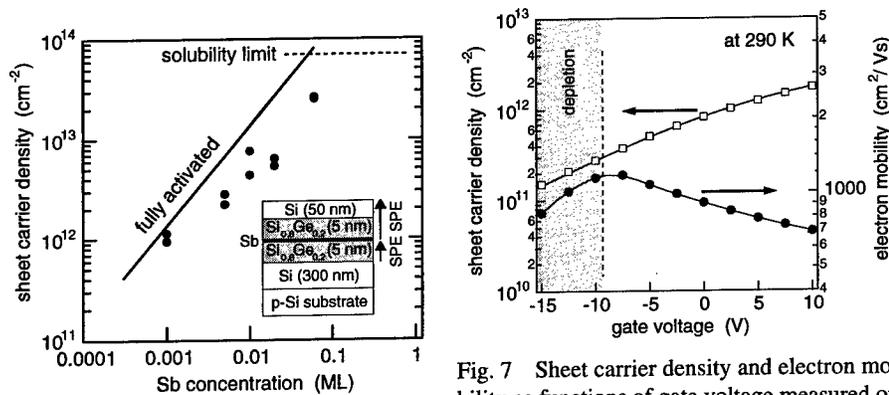

Fig. 6 Dependence of sheet carrier density on Sb concentration. Sample structure is shown in inset.
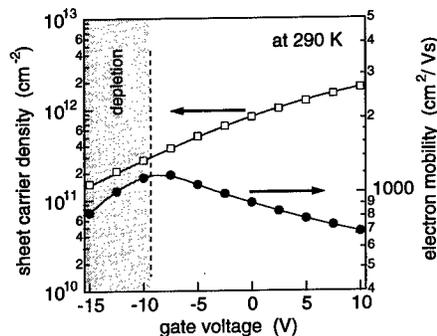
Fig. 7 Sheet carrier density and electron mobility as functions of gate voltage measured on a bar-shaped sample with a gate electrode (modulation-doped heterostructure grown by two-step SPE).

electron mobility under -10 V in Fig. 7 might be due to parallel conduction through the $Si_{1-x}Ge_x$-buffer layer when the carriers in the channel and the doped layer were depleted. Moreover, at 77 K (not shown in the figure), the carrier density was as high as 5×10^{10} cm^{-2} where the carriers in the doped layer were almost depleted at negative gate bias.

These results indicate that even with the considerable doping of Sb impurities in the $Si_{0.8}Ge_{0.2}$ layer, most of the carriers remained in this layer, and very few carriers were modulation doped. Why is the number of modulation carriers so small? To answer that question we simulated the carrier distribution between the channel and the doped layer based on the drift-diffusion model including the Fermi-Dirac distribution [12]. The results indicate that a large drop in the conduction-band-energy level occurs in the doped region when the impurities are doped with a sharp profile and that the number of carriers in the channel is smaller than that in the doped layer. An extremely sharp doping profile, which can be obtained by two-step SPE, might lower modulation-doped-carrier densities. So the two-step SPE technique may therefore have to be modified in order to control the spatial distribution as well as the density of dopants. A study on how the modulation doping behavior is affected by changing the dopant-layer thickness is now under way.

CONCLUSION

We have developed a two-step SPE technique for fabricating high-quality $Si_{1-x}Ge_x$ / Si / $Si_{1-x}Ge_x$ heterostructures. SIMS analyses and Hall-effect measurements revealed that the Sb-doping profile is sharp and the electrical activation is high in the doped layer. With this technique, both the formation of an abrupt interface between $Si_{1-x}Ge_x$ and Si and precise doping control in the $Si_{1-x}Ge_x$ layer are possible for the first time. Our gated Hall measurement and calculation of the carrier distribution between the channel and the doped layer suggest that the carrier density in the channel is low due to the sharpness of the doping profile. However, more precise doping control of the modulation-doped-carrier density by optimizing the spatial distribution of the dopant through a modified two-step SPE process is necessary.

ACKNOWLEDGMENTS

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FERMI-LEVEL EFFECT AND JUNCTION CARRIER CONCENTRATION EFFECT ON BORON DISTRIBUTION IN Ge$_x$Si$_{1-x}$/Si HETEROSTRUCTURES

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ABSTRACT

Dopant segregation mechanism in general involves the chemical effect, the Fermi-level effect, and the effect of the junction carrier concentrations. Satisfactory fits of available B distribution profiles in Ge$_x$Si$_{1-x}$/Si heterostructures have been obtained using such a model, but with the chemical effect not important. The Fermi-level effect determines the difference in the ionized B solubilities in Ge$_x$Si$_{1-x}$ and Si. The singly-positively charged crystal self-interstitials I^+ governs the boron diffusion process. The junction carrier concentration affects the concentration of I^+ and solubility of B in the region and hence controls B diffusion across the heterojunction.

INTRODUCTION

Boron diffusion in Ge$_x$Si$_{1-x}$ epitaxial layers grown on Si substrates has recently drawn an attention [1-4]. Due to the higher electron mobilities, p-type Ge$_x$Si$_{1-x}$ layers are envisaged to constitute excellent base regions in high performance Si-based heterojunction bipolar transistors [5,6]. In these studies [1-4], the epitaxial layers were in situ doped by B during growth, and subsequently annealed to investigate the B diffusion behavior. In the studies of Kuo et al. [1,2] and Fang et al. [3], distribution of B is primarily confined inside the Ge$_x$Si$_{1-x}$ layers. The shape of these B profiles are somewhat different from those expected for B in Si, indicating the existence of a difference in mechanisms governing the distribution of B in the two different cases. In the study of Lever et al. [4], B was introduced to an epitaxial Si layer confined between two Ge$_x$Si$_{1-x}$ layers and the diffused B profiles showed two concentration peaks in these confining Ge$_x$Si$_{1-x}$ layers. These authors have obtained satisfactory fits to their B diffusion profiles [1-4] by postulating the formation of BGe pairs. This assumption seems to be highly speculative, and the fitting schemes involve a number of parameters that are adjusted from case to case.

We have satisfactorily modeled the p-type dopant distribution problem in III-V compound superlattice (SL) structures (see the accompanying article [7]), with the most outstanding feature being that Zn and Be exhibit a prominent segregation behavior, attributed to the dopant solubility difference in the SL layers. The dopant solubility is determined by a chemical effect, a Fermi-level effect, and an effect of the junction carrier concentrations. A similar model should be applicable to also the case of B distribution in the Ge$_x$Si$_{1-x}$/Si heterostructures. Here we report that indeed the available experimental B diffusion profiles [1-4] have been satisfactorily fitted using such a model. In the present model there is no case to case adjustable parameter for B distribution involving Si and Ge$_x$Si$_{1-x}$ layers with x in the range of 0-0.22.

FORMULATION OF THE PROBLEM

We use the B$^-$ diffusivity as suggested by Fair and Pappas [8] and by Fair [9] for Si,

$$D_s^{eff} = D^+ (n_i)(p/n_i) , \qquad (1)$$

where D_s^{eff} is the substitutional B$^-$ atom diffusivity, $D^+(n_i)$ is D_s^{eff} under intrinsic conditions, n_i is the Si intrinsic carrier concentration, p is the hole concentration, k_B is Boltzmann's constant, and T is the absolute temperature. The value of $D^+(n_i)$ is taken to be $13.1\exp(-3.7\ eV/k_BT)$ cm^{2}s^{-1}. In Eq. (1) the B$^-$ atom diffusivity is designated as an effective diffusivity D_s^{eff} by reason of the B diffusion mechanism which we now discuss. The form of Eq. (1) indicates that a positively-charged point defect species governs B diffusion. This positively-charged point defect species should be the Si self-interstitial I^+ [10], and B diffuses via the interstitialcy mechanism according to

275

$$B_i^0 \Leftrightarrow B_s^- + I^+ , \tag{2}$$

where B_s^- is an ionized boron acceptor atom on a Si lattice site, and B_i^0 is a neutral boron atom occupying a bond-centered interstitial position [11]. In this interstitialcy mechanism, diffusion of the B_s^- atoms, which are themselves immobile, is accomplished by the migration of B_i^0 atoms, for which the rate is high, and the subsequent change-over of a B_i^0 to become a B_s^- and produce an I^+ simultaneously. The thermal equilibrium concentration of B_s^- is large while that of B_i^0 is small, and hence the measured B concentration is simply that of B_s^-. The Si vacancy species also make a small contribution to B_s^- diffusion [10], which we ignore in the present analysis.

Details of the Fermi-level effect on the thermal equilibrium concentrations of ionized shallow acceptor and on other charged species have been discussed in the accompanying paper [7]. Accordingly, we have

$$C_s^{eq} = (1/g)\, C_{s\delta}^{eq}\, (n_i/p) \exp\left((E_i - E_v)/(k_B T)\right) , \tag{3}$$

where g is the acceptor level degeneracy factor of ~4, C_s^{eq} is the thermal equilibrium concentration of B_s^-, $C_{s\delta}^{eq}$ is the thermal equilibrium concentration of the neutral boron atoms, B_s^0, which is a constant in a single material, n_i is the crystal intrinsic carrier concentration, p is the hole concentration, E_i is the intrinsic Fermi level, E_v is the valence band edge energy. We also have

$$C_I^{eq} = C_I^{eq}(n_i)(p/n_i) , \tag{4}$$

where C_I^{eq} is the thermal equilibrium concentration of I^+, and $C_I^{eq}(n_i)$ is the same quantity under intrinsic conditions.

Our starting equations describing the diffusion processes of the three species B_s^-, I^+ and B_i^0 are

$$C_i/(C_s C_I) = C_i^{eq}/\left(C_s^{eq} C_I^{eq}\right) = K , \tag{5}$$

$$C_I = C_I^{eq} , \tag{6}$$

$$\partial C_i/\partial t = \partial\left(D_i\, \partial C_i/\partial x - \left(C_i/C_i^{eq}\right)\left(\partial C_i^{eq}/\partial x\right)\right)/\partial x - \partial C_s/\partial t , \tag{7}$$

where C_i, C_s, and C_I are respectively the actual concentrations of B_i^0, B_s^-, and I^+, and D_i is the diffusivity of B_i^0. Equation (5) is obtained according to reaction (2) by assuming dynamic equilibrium holding among B_i^0, B_s^-, and I^+. Equation (6) is obtained because B diffusion is slow and hence the I^+ concentration should not have been perturbed substantially from that under thermal equilibrium conditions. Equation (7) is obtained in accordance with reaction (2) using the diffusion-segregation formulation method [12], with the term $\left(C_i/C_i^{eq}\right)\left(\partial C_i^{eq}/\partial x\right)$ on its right-hand side accounting for the solubility difference of B_i^0 in $Ge_x Si_{1-x}$ and in Si. In either material, C_i^{eq} is a constant independent of p since B_i^0 is uncharged. Using Eqs. (3) and (4), and noting that $C_s + C_i \approx C_s$ holds and hence $\partial(C_s + C_i)/\partial t \approx \partial C_s/\partial t$ also holds, Eqs. (5)-(7) yield

$$\frac{\partial C_s}{\partial t} = \frac{\partial}{\partial x}\left[D_s^{eff}\left(\frac{\partial C_s}{\partial x} + \frac{C_s}{p}\frac{\partial p}{\partial x} - \frac{C_s}{n_i}\frac{\partial n_i}{\partial x} - \frac{1}{k_B T}\left(\frac{\partial E_i}{\partial x} - \frac{\partial E_v}{\partial x}\right) - \frac{C_s}{C_{s\delta}^{eq}}\frac{\partial C_{s\delta}^{eq}}{\partial x}\right)\right] , \tag{8}$$

where D_s^{eff} is the B_s^- effective diffusivity given by

$$D_s^{eff}(n_i) = K\, C_I^{eq}(n_i)\, D_i\,(p/n_i) . \tag{9}$$

Compare to Eq. (1), we see that $D^+(n_i) = K\, C_I^{eq}(n_i)\, D_i$.

A generalized hole transport equation has been derived for application in III-V compound SL layers, see the accompanying article [7]. The treated effects include the hole segregation property in the layers and the junction electric field on the hole concentrations in the junction regions. This equation is applicable also to the $Ge_x Si_{1-x}/Si$ type heterostructures. Accordingly, we have

$$\partial p/\partial t = \partial\left[D_p\left(\partial p/\partial x - (p/N_v)\left(\partial N_v/\partial x\right) - (p/k_BT)\left(\partial E_v/\partial x\right) + (pq/k_BT)\left(\partial\phi/\partial x\right)\right)\right]/\partial x , \quad (10)$$

where D_p is the hole diffusivity, N_v is the valence band effective density of states, q is the magnitude of the electron charge (taken to be positive), and ϕ is the electrostatic potential at the junctions. The potential ϕ satisfies Poisson's equation

$$\partial^2\phi/\partial x^2 = (q/\varepsilon)[n - p + C_{a^-} - C_{d^+} - C_I], \quad (11)$$

where ε is the layer material dielectric constant, C_{a^-} is the ionized shallow acceptor density of all species that may be present, e.g., B$^-$ and Al$^-$, C_{d^+} is the ionized donor density, and C_I is the I^+ concentration. The quantity C_{d^+} is included in Eq. (11) to account for also the possible presence of donors in the material layers. In the absence of the electric field, Eq. (11) is just the charge neutrality condition. Because of the presence of the electrostatic potential ϕ, the carrier concentration at the junctions are differing from those in the bulk of the involved material layers. The junction carrier concentrations influence the dopant distribution rate via their influences on the B_s^- solubility and on the concentration of I^+.

ANALYSIS OF EXPERIMENTAL RESULTS

To analyze the experimental results of B_s^- diffusion in Ge$_x$Si$_{1-x}$/Si structures [1-4], Eqs. (9), (10), (12) and (13) are solved numerically using the general purposed partial different equation solver ZOMBIE [13]. Among the reported experimental results [1-4], Fang et al. [3] and lever et al. [4] have given B_s^- diffusion profiles that are suitable for analyses. We have fitted these available B_s^- diffusion profiles. Kuo et al. [1,2] reported extracted B_s^- diffusivity information but did not give useful B_s^- diffusion profiles.

Figure 1 shows an example of the fits and the B_s^- experimental profiles of Lever et al. [4] obtained at 850°C, from which it is seen that the fits are satisfactory. We have fitted all of their data to the same degree of satisfaction. The materials constants used in obtaining the fits, including the diffusivity value of B_s^-, are listed in Table 1. The other constants include N_v, E_v, and n_i. For Si and Ge, the listed values are those available from the literature. For Ge$_x$Si$_{1-x}$, either available literature values of the appropriate quantity, or values weighted linearly by x from the Si and Ge values, have been used. These used values are room temperature values, because high temperature ones are not available, and there also lacks some needed basic information for extrapolating them from the room temperature ones to high temperature ones.
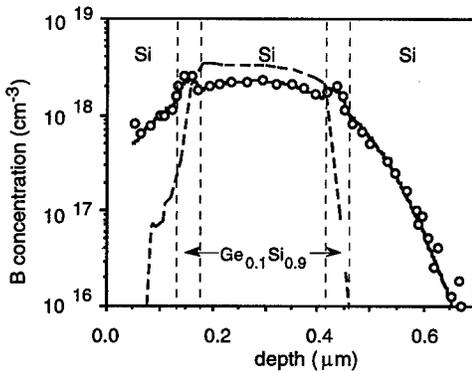

Fig. 1. B_s^- distribution data of Lever et al. [4] at 850°C/5760 min, fitted by the Fermi-level effect model with the effect of the junction carrier concentration also considered. Dotted line is the initial B_s^- profile, circles are those after annealing, and the solid line is our calculated fitting curve.

Figure 2 shows one example of the fits of the B_s^- experimental profiles of Fang et al. [3] obtained at 850°C (for x=0.095 and 0.225), from which it is seen that the fits are also satisfactory. For space reasons, the materials constants used in obtaining the fits cannot be not given here.

Table 1.   Values of materials constants used for obtaining fits to the experimental results of Lever et al. [4], including those for the $Ge_{0.03}Si_{0.97}$ and the $Ge_{0.1}Si_{0.9}$ samples. The values of E_i and E_v are referenced to the vacuum level at 0 eV.

material	n_i (cm^{-3})	E_i (eV)	E_v (eV)	N_v (cm^{-3})	structure	$D_s^{eff}(n_i)$ $[cm^2 s^{-1}]$
a: Si	3.4×10^{18}	-4.62	-5.15	8.2×10^{20}		
b: $Ge_{0.03}Si_{0.97}$	3.86×10^{18}	-4.606	-5.1278	8.2×10^{20}		
c: $Ge_{0.1}Si_{0.9}$	5.2×10^{18}	-4.574	-5.076	5.72×10^{20}		
					a/b/a/b/a	2.8×10^{-16}
					a/c/a/c/a	1.5×10^{-16}
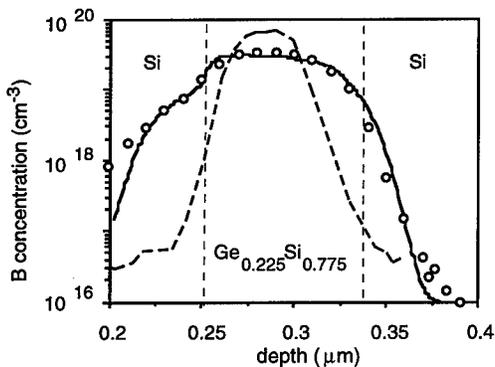
Fig. 2. B_s^- distribution data of Fang et al. [3] at 850°C, fitted by the Fermi-level effect model with the effect of the junction carrier concentration also considered. The sample structural conditions and other experimental conditions are included in the drawing for each case. Dotted line is the initial B_s^- profile, circles are those after annealing, and the solid line is our calculated fitting curve.

We specifically note that, in obtaining these fits, the thermal equilibrium concentrations of the neutral B atoms in the Ge_xSi_{1-x} and Si materials, $C_{s\delta}^{eq}$, are taken to be of the same value.

DISCUSSIONS

Segregation of dopant are determined by: (i) a chemical effect on the thermal equilibrium concentrations of the acceptor species in the neutral state; (ii) in addition to the chemical effect, a Fermi-level effect on the thermal equilibrium concentrations of the acceptor species in ionized state; and (iii) the effect of the junction carrier concentrations which influences also the diffusion process of the acceptor atoms. Because of the use of the condition that $C_{s\delta}^{eq}$ are taken to be of the same value in Si and in Ge_xSi_{1-x} alloys, we see that here the chemical effect is of no importance. Thus, B segregation between the Si and Ge_xSi_{1-x} materials is due to the two other effects, particularly that of the Fermi-level dependence of the B_s^- solubility.

Our present fits to the experimental B_s^- diffusion profiles in the Ge_xSi_{1-x}/Si structure are satisfactory. These B diffusion profiles have also been satisfactorily fitted by the original authors themselves [3,4] using a model invoking the BGe pair formation via the reaction $B+Ge \Leftrightarrow BGe$. Therefore, distinguishing features between the present and previous models do not include the degree of satisfaction of the fits. Rather, the distinguishing features are the involved physical factors. In the present model the role of the B solubility difference in the materials and the carrier concentration at the heterojunctions are emphasized, while these factors have been ignored in the previously employed model [1-4]. But these factors play an essential roles in B_s^- distribution, and hence should have been also included in the model of the previous authors' [1-4]. The BGe pair formation process seems to be just a postulate. We are not aware that existence of the BGe pairs has been detected in experiments.

Irrespective of being a daily used p-type dopant in Si, the exact nature of the physical mechanism of B diffusion is still not clear even just in Si and in Ge. There is a substantial difference in the assumed B diffusing mechanisms between the present and previous model. In contrast to the present model, B_s^- diffusivity is assumed to be given by

$$D = D^0 + D^-(n_i)(P/n_i) \qquad (12)$$

in the previous model [1-4]. According to Eq. (12), B_s^- diffusion is governed by two point defect species, a neutral one leading to the term D^0, and a singly-positively charged one leading to the term $D^-(p/n_i)$. This is clearly in contrast to our presently assumed B_s^- diffusion mechanism as expressed by Eq. (1), for which the governing point defect species is assumed to be just the singly-positively charged self-interstitial I^+. The two different mechanisms, as represented by Eqs. (1) and (12), are both arrived at for B_s^- diffusion in Si based on fits to experimental results. It is still not clear which is superior. That is, either one would offer better fits to some profiles, but usually not by much. Therefore, in principle, the use of either mechanism should be regarded as valid at the present time. We have chosen the I^+ only model to start with because then Eq. (1) is obtained via a derivation in accordance with the chosen mechanism, which allows the treatment to be self-consistent. Presently, Eq. (12) is still of an empirical form, i.e., it has not yet been consistently derived from the chosen mechanism of involving the contributions of both I^0 and I^+.

We believe that the strongest factor supporting the validity of the present model is the situation in III-V compounds, see the accompanying article [7]. In a number of III-V compound SL structures, the shallow acceptor species Zn and Be exhibit a similar distribution anomaly, but with the phenomenon so much more pronounced that it is readily apparent that the dopants are strongly segregated among the SL layers. In these layers, the acceptor atom concentration difference can be a couple orders of magnitude, but in each layer Zn or Be atoms are nearly totally ionized. Therefore, the Zn or Be segregation behavior cannot be due to clustering or pairing of the acceptor atoms with the matrix material atoms in some layers, but rather due to a solubility difference [7]. Since B distribution in the Ge_xSi_{1-x}/Si heterostructures and Zn or Be distribution in III-V compound SLs are analogous cases, we expect the same mechanism to play a role in all these cases.

The B_s^- diffusivity values used in the previous analyses rise some concerns. The used values of D^0 in Eq. (12) by Lever et al. [4] vary as x is changed, which is in principle acceptable. But, the used values also vary with the initial B concentration and annealing times, which is unwarranted. Furthermore, according to Kuo et al. [1,2], the used values of the quantity $D'=D^0+D^-(n_i)$, for obtaining the fits in the range of x values from 0 to 0.22 at 850°C [2] and from 0 to 0.53 at 800°C [1], decreases as the x value in the Ge_xSi_{1-x} layer is increased, see Fig. 3. There is no data available for still larger x values except for pure Ge at 800°C [14], see also Fig. 3.
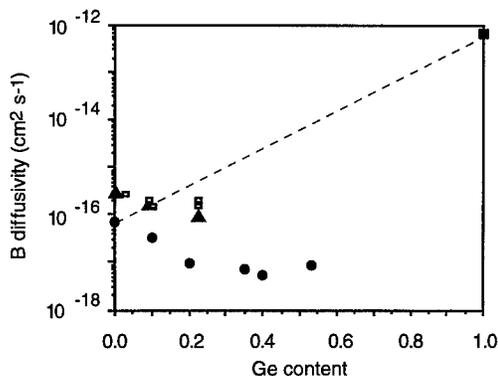

Fig. 3.   Effective B_s^- diffusivity values needed to fit the experimental data. Those of Kuo et al. are the $D'=D^0+D^-(n_i)$ values, and those for the present work are that given by Eq. (10). The dashed line indicates the value expected from a first order effect of averaging the B_s^- diffusivity values in Si and in Ge in proportion to Ge content in the Ge_xSi_{1-x} material. The symbols are: filled circles (Kuo et al./800°C), filled triangles (Kuo et al./850°C), filled square (Sharma/800°C), open squares (present work).

It has been suggested [15] that, as x increases from 0 to 1, the B_s^- diffusion mechanism in Ge_xSi_{1-x} changes from that governed by self-interstitials I to that governed by vacancies V, with V assumed to be the point defect species governing B_s^- diffusion in Ge. However, judged by this suggestion, the B diffusivity D' dependence on x [1,2] would seem to be unsettling on a quantitative basis. Consider that both I and V make contributions, B_s^- diffusivity in Ge_xSi_{1-x} may be written as

$$D_{GeSi} = D_{GeSi}^I + D_{GeSi}^V .$$ (13)

On the basis of a first order effect, let us assume that the Ge_xSi_{1-x} alloy constitutes an ideal solution. Then, we expect that D_{GeSi}^I and D_{GeSi}^V are linear combinations of the appropriate I and V contributions to B_s^- diffusion in Ge and in Si, in proportion to composition x of the Ge_xSi_{1-x} material. Hence, $D_{GeSi}^I = x D_{Ge}^I + (1-x)D_{Si}^I$ and $D_{GeSi}^V = x D_{Ge}^V + (1-x)D_{Si}^V$ hold. However, the B diffusivity in Ge and in Si are $D_{Ge} = D_{Ge}^I + D_{Ge}^V$ and $D_{Si} = D_{Si}^I + D_{Si}^V$ respectively. These expressions yield

$$D_{GeSi} = x D_{Ge} + (1-x)D_{Si} .$$ (14)

Equation (14) means that, on the basis of a first order effect, the B diffusivity in Ge_xSi_{1-x} is simply the average of the B_s^- diffusivities in Ge and in Si weighted by x. With B_s^- diffusivities in Ge and in Si known, the value of Eq. (18) is the straight line indicated in Fig. 3. It is seen that the D' values of Kuo et al. [1,2] deviated prominently from that predicted by Eq. (14). While this first order analysis is not expected to be accurate, we would nevertheless also expect that the deviation from that predicted by Eq. (14) should not have been so large.

CONCLUDING REMARKS

It appears that the most important physical factors leading to the B_s^- diffusion anomalies in Ge_xSi_{1-x}/Si structures are the Fermi-level effect on the solubilities of B_s^- in the materials and the carrier concentration effect at the heterojunctions. Diffusion of B_s^- in Si and in Ge_xSi_{1-x} for small x values are most likely governed by the singly-positively charged self-interstitial I^+.

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SURFACE TERMINATION OF THE Ge(100) AND Si(100) SURFACES
BY USING DHF SOLUTION DIPPING

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ABSTRACT

Surface termination of Ge(100) and Si(100) was investigated after diluted HF (DHF) solution dipping. On the Ge(100) surface as picked up from DHF, Ge-hydride was observed only in the HF concentration (C_{HF}) region above 10%. The adsorbed fluorine increased with increasing C_{HF}, and the concentration reached around 10^{14} cm^{-2} at the C_{HF} of 40-50%. In the case of the DHF dipped Si(100) surface, Si-hydride and hydrophobicity against both DHF and deionized water (DIW) were observed for all the conditions studied, while the fluorine concentration increased and saturated to about 10^{14} cm^{-2} in the C_{HF} region above 15%. Hydrophobicity against DHF was observed in the C_{HF} region of 10-30%, but degraded below 5% and above 30%. By transferring the DHF dipped Ge(100) into DIW, hydrophobicity appeared within a few seconds and then was degraded with increase of DIW dipping time. The degradation proceeded slower after dipped in higher concentration DHF. Corresponding to the degradation, it was observed that the total amount of the adsorbed fluoride was gradually decreasing, while the Ge-hydride coverage scarcely decreased. From these results, hydrophobicity of Ge(100) seems to be attributed not only to the hydrogen termination but also to the fluoride adsorption, which is much different from the case of Si(100).

INTRODUCTION

Si$_{1-x}$Ge$_x$/Si (0<x<1) heterostructures have been applied to various Si-based hetero-junction devices[1-3] such as heterobipolar transistors, high electron/hole mobility transistors and multiple quantum well photodiodes. Especially, Si-based atomicallycontrolled heterostructures are becoming very attractive for the future high performance device. In atomically-controlled processes[4-6] using an ultraclean low temperature reaction environment of low pressure chemical vapor deposition (LPCVD), atomic-order ultrathin layer growth of Si on Ge(100) and Ge on Si(100) was greatly affected by hydrogen termination on the initial surfaces[7,8] Hydrogen termination on the Si surface and its stability have been studied by using atomic hydrogen irradiation in ultrahigh vacuum (UHV), diluted HF (DHF) dipping and H$_2$ annealing[9-11] Particularly, the DHF dipped Si(100) and the H$_2$ annealed Si(100) surfaces have an excellent stability against oxidation in air by the hydrogen termination[10,11] In this way, to control the surface termination is very important for control the low-temperature surface reaction as well as surface cleanliness. On the other hand, hydrogen termination on the Ge surface has been investigated only by using atomic hydrogen irradiation in UHV[9,12] As an easier and more reproducible method for obtaining a clean and termination-controlled surface, a wet chemical process is one of the candidates for applying Si-Ge heterostructures to the Si LSI process, such as a selectively regrowth process of SiGe on the limited area of SiGe surface. In the present work, surface termination of Ge(100) by DHF dipping, as well as on Si(100), have been investigated in relation to the surface treatment condition and the surface hydrophobicity against the solution.

EXPERIMENTAL

The substrates used were the Si(100) wafers of 2-20 ohm·cm and 30×30 mm^2 with a

mirror polished surface. As a Ge(100) substrate, the epitaxial Ge film (about 1500-3000Å-thick) on the Si(100) substrate was grown by an ultraclean LPCVD system using GeH$_4$ and H$_2$ gases at 350 °C.[13] Wet chemical treatment of the substrates was examined by dipping into DHF solution with various HF concentration (C_{HF}) and deionized water (DIW). After the above treatments, coverages of Ge-hydrides and Si-hydrides were measured in N$_2$ purged environment by the Fourier-transform infrared reflection absorption spectroscopy (FTIR/RAS). Concentrations of the fluorine atom and the oxide on the substrates were evaluated by measuring the area intensities of the peak of F 1s and of the peaks of Ge 3d and Si 2p chemically-shifted by bonding to oxygen atom in x-ray photoelectron spectroscopy (XPS). During the transport to each evaluation apparatus, the samples were exposed to the cleanroom air (relative humidity (RH) of about 25-46%) for a few minutes.

RESULTS AND DISCUSSION

Hydrogen Terminated Structures of Ge(100) and Si(100)

Figure 1 shows the FTIR/RAS absorption spectra of Ge(100) and Si(100) after DHF dipping for 2 min and after H$_2$ annealing followed by cooling in H$_2$ down to below 100 °C.[14] Here, C_{HF} of DHF is 20% for Ge(100) and 0.5% for Si(100). After the DHF dipping, broard absorption peaks were observed at 2008 cm^{-1} for Ge(100) and at 2108 cm^{-1} and 2140 cm^{-1} for Si(100) assigned as Si-dihydride and Si-trihydride, respectively.[15] The peak positions are about 100 cm^{-1} different mainly due to differences of the binding force and the atomic weight between Ge-H and Si-H. As a reference, after the H$_2$ annealing, sharp absorption peaks are observed at 1992 cm^{-1} for Ge(100) and at 2100 cm^{-1} for Si(100) assigned as monohydride in the Ge-Ge and Si-Si dimer[14,16] (dimer monohydride), respectively. For either Ge(100) or Si(100), as shown in Fig. 1, the absorption peak position for the H$_2$ annealed surface is apparently shifted lower than that for the DHF dipped surface. Thus, similar hydrogen terminated structures are expected both on Ge(100) and on Si(100).
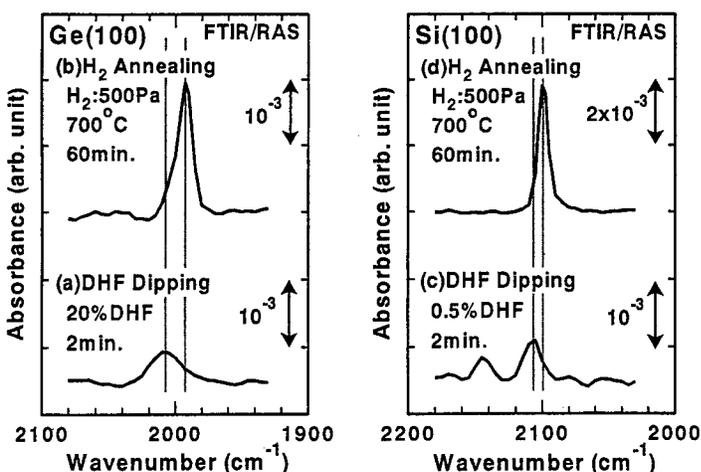
Fig. 1. FTIR/RAS absorption spectra of Ge(100) and Si(100) (a)(c)after HF dipping for 2 min and (b)(d)after H$_2$ annealing at 700 °C for 60 min followed by cooling in H$_2$ down to below 100 °C. The H$_2$ pressure was main- tained at 500 Pa.
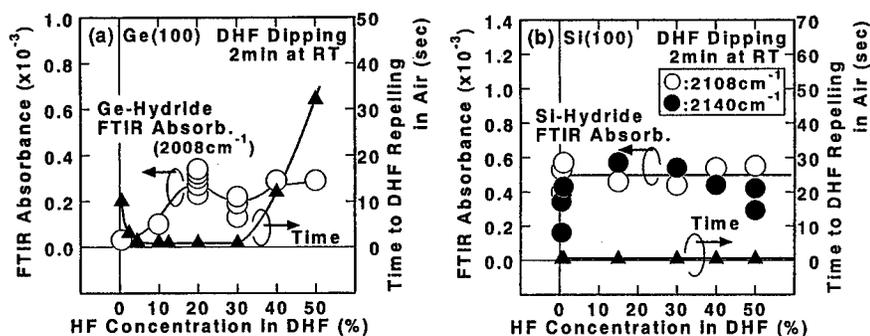
Fig. 2. C_{HF} dependences of the FTIR absorbance of the hydride and the time to DHF repelling just after picking up the Ge(100) and Si(100) substrates from the DHF solution in the 25%-RH air.

Figure 2 shows the C_{HF} dependences of the FTIR absorbance of the hydride and the time to DHF repelling on Ge(100) and Si(100) just after picking up the sample from the DHF solution in the 25%-RH air. Here, the longer repelling time means the degradation of surface hydrophobicity against the solution and conversion to the hydrophilic surface. In the case of the DHF dipped Ge(100) surface, higher C_{HF} than 10% is more effective to obtain the hydrophobic hydrogen terminated surface, as shown in Fig. 2a. From another result that the chemically-shifted XPS Ge $3d$ peak was lowering with the increase of C_{HF} up to 30%, the hydrophilicity is considered to be caused by the existence of the native oxide. However, too high C_{HF} beyond 30% results in a hydrophiric surface, while the hydrogen termination is still observed, and the surface was obviously covered with the sticky solution after picking up the substrate. Because the viscosity of the HF solution is not so widely varied with the C_{HF} region of 0-50% (0.9 for 0% and 0.8 for 50% at 25 °C [17]), one of the origins of the another hydrophilicity is considered to be drastical change of some surface property as related to the results in Fig. 3. On the other hand, in the case of the DHF dipped Si(100) surface as shown in Fig. 2b, the FTIR absorbances of Si-hydrides such as dihydride (SiH$_2$; 2108 cm^{-1}) and trihydride (SiH$_3$; 2140 cm^{-1}) are always observed around 5×10^{-4} and 2-5×10^{-4}, respectively, and the surface showed perfect hydrophobicity in the C_{HF} region of 0.5-50%.

Fluorine Adsorption in the DHF Solution

The adsorbed fluorine on the DHF dipped Ge(100) increased with increasing C_{HF}, and the C_{HF} which resulted in C_F around 10^{14} cm^{-2} was 40-50%. In the case of the DHF dipped Si(100) surface, the C_F increased and saturated to about 10^{14} cm^{-2} in the C_{HF} region above 15%. Figure 3 shows the C_{HF} dependences of the XPS intensity of the fluorine atom on the DHF dipped Ge(100) and Si(100) surfaces just after picking up the samples from the DHF solution in the 25%-RH air. A few kinds of XPS F $1s$ peaks were distinguished at the binding energy about 683-690eV, and the peak positions were determined within the error width of ±0.2eV. In the case of the DHF dipped Ge(100) as shown in Fig. 3a, up to the C_{HF} of 30%, 685.4eV-peak is dominant. However, beyond 30%, 683.8eV-peak is dominant instead of the 685.4eV-peak. The F $1s$ binding energies in GeF$_n$ (n=1-2; [GeF$_1$]/[GeF$_2$]=1.35) and in GeF$_4$ on the Ge surface were determined to be 684.9eV and 687.0eV, respectively[18] When the linear
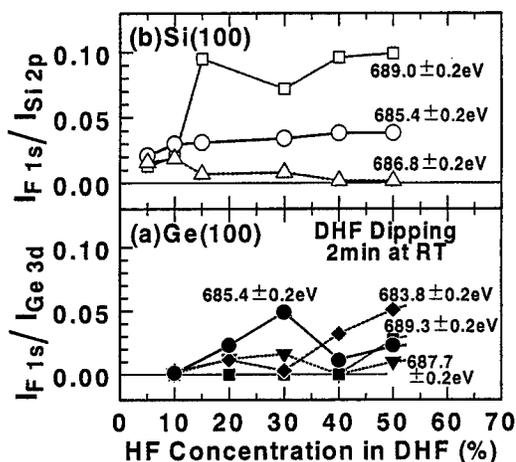
Fig. 3. C_{HF} dependences of the XPS peak intensity of the fluorine atom on the DHF dipped Ge(100) and Si(100) surfaces just after picking up the samples from the DHF solution in the 25%-RH air. DHF dipping time is 2 min. In the case of absence of hydrophobicity, the residual solution on the surface was removed by N_2 gas blow.

relation is extensively assumed between the binding energy and n ($1 \leq n \leq 4$), the binding energies of 683.8 eV and 685.4eV are estimated to correspond to the fluorine atom in GeF_1 ($n=1$) and the fluorine atom in GeF_2 ($n=2$), respectively. From these results, it is suggested that the change of the surface fluoride species is closely related to the surface hydrophobicity as discussed in Fig. 2a.

In the case of Si(100), *Chuang* concluded that the F $1s$ binding energies in SiF_2 and SiF_4 on the Si surface were 685.5eV and 686.8-687.0eV, respectively.[19] As shown in Fig. 3b, 685.4eV-peak is always dominant rather than 686.8eV-peak. On the other hand, the 685.4eV-peak intensity increases and saturates (to around $I_F/I_{Si}=0.04$; 4×10^{13} cm^{-2}) with increase of the C_{HF}, while the 686.8eV-peak intensity decreased with increase of the 685.4eV-peak intensity. Moreover, corresponding to the decrease of the the 686.8eV-peak intensity, 689.0eV-peak becomes dominant at the higher C_{HF} than 15%. Higher binding energies than 687.2eV were especially characterized by the F $1s$ in carbon fluorides (CF).[20] In the used XPS measurement system, it is expected that an oil contamination from the exhaust line occured and CF were produced by the reaction of the adsorbed fluorides and the contaminant. Therefore, from the existence of high concentration CF ($I_F/I_{Si}=0.10$; 1.0×10^{14} cm^{-2}) on Si(100), it is suggested that, just after the DHF dipping, reactive molecules such as HF physically adsorbed on hydrogen and fluorine terminated Si(100) at the higher C_{HF} than 15%.

Figure 4 shows the DIW dipping time dependence of the time to DIW repelling just after picking the DIW rinsed Ge(100) substrate from the DIW in the 37%-RH air. By transferring the DHF dipped Ge(100) into DIW, hydrophobicity against DIW appeared within a few seconds and then was degraded with DIW dipping time. The degradation proceeded slower when dipped in higher concentration DHF. Corresponding to the degradation, it was observed that the total amount of the adsorbed fluoride (1.3×10^{14} cm^{-2} and 1.4×10^{14} cm^{-2} respectively on the 50%-DHF dipped Ge(100) and Si(100) surfaces) was gradually decreasing with the decay time constant of around 25 sec, while the hydrogen termination was maintained during the DIW dipping within 120 sec. From these results, hydrophobicity of Ge(100) seems to be attributed not only to the hydrogen termination but also to the fluoride adsorption, which is much different

Fig. 4. DIW dipping time dependence of the time to DIW repelling just after picking the DIW rinsed Ge(100) substrate from the DIW in the 37%-RH air.

from the case of Si(100).

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IMPROVED PROCESS WINDOW USING LOW-CARBON
Ge$_x$Si$_{1-x-y}$C$_y$ EPITAXIAL LAYERS

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ABSTRACT

Processing of silicon-based heterojunction devices is severely constrained by the relaxation of strained epitaxial layers. Generally the equilbrium critical thickness cannot be exceeded if high-temperature process steps such as oxidation and diffusion are performed. In this paper, we report on the beneficial effects of small amounts of carbon ($\lesssim$ 0.2%) added to germanium-silicon epitaxial layers. We will show that such low concentrations result in a substantial decrease of boron diffusivity and strain relaxation. We will also report on the fabrication of Ge$_x$Si$_{1-x-y}$C$_y$ heterostructure MOS capacitors with a channel thickness of 300 Å and a maximum germanium fraction of 50%. A thermal oxidation at 800 °C was performed resulting in good C(V$_G$) characteristics along with improved hole confinement.

INTRODUCTION

Since the successful application of strained germanium-silicon epitaxial layers in heterojunction bipolar transistors, there has been much interest in the further development of column IV alloy semiconductors. The growth of Si$_{1-y}$C$_y$ and Ge$_x$Si$_{1-x-y}$C$_y$ materials was a natural objective, although the low equilibrium solid solubility of carbon made this much more challenging than Ge$_x$Si$_{1-x}$ growth. The first report of high-quality Si$_{1-y}$C$_y$ films was by Iyer et al. [1], who used molecular beam epitaxy. Subsequently, Ge$_x$Si$_{1-x-y}$C$_y$ layers were grown by CVD by Bodnar and Regolini [2] and St. Amour et al. [3]. Much of this work was directed at the incorporation of the maximum amount of substitutional carbon in order to obtain the greatest change in energy gap. Lanzerotti et al. [4] reported that incorporation of 0.45-1.1% carbon resulted in significantly improved heterojunction bipolar transistors since the carbon increased the bandgap difference for a given strain. This effect becomes more pronounced as the carbon concentration increases. It was also reported that material with high carbon concentrations had improved thermal stability [5] and reduced boron diffusion [6].

In this paper, we consider the beneficial effects of small carbon concentrations ($\lesssim$ 0.2%). This work was in part motivated by the difficulty of obtaining large substitutional carbon concentrations in UHV/CVD [7]. We will show that improved thermal stability and reduced boron diffusion are also obtained in low-carbon material.

GROWTH OF Ge$_x$Si$_{1-x-y}$C$_y$

The Ge$_x$Si$_{1-x-y}$C$_y$ layers used in this work were grown by UHV/CVD using silane, 10% germane in hydrogen, and 2% methylsilane in hydrogen as the reactants. The growth temperature was 600 °C. Deposited layers were characterized by high-resolution X-ray diffraction and the total carbon concentration was determined by SIMS.

Figure 1 shows HRXRD scans for layers grown with 6 sccm silane, 2.4 sccm germane, and varying methylsilane flow. (With zero methylsilane flow this gas mixture would result in a

287

germanium fraction of 11.2%). The GeSi layer is quite thick (5700 Å) and consequently thickness fringes are not resolved. Thickness fringes are pronounced in the samples with methylsilane flows of 0.26 and 0.66 sccm indicating that these layers are uniformly strained and of high quality. These layers have total carbon concentrations of 0.27 and 0.66, respectively. The growth rate decreases with increasing methylsilane flow rate and consequently the fringes become more widely spaced.
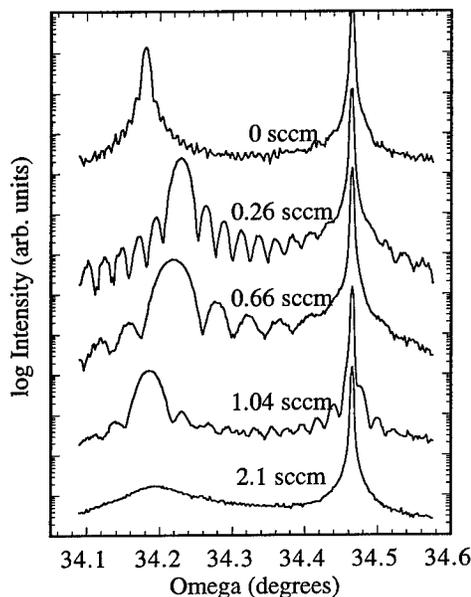

Figure 1. HRXRD scan of layers grown with 6 sccm SiH_4, 2.4 sccm GeH_4/H_2, and varying methylsilane flow. The growth temperature was 600 °C.

Figure 1 also shows that the principal peak due to the epitaxial layer initially shifts to the right (consistent with increasing carbon concentration and decreasing strain) but then shifts back to the left with further increases in methylsilane flow. SIMS measurements show that this is due to an interaction between germanium and carbon incorporation rates (that is, increasing carbon causes an increase in the germanium incorporation rate) [7]. Comparison of the total carbon concentration as measured by SIMS and the substitutional carbon concentration extracted from the X-ray measurements shows that the carbon is nearly completely substitutional up to about 0.23%. Above this value an increasing amount of the carbon is incorporated into interstitial sites.

In UHV/CVD growth of $Si_{1-y}C_y$, the maximum fully substitutional carbon concentration is greater than observed in MBE and lower than RTCVD growth at the same temperature [8]. This has been attributed to the effects of hydrogen surface coverage [9] and gas phase reactions [8]. The results reported here suggest that similar phenomena occur when $Ge_xSi_{1-x-y}C_y$ is grown.

STRAINED LAYER RELAXATION

The *equilibrium* critical thickness of a strained epitaxial layer is the thickness at which it is energetically favorable for the strained layer to relax by the formation of misfit dislocations. When layers are grown at low temperatures, kinetic limitations retard the formation and propagation of dislocations. Relaxation can still occur during subsequent high-temperature steps, such as those required for emitter implant annealing and thermal oxidation. Consequently, design of devices with strained epitaxial layers is severely constrained when compatibility with conventional silicon processing is required.

The effect of carbon on relaxation of $Ge_{0.17}Si_{0.81}C_{0.019}$ epitaxial layers has been reported by Riley et al. [5]. They observed no change in the in-plane lattice constant upon annealing at temperatures of 900 °C and above. We consider here the relaxation of layers containing much less carbon. Lower carbon concentrations are easier to obtain by CVD and may also be less susceptible to the formation of silicon carbide precipitates.

Figure 2 compares X-ray diffraction scans of two layers with approximately equal thickness and strain. A 1650 Å $Si_{0.91}Ge_{0.09}$ layer containing no carbon shows substantial broadening of the principal layer peak after annealing for one hour at 700 °C. The perpendicular lattice constant shifts to a smaller value, consistent with relaxation by the formation of misfit dislocations. In contrast, the 1800 Å $Si_{0.888}Ge_{0.11}C_{0.002}$ layer shows no evidence of relaxation at 900 °C and is substantially broadened only after annealing for the same time at 1000 °C. Annealing causes the principal layer peak to shift to lower angles, indicating that the lattice constant is increasing. This can be due to transfer of carbon from substitutional to interstitial sites or the formation of silicon carbide precipitates. We see that carbon-containing layers are stable at temperatures useful for thermal oxidation and implant annealing.
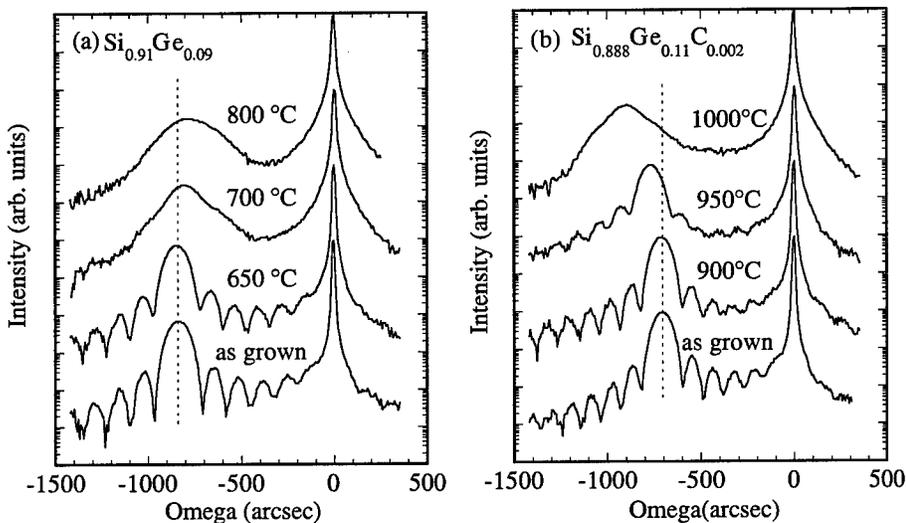
Figure 2. Effect of one hour anneals on $Si_{0.91}Ge_{0.09}$ and $Si_{0.888}Ge_{0.11}C_{0.002}$ layers.

BORON DIFFUSION

Boron diffusion can result in the formation of a barrier at the base-collector junction, reducing the transistor current gain. Consequently, reduction of boron diffusion is important in improving the process margin in heterojunction bipolar transistor fabrication.

Figure 3 shows the effect of annealing on a boron profile in a germanium-silicon-carbon layer. The initial profile was grown in during epitaxial layer growth and corresponds roughly to profiles used in heterojunction bipolar transistor fabrication. The boron concentration profile is in part limited by the SIMS resolution, particularly on the downslope. The upper curve illustrates the measured profile after a one hour anneal at 900 °C. It is evident that, within experimental error, there is no broadening of the boron profile.
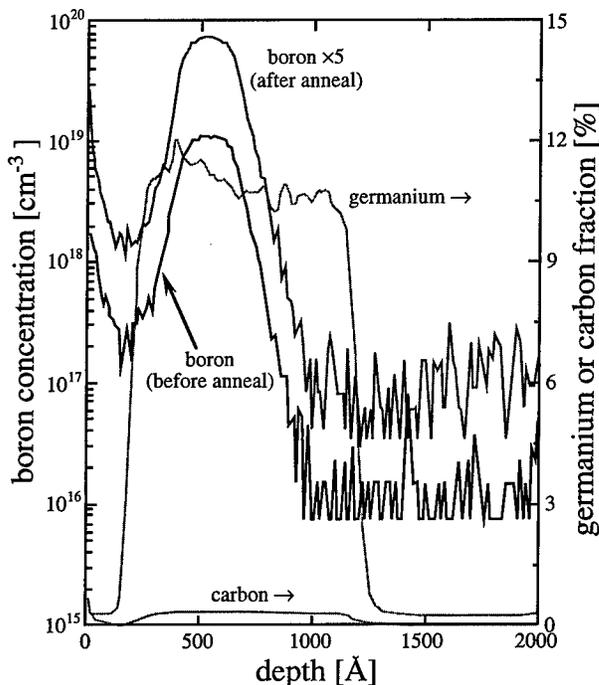
Figure 3. Boron profiles before (black) and after (dark gray, ×5) a one hour anneal at 900 °C.

It would be desirable to compare these measurements with a similar boron profile grown into a germanium-silicon layer. Unfortunately a layer of this thickness would relax during the anneal, and enhanced diffusion along dislocations would invalidate the comparison. Nevertheless, these results indicate that boron profile broadening is negligible in $Ge_xSi_{1-x-y}C_y$ at least up to 900 °C.

GROWTH AND CHARACTERIZATION OF MOS CAPACITORS

In order to illustrate the applicability of low-carbon $Ge_xSi_{1-x-y}C_y$ layers, we have fabricated heterostructure MOS capacitors. This structure has a buried hole channel similar to that in Ge_xSi_{1-}

$_x$ heterostructure field effect transistors. In this device, the surface hole density is limited by the depth of the potential well. The depth of the potential well can be increased by increasing the germanium fraction, but then the thermal stability of the structure will be degraded.

Figure 4 illustrates the structure investigated in this work. A 300 Å thick $Ge_xSi_{1-x-y}C_y$ channel region is grown with a varying germanium concentration varying linearly from 10 to 50%. The plot shows the calculated valence band energy as a function of position for an applied bias which corresponds to inversion in the channel but not at the surface. The 200 Å gate insulator was grown by thermal oxidation at 800 °C, and the gate electrodes were sputtered aluminum contacts 1.2×10^{-3} cm^2 in area.
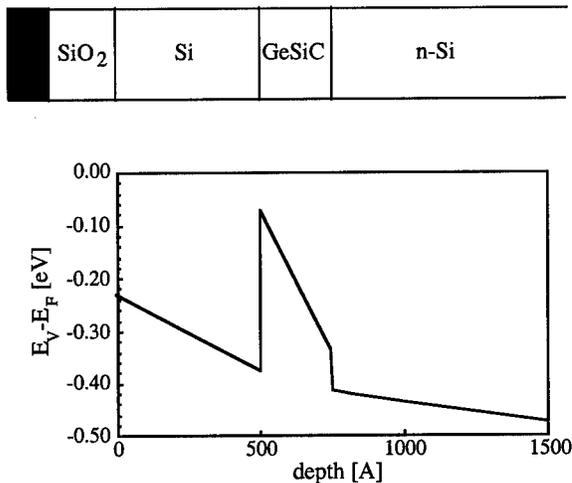
Fig. 4. Heterostructure MOS capacitor (top) and calculated valence band energy as a function of position (bottom) as calculated by a one-dimensional Poisson simulator.

Figure 5 shows the measured high-frequency (1 MHz) and quasistatic $C(V_G)$ curves for this device. The quasistatic curve shows the ledge characteristic of hole confinement in the buried channel. The high frequency curve is close to ideal with no detectable stretchout due to interface states and no hysteresis as is expected for a high-quality thermal oxide.

It is important to note that a 300 Å germanium-silicon layer with the same germanium profile would be approximately double the equilibrium critical thickness. Such a layer would probably require use of a low-temperature silicon dioxide layer in order to prevent relaxation. Low-temperature oxides are always inferior to thermally grown oxides and usually exhibit substantial hysteresis.

These results show that $Ge_xSi_{1-x-y}C_y$ is highly suitable for application in heterostructure MOS transistors. The improved thermal stability of $Ge_xSi_{1-x-y}C_y$ makes it possible to increase the total charge density in the channel while the reduced boron diffusivity minimizes diffusion of the p-type doped region. Similar benefits can be expected in heterojunction bipolar transistors were there are similar problems of layer relaxation and dopant diffusion.
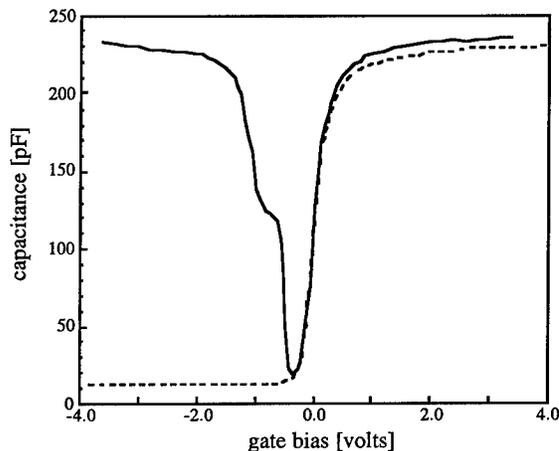
Figure 5. Measured high-frequency (dashed) and quasistatic $C(V_G)$ characteristics of a buried-channel heterostructure MOS capacitor.

SUMMARY

$Ge_xSi_{1-x-y}C_y$ layers with substitutional carbon concentrations of 0.2% have been grown by UHV/CVD. The maximum fully substitutional carbon concentration is not as great as observed with high-pressure CVD techniques. Nevertheless, a significant improvement in thermal stability and boron diffusion rate are observed. Low-carbon layers are expected to be applicable to heterojunction bipolar transistors and heterstructure field effect transistors.

ACKNOWLEDGEMENTS

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MOBILITY CHARACTERIZATION OF P-TYPE AND N-TYPE STRAINED Si$_{1-x-y}$Ge$_x$C$_y$/Si EPILAYER HALL DEVICES

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ABSTRACT

Mobilities in Si$_{1-x-y}$Ge$_x$C$_y$ layers were measured using mesa etched Van der Pauw structures for alloy layers with $0 < x < 0.30$ and $0 < y < 0.02$ and doping levels of $10^{15} < N < 10^{18}$ cm^{-3}. Mobilities in Si$_{1-x-y}$Ge$_x$C$_y$ layers with $x = 0.27$ were found to approach Si mobilities for both μ_n and μ_p. While electron mobilities in phosphorous-doped SiGeC decrease with doping concentration, hole mobilities in boron-doped SiGeC increase with doping level, indicating ionized impurity scattering is not dominant for μ_p over the temperature range studied.

INTRODUCTION

As advantages of SiGeC alloys become clear, it is critical to understand the effect of substitutional and interstitial C incorporation on mobility and other carrier properties. The purpose of this work is to address the effect that C incorporation into SiGe has on carrier mobilities. To our knowledge, this is the first time this subject has been addressed in a systematic manner for this material system in the literature.

EXPERIMENT

Strained Si$_{1-x-y}$Ge$_x$C$_y$ epitaxial layers on (100) Si were grown using atmospheric-pressure chemical vapor deposition (APCVD) at temperatures ranging from 625°C to 675°C. Ge compositions of these epilayers range from $x = 0$ to $x = 0.30$ and C compositions from $y = 0$ to $y = 0.02$ as determined using Rutherford back-scattering (RBS) analysis. Analysis of similar layers using double crystal x-ray diffraction (DCXRD) has shown this material to be fully strained with compressive strain occurring in the plane parallel to the heterojunction and tensile strain along the axis normal to the heterojunction. It should be pointed out that the C concentrations found by RBS include both substitutional and interstitial C atoms. Raman and FTIR measurements on similar samples (unpublished, performed in collaboration with the University of Barcelona) has shown the ratio of substitutional C to interstitial C to decrease as the total C concentration in the alloy layer is increased. For low C concentrations (~1%), most of the C incorporation occurs substitutionally. The layers in this present study have not been measured using these methods, but from previous measurements we would estimate the C to be incorporated substitutionally for the greatest part. Epilayer thickness, ranging from 191nm to

348nm, was also determined by RBS and verified using spreading resistance profiling (SRP). Epitaxial doping levels were determined using SRP to range from 10^{15} to 10^{18}cm^{-3}.

Hall measurement structures were formed by mesa-etching Si$_{1-x-y}$Ge$_x$C$_y$ epitaxial layers to define discrete Van der Pauw or 'Greek cross' structures extending completely through each epilayer; Figure 1(a) shows a plan view of the 1mm Van der Pauw structure used for the measurements in the present work.
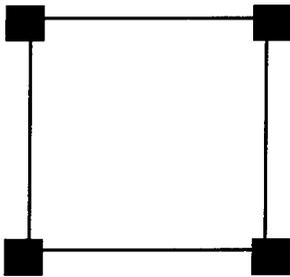

Figure 1(a) - Plan view of the 1mm x 1mm Van der Pauw structure used for Hall measurements.
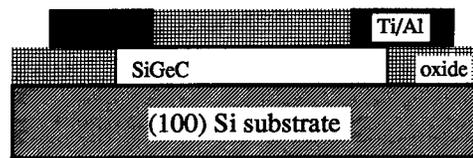
Figure 1(b) - Cross-section of the Hall measurement structure.

These patterns were mesa-etched through the strained SiGeC epilayers using either reactive ion etching (RIE) or standard wet etching. RIE etching was done using an SF$_6$/O$_2$ gas mixture at 7.5sccm and 2.5sccm, respectively, and a pressure of 100mTorr. Wet mesa-etch samples were formed using HNA etching at room temperature. After mesa-etch, all samples were examined using a standard differential step-height profilometer to verify that the Hall structures extend completely through each epilayer. The Hall structures were next covered by an oxide dielectric layer, patterned for contact holes, and covered by Ti/Al metallization deposited using electron-beam evaporation. A final patterning step on the Ti/Al layers followed by a standard clean step and a 425°C/30 minute furnace anneal in forming gas, results in contact to the measurement structures via bondpads. Finally, the backside oxide was removed and the wafer cleaned. Figure 1(b) shows a cross-section of the completed measurement structure; note that this structure is measuring the in-plane mobility. After fabrication, samples were diced using a wafer saw and placed into dual in-line packages (DIP) for measurement.

Hall measurements were performed using the Keithley model 7065 Hall Measurement system, over a temperature range of 83K to 673K with a magnetic field strength of 4.8KG. The Hall coefficient for this setup is estimated to be 1.18 assuming lattice scattering dominates these measurements [1].

RESULTS/DISCUSSION

Figure 2 shows a plot of hole mobilities in boron-doped SiGeC layers on p-type (100) Si. Measurement results for four strained SiGeC/Si samples, as well as for a reference Si device constructed simultaneously with these samples, are represented by the symbols enclosed by the legend box in Figure 2. Also shown are reference curves for hole mobilities in unstrained Si from Jacoboni et al. [2] and for hole mobilities in strained SiGe channels from Wang et al. [3].
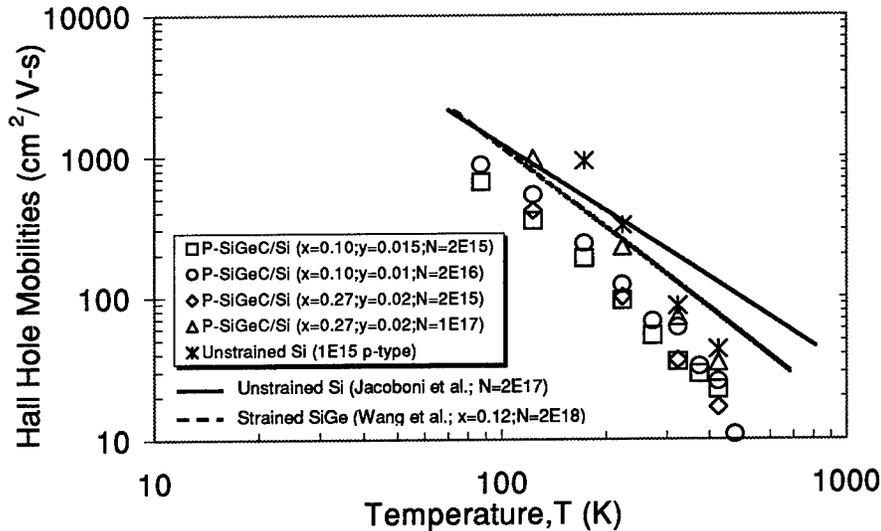
Figure 2 – Measured hole mobilities (μ_p) in boron-doped SiGeC layers on p-type Si (composition and doping shown in legend) and a single unstrained Si substrate. The lines represent reference data from the literature. Solid line: unstrained Si μ_p from Jacoboni et al. [2]. Dashed line: μ_p in strained SiGe channels from Wang et al. [3].

Figure 2 shows the strained SiGeC hole mobilities to be slightly below those for the Si reference device. In comparing the slope of the mobility vs. temperature, both reference Si and strained SiGeC layer curves have slightly higher slopes than the curves from literature, which we have not explained at this time. At a temperature of 123 K, the alloy layer combining high Ge concentration (x = 0.27) and high doping ($N_A = 1 \times 10^{17} cm^{-3}$) has the highest SiGeC μ_p value we measured in this work, 900cm^2/V-s; this exceeds the μ_p for Si data from the literature [2]. In comparing data series 1 to 3 and data series 2 to 4, it is seen that the layers with higher Ge concentrations have enhanced mobilities over those that have lower Ge concentrations when other parameters are equal.
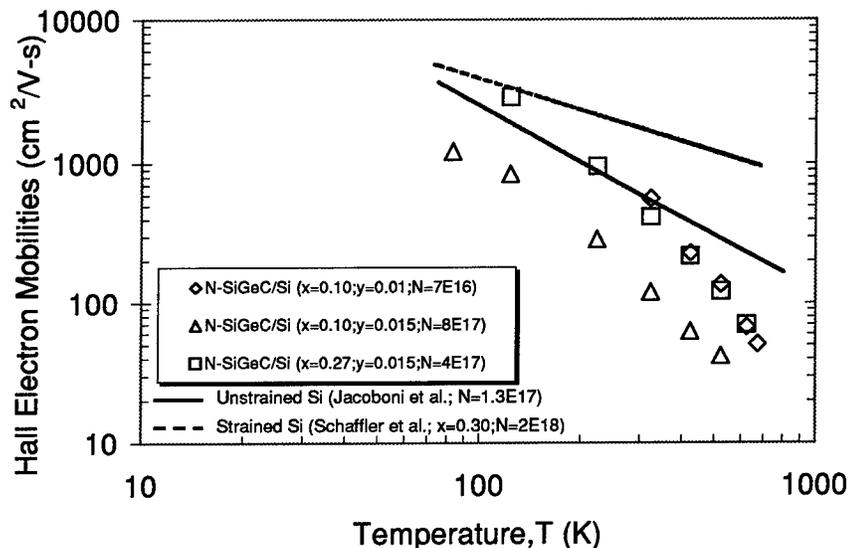
Figure 3 – Measured electron mobilities (μ_n) in phosphorous-doped SiGeC layers on n-type Si (composition and doping shown in legend). The lines represent reference data from the literature. Solid line: unstrained Si μ_n from Jacoboni et al. [2]. Dashed line: μ_n in strained Si on SiGe from Schaffler et al. [4].

Figure 3 shows a plot of electron mobilities for phosphorous-doped SiGeC layers on n-type (100) Si. Measurement results for three strained SiGeC/Si samples are represented by the symbols enclosed in the legend box; also shown in Figure 3 are reference curves for electron mobilities in unstrained Si from Jacoboni et al. [2] and for electron mobilities in strained Si on SiGe taken from Schaffler et al. [4]. Similar to the results seen for hole mobilities, μ_n is enhanced for alloy layers with increased Ge concentrations; this may be seen in Figure 3 by comparing curves 2 and 3. Figure 3 also shows two alloy layers with μ_n that exceeds that found in the literature for Si (shown by the solid line). At a temperature of 123 K, we measured the highest μ_n recorded for strained SiGeC layers in this work with a value of 2880cm^2/V-s ($x = 0.27$, $y = 0.015$, $N_d = 4\times10^{17}$cm^{-3}). It is expected that the μ_n for the alloy layer in the first data series in Figure 3 ($x = 0.10$, $y = 0.01$, $N_d = 7\times10^{16}$cm^{-3}) will display even higher mobilities when the measurements are extended to lower temperatures.

An examination of the μ_n versus temperature slope in Figure 3 shows that an inflection point in the slope occurs at about 200 K. We believe this to be the temperature at which ionized impurity scattering dominates the μ_n of the alloy layer. Figure 2 shows that this effect is not present in the μ_p versus T curves.

Figure 4 shows the effect of alloy doping levels on SiGeC mobilities for temperatures of 323 K. Also shown are reference curves from Jacoboni et al. for both n-type (solid line) and p-type (dashed line) unstrained Si layers [2].
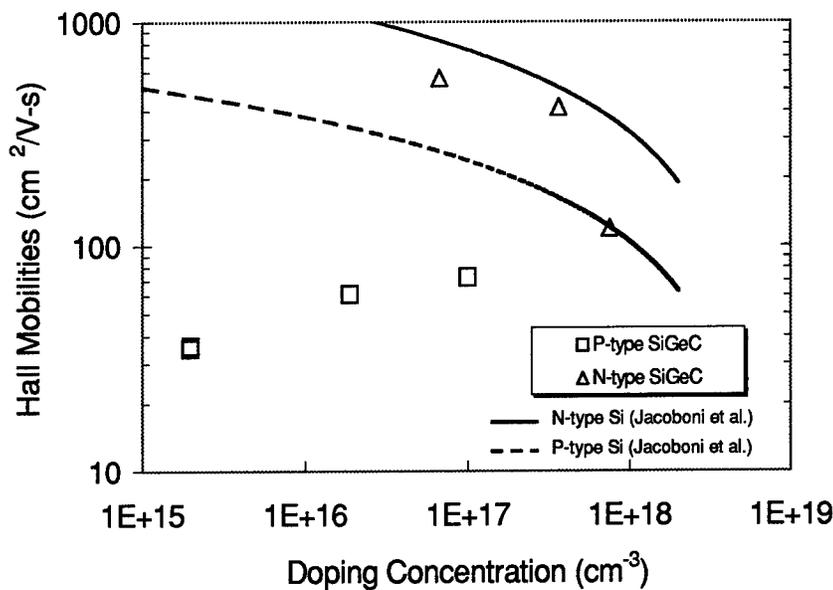
Figure 4 - Measured doping effect on strained SiGeC mobilities at 323 K. The lines show 300K reference data from Jacoboni et al.[2]. Solid line: unstrained n-type Si. Dashed line: unstrained p-type Si.

Figure 4 shows that the behavior of SiGeC μ_n parallels the unstrained Si reference quite well, indicating that ionized impurity scattering appears to affect the SiGeC μ_n in a way quite similar to Si. The effect of doping on the SiGeC μ_p is quite different from the doping effect on Si, however; our data shows that the SiGeC μ_p increases with doping level, suggesting that μ_p is not dominated by ionized impurity scattering. While these data indicate that the limiter for μ_p in SiGeC layers is a mechanism other than ionized impurity scattering, we do not know from these measurements that ionized impurity scattering is not occurring at a rate comparable to that in Si – only that any ionized impurity scattering which may be present is not the dominant scattering mechanism at this temperature.

We propose a theory to account for the rise in SiGeC μ_p with doping, which is shown in Figure 4. We suggest that the effect could be explained by boron induced strain in the alloy layers. The incorporation of boron in SiGe layers has previously been shown to introduce strain into the alloy layer. The μ_p in SiGe has also been shown in previous work to increase with both

tensile and compressive stress [5]. We propose that increased boron incorporation in these p-type SiGeC layers is resulting in μ_p enhancement by increasing strain in the alloy layer.

Measurements on anisotype SiGeC/Si structures have also been initiated. In isotype n-type SiGeC/n-type Si heterojunctions, the possibility exists for small amounts of parallel conduction (in the substrate) leading to a slight over-estimate of the mobility. While the valence band discontinuity makes parallel conduction for p-type SiGeC/p-type Si unlikely, n-type mobility measurements may be refined to account for parallel conduction of the order of several percent.

CONCLUSIONS

We have studied the electron and hole mobilities in strained $Si_{1-x-y}Ge_xC_y$ layers using Hall effect mobility measurements. Carrier mobilities in these layers were found to increase with increasing Ge concentration; for $x = 0.27$, SiGeC μ_n and μ_p approach or exceed carrier mobilities for unstrained Si. While electron mobilities in SiGeC decrease with doping concentration, hole mobilities rise indicating ionized impurity scattering is not the limiting factor for μ_p over the temperature range studied. Work is underway to explore this effect over a wider range of dopant concentrations.

ACKNOWLEDGEMENTS

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FIRST-PRINCIPLES INVESTIGATION OF THE ORDERED Si$_4$C COMPOUND

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ABSTRACT

We have performed intensive theoretical studies on the ordered Si$_4$C phase which has been proposed first by Rücker et al. [Phys. Rev. Lett. **72**, 3578 (1994)] and which recently has been reportedly synthesized by Kouvetakis et al. [Appl. Phys. Lett. **72**, 930 (1998)]. We calculate structural parameters which are significantly different from experimental values, and an IR spectrum with a peak position very similar to their experiment but a much narrower width. We suggest that the experimental findings might be consistent with the assumption of a system of Si$_4$C sections/crystallites and other Si-C structures embedded in a Si matrix.

INTRODUCTION

Since it was thought for a long time that no ordered Si-C structures besides the stoichiometric SiC compounds exist, the idea of trying to grow Si$_{1-y}$C$_y$ or—to reduce the strain in the specimens arising from the strongly different "sizes" of Si and C atoms—Si$_{1-x-y}$Ge$_x$C$_y$ random alloys gave recently rise to a substantial research effort.[1,2] However, two limitations of this approach became quickly clear: First, because of the low solubility of C in Si/SiGe— less than 2×10^{-3} at. % in Si and even smaller in Ge—[3], only alloys with a few percent (roughly 1–4%) C can be grown using even the most elaborate techniques.[1,4] For higher concentrations, segregation of C and formation of the ordered SiC phases take place.

Recently, however, it was predicted theoretically that an ordered Si$_4$C structure where the C atoms form a continuous third-neighbor (3N) network would be energetically more favorable than a random alloy because such a structure allows the stretched Si-C bond to exist with minimum strain.[5] This prediction has been examined experimentally by Kouvetakis et al. who reported to have grown and characterized Si$_{80}$C$_{20}$ films with such a structure.[6] They found by means of diffractometry that the lattice constants in their Si$_{80}$C$_{20}$ films ranged from 5.25 to 5.4 Å which is slightly lower than that of Si but significantly higher than the Vegard value (5.06 Å). Furthermore, they found one infrared (IR) active (supposedly Si-C stretching) mode centered at 740 cm^{-1} with a broad absorption band whose width was interpreted to be probably due to the lack of long-range order. The value of 740 cm^{-1} is considerably higher than that of isolated C in Si (605 cm^{-1}), but notably lower than the IR active mode of β-SiC (796 cm^{-1}); therefore, it was concluded that the value of 740 cm^{-1} is symptomatic of a weakened bond presumably due to steric strain. These findings are highly interesting and are accessible to first-principles calculations, and therefore are re-examined from a theoretical point of view in the following. In addition, we also study the elastic and electronic properties of Si$_4$C, which are essential for device applications of such a material.

COMPUTATIONAL DETAILS

Our calculations are based on a generalized gradient approximation[7] (GGA) to the local-density approximation. We use the efficient plane-wave ultrasoft pseudopotential[8] based code VASP.[9] The plane wave cutoff energy is 211 eV, which is enough to converge energy differences to within 0.03 eV. For all ordered structures that are discussed in the following we use a primitive simulation cell, and for Si-C random alloys a cubic 64-atom supercell. We use throughout special k-point meshes that guarantee convergence of our results to within 0.05 eV, e.g., for the 64-atom cubic cell a 4^3 mesh. For the phonon calculations necessary for the calculation of the IR spectrum, we used a finite difference method implemented into the

self-consistent local-orbital simplified LDA code FIREBALL96 with a sp^3 minimal basis and the same **k**-point sampling as above.[10] Furthermore, we use MSI's CERIUS2 software suite to construct the different simulation cells and for qualitative studies as described in the discussion section.

RESULTS

Structure

Besides the well-known stoichiometric SiC polytypes, Si_4C is the only ordered Si-C compound that has been reported to date. Its structure can be derived from the Si-diamond lattice by replacing rows of Si atoms along one of the cubic axes by C atoms, where the projection of the rows on the surface are arranged in a 3N "knight's-move" pattern.[5] The ideal Si_4C crystal has a lattice which is body-centered tetragonal with a c/a ratio of $\sqrt{2/5}$ (0.632). The space group is $I4_1/a$, No. 88 of the International Tables of Crystallography, and belongs to the tetragonal-dipyramidal point group ($4/m$ in international, C_{4h} in Schönflies notation). In Ref. 5, this structure had been found by systematically scanning ordered $Si_{n-1}C$/Si structures with $n \leq 8$ for low-energy configurations. We compared the energy of the ordered Si_4C structure with that of Si-C random alloys of the same C concentration and found the ordered structure to be lower in energy.[11]

Optimizing internal and external parameters, we find for the Si_4C structure ground-state lattice parameters of $a = 7.93$ Å and $c = 5.04$ Å ($c/a = 0.636$). This results in bond lengths of $d_{Si-Si} = 2.33$ Å and $d_{Si-C} = 1.93$ Å as compared to theoretical bondlengths for Si and β-SiC bulk materials of $d_{Si-Si} = 2.37$ Å and $d_{Si-C} = 1.89$ Å, respectively. The lattice constant for a cubic cell with the same volume/atom as our tetragonal cell is 5.02 Å, 1.3% smaller than the corresponding theoretical Vegard value. Our calculated results are significantly different from the experimental findings of Ref. 6 where a lattice constant of 5.25–5.4 Å (only slightly smaller than that of Si) was found and, consequently, a substantial elongation of the Si-C bond was suggested.

In order to check if our results are reasonable, we calculated the Si-C bond lengths for Si_4C and β-SiC in comparison to those of random alloys with corresponding C concentrations (20 and 50%, respectively).[11] For SiC, it has been pointed out before that the bond length of the ordered structure is always smaller than that of the corresponding random alloy.[12] We find a bond length of 1.89 Å for the ordered SiC structure, 3.3% shorter than that of the random alloy. Comparing Si_4C and SiC, the bond length of Si_4C (1.93 Å, 2.5% shorter than the random alloy) looks very reasonable. We furthermore calculated the bond lengths for other ordered Si-C compounds with a smaller C concentration than 20% and found for those bond elongations of approximately 7% in agreement with the general findings of Ref. 5 where no separate value was given for Si_4C.

Infrared and Raman spectra

Since our structural results are not consistent with the findings of Ref. 6, we also calculated the IR spectrum of Si_4C in order to compare it to experiment. We calculated the zone-center phonons of Si_4C with FIREBALL96,[10] furthermore the IR spectrum from the phonon frequencies and eigenvectors as given, e.g., in Ref. 13. We find an IR spectrum with one prominent peak at 812 cm^{-1}. The Si_4C peak is 12% lower (90 cm^{-1}) than the theoretical one for SiC. However, the FIREBALL96 method tends to overestimate the phonon frequencies of semiconductor materials: For Si, the zone-center phonon is calculated to be 6% higher than the experimental value, and for SiC, the TO Γ-point phonon is 14% higher than experiment. In order to compensate this theoretical over-estimate, we interpolate between the errors for Si and SiC linearly for Si_4C, and rescale the frequency axis of our calculated spectrum correspondingly by a factor of 0.92%. The y-axis has been rescaled to match the minimum

transmittance of the experiment for easier comparison. Our "ab-initio" rescaled spectrum has its new major peak at 746 cm^{-1} and can be found, together with the measurements from Ref. 6, in Fig. 1(a).
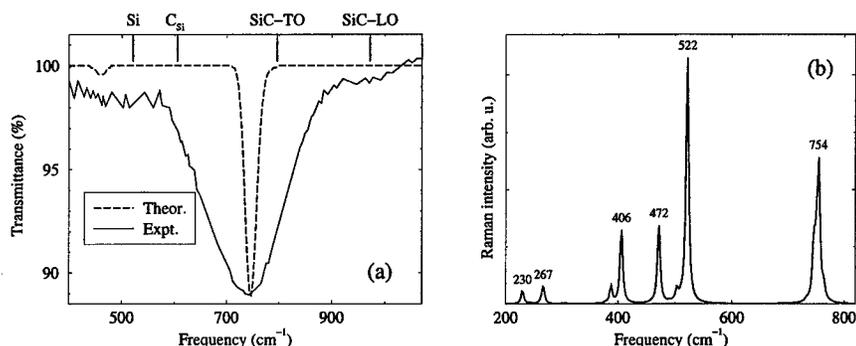

FIG. 1. (a) Theoretical IR spectrum for Si_4C (dashed line) in comparison to the measurements of Ref. 6 (solid line). Also, we indicate the frequencies of other relevant vibrational modes as discussed in the text. (b) Theoretical prediction for the Raman spectrum of Si_4C. The theoretical curves have been rescaled as described in the text.

Even if the experimental peak is extremely broad and covers well the frequencies of a number of possible atomic arrangements (C impurity in Si at 605 cm^{-1}, Si_4C expected at 746 cm^{-1}, SiC at 796 cm^{-1}), its center is clearly between the frequencies for C impurities and SiC and matches very well the theoretical prediction for Si_4C. We believe the lower IR frequency in Si_4C as compared to SiC is a consequence of the C bonding which is weaker in Si_4C than in SiC: Whereas in SiC a complete hybridization involving all valence electrons creates very strong bonds, the large chemical differences between Si and C causes the s^2 electrons in C to participate only weakly in the bonding process in the case of dilute C concentrations which in turn lowers the force constants and therefore the phonon frequencies.[14] This is the reason why the frequency of isolated C impurities is 200 cm^{-1} lower than that of SiC, at least 50 cm^{-1} less than the most favorable estimate for a pure bond-length effect. Consistently, Si_4C has an IR frequency between those of SiC and C impurities.

Since the IR results seem to be the most reliable "fingerprint" of the Si_4C structure, a complementary technique to probe the presence of the Si_4C phase in a sample might be Raman scattering, since more modes than the IR active Si-C mode can be expected to be Raman active (bulk Si which shows no first-order IR lines has a Raman-active mode at 521 cm^{-1}). Therefore, we have calculated the Raman spectrum of Si_4C with a bond-polarizability model,[15] starting from FIREBALL96 phonons. Our result (with the frequency axis rescaled in the same way as for the IR spectrum) is shown in Fig. 1(b). We find that the Si_4C Raman spectrum shows besides the Si-C mode a prominent Si-Si peak (522 cm^{-1}) and mainly two other (smaller) Si-Si modes (406 and 472 cm^{-1}). Even if the relative intensities of the single peaks might be different in experiment—in the calculation, we assume the bond polarizabilities to be the same for all bonds—, a Raman measurement could be a valuable further probe for the existence of Si_4C, since it displays besides the Si-C peak at 754 cm^{-1} Si-Si peaks other than the familiar 521 cm^{-1} line that are characteristic of this compound.

Elastic properties

For the bulk modulus, we find $B_0 = 1.2$ Mbar which is 30% smaller than the Vegard value interpolated between bulk Si and C, in accordance with general findings of a bowing in the

elastic parameters of Si-C alloys.[12,14] In Ref. 14, bowing parameters had been determined for the elastic constants of Si-C random alloys from (simplified) first-principles calculations as well as from classical Tersoff-potential calculations. From these bowing parameters, the one for the bulk modulus can be extracted assuming an isotropic C distribution (and therefore cubic symmetry) using $B_0 = 1/3 (c_{11} + 2c_{12})$. We find a bulk modulus bowing parameter of -1.7 Mbar from the FIREBALL96 calculations of Ref. 14, and -2.1 Mbar from the Tersoff results, respectively. Using either of these bowing parameters for the Si_4C crystal (20% C), we find a bulk modulus of $B_0 = 1.2$ Mbar, in excellent agreement with our directly calculated value. This is a very reasonable result since the bulk modulus of β-SiC, although higher, is also close to the bowing-interpolated value using the above bowing parameters.

The Si_4C structure shows no remarkable peculiarities under pressure. Performing constant-pressure calculations up to 400 kbar, we find the structure to compress nearly isotropically with a very weak pressure dependence of the c/a ratio in the form of $c/a(P) = 0.636 + 0.30\,\mathrm{Mbar}^{-1} P$.

Electronic properties

Since the interest in Si-C compounds was fueled recently by the demand for new semi-conductor alloys with tunable band gaps, the electronic structure of Si_4C is an important question in a theoretical investigation of this compound. Our calculated band structures can be found in Fig. 2.
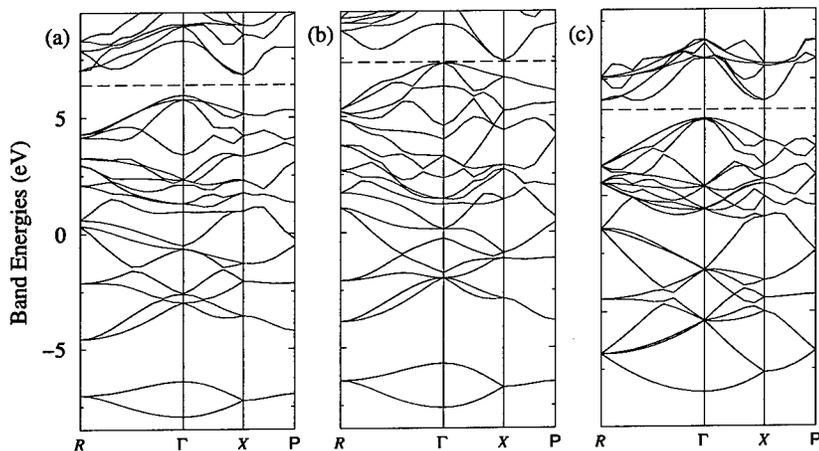
FIG. 2. Calculated band structure for (a) Si_4C at zero pressure, (b) Si_4C at 390 kbar, and (c) Si calculated in a supercell analogous to the Si_4C cell, at zero pressure.

Si_4C has an indirect band gap of 0.87 eV with the top of the valence band being at the Γ-point, and the bottom of the conduction band being at the X-point of the Brillouin zone. This is slightly larger than what we find for Si (0.64 eV; for comparison, we show in Fig. 2(c) the Si band structure in a 10-atom supercell analogous to the Si_4C primitive cell) and was to be expected from previous band structure calculations for Si-C random alloys, since the C concentration is larger than 12.5%.[16] Interestingly, in this concentration regime an exponential interpolation between the theoretical values for Si and C as previously proposed[17] which has been shown to fail to predict the decrease in the gap for concentrations

smaller than 12.5%[16] gives a reasonable estimate for the band gap of 0.93 eV. Note that all theoretical GGA band gaps are too small as compared to experiments due to Coulomb effects.[18]

Since it had been shown that isolated C impurities form localized states ("deep levels" in the sense of Ref. 19) in Si,[14] one could expect that the Si_4C compound with a relatively low C concentration might represent something like a "semi-deep" system with an interesting pressure behavior. Therefore, we calculated the band structure of Si_4C under pressures up to 390 kbar where the theoretical band gap starts to close [see Fig. 2(b)]. This value is relatively small considering that the GGA band gap of Si, which has a smaller gap and a smaller bulk modulus, disappears in our calculation at approximately 550 kbar and is a sign of the above mentioned chemical differences between Si and C.

DISCUSSION

In order to understand the discrepancy in the lattice constant between experiment and our theoretical results, we performed a qualitative study using a classical force field within MSI's CERIUS2 software. We determined the lattice constant for a structure consisting of 540 atoms which contained 9 Si_4C conventional cells, where the C atoms in the eight outer cells were exchanged by Si atoms, therefore representing a Si_4C cell embedded into Si. For this arrangement, we found the lattice constant to be 6% larger than that of the ordered Si_4C structure which means a value of 5.32 Å instead of 5.02 Å.

Next, we checked if the assumption of Si_4C sections (or crystallites) in a Si matrix is also consistent with the experimental findings for the IR spectrum. In Ref. 6, a peak with a frequency very close to our theoretical prediction, but with a much larger width, had been found. In order to see if this effect also appears for our system with the embedded Si_4C, we calculated the IR spectra for the embedded and for the simple Si_4C systems. Whereas for the Si_4C system, there is only one active mode, we find for the embedded structure—which is still highly ordered—besides the (only slightly shifted) main peak a whole variety of satellite peaks spreading over a frequency range of 12 cm^{-1}. Even if this number is small as compared to the experimental width, it shows the well-known broadening effect of confinement on spectroscopic lines. A further sign of disorder might be the shoulders below 560 cm^{-1} and between 890 and 1020 cm^{-1} which might be due to disorder-activated usually non-IR-active modes (e.g., the Si optical mode is at 521 cm^{-1}, and the highest SiC mode, LO(Γ), at 972 cm^{-1}). A homogeneous distribution of Si and SiC crystallites besides Si_4C would also agree with the experimental SIMS results of homogeneous Si and C distributions throughout the sample.[6]

In summary, we find that the experimental findings of Ref. 6 might be consistent with the assumption of Si_4C sections (and other C-related complexes like SiC) embedded into a Si matrix.

CONCLUSIONS

In our theoretical study of Si_4C, we found for the structural parameters of Si_4C values considerably smaller than the experimental measurements of Kouvetakis *et al.*[6] For the IR spectrum, the frequency of the IR active peak in theory and experiment agree well, even if the experimental peak has a very large width. The theoretical Si-C bond length is not found to be elongated as was proposed in Ref. 6. However, the frequency of the Si-C mode can be understood from the different bonding situations in SiC, Si_4C, and Si with C impurities. Calculating lattice parameters and IR spectra using an empirical potential, we found that the experimental values of Ref. 6 might be consistent with Si_4C sections (and other Si-C structures like SiC) embedded into a Si matrix.

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AUTHOR INDEX

SUBJECT INDEX

adhesion, 165
$Al_xGa_{1-x}N$, 91
AlN, 113, 133
aluminum
    arsenide, 179
    gallium arsenide, 179, 243
    nitride, 213
    oxide, 133
amorphous, 213
annihilation radius, 9
antimonide, 225

bias temperature annealing, 243
bipolar, 257
bi-stability, 243
bonding, 159
branch defects, 27

CaF_2, 51
cathodoluminescence, 83
chemical effect, 219
circulator, 159
CMOS, 257, 293
compliant substrate, 3, 45, 107
conformal vapor phase epitaxy, 139
Cu metallization, 237

deep level(s), 59, 77, 243
delamination, 121
diamond, 133
diffusion, 275
dislocation(s), 3, 15
    dynamics, 27
dopant, 275

elastic accommodation, 127
electronic properties, 64
ellipsometry, 201
epitaxy, 151, 269, 287

Fe-modelling, 171
Fermi-level effect, 219
ferrite, 159

GaAs, 39, 45, 55, 71, 151
GaAsP, 145
GaAs/Si, 33, 139
gallium
    arsenide(/)
        aluminum gallium arsenide, 257
        high electron mobility transistors, 237
    nitride, 257
GaN, 91, 101
Gd_2O_3, 151
graded buffer, 27

heteroepitaxy, 39, 51, 145
heterointerface, 113

heterostructure(s), 15, 71, 201, 257, 269,
    275, 281, 287, 293
HVPE GaAs, 33
hydrofluoric acid (HF), 281
hydrogen, 237

IGBT, 171
InAs, 65
indium phosphide, 207, 231, 257
infrared, 299
InGaAsN, 59
InGaP, 29
InP, 83
InSb, 249
in situ
    control, 201
    monitoring, 189
integration, 159
interband tunneling, 225
interface, 127, 165
    defects, 45
island formation, 51

junction carrier concentration effect, 219

kinetic VPE modelling, 33

lateral
    epitaxial overgrowth, 91
    oxidation, 21
lattice
    engineered substrates, 21
    mismatch, 65
    mismatched epitaxy, 21
    parameter, 299
LED, 145
low
    leakage currents, 151
    noise amplifiers, 299
luminescence, 83

metal organic chemical vapor deposition, 207
microcavity LEDS, 139
MISFET, 249
misfit dislocations, 21, 65
mobility, 269, 293
MOCVD, 59
modulation doping, 269
molecular beam epitaxy (MBE), 39, 65, 113,
    231
MOMBE, 145
monolithic integration, 139
multiple quantum well, 71

nucleation, 39

OMVPE, 83
optoelectronic interconnects, 139

307