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Analysis of a PWM Resonant Buck Chopper for Use as a Ship Service Converter Module

by

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13. ABSTRACT (Maximum 200 words)

The Navy's interest in implementing a DC Zonal Electric Distribution System (DC ZEDS) in the next generation of surface combatant has motivated considerable research work into dc-dc converters. The switching frequency of a hard-switched dc-dc converter is limited by the maximum admissible switching losses allowed by the switch, heat sink, and cooling process. Also, hard-switched converters contribute significant Electromagnetic Interference (EMI) concerns for the system. This study provides a background analysis into resonant converters which utilize zero-voltage-switching and zero-current-switching techniques to mitigate the aforementioned concerns and facilitate high-bandwidth control loops. In particular, one candidate circuit is identified which can be readily realized using existing hardware and a straightforward control. The report documents the modes of operation of the circuit, sets forth the governing differential equation and mode-transition conditions, examines an ACSL simulation representation of the circuit, formulates design criteria for component selection, identifies key fabrication nuances, and documents a PSpice simulation of the circuit. Both simulation models are used to explain the operating modes of the circuit, provide insight into parameter selection, and ultimately to design the proper control of the circuit.

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Background

The U.S. Navy is actively engaged in promoting the application of state-of-the-art and commercial-off-the-shelf technologies to realize cost-effective platforms. In particular, research and development is focused on improving producibility, enhancing operational flexibility, maximizing survivability, decreasing manning requirements and decreasing overall system cost. From the power system perspective, these goals have translated into research initiatives seeking to reduce the size and weight of the principle distribution components and to optimize the operation and survivability of key system elements. The principle initiative, the development of an Integrated Power System (IPS) architecture [1], considers the implementation of a DC Zonal Electric Distribution System (DC ZEDS).

A zonal architecture [2] has a number of advantages over the current radial distribution architecture. The radial network includes generators supplying switchboards then a myriad of feeder cables strewn throughout the ship to provide power to vital and non-vital electrical loads. The zonal architecture is based on implementing a port and starboard bus and sectioning the ship service electrical loads into a number of zones delineated by watertight bulkhead compartments. Vital loads within a zone are connected to either bus via an auctioneering process. The advantages of zonal include the elimination of a significant amount of feeder cables, main busses only transition watertight compartments, the ship may be fabricated and tested in zones, and ship construction is markedly simplified.

The DC ZEDS program is investigating the feasibility of zonal dc distribution. In DC ZEDS, the ac generator voltages are immediately rectified and approximately 1100 Vdc is sent to the port and starboard busses. Each bus is connected to an electrical zone through a power converter called a Ship Service Converter Module (SSCM). The SSCM buffers the main bus and intra-zonal loads, monitors zone conditions, and adjusts and regulates the main bus voltage downward to a level commensurate with dc-to-ac inverter requirements (approximately 950 Vdc). Three-phase and single-phase ac voltages are synthesized within a zone by a power converter called a Ship Service Inverter Module (SSIM). The SSIM employs "intelligent" feedback control to provide tightly-regulated ac voltage and current to the corresponding loads. In addition, the SSIM on-board intelligence facilitates rapid current limiting which allows for a degree of self protection. It is envisioned that standardized converter modules will be paralleled to achieve the required zone power requirements.

The principle benefits of DC ZEDS are that fault detection and clearing are both simpler and faster and that faults are now isolated to a particular zone. The time lag associated with initiating ac bus transfers is virtually eliminated, enhancing the integrity of

power flow to critical electrical apparatus. In addition, DC ZEDS eliminates the need for most of the distribution transformers and ac switchgear providing substantial savings in size and weight. The ready availability of feedback-controlled dc-to-ac inverters facilitates the application of variable speed drives which in turn optimize the operation of blowers and pumps while implementing an automatic limiting of the in-rush currents experienced when starting large motors. DC ZEDS also eliminates the requirement that the ship service generators be operated at 60 Hz. This allows for a more optimized generator design in terms of size, weight and cost. Finally SSCMs and SSIMs are multifunctional and allow for the inclusion of more intelligent power management and fault protection.

The current Reduced Scale Advanced Development (RSAD) versions of the SSCMs are hard-switched converters operating with switching frequencies on the order of 4kHz. It is desirable to maximize the switching frequency so as to reduce the converter size and weight and to facilitate a higher control bandwidth and therefore a faster transient response. Once again in most military or mobile applications, it is key to maximize the converter power density by minimizing the size of the magnetic components and the filtering capacitors. Unfortunately, higher switching frequencies correspond to higher switching losses. Each time a switch is closed with a non-zero voltage across it and then current is made to flow through it, a power loss occurs. The same happens during turn-off when the switch is transitioned into its blocking state. The aggregate switching losses show up as heat in the semiconductor device and the converter itself. This then requires the derating of the switch devices and more elaborate cooling procedures and heat-sinking for the apparatus. At high enough switching frequency, the hard-switched circuit can no longer be used. In addition, the large dV/dt and dI/dt conditions introduced by hard-switching semiconductor devices result in considerable Electromagnetic Interference (EMI) which may vex system integrators.

Converter topologies which result in zero-voltage and/or zero-current switchings are termed soft-switching converters. Since many of these architectures employ LC-resonance to achieve the zero-voltage or zero-current conditions, these converters are broadly called resonant converters. This report seeks to provide a brief overview of resonant converters then will set forth an in-depth analysis of a particular candidate topology which offers promise for use as an SSCM.

The following classification for resonant dc-dc converters may be adopted:

- Load-resonant converters
- Resonant-switch converters

Other resonant topologies exist but are generally relevant to dc-ac inverters (ie., resonant dc-link and high-frequency-link integral-half-cycle converters).

Load-resonant converters employ either a series or parallel LC-resonant tank circuit to achieve the zero voltage and/or zero current switching. Power flow is controlled by the resonant tank impedance, which in turn is controlled by the switching frequency. Mohan [3] further subclassifies these converters as

1. Voltage-source series-resonant converters
    a. Series-loaded resonant (SLR) converters
    b. Parallel-loaded resonant (PLR) converters
    c. Hybrid-resonant converters
2. Current-source parallel-resonant converters
3. Class-E and subclass-E resonant converters

These converters are not attractive for application in DC ZEDS since their desirable resonant properties are load dependent and the switching frequency control complicates the design, analysis and operation.

In resonant switch converters, an LC-resonance is used during a portion of a cycle to shape the switch voltage and current characteristics to realize the zero-voltage and/or zero-current switchings. Mohan [3] further categorizes these converters according to

1. Zero-voltage switching (ZVS)
2. Zero-current switching (ZCS)
3. Zero-voltage switching, clamped-voltage (ZVS-CV)

These converters are more attractive for application in DC ZEDS since the resonance properties are less sensitive to the load resistance and the control may use fixed-frequency Pulse-Width-Modulation (PWM). Several representative topologies are considered in this section.

The literature is replete with soft-switching dc-dc converter topologies and control strategies. The emergence of the zero-current-switching quasi-resonant converter family occurred in 1987 [4]. These circuits, however, offer no solution for the turn-on switching losses and were soon followed by the development of a zero-voltage-switching technique [5]. This was also a quasi-resonant circuit and it suffered from transistor voltage stresses that were load dependent. Parasitic ringing caused by the junction capacitance of the

rectifying diode also resulted in regulation and stability problems. Some of these issues were later addressed by the development of the ZVS multi-resonant converter [6]. Unfortunately, these converters employ variable switching frequency control which makes it difficult to optimize the design of the filter components and control loop. From this standpoint, fixed-frequency operation is clearly desirable.

Two early examples of constant-frequency ZVS resonant-mode converters include [7]-[8]. The remainder of this section will document a number of recent topologies that are candidates for application in DC ZEDS. The basic circuit layouts are presented and, where appropriate, the advantages and disadvantages of each are highlighted. The first candidate [9] is illustrated in Figure 1. This is a ZVS PWM buck converter topology where the auxiliary circuit consists of an active switch S_r, diodes D_r and D_2, and reactive elements L_r, C_1 and C_2. The details of operation of this circuit are not presented here but suffice it to say that the control is simple. The principle disadvantage of the circuit is that there are additional diode drops in both the forward path and the resonant path. So even though there is no additional voltage or current stress on the main switch S_1, there are important new losses to account for in the auxiliary circuitry.

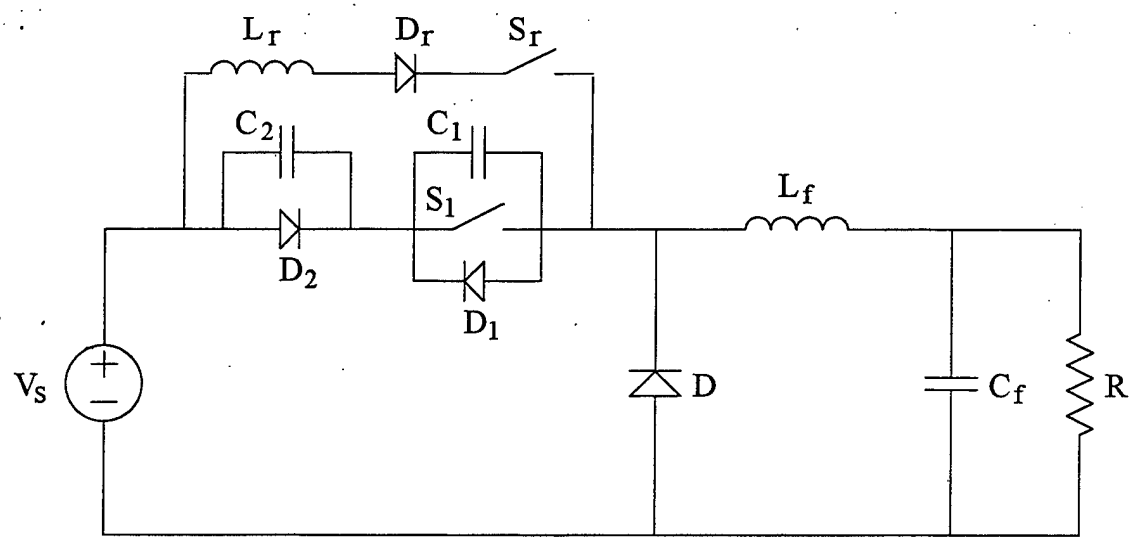


Figure 1 - Zero-Voltage-Transition PWM Buck Converter

The second candidate circuit [10] is a constant switching frequency ZVS-PWM buck converter, illustrated in Figure 2. It consists of two power switches (S_1, D_1 and S_2, D_2), two free-wheeling diodes (D_3 and D_4), a resonant inductor and capacitor (L_r and C_r) and the output filter. Its main claim of advantage is that it operates over a wide range of load with small losses. The principle disadvantages are that there are two switches in the main

path, two diodes in the freewheeling path and there is a mode in which S_2 can experience switching losses.

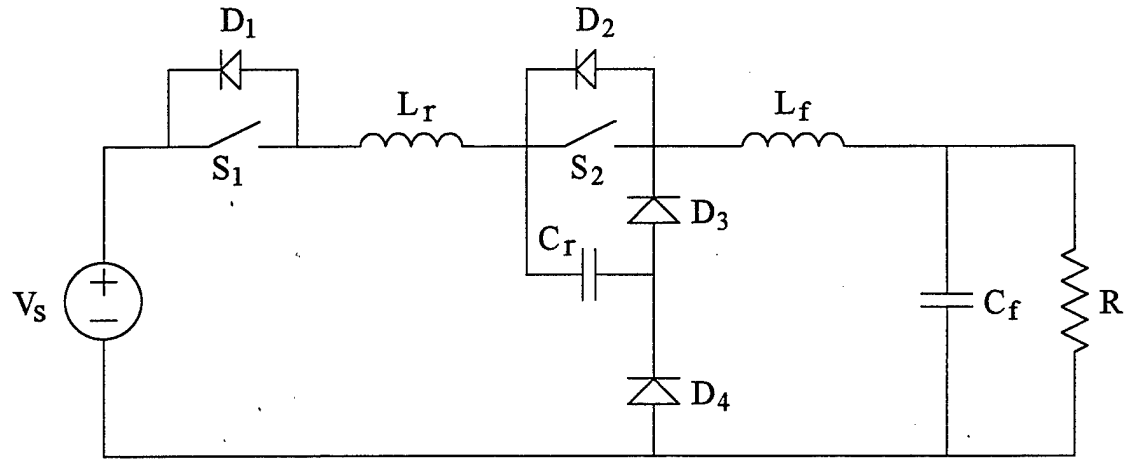


Figure 2 - ZCS-ZVS PWM Buck Converter

The next candidate circuit [11] is a constant switching frequency ZVS-PWM buck converter, illustrated in Figure 3. It differs from a conventional PWM buck by the addition of a resonant network consisting of inductor L_r, capacitor C_r, an auxiliary switch S_r, an auxiliary diode D_r and two input sources V_1 and V_2. The attractive features of the circuit are that the zero-voltage switching is independent of the load current, the voltage across the main switch is clamped to the input voltage (independent of load), and operation is at constant frequency. The main detraction is the requirement of two sources. This aspect, however, is important in DC ZEDS and thus this circuit must be discounted from further consideration.

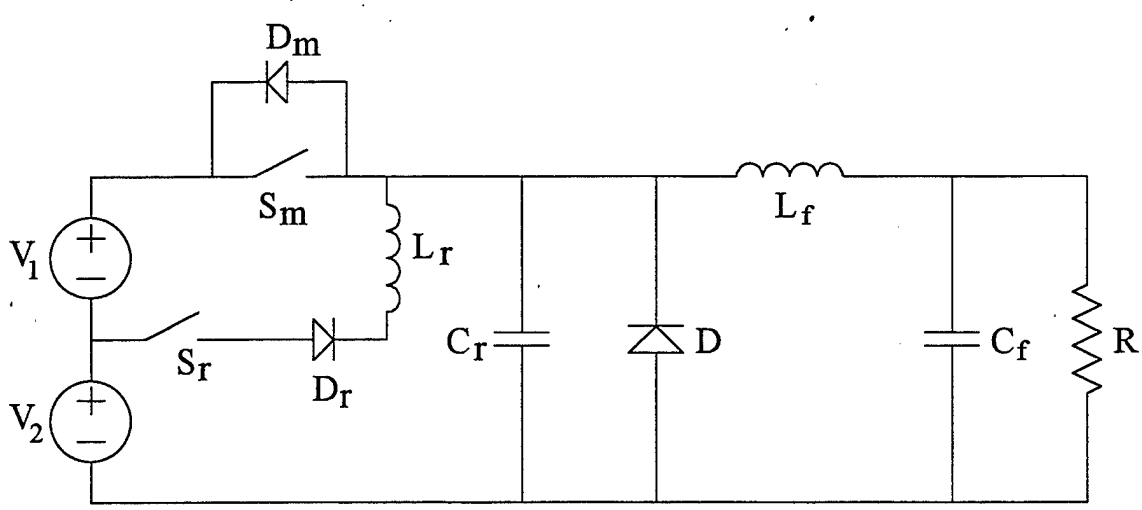


Figure 3 - Zero-Voltage-Transition PWM Converter

The fourth circuit [12] is a constant frequency ZVS quasi-resonant buck converter and is depicted in Figure 4. S_1 is the principle switch, L_r and C_r form the resonant circuit together with switch S_2. The novel feature of this circuit is that the output voltage is regulated by controlling the freewheeling period of the resonant inductor. The disadvantages include the requirement of a series diode with S_2 since the current through L_r must be bidirectional. This current freewheeling through L_r is not an optimal situation from the standpoint of losses. Also, the control for this converter is somewhat involved and the gating for the main switch must be well-timed to ensure that the circuit transitions to the correct mode. The resonant cycle is initiated by the turn-off of the main switch versus the turn-on.

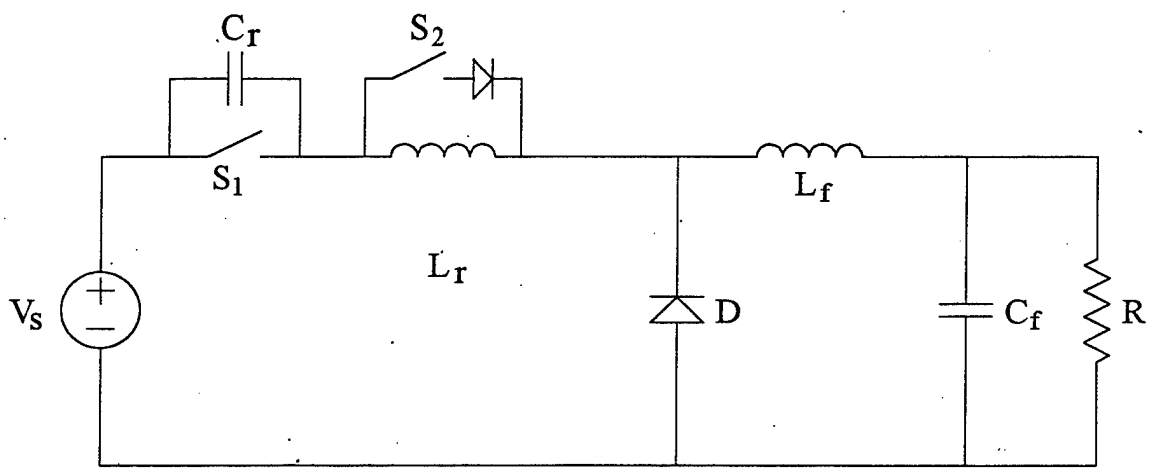


Figure 4 - ZVS Quasi-Resonant Buck Converter

The circuit illustrated in Figure 5 is the candidate topology described in [13]. This is an example of a single-switch ZVS-CV dc-dc converter. One immediate advantage of this circuit is that it is derived by simply adding components to the conventional buck circuit. Also, the requirement of a single switch is very attractive from the standpoint of control and minimizing active components. The circuit performs very well in terms of voltage stresses on the transistor and freewheeling diode. The disadvantages include the requirement of frequency control, though since only one switch is required, this is not overwhelming. The voltage control of the buck is limited to output-to-input voltage ratios extending from 0.5 to unity. As a consequence, the dynamic range of the control is quite limited and would probably not be acceptable for regulating large swinging loads. The control may also be viewed as being more "difficult" since the resonant cycle is initiated by turning the main

switch off. Thus, despite being attractive from the standpoint of part minimization, the entire control would have to be reformulated to modify existing DC ZEDS hardware.

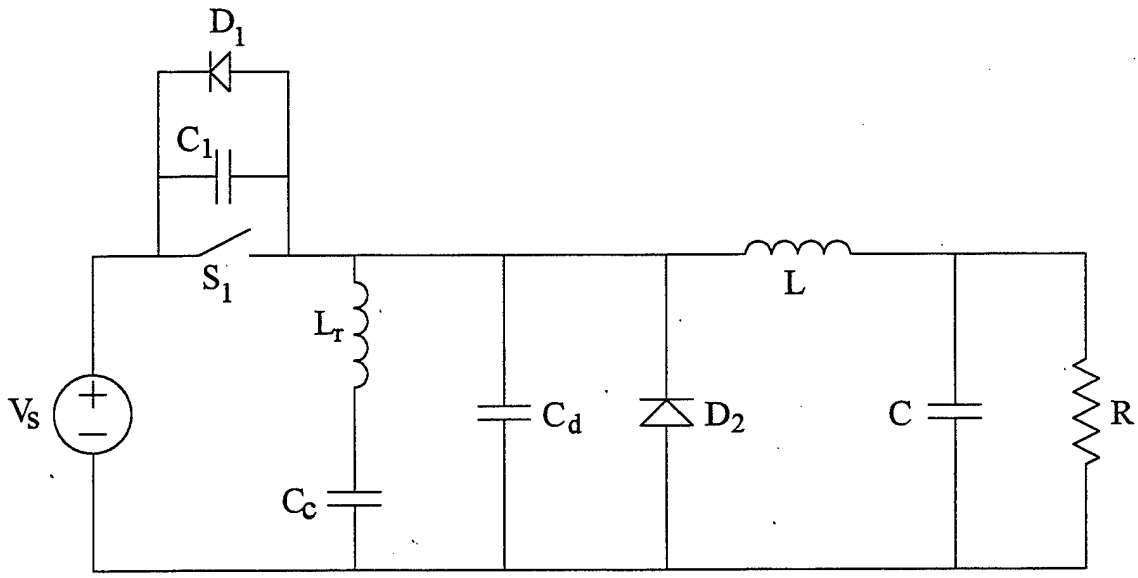


Figure 5 - Single-Switch ZVS Clamped-Voltage Buck Converter

The fifth candidate [14] is illustrated in Figure 6. This circuit is precisely the same as that described in [12] except for the inclusion of a capacitor across the main diode. The capacitor eliminates a ringing problem on the main diode but also introduces additional dynamics that must be considered in the design process. This point together with the disadvantages described with [12] eliminated this circuit as an option.

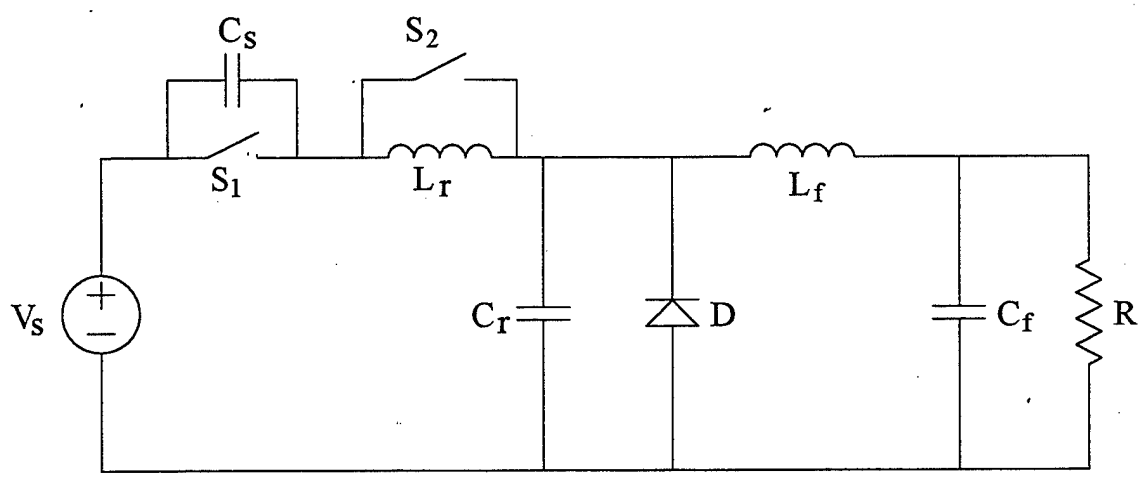


Figure 6 - PWM ZVS Multi-Resonant Converter

The sixth candidate circuit [15]-[16] is illustrated in Figure 7. This is a constant frequency PWM buck circuit which employs both ZVS and ZCS switching characteristics.

Switch S_2 is the main switch that provides the PWM operation. Switch S_1 is the auxiliary switch responsible for charging the resonant capacitor C_r. The circuit appears to have excellent characteristics with no problems regarding voltage or current stresses on the switches. It does require a series diode in the resonant circuit and the auxiliary circuit does feed off of the load and not the source. This aspect of the auxiliary circuit feeding off the load seems to be a topological departure that may be undesirable from the standpoints of feedback and isolation.

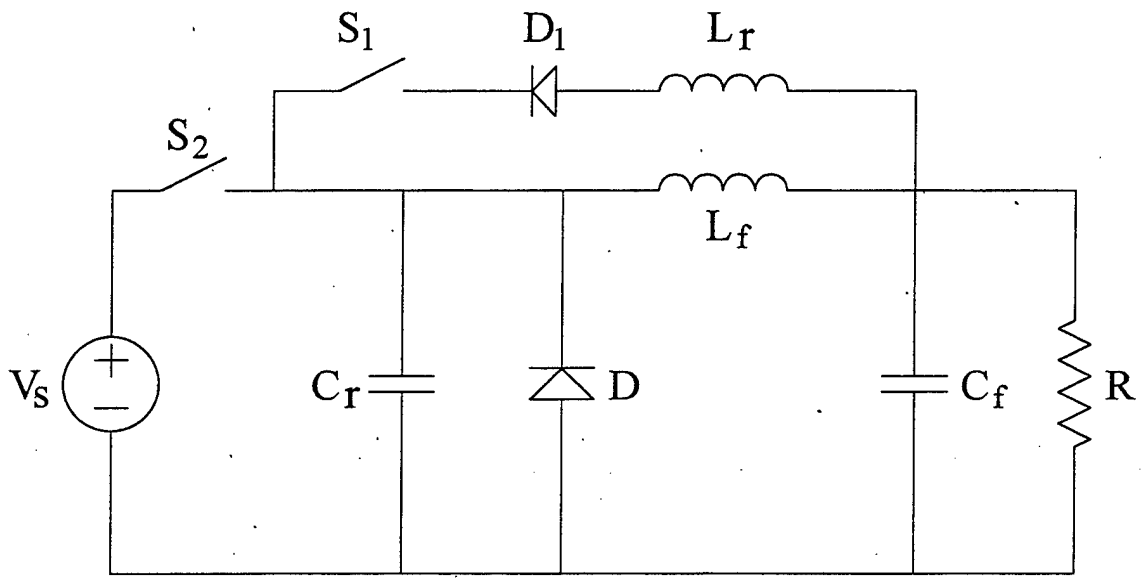


Figure 7 - ZCS-ZVS PWM Buck Converter

The final candidate circuit [17] is illustrated in Figure 8. This circuit is a fixed-frequency ZVS buck converter. Only a single source is required for operation. The resonant cycle initiates the closing of the main switch. Existing hardware can be modified to assemble the circuit. Constant switching frequency control is used. There are no wide constraints on the admissible output-to-input voltage ratio. Semiconductor switch stresses are not significantly increased. As a consequence, this circuit will be the focus of the remainder of this report.

It will be our intent to explain precisely how this circuit operates, document the equations and logic required to implement an ACSL simulation, describe representative output waveforms from this simulation, provide design specifications and analysis to aid in component selection, characterize PSPICE simulation results and set forth some additional fabrication nuances.

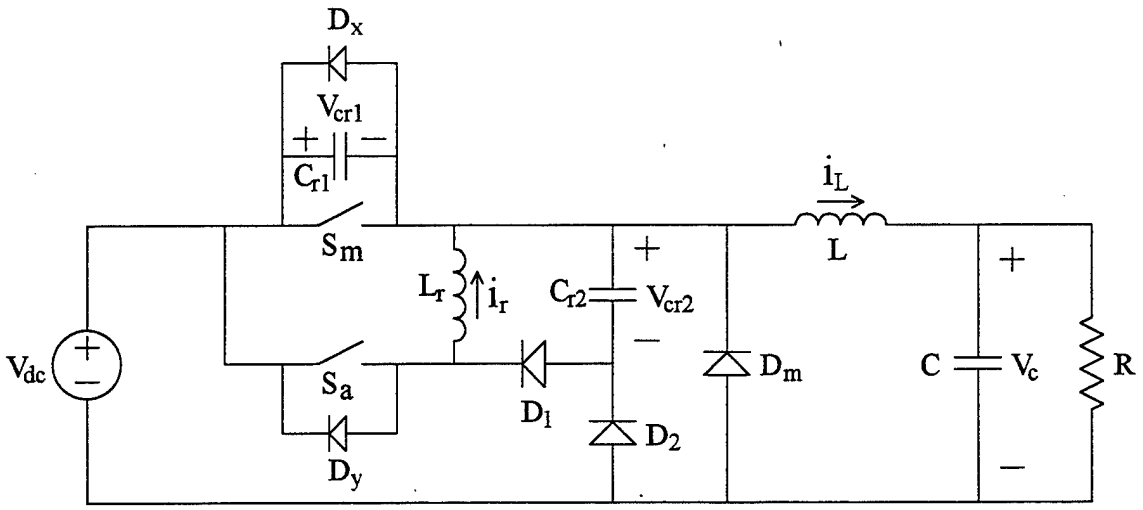


Figure 8 - ZVS PWM Buck Converter

I. Principle of Operation

The literature is replete with various topologies and switching strategies for resonant dc-dc converters [4-17]. The circuit under consideration [17] was selected owing to its simplicity and similitude to the hard-switched buck converters being evaluated by the Naval Surface Warfare Center, Annapolis Detachment. In particular, as illustrated in Figure 9, the resonant soft-switching properties are realized by inserting a number of diodes, capacitors and a single auxiliary switch into the hard-switched buck configuration. In this section, the qualitative details of operation are explained. Later sections document the modeling, simulation, design and control of a particular unit.

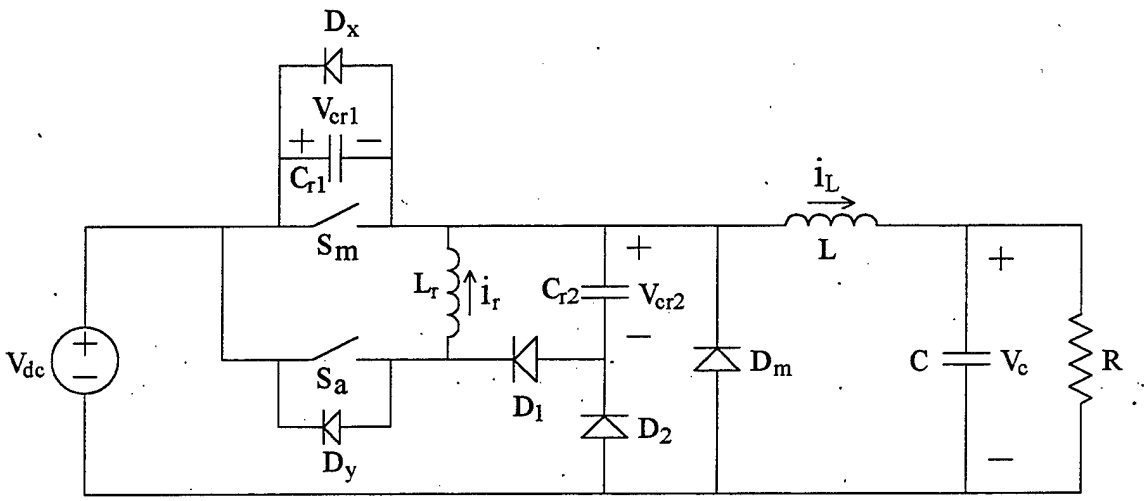


Figure 9 - Proposed Candidate Circuit [17]

The operation of the circuit is best explained by considering one steady-state switching cycle which consists of eight modes. For each mode a circuit schematic is referenced which depicts the principle path(s) of current through the various devices. In addition, the mode initial conditions and transition condition(s) are documented. Initially continuous current conduction mode is assumed. Extensions to discontinuous current conduction are addressed in a later section.

A hard-switched dc-dc buck chopper operates by cyclically closing the main switch (S_m). In voltage-mode control, a duty cycle signal specifies the portion of the switching period T_s that S_m is closed ($D = t_{on} / T_s$). While S_m is closed, the inductor current i_L builds up, charging up the output capacitor and supplying current to the load. When S_m is opened, the inductor current free-wheels through D_m, decaying linearly, and the capacitor discharges into the load. When S_m is closed, the full dc input voltage is impressed across the switch and switching losses occur. The object of the resonant converter is to realize zero voltage across S_m at the moment it is closed.

Mode 1

Mode 1 corresponds to the portion of the switching period in which the main diode D_m is conducting i_L. The current paths are documented in Figure 10 (solid lines). Note, the output capacitor voltage is at its steady-state regulated value, $V_c = DV_{dc}$, capacitor C_{r1} is charged to the input dc voltage, $V_{cr1} = V_{dc}$, capacitor C_{r2} is completely discharged, $V_{cr2} = 0\text{V}$, and there is no current flowing in the resonant inductor L_r, $i_r = 0\text{A}$. During mode 1, the inductor current is ramping downward with a negative potential of approximately $-V_c$ across it. The transition to mode 2 occurs when the inductor current is at its minimum value, $i_L = I_{L,\min}$, and the auxiliary switch, S_a, is activated.

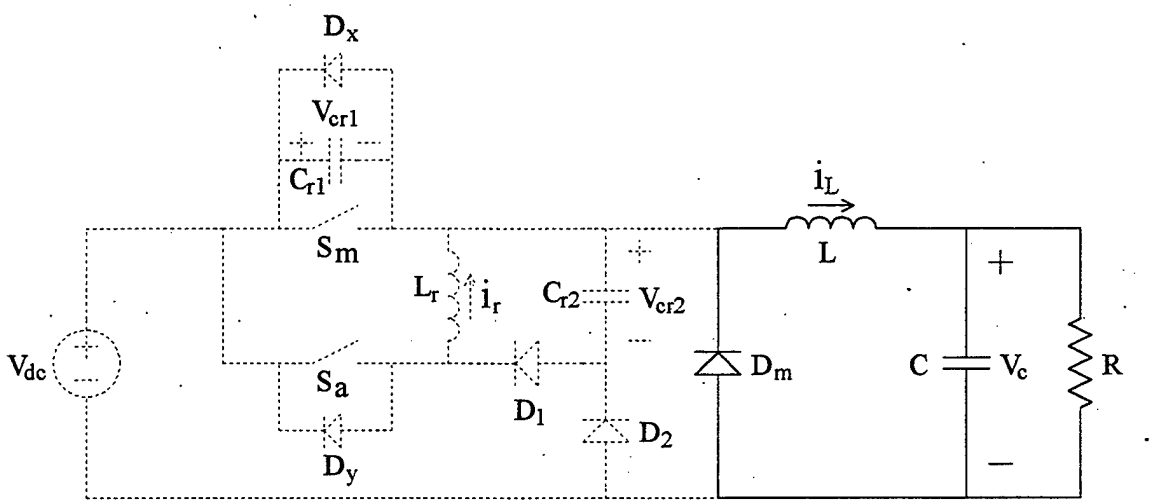


Figure10 - Circuit in Mode 1

Mode 2

With S_a closed and D_m conducting, the voltage across L_r is approximately V_{dc}. The current paths for mode 2 are illustrated in Figure 11. Since $\frac{d}{dt} i_r = V_{dc} / L_r$, the resonant inductor current ramps up quickly until $i_r = i_L$ (where i_L is still quite close to $I_{L,min}$). At this point, the main diode D_m is starved of current and turns off. With D_m off, the right node of C_{r1} is no longer common with the bottom rail and thus C_{r1} is not in parallel with V_{dc}. Therefore, V_{cr1} is now free to change as dictated by the resonant circuit.

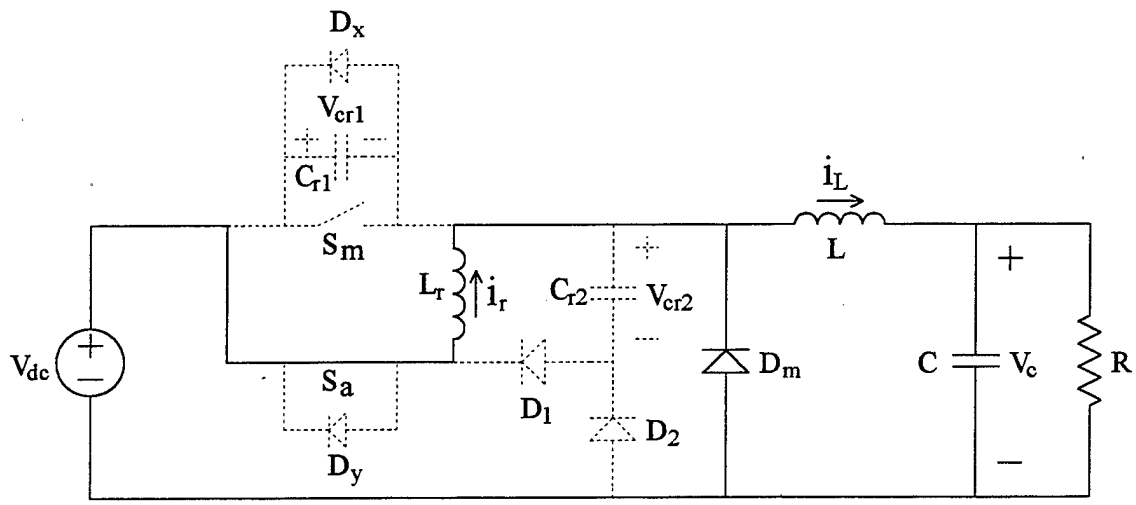


Figure 11 - Circuit in Mode 2

Mode 3

A resonant condition is now set up to enable V_{cr1} to change as illustrated in Figure 12. The initial conditions are $i_r = i_L$ and $V_{cr1} = V_{dc}$. The L_r and C_{r1} loop drives V_{cr1} down towards the new equilibrium condition of $V_{cr1} = 0\text{V}$. The diode D_x prevents V_{cr1} from resonating past approximately -1V. At this point, the near zero voltage condition on the main switch has been realized.

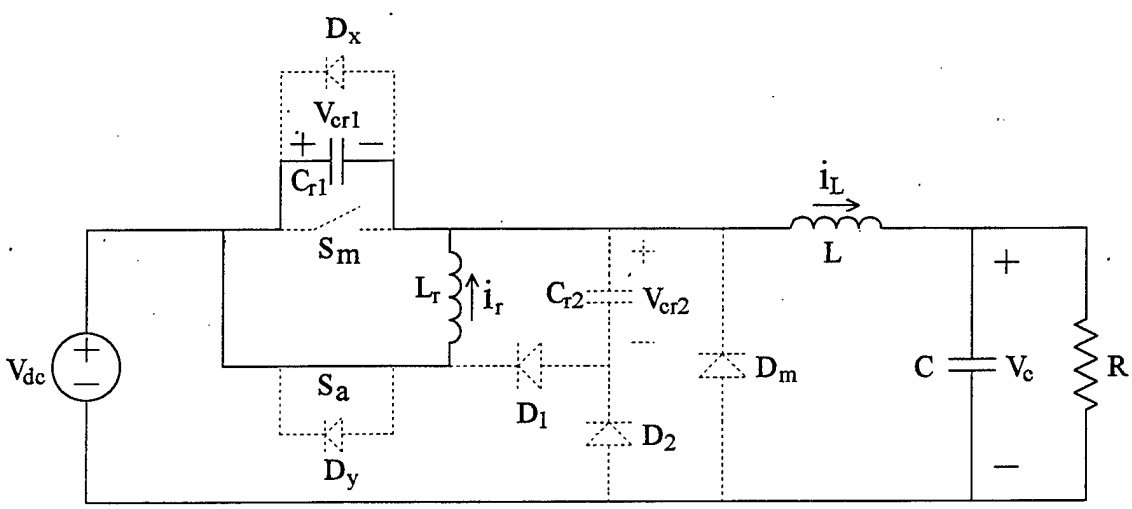


Figure 12 - Circuit in Mode 3

Once V_{cr1} obtains a slight negative charge, D_x becomes forward biased and the circuit topology of Figure 13 governs operation.

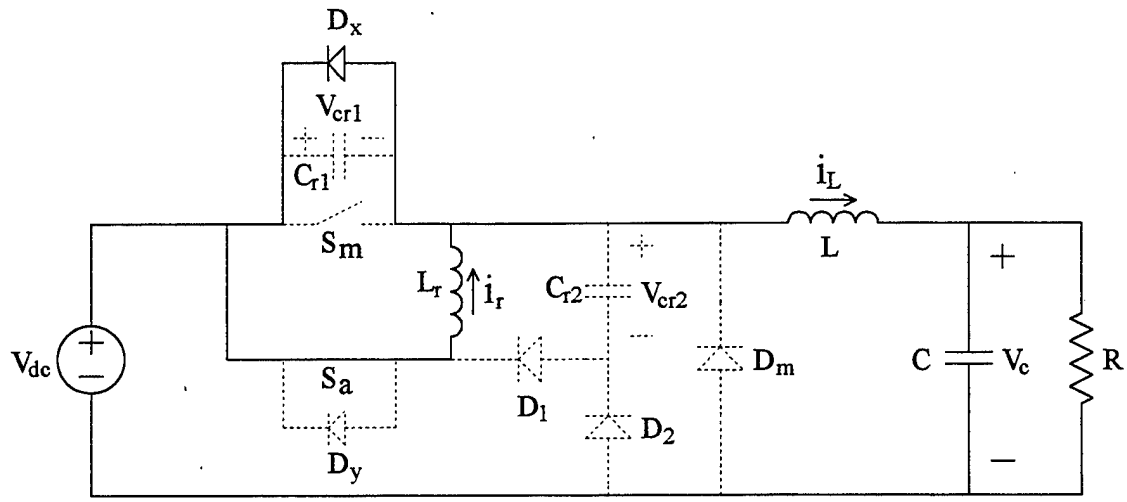


Figure 13 - Circuit with D_x Clamped On

Mode 4

The main switch, S_m, is closed with V_{cr1} at approximately zero volts. The voltage across C_{r1} is clamped at near zero volts as S_m assumes conduction of some of i_L. Also, since L_r is effectively in parallel with a conducting switch, the voltage across it is approximately zero so that i_r is held constant. This guarantees that the current build-up in S_m tracks the linear increase in current through the main inductor. The current paths are depicted in Figure 14. With S_m gated with nearly zero voltage across it, the auxiliary circuit switch may now be turned off.

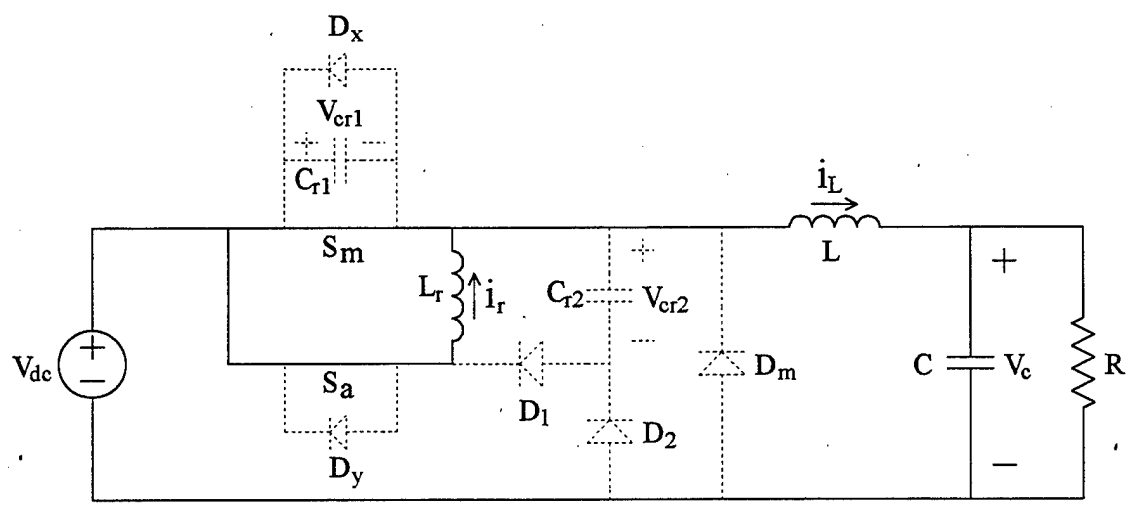


Figure 14 - Circuit Following Turn-on of S_m (Mode 4)

Mode 5

The auxiliary switch S_a is opened initiating the transfer of the remainder of i_L to the main switch S_m. This transfer is illustrated in Figure 15. Since i_r must continue to flow, diode D_1 turns on and the previously uncharged C_{r2} begins to charge. The resonant loop formed by L_r and C_{r2} drives i_r to zero then diode D_1 is current starved and C_{r2} stops charging. At this point, all of the main inductor current is being carried by S_m.

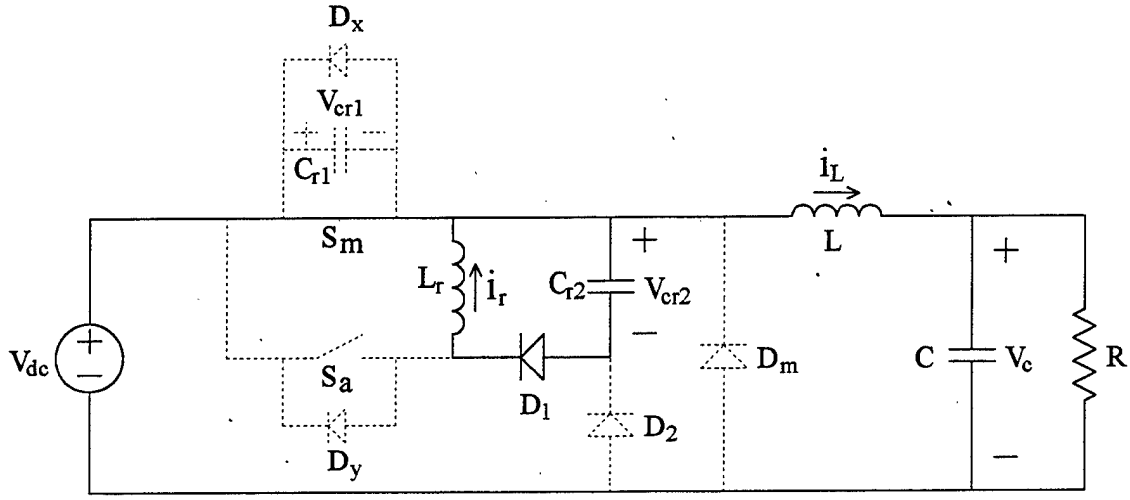


Figure 15 - Circuit in Mode 5

Mode 5x

If the charging of resonant capacitor voltage V_{cr2} attempts to exceed V_{dc}, then diode D_2 becomes forward biased. The "new" decay path for i_r is illustrated in Figure 16. With $\frac{d}{dt} i_r = -V_{dc} / L_r$, i_r quickly decays to zero while V_{cr2} is frozen at approximately V_{dc}.

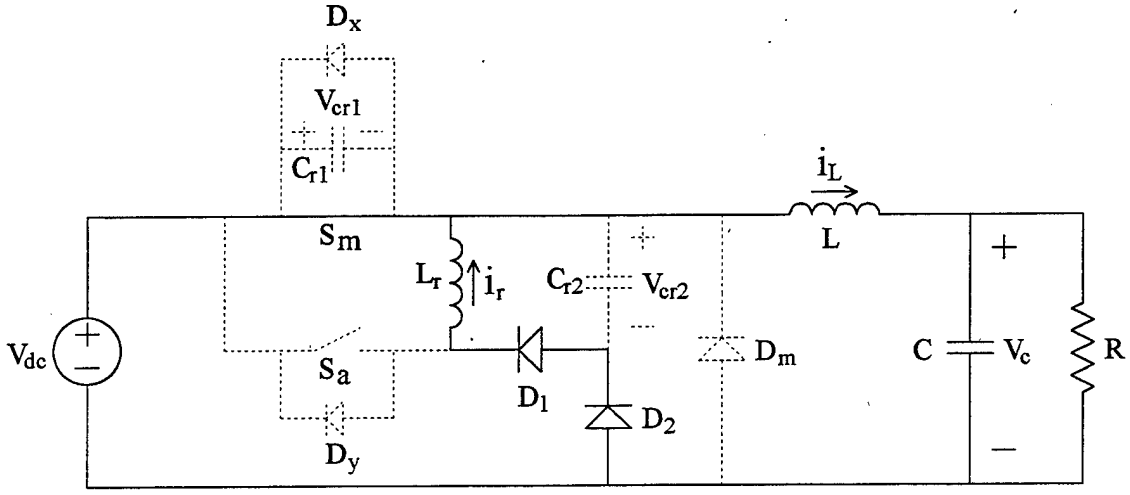


Figure 16 - Circuit in Mode 5x

Mode 6

Mode 6 corresponds to the interval of time in which the main switch S_m carries the full inductor current i_L as dictated by the duty-cycle control. The current paths are shown in Figure 17. The resonant capacitor voltage V_{cr2} has been charged to some positive voltage between 0V and V_{dc} and the resonant inductor current i_r is zero.

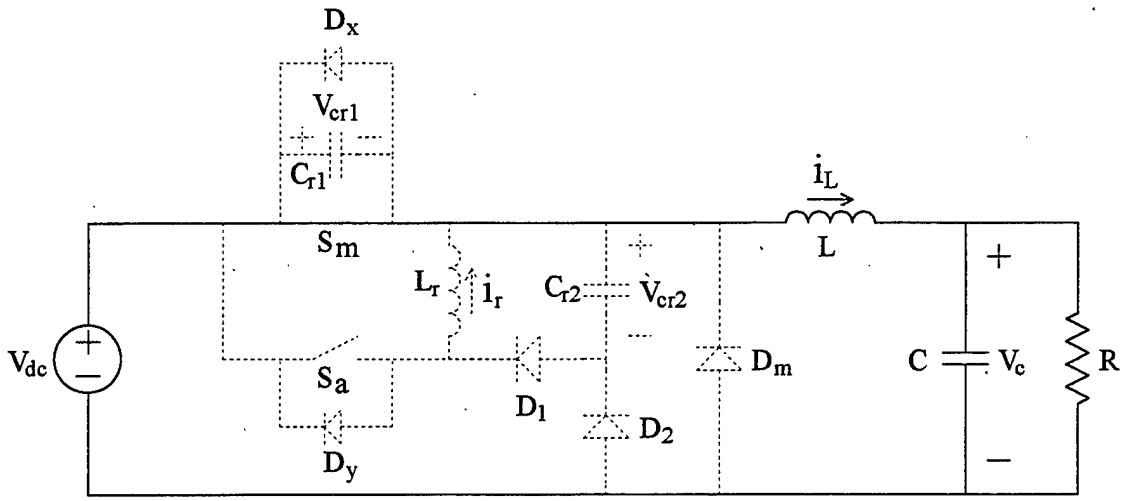


Figure 17 - Circuit in Mode 6

Mode 7 or mode 8 is initiated by opening the main switch S_m. The circuit is now transitioning to the state required for the next firing of the auxiliary switch S_a. Whether mode 7 or mode 8 is entered depends on the level to which V_{cr2} has been charged. If V_{cr2} is less than V_{dc}, then operation is described by mode 7; otherwise, operation skips to mode 8.

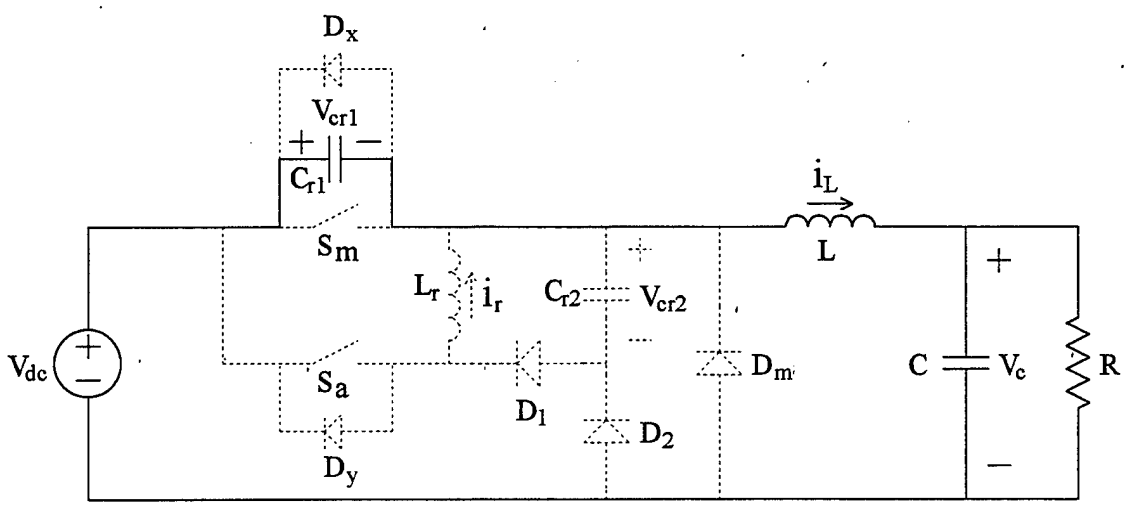


Figure 18 - Circuit in Mode 7

Mode 7

Recall, V_{cr1} is initially at approximately zero volts. When S_m is opened, the current i_L must stay continuous and therefore will flow through C_{r1}. This current path is documented in Figure 18. Since $V_{D2} = V_{cr1} + V_{cr2} - V_{dc}$, the charging of C_{r1} will eventually cause V_{D2} to go positive so that D_2 is forward biased and begins conducting. This transitions operation to Mode 8.

Mode 8

With $V_{D2} = V_{cr1} + V_{cr2} - V_{dc}$ and C_{r1} charging, D_2 begins conducting and the governing circuit is illustrated in Figure 19. Since Kirchhoff's Current Law demands that $V_{cr1} + V_{cr2} = V_{dc}$, as C_{r1} is charging, C_{r2} must be discharging. Mode 8 completes when V_{cr1} charges slightly past V_{dc} and V_{cr2} is approximately zero.

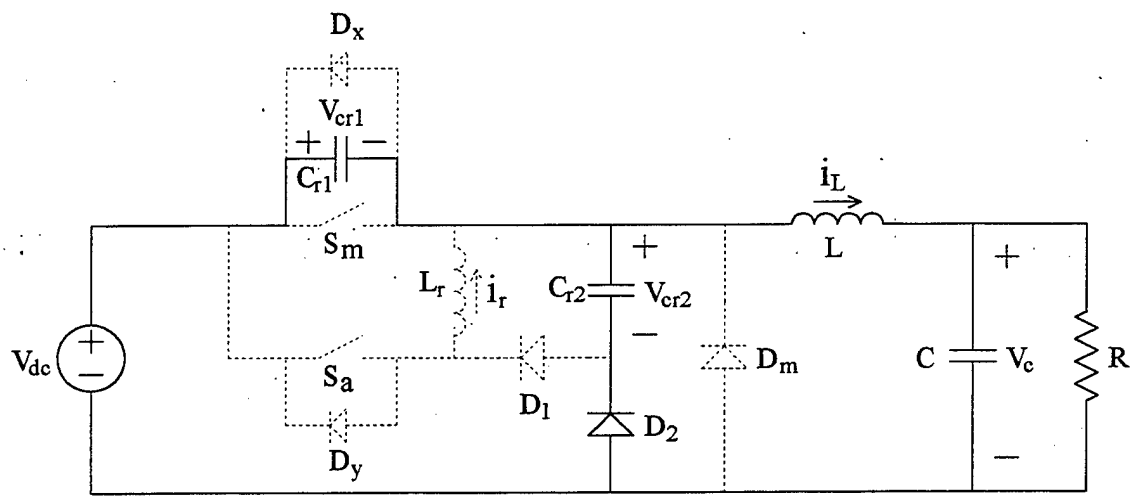


Figure 19 - Circuit in Mode 8

Mode 1 is re-initiated once V_{cr1} charges slightly past V_{dc} and the main diode D_m becomes forward biased since $V_{Dm} = V_{cr1} - V_{dc}$. Based also on the fact that with $V_{cr1} + V_{cr2} = V_{dc}$, implying that C_{r2} is discharged, all of the inductor current i_L is transferred to D_m. The current paths are highlighted in Figure 20. The next cycle is now ready to take place as $V_{cr2} = 0\text{V}$, $i_r = 0\text{A}$ and $V_{cr1} = V_{dc}$.

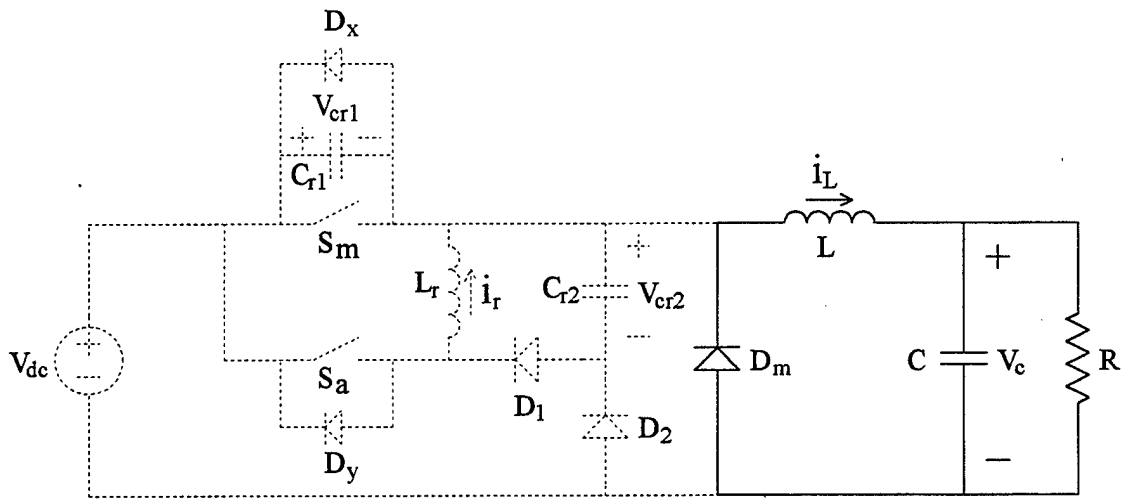


Figure 20 - Circuit in Mode 1

II. Dynamic Modeling of Modes

Each of the eight modes previously described are governed by a set of differential equations prescribed by the circuit configuration. The transitions between modes are specified by conditions on the network state variables. This section documents the state equations for each mode and sets forth each transition constraint.

For the circuit under consideration [17], the state variables correspond to the currents or voltages of the five energy storage elements. In particular, i_L, V_c, V_{cr1}, V_{cr2}, and i_r are the state variables. All equations are derived assuming zero switch and diode conduction drops, ideal inductors and capacitors, and a stiff dc input voltage source. The following equations describe the corresponding dynamics for each mode.

Mode 1

The dynamics are derived by analyzing the circuit depicted in Figure 10.

$$\frac{d}{dt} i_L = -\frac{V_c}{L} \tag{2.1}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.2}$$

$$\frac{d}{dt} i_r = 0 \tag{2.3}$$

$$\frac{d}{dt} V_{cr1} = 0 \tag{2.4}$$

$$\frac{d}{dt} V_{cr2} = 0 \tag{2.5}$$

For the quantities not changing, they are held at the values achieved at the end of mode 8. The circuit transitions to mode 2 when a gating signal is applied to the auxiliary switch S_a. This signal is synchronized with the clocking signal used to activate the main switch in a later mode.

Mode 2

The dynamics are derived by analyzing the circuit depicted in Figure 11.

$$\frac{d}{dt} i_L = -\frac{V_c}{L} \tag{2.6}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.7}$$

$$\frac{d}{dt} i_r = \frac{V_{dc}}{L_r} \tag{2.8}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{2.9}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{2.10}$$

These equations govern circuit operation up until $i_r = i_L$. At this point, the circuit transitions to mode 3 operation.

Mode 3

The dynamics are derived by analyzing the circuit depicted in Figure 12.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c - V_{cr1}}{L} \tag{2.11}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{2.12}$$

$$\frac{d}{dt}i_r = \frac{V_{cr1}}{L_r} \tag{2.13}$$

$$\frac{d}{dt}V_{cr1} = \frac{i_L - i_r}{C_{r1}} \tag{2.14}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{2.15}$$

The initial condition of V_{cr1} is approximately V_{dc} as set by a subsequent mode. Also, diode D_x constrains V_{cr1} from going negative. Thus, V_{cr1} must be monitored for this condition in order for the circuit to correctly transition to mode 4.

Mode 4

Mode 4 is initiated when either $V_{cr1} = 0\,V$ (if that condition is used in the control) or when the main switch is closed as dictated by the duty-cycle control. The dynamics are derived by analyzing the circuit depicted in either Figure 13 or 14.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c}{L} \tag{2.16}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{2.17}$$

$$\frac{d}{dt}i_r = 0 \tag{2.18}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{2.19}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{2.20}$$

The current through the main switch is given by

$$i_{sm} = i_L - i_r \tag{2.21}$$

Mode 5

Mode 5 is initiated when the auxiliary switch is turned off. The turn off may be specified based on some sensed variable or based simply on a timing criterion (more on this later). The dynamics are derived by analyzing the circuit depicted in Figure 15.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \tag{2.22}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.23}$$

$$\frac{d}{dt} i_r = -\frac{V_{cr2}}{L_r} \tag{2.24}$$

$$\frac{d}{dt} V_{cr1} = 0 \tag{2.25}$$

$$\frac{d}{dt} V_{cr2} = \frac{i_r}{C_{r2}} \tag{2.26}$$

These dynamics govern up until i_r decays to zero or if V_{cr2} increases up to V_{dc}, then the circuit transitions to mode 5x.

Mode 5x

If V_{cr2} tries to go above V_{dc} then

$$\frac{d}{dt} V_{cr2} = 0 \tag{2.27}$$

so that

$$V_{cr2} = V_{dc} \tag{2.28}$$

Also as shown in Figure 16,

$$\frac{d}{dt} i_r = -\frac{V_{dc}}{L_r} \tag{2.29}$$

This mode persists up until i_r goes to zero.

Mode 6

Mode 6 is entered once i_r goes to zero and the governing equations are found upon inspection of Figure 17.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \tag{2.30}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.31}$$

$$\frac{d}{dt} i_r = 0 \tag{2.32}$$

$$\frac{d}{dt} V_{cr1} = 0 \tag{2.33}$$

$$\frac{d}{dt} V_{cr2} = 0 \tag{2.34}$$

For the above, V_{cr2} is held at some positive value between zero and V_{dc} and i_r is held at zero. These equations hold until the main switch is opened.

Mode 7

If V_{cr1} is less than V_{dc}, then the state variable dynamics are given by analysis of Figure 18.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c - V_{cr1}}{L} \tag{2.35}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.36}$$

$$\frac{d}{dt} i_r = 0 \tag{2.37}$$

$$\frac{d}{dt} V_{cr1} = \frac{i_L}{C_{r1}} \tag{2.38}$$

$$\frac{d}{dt} V_{cr2} = 0 \tag{2.39}$$

These equations hold up until $V_{cr1} + V_{cr2} = V_{dc}$. At which point, D_2 begins conducting and the circuit transitions to the next mode.

Mode 8

The dynamic equations are found by analysis of Figure 19.

$$\frac{d}{dt} i_L = \frac{V_{cr2} - V_c}{L} \tag{2.40}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{2.41}$$

$$\frac{d}{dt} V_{cr1} = \frac{i_L}{C_{r1} + C_{r2}} \tag{2.42}$$

$$\frac{d}{dt} i_r = 0 \tag{2.43}$$

Since V_{cr2} is algebraically related to state and input as shown in Figure 19, it is constrained by

$$V_{cr2} = V_{dc} - V_{cr1} \tag{2.44}$$

These equations govern operation up until $V_{cr1} = V_{dc}$. That transition condition then moves operation back to mode 1.

This section has set forth the dynamic equations for the individual modes together with the transition conditions. The next section outlines how these equations are incorporated into a dynamic ACSL simulation.

III. ACSL Dynamic Simulation

In most instances, an ACSL representation of a power converter employs simplifying assumptions in modeling switching elements such as transistors or diodes. The conduction voltages and reverse currents are typically orders of magnitude smaller than the converter input/output voltages and currents. As a result, a conducting transistor or diode is modeled as a short circuit (or with a small voltage drop and/or small resistance) and a non-conducting transistor or diode is modeled as an open circuit (or a large resistance). Thus, the ACSL simulation is more focussed on representing the input/output characteristics of the circuit and is not intended to faithfully reproduce switch behavior or quantify switching losses. Such device-level nuances, which are critical in a design, are more appropriately studied with a software package like PSPICE. The ACSL simulation enables quick study of issues relating to control, the sizing of circuit parameters, and the investigation of gross waveforms during steady-state and transient conditions.

In modeling a network such as the soft-switching buck chopper, the first steps are to understand how the circuit is intended to be operated and identify the individual "modes" that govern operation. The equations governing each mode are then set forth together with the necessary conditions required to enter the mode. Often times auxiliary devices such as small capacitors, small inductances or large resistances must be inserted into a network to either arrive at a consistent set of equations of in order to establish voltages or currents required for the transitioning logic. For example, establishing the forward bias of a diode or determining when the current flowing through an SCR drops below the holding current. The keys then are to not miss any modes and to correctly program the transition between modes.

For the circuit under consideration [17], it was found that no anciliary devices were required for the simulation. The network state variables togther with the switch actuation signals were sufficient to uniquely identify the required modes of operation. The following hierarchy of logic was used: the conduction status for the main and auxiliary switches were based on an oscillator signal which was simply a function of time, the conduction status of the three diodes was determined based on the switch status and the state variables, the conduction status of the switches and diodes was then used to program the circuit mode of operation, and knowing the circuit mode, the correct set of differential equations could be assigned and numerically integrated.

A ramp waveform at the desired switching frequency was generated with an amplitude which ranged from zero to the switching period. Three times (t_α, t_β and t_γ) were then used to fix the main and auxiliary switching instances. As the ramp resets to zero, the auxiliary switch is gated, initiating the cycle. Upon hitting the first specified time, t_α, the main switch is closed. The second specified time, t_β, turns off the auxiliary switch and the

third specified time, t_γ, turns off the main switch. Each of these times, of course, could be made part of the feedback control and could be functions of the state or circuit variables. For instance, if V_{cr1} has not been sufficiently discharged so that zero volts exist across the main switch, then t_α may be suppressed so that S_m is not gated and destroyed. The logical variable *dutym* represents the conduction status of the main switch (TRUE is conducting and FALSE is non-conducting) while logical variable *dutya* represents the conduction status of the auxiliary switch.

The next phase of modeling entailed identifying the conditions necessary for each diode to begin conducting and to cease conducting. It was decided to not utilize SCHEDULE statements to do this but instead to formulate an IF-THEN-ELSE construct. This sacrifices some precision since the exact moment of the penetration of a boundary condition may be slightly off. Subsequent simulation studies confirmed that the roundoff error was trivial and further motivated avoidance of the added complexity of the SCHEDULE statements. The error is minimized by selecting a suitably small integration time step (maxt).

The main diode conducts when both switches are open and the voltage V_{cR1} is greater than the input dc voltage. If the main switch is conducting, the dc voltage reverse biases the main diode, and it shuts off. Also, the main diode stops conducting if the auxiliary switch is on, the main switch is off and the resonant current has ramped up to the value of the main inductor current (effectively starving it of current). Diode D_1 conducts when the main switch is closed, the auxiliary switch is open and the resonant inductor current is flowing. This diode then turns off when that current attempts to go negative. Diode D_2 turns on under two situations. First, if the main switch is conducting and V_{cR2} is greater than the input voltage, then D_2 is forward biased. Second, if neither switch is on, diode D_m is not forward biased by V_{cR1}, and $V_{cR1} + V_{cR2}$ is greater than the input dc voltage, then D_2 is forward biased and will be conducting. Diode D_2 stops conducting either when D_m begins conducting or when the main switch is gated and the resonant inductor current i_r drops to zero.

The above conditions can be arranged in the following IF-THEN-ELSE construct where the variables *Dmcond*, *D1cond*, and *D2cond* represent the conduction status of D_m, D_1 and D_2, respectively.

```
IF (dutym) THEN
        Dmcond = .FALSE.
        IF (VcR2 .GE. Vdc) THEN
                D2cond = .TRUE.
        ENDIF
        IF (iR .LE. 0.0) THEN
```

```
                    D2cond = .FALSE.
                    IF (.NOT.(dutya)) THEN
                              D1cond = .FALSE.
                    ENDIF
          ELSE
                    IF (.NOT.(dutya)) THEN
                              D1cond = .TRUE.
                    ENDIF
          ENDIF
ELSE
          IF ((iR .GE. iL) .AND. (dutya)) THEN
                    Dmcond = .FALSE.
          ENDIF
          IF (.NOT.(dutya)) THEN
                    IF (VcR1 .GE. Vdc) THEN
                              Dmcond = .TRUE.
                              D2cond = .FALSE.
                    ELSE
                              Dmcond = .FALSE.
                              IF ((Vcr1+VcR2).GE.Vdc) THEN
                                        D2cond = .TRUE.
                              ENDIF
                    ENDIF
          ENDIF
ENDIF
```

The actuation signals for the main and auxiliary switches are functions of time and the conduction of diodes D_m, D_1 and D_2 are functions of the switch conduction and the state variables. Once the conduction status of each of these five devices is identified, the particular mode of operation may be found. This is accomplished by using another IF-THEN-ELSE construct. SCHEDULE statements would unduly complicate the program. The logic is listed below where the integer variable *mode* specifies the resultant configuration. Mode 5x is renamed mode 9 for convenience.

```
IF (dutym) THEN
          IF (dutya) THEN
                    mode = 4
          ELSE
                    IF (D2cond) THEN
                              mode = 9
                    ELSE
                              IF (D1cond) THEN
                                        mode = 5
                              ELSE
                                        mode = 6
                              ENDIF
```

```
                    ENDIF
          ENDIF
ELSE
          IF (dutya) THEN
                    IF (Dmcond) THEN
                              mode = 2
                    ELSE
                              mode = 3
                    ENDIF
          ELSE
                    IF (Dmcond) THEN
                              mode = 1
                    ELSE
                              IF (D2cond) THEN
                                        mode = 8
                              ELSE
                                        mode = 7
                              ENDIF
                    ENDIF
          ENDIF
ENDIF
```

The remainder of the program implements the appropriate state equations based on the identified mode. That is, given the mode, the appropriate set of differential equations are set forth. Note, that the equation for $\frac{d}{dt} V_c$ is the same for each mode so this equation may be included outside and separate of the the various IF constructs.

```
IF (mode .EQ. 1) THEN
          diL  = -Vc/L
          diR  = 0.0
          dVcR1 = 0.0
          dVcR2 = 0.0
ENDIF
IF (mode .EQ. 2) THEN
          diL  = -Vc/L
          diR  = Vdc/LR
          dVcR1 = 0.0
          dVcR2 = 0.0
ENDIF
IF (mode .EQ. 3) THEN
          diL  = (Vdc-Vc-VcR1)/L
          diR  = VcR1/LR
          dVcR1 = (iL - iR)/CR1
          dVcR2 = 0.0
ENDIF
IF (mode .EQ. 4) THEN
```

```
            diL   = (Vdc-Vc)/L
            diR   = 0.0
            dVcR1 = 0.0
            dVcR2 = 0.0
ENDIF
IF (mode .EQ. 5) THEN
            diL   = (Vdc-Vc)/L
            diR   = -VcR2/LR
            dVcR1 = 0.0
            dVcR2 = iR/CR2
ENDIF
IF (mode .EQ. 9) THEN
            diL   = (Vdc-Vc)/L
            diR   = -Vdc/LR
            dVcR1 = 0.0
            dVcR2 = 0.0
ENDIF
IF (mode .EQ. 6) THEN
            diL   = (Vdc-Vc)/L
            diR   = 0.0
            dVcR1 = 0.0
            dVcR2 = 0.0
ENDIF
IF (mode .EQ. 7) THEN
            diL   = (Vdc-Vc-VcR1)/L
            diR   = 0.0
            dVcR1 = iL/CR1
            dVcR2 = 0.0
ENDIF
IF (mode .EQ. 8) THEN
            diL   = (VcR2-Vc)/L
            diR   = 0.0
            dVcR1 = iL/(CR1+CR2)
            dVcR2 = -iL/(CR1+CR2)
ENDIF
dVc   = (iL-(Vc/R))/C
```

In ACSL, the differential equations are then numerically integrated via a user-specified algorithm. The following 'integration' statements are required:

```
iL   = INTEG(diL, iLic)
Vc   = INTEG(dVc, Vcic)
iR   = INTEG(diR, iRic)
VcR1 = LIMINT(dVcr1,vcR1ic,0.0,1.0e6)
VcR2 = INTEG(dVcR2, VcR2ic)
```

where iLic, Vcic, iRic, VcR1ic and VcR2ic are the initial conditions of the state variables.

The LIMINT statement is required for V_{cR1} since that capacitor voltage is restricted from going negative by the diode D_x.

A simulation was developed and evaluated for a representative system operating open loop. The parameters listed in Table 1 were used in the subsequent studies.

Table 1. Parameters Used in Preliminary ACSL Simulations

$L = 42.5\,mH$	$C = 400\,\mu F$	$L_r = 1.4\,mH$	$C_{r1} = 0.1\,\mu F$
$C_{r2} = 1.0\,\mu F$	$V_{dc} = 50\,V$	$R = 19\,\Omega$	$f_{sw} = 2\,kHz$

In terms of gating signals, it is assumed that the auxiliary switch is activated at the beginning of the switching interval, $t_\alpha = \frac{T_{sw}}{5}$, $t_\beta = \frac{T_{sw}}{4}$, and $t_\gamma = \frac{7\,T_{sw}}{10}$. That is with the fundamental switching period of 500 µsec, the main switch is fired 100 µsec after the auxiliary switch, the auxiliary switch is turned off 25 µsec later and the main switch is left on for a total of 250 µsec. The length of time the auxiliary switch is gated prior to turning on the main switch is exaggerated together with the size of the resonant circuit parameters in order to illustrate the circuit modes of operation.

The first study was conducted using the fourth-order Runge-Kutta integration algorithm with a time step of *maxt = 1.0e-7*. The simulation was run until steady state (approximately 0.1sec) and then one switching cycle of data was collected. The waveforms are illustrated in Figures 21 and 22. In Figure 21, the switch actuation signals are shown together with the current mode of operation of the converter. In Figure 22, the five state variables are depicted. The circuit is initially shown operating in mode 1, the main diode is conducting and both switches are open. At approximately 0.1015sec, the auxiliary switch is energized and i_r rapidly builds to the value of i_L (mode 2). The capacitor voltage across the main switch, V_{cr1}, then resonates down towards zero volts (mode 3). Once V_{cr1} hits zero volts, diode D_x turns on and i_r is held at approximately 2A till 0.1016sec at which point the main switch is activated (mode 4). The auxiliary switch is turned off 25 µsec later (mode 5) and V_{cr2} begins to rapidly charge up to V_{dc} while i_r decays down towards zero. At about 0.10165, V_{cr2} is completely charged and operation switches to mode 5x (mode 9). The resonant inductor current eventually falls to zero and the circuit transitions to mode 6. Now the main switch carries the full inductor current. Since V_{cr2} has charged to V_{dc}, the circuit next enters mode 8 at approximately 0.10185sec when the main switch is opened. At this point, capacitor C_{r1} is charging while capacitor C_{r2} is discharging. The circuit re-eneters mode 1 when V_{cr1} has charged sufficiently to forward-bias the main diode.

The simulation was structured so that the various resonant phenomenon were visible within a single switching cycle. Obviously, the resonant parameters should be selected much smaller so that the resonant intervals are but a fraction of the cycle. The point of the simulation was to further illustrate the modes of operation and demonstrate how ACSL could be used to predict system dynamics. A discussion on how to assemble more representative component values is presented in a subsequent section. An interesting point to note is that despite the fact that the main switch is operating with a duty cycle of 0.5, the output voltage is actually greater than $\frac{V_{dc}}{2}$. This occurs because the resonant cycle is a large part of the overall switching cycle. In particular, modes 3 and 4 constitute additional charging modes in addtion to the actual time that the main switch is closed. Thus, the effective "on" time of the main switch is lengthened by these modes and the output voltage is anticipated to be higher. If we desire that the duty cycle of the main switch control the output voltage, then the resonant circuit should be designed to minimize the time in modes 3 and 4.

A second study was conducted in which the load resistance was made much larger, $R = 95\,\Omega$. Once again the converter was run till the steady state and data collected from a switching cycle. The results are illustrated in Figures 23 and 24. Shortly after 0.1014sec, the converter transitions to mode 1 where the main diode conducts the inductor current. Then at 0.1015sec, the auxiliary switch is activated and i_r quickly builds to i_L. Here we notice that since the inductor current is much smaller, the converter remains only briefly in mode 2. Next, C_{r1} resonates down to zero volts. This time is independent of the load situation as documented in the subsequent analysis. The converter then operates for a substantial amount of time with i_r freewheeling through diode D_x. The main switch closes at 0.1016sec and 25 µsec later the auxiliary switch is opened. During mode 5, the capacitor voltage V_{cr2} builds but does not reach V_{dc} before i_r decays to zero. Thus, for this situation, the circuit does not enter mode 5x (mode 9). The circuit then operates normally in mode 6 with the main switch conducting all of the main inductor current. When the main switch opens at 0.10185sec, the circuit briefly enters mode 7 since V_{cr2} is not at V_{dc}. The voltage V_{cr1} charges up to the level of V_{cr2} transitioning the circuit to mode 8. At this point, V_{cr1} continues charging up to V_{dc} while V_{cr2} decays back to zero.

Once again, it is clear from the plot of V_c that the 50% duty cycle of the main switch is not resulting in the output voltage being $\frac{V_{dc}}{2}$. The extended period of time in mode 3 results in a substantially larger effective duty cycle and the voltage rises above 35V. This effect can be minimized by proper design of the auxiliary circuitry.

The ACSL simulation appears to offer a very convenient tool for assessing the current through and voltage across the various network components. This is particularly useful for

the proper selection of device ratings. In addition, the simulation facilitates the examination of the timing of the gating signals which is another crucial issue.

A simulation tool is very useful in the design process; however, engineering judgment often times supercedes the iterative simulation process. The next section reports on the analysis of the converter from a design perspective. It outlines the approximate governing equations and sets forth a rationale for selecting component values. In addition, it lays out the design of a higher-voltage higher-switching frequency resonant buck chopper.

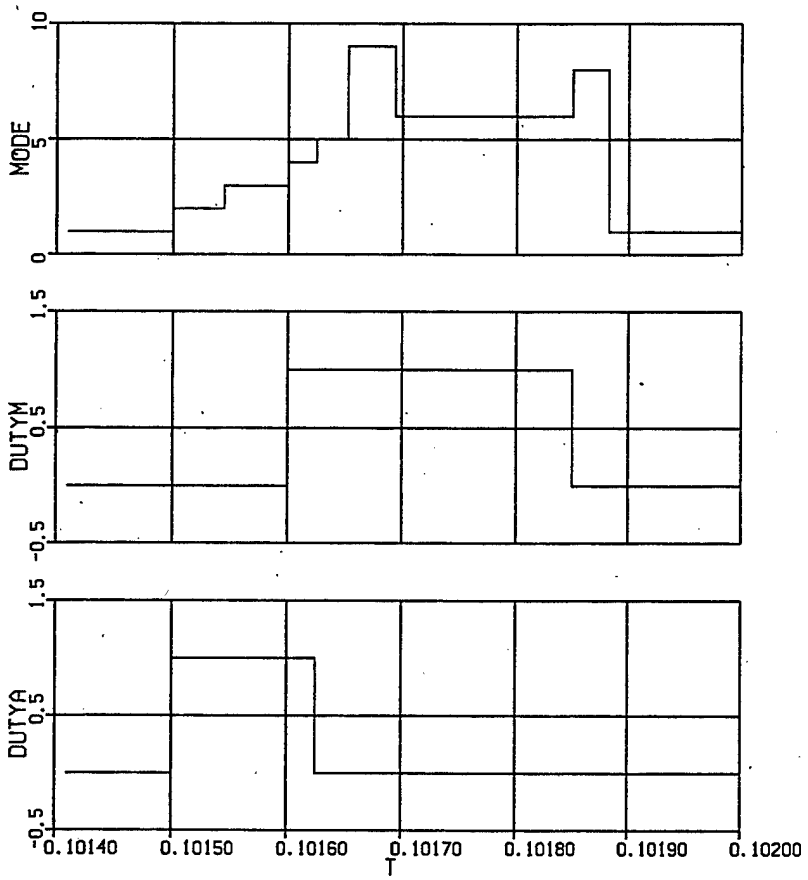


Figure 21 - Switch Actuation Signals and Converter Mode of Operation (R=19Ω)

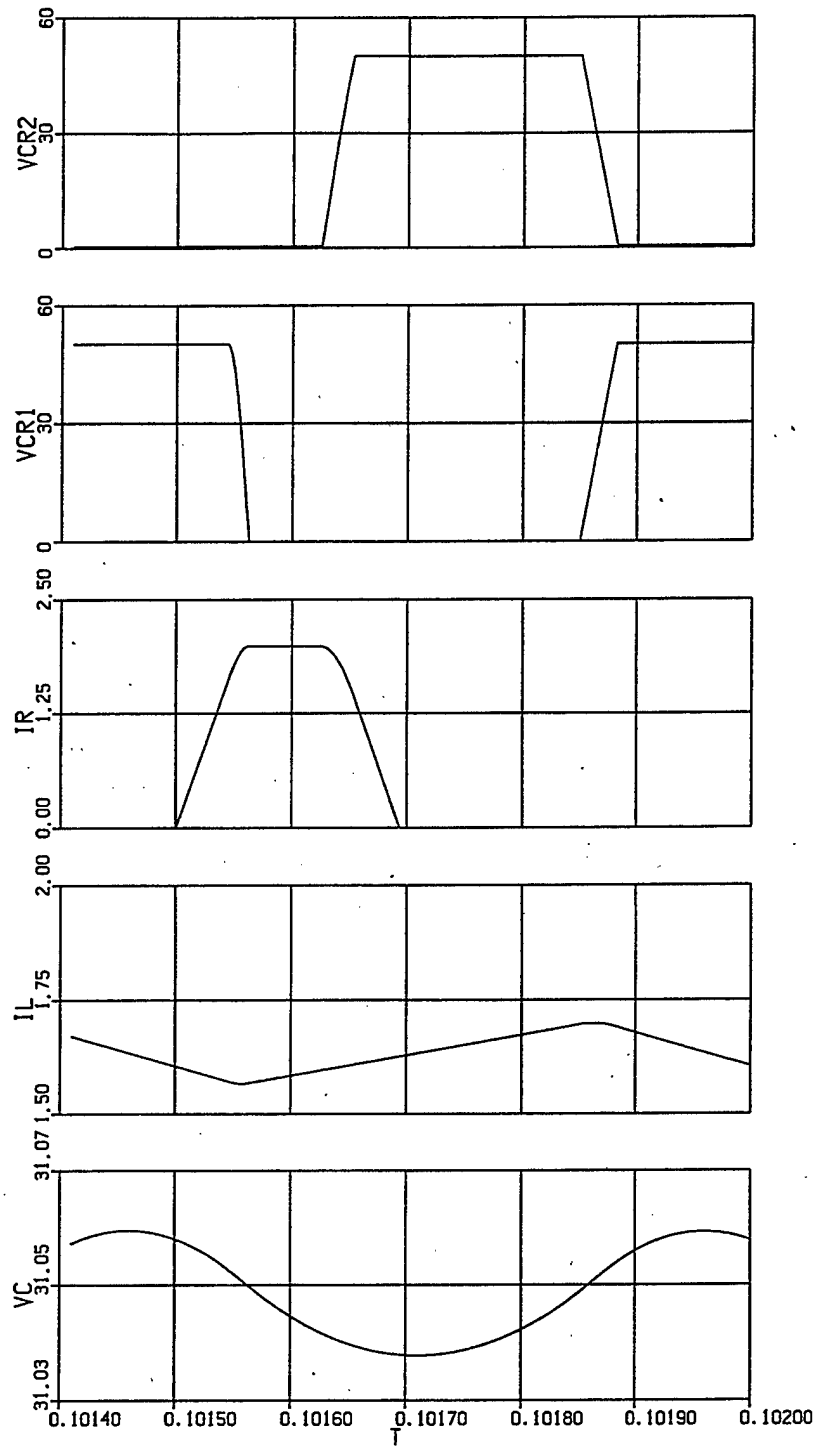


Figure 22- Converter State Variables (R=19Ω)

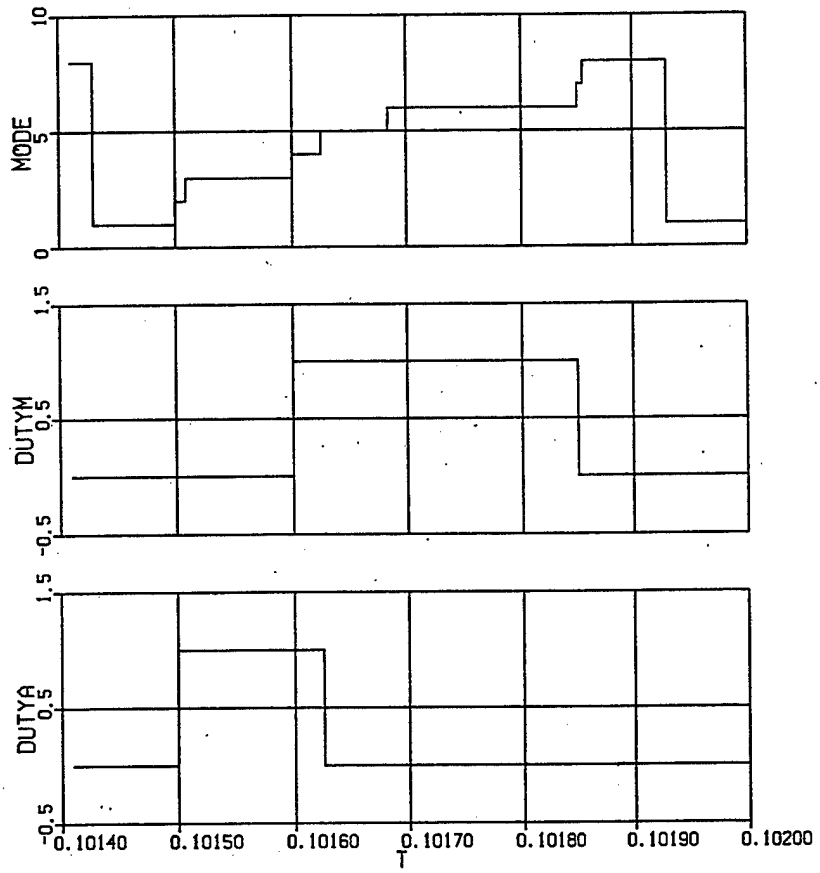


Figure 23 - Switch Actuation Signals and Converter Mode of Operation (R=95Ω)

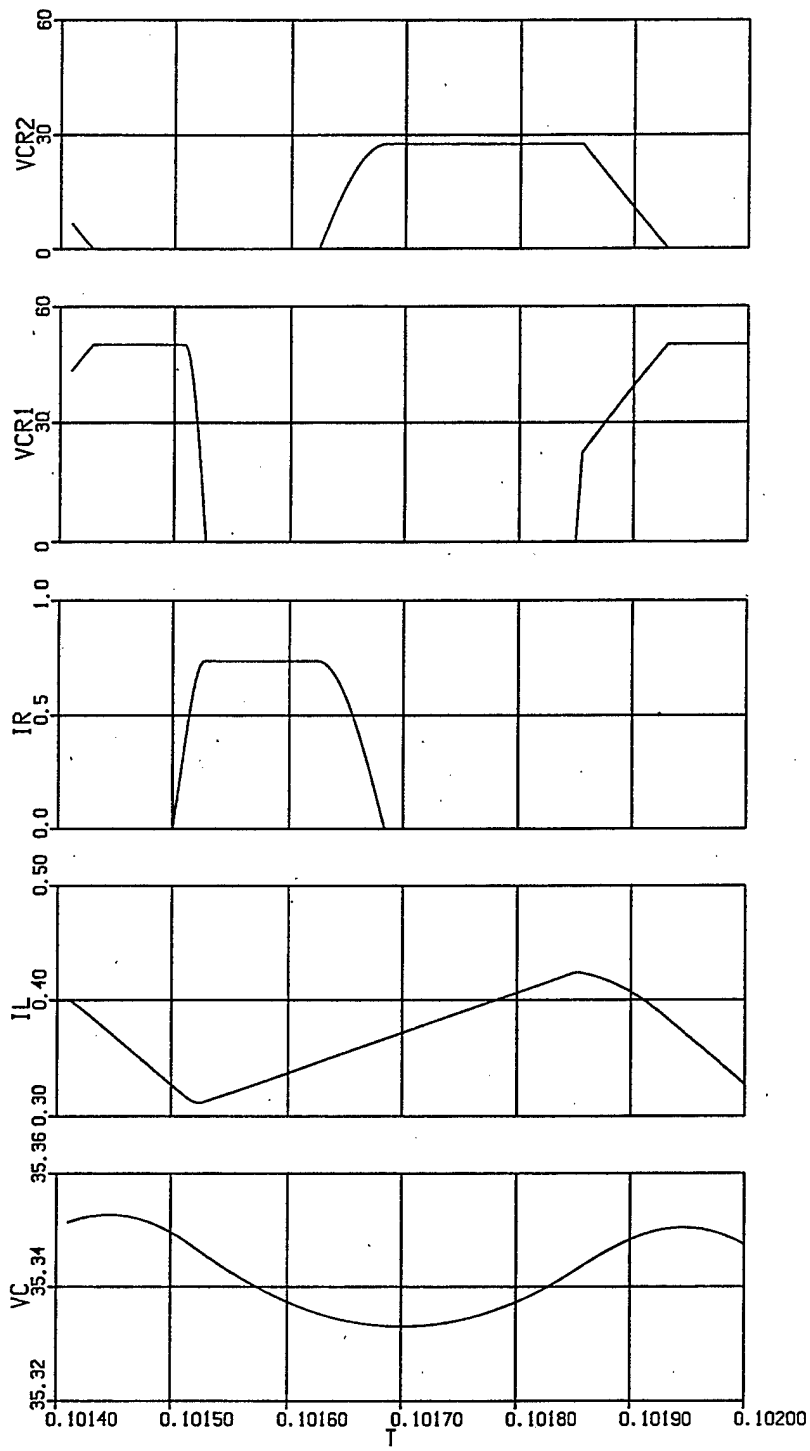


Figure 24 - Converter State Variables (R=95Ω)

IV. Parameter Design

For the circuit under consideration [17], the design engineer must select five component values: the main inductance L, the main output capacitance C, the resonant inductance L_r, and the two resonant capacitances C_{r1} and C_{r2}. In addition, the designer must specify the switching frequency and establish the criteria for turning S_a off. A control algorithm must be formulated and suitably fast diodes selected for the network. One nuance that has thus far been overlooked is the presence of C_{r1} directly across switch S_m. If there exists any charge on C_{r1} when S_m is closed, the switch could be stressed or destroyed. Therefore, it is probably more proper to think of this capacitance as internal to the switch itself. For this section and in order to gain an appreciation for the dependence of the parameter values on the circuit operation, we will assume that C_{r1} is a passive component that we will choose.

The basic design of a buck chopper is well understood and will be briefly highlighted next. For convenience, the following specifications are assumed: the input voltage V_{dc} is a fixed 300V, the desired output voltage V_{out} is 208V, the rated output load is 3kW, the switching frequency is set at 20kHz, and the output ripple should be less than 0.5V. The main inductor is sized principally to ensure that the converter remains in the continuous current conduction mode for all loads greater than 10% of rated ($R_{rat} = 14.42\,\Omega$). With the nominal duty cycle given by

$$D_o = \frac{208\,V}{300\,V} = 0.6933 \tag{4.1}$$

and the load resistance at 10% power given by

$$R_{crit} = 10\,R_{rat} = 144.2\,\Omega \tag{4.2}$$

The critical inductance is found to be

$$L_{crit} = \frac{R_{crit}}{2\,f_s}(1 - D_o) = 1.1\,mH \tag{4.3}$$

where f_s is the switching frequency in Hz. Let's assume we fix $L = 1.3\,mH$ to provide a bit of margin. Next, the minimum capacitance is estimated from the following steady-state ripple constraint:

$$C_{min} = \frac{D_o}{8\,L\,f_s^2\,\Delta V_{out}}(V_{dc} - V_{out}) = 30.7\,\mu F \tag{4.4}$$

where ΔV_{out} is the assumed peak-to-peak output ripple of 0.5V. The actual selection of the capacitor is strongly influenced by the control loop design. If C is selected too small then there is insufficient energy in the capacitor to maintain the output voltage during a transient. If C is selected too large then small variations in the output voltage result in the

duty cycle bouncing between full-on and full-off. This occurs because there is too much energy in the capacitor compared to what the inductor can handle. In this case, we will postulate that $C = 400\,\mu F$ yields a good compromise between available energy for transients and dynamic range in the control loop.

For rated load, it is also of interest to quantify the expected ripple current. The minimum steady-state inductor current is found to be

$$I_{Lmin} = \frac{V_{out}}{R_{rat}}\left[1 - \frac{R}{2Lf_s}(1 - D_o)\right] = 13.2\,A \tag{4.5}$$

while the maximum steady-state inductor current is found to be

$$I_{Lmax} = \frac{V_{out}}{R_{rat}}\left[1 + \frac{R}{2Lf_s}(1 - D_o)\right] = 15.65\,A \tag{4.6}$$

The resonant parameters may be estimated once the equations governing the various modes are solved analytically. Fortunately as derived, each mode is governed by a set of linear differential equations which are readily solved using Laplace transform techniques. In particular, during mode 2 when the resonant inductor current is charging up to approximately the minimum of the inductor current, the following holds:

$$i_r = \frac{V_{dc}}{L_r}\,t \tag{4.7}$$

Assuming that the inductor current does not change much during mode 3, the resonant capacitor voltage decays according to

$$V_{cr1} = V_{dc}\cos\left[\frac{1}{\sqrt{L_r C_{r1}}}\,t\right] \tag{4.8}$$

while the resonant inductor current builds according to

$$i_r = I_{Lmin} + V_{dc}\sqrt{C_{r1}/L_r}\,\sin\left[\frac{1}{\sqrt{L_r C_{r1}}}\,t\right] \tag{4.9}$$

Here, we have assumed that 't' starts at the end of mode 2. For simplicity, the following equations will make similar assumptions -- that the symbol 't' is zero at the beginning of the respective mode. The time in mode 4 is fixed by the delay between closing S_m and opening S_a. The initial conditions for mode 5 are $V_{cr2}(0) = 0$ and the resonant inductor current fixed at its maximum value $i_r(0) = i_{rmax}$. The equations governing mode 5 are given by:

$$V_{cr2} = i_{rmax}\sqrt{L_r/C_{r2}}\,\sin\left[\frac{1}{\sqrt{L_r C_{r2}}}\,t\right] \tag{4.10}$$

$$i_r = i_{rmax} \cos\left[\frac{1}{\sqrt{L_r C_{r2}}} t\right] \tag{4.11}$$

If we asume that V_{cr2} charges up to V_{dc} prior to i_r decaying to zero, then the circuit enters mode 5x. If we further assume that i_r decays to i_{r5} at the end of mode 5, then the following holds for mode 5x:

$$i_r = i_{r5} - \frac{V_{dc}}{L_r} t \tag{4.12}$$

Mode 6 is then entered and the main switch conducts until the control specifies that S_m open. If we assume that V_{cr2} has charged up to V_{dc} (as we did above), then the circuit transitions to mode 8. Capacitor C_{cr2} discharges and C_{cr1} charges. At this point, the inductor current is at its maximum value and if we assume that we size the capacitor sufficiently small so that the main inductor current does not appreciably change over this interval then

$$V_{cr1} = \frac{I_{Lmax}}{C_{r1} + C_{r2}} t \tag{4.13}$$

The above equations provide a blueprint for estimating the required resonant parameters. First of all, we understand that the resonant portions of the cycle should be very small relative to the fundamental switching period. That is, the circuit should be in mode 6 for approximately $D_o T_{sw} = 35\,\mu\text{sec}$ and in mode 1 for approximately $(1\ D_o) T_{sw} = 15\,\mu\text{sec}$. To illustrate the sizing of the various parameters, let's assume that we wish to be in mode 2 no longer than $1.5\,\mu\text{sec}$ (probably a bit high of a choice). It follows from (4.7) that

$$L_r = \frac{V_{dc}\, 1.5\,\mu\text{sec}}{I_{Lmin}} = 34.11\,\mu\text{H} \tag{4.14}$$

From (4.8), we see that during mode 3, it will take a quarter cycle for V_{cr1} to decay to zero. If we fix this time at $0.3\,\mu\text{sec}$, we have a mechanism for finding C_{r1}.

$$\frac{\pi}{2} \sqrt{L_r C_{r1}} = 0.3\,\mu\text{sec} \tag{4.15}$$

which results in

$$C_{r1} = 1\,\text{nF} \tag{4.16}$$

During this quarter cycle, the resonant inductor current builds to a maximum established from (4.9) to be

$$i_{rmax} = I_{Lmin} + V_{dc} \sqrt{\frac{C_{r1}}{L_r}} = 14.81\,\text{A} \tag{4.17}$$

The remaining paramter is C_{r2}. We understand that during mode 8, the voltage V_{cr1} must rise to V_{dc}. Let's assume that we want this to happen in 0.2 µsec. Plugging into (4.13)

$$V_{cr1} = \frac{i_{Lmax}}{C_{r1} + C_{r2}} 0.2\,\mu\text{sec} = 300\,\text{V} \tag{4.18}$$

and solving for C_{r2} yields

$$C_{r2} = 9.4\,\text{nF} \tag{4.19}$$

We have not used the modeling equations for modes 5 and 5x so let's return to them and examine how much time the circuit operates in those two modes.

$$V_{cr2} = i_{rmax}\sqrt{L_r/C_{r2}}\,\sin\left[\frac{1}{\sqrt{L_r C_{r2}}}\,t\right] = 300\,\text{V} \tag{4.20}$$

Solving for the time required for V_{cr2} to charge to 300 V yields

$$t_5 = 0.194\,\mu\text{sec} \tag{4.21}$$

During t_5 equation (4.11) predicts that i_r decays down to

$$i_{r5} = 13.95\,\text{A} \tag{4.22}$$

Therefore, the circuit enters mode 5x and the required decay time is found from (4.12) to be

$$t_{5x} = \frac{i_{r5}\,L_r}{V_{dc}} = 1.59\,\mu\text{sec} \tag{4.23}$$

If resonant parameter values $L_r = 34.11\,\mu\text{H}$, $C_{r1} = 1\,\text{nF}$ and $C_{r2} = 9.4\,\text{nF}$ are not acceptable (as shown by simulation), then the process can be iterated.

Due to the highly oscillatory response of the buck chopper output filter, feedback control is required to guarantee acceptable transient response and steady-state regulation. The authors have primarily emphasized voltage-mode control techniques in past efforts, taking advantage of Pulse-Width-Modulation chips that were well understood and readily available. Higher control bandwidths are realizable going to current-mode control; however, additional subtleties exist. In this section, a basic multi-loop voltage-mode control will be reviewed to illustrate this portion of the design process.

The duty cycle equation for the multi-loop control with feedforward is given by

$$d(t) = \frac{V_{ref}}{V_{dc}} - h_v\,K_v\,K_{pwm}(v_{out} - V_{ref}) \tag{4.24}$$

$$- h_n\,K_v\,K_{pwm}\int(v_{out} - V_{ref})\,dt - h_i\,K_i\,K_{pwm}(i_L - i_{out})$$

where h_v, h_n, and h_i are the feedback gains, K_v and K_i are the voltage and current sensor

gains, K_{pwm} is the gain of the pwm modulator chip, V_{ref} is the desired output voltage, and i_{out} is the sensed output current. Here we have assumed that the unit is operating in isolation and we are not concerned with parallel operation. Parallel operation can be incorporated using droop techniques, current wire or frequency-injection approaches. For now, we will omit this discussion and further assume that the resonant portion of the circuit has been designed properly so that for the frequencies under consideration, the resonant portion of the cycle is transparent.

One can note in (4.24) that the current feedback term significantly increases the speed of response while the feedforward term, $\frac{V_{ref}}{V_{dc}}$, minimizes the impact of changes in the input voltage.

If V_{ref} is assumed constant and a resistive load is assumed at the output, then a set of linear differential equations govern the operation of the buck chopper. A desired characteristic polynomial may be specified as

$$s^3 + d_2 s^2 + d_1 s + d_0 \tag{4.25}$$

where the coefficients transmit information about the pole locations and thus the transient response. By coefficient matching with the characteristic equation of the buck chopper with the above duty cycle equation inserted, we uncover the following gain relationships

$$h_v K_v K_{pwm} = \frac{LC}{V_{dc}}\left(d_1 - \frac{1}{LC}\right) \tag{4.26}$$

$$h_n K_v K_{pwm} = \frac{d_0 LC}{V_{dc}} \tag{4.27}$$

$$h_i K_i K_{pwm} = \frac{L}{V_{dc}}\left(d_2 - \frac{1}{RC}\right) \tag{4.28}$$

The control gains are minimized if the closed-loop poles are clustered using a Bessel function polynomial approximation. The pole locations are specified by

$$s_{1,2} = -0.7455\,\omega \;+/-\; j0.7112\,\omega \tag{4.29}$$

$$s_3 = -0.9420\,\omega \tag{4.30}$$

where ω is the desired closed-loop bandwidth. First, ω must be sized at least one decade smaller than the radian switching frequency $(2\pi 20{,}000)$ to prevent unwanted controller interactions. Second, selection of ω should not require excessive duty cycle control effort which introduces unwanted noise in the controller. Third, ω must be large enough to produce the required transient response times. Based on these criteria, let's consider

$$\omega = 3000\,\text{rad/sec} \tag{4.31}$$

This results in a characteristic equation that leads to the following pole locations

$$s_{1,2} = -2237 \ +/- \ j2134 \tag{4.32}$$

$$s_3 = -2826 \tag{4.33}$$

and gain slections

$$h_v K_v K_{pwm} = 0.03514 \tag{4.34}$$

$$h_n K_v K_{pwm} = 46.80 \tag{4.35}$$

$$h_i K_i K_{pwm} = 0.03088 \tag{4.36}$$

With these gains and the load resistance at $R = 144.2\,\Omega$ (10% of rated power), the closed-loop poles shift to the following locations:

$$s_{1,2} = -2271 \ +/- \ j2286 \tag{4.37}$$

$$s_3 = -2601 \tag{4.38}$$

Since the poles remain in the same general vicinity, the design appears robust over the range of continuous conduction mode.

The above parameters were next employed in an open-loop ACSL simulation. This time the auxiliary switch is gated on at the beginning of the switching cycle, the main switch is gated on 2.5 µsec later, the auxiliary switch is then turned-off following an additional 2.5 µsec, and finally the main switch is turned off 37.17 µsec into the switching cycle. This results in a net on-time of 34.67 µsec for the main switch or a duty cycle 0f 0.6934. With the switching frequency increased to 20kHz, the integration time step was decreased to *maxt=1.0e-8*. The converter was run till the steady state (approximately 0.04sec) and data was then collected. The results are presented in Figures 25-28. The first two figures capture the circuit variables during the initial modes. Note that modes 3 and 4 now only occupy approximately 3 µsec. As a consequence, the output voltage does track the prescribed duty cycle fairly well. the desired output voltage was 208V whereas the actual output voltage is about 213V. Note also that i_r obtains a maximum value consistent with the design equations and that the circuit does maintain zero volts across the main switch for soft switching. The time interval in modes 3 and 4 can be further minimized by gating the main switch on earlier in the cycle and any residual voltage error may be removed by proper design of the feedback control law. The next two figures capture the response at the end of the cycle. The middle portion of the response has the circuit operating entirely in mode 6 (not very exciting to illustrate in a plot). At the end of the cycle when the main switch opens, we recognize that V_{cr2} is at V_{dc}, so the converter transitions to mode 8 where V_{cr1} now charges back up to V_{dc} in anticipation of the next auxiliary cycle. The circuit then transitions to mode 1 in which the main diode conducts

and both switches are open. The ACSL simulation confirms the basic design analysis and further illustrates the design guidance that can be obtained from conducting various studies. The next section of the report details several important design nuances that are critical in the actual fabrication of a resonant buck chopper.

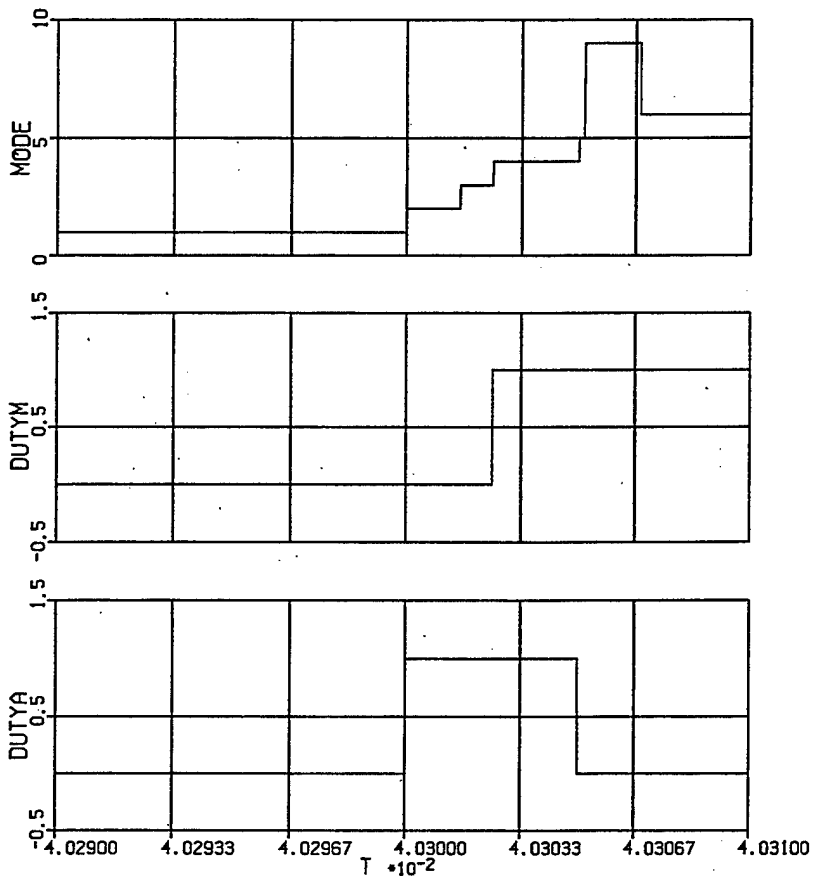


Figure 25 - Switch Actuation Signals and Converter Mode of Operation
(V_{dc}=300V, R=14.42Ω, 20kHz, Beginning of Cycle)

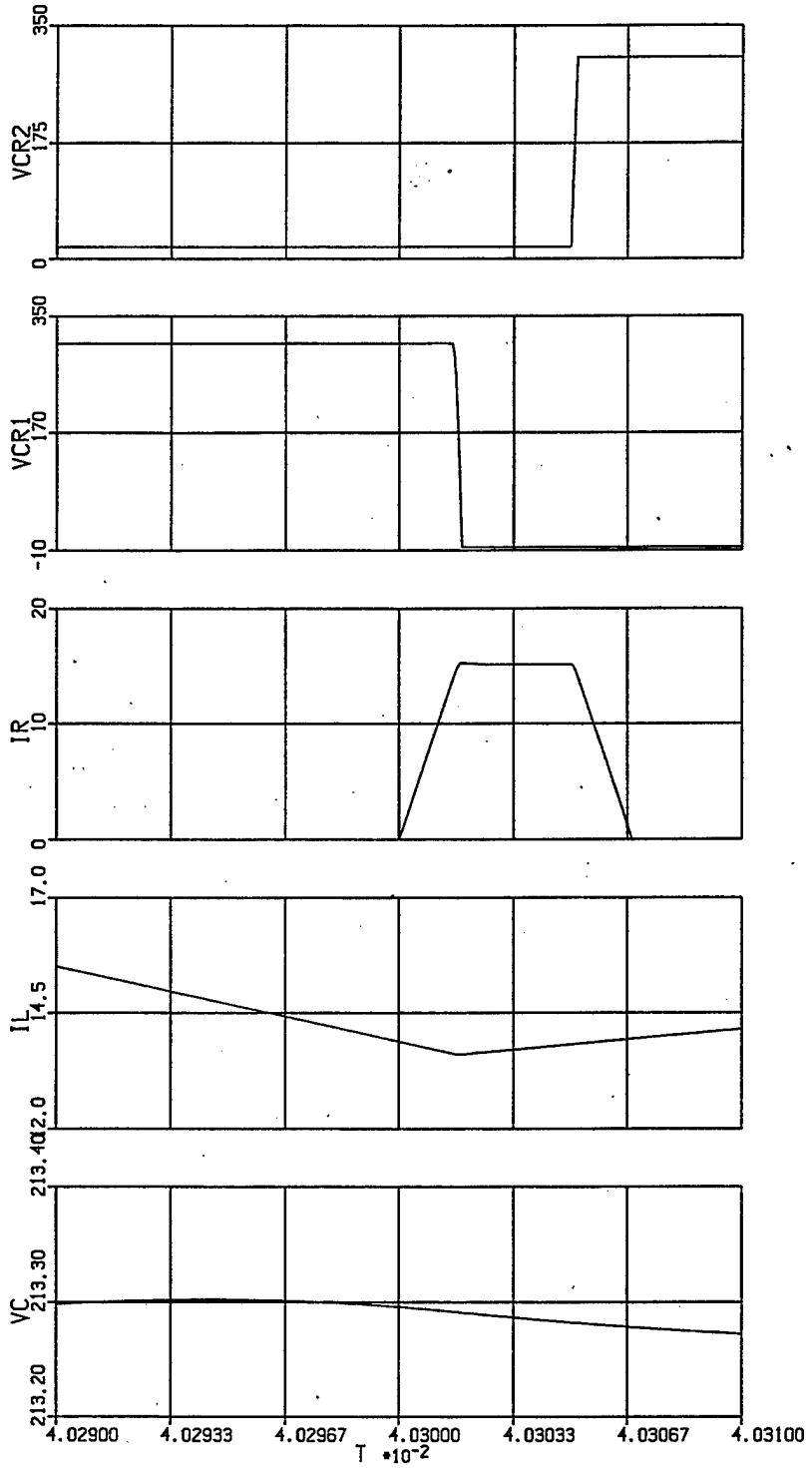


Figure 26- Converter State Variables
(V_{dc}=300V, R=14.42Ω, 20kHz, Beginning of Cycle)

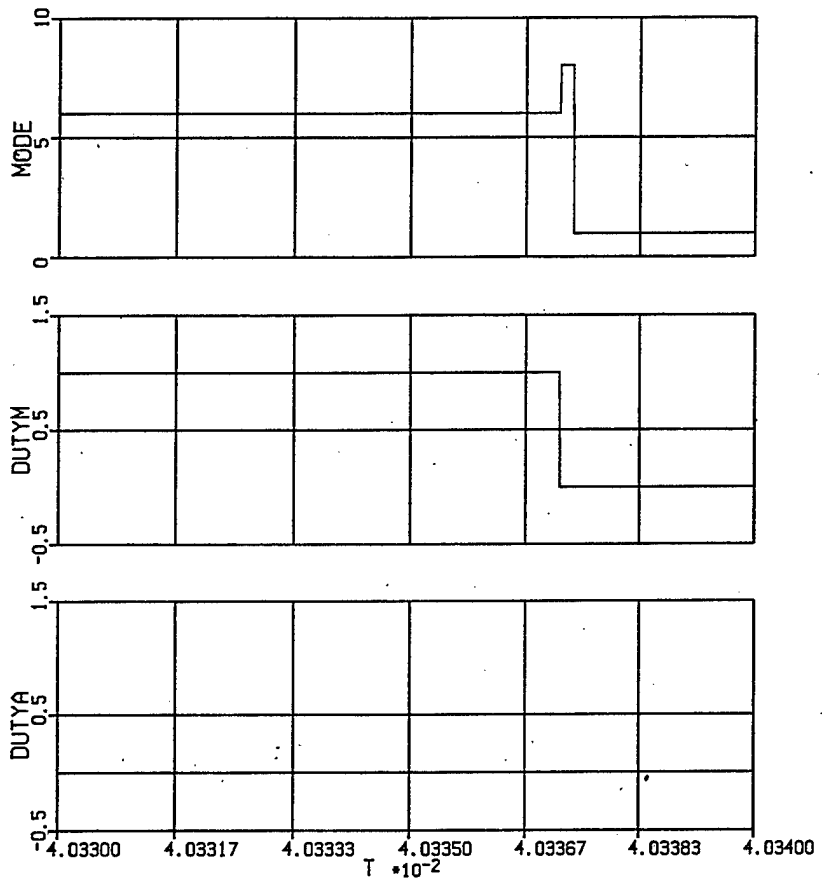


Figure 27 - Switch Actuation Signals and Converter Mode of Operation
(V_{dc}=300V, R=14.42Ω, 20kHz, End of Cycle)

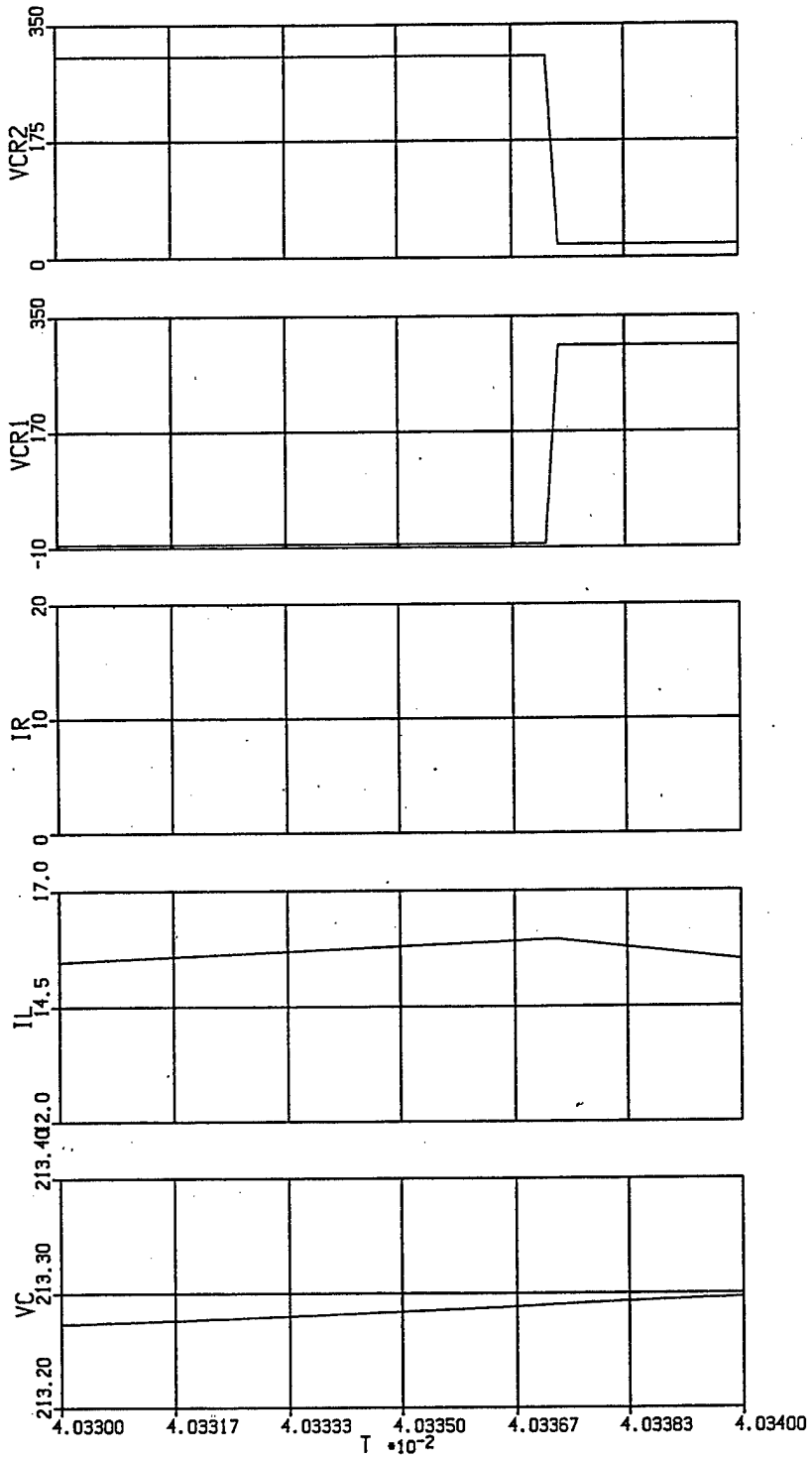


Figure 28 - Converter State Variables
(V_{dc}=300V, R=14.42Ω, 20kHz, End of Cycle)

V. Design Nuances

As with any circuit, component choice and placement is critical to proper operation. Improper component choice, such as using electrolytic instead of ceramic capacitors for bypassing, can cause switch and diode stresses and failures in power switching circuits. The result is the same if inductive loops exist in critical paths due to poor component layout. Below is an outline containing some necessary steps for proper operation of the chosen resonant converter.

Since all of the diodes are in switching paths or in a resonant loop they must be fast or ultra-fast recovery diodes. These diodes should have a reverse recovery time (t_{rr}) less than or equal to the turn-on and turn-off times of the main and auxiliary switches. In the extreme case where t_{rr} is large and the switching frequency is relatively high, a slow diode would simply act like a short in both directions causing a catastrophic failure in the weakest component. There appears to be no normal or transient mode of operation where D_y will conduct when using the ideal model for the circuit. However, D_y may be necessary because of switch body capacitance as will be seen in section VI which contains the PSPICE model of the circuit.

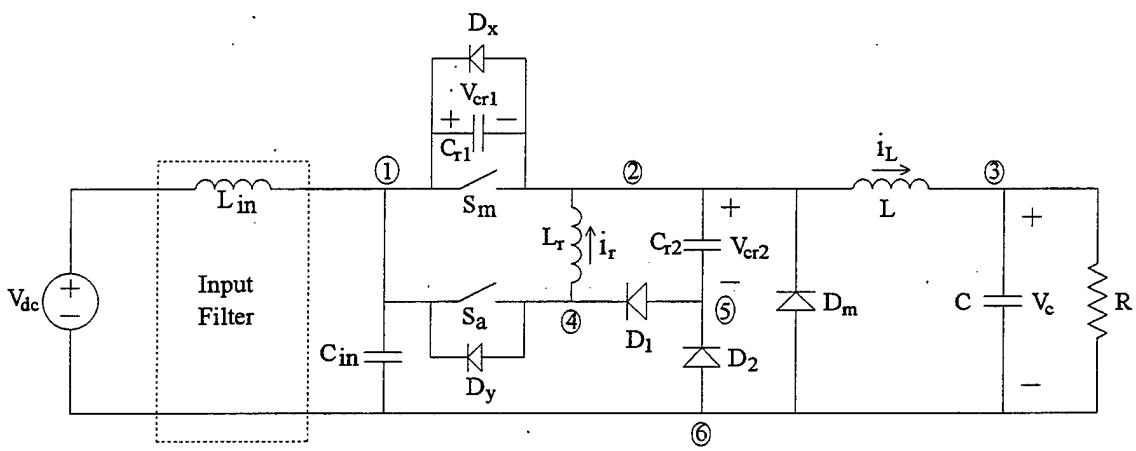


Figure 29 - Proposed Circuit with Node Designations

In order to eliminate potential overvoltages in the circuit, inductive paths between switching elements (transistors and diodes) and other components must be limited. Even a small inductance in series with a power MOSFET can destroy the device at the turn-off point of the switch. The following is a description of important node connections and parallel component connections. For both types of connections, the components referred

to should have the minimum practical lead length between component bodies. The critical node connections are listed in Table 2 according to the node numbers found in Figure 29. As can be seen in the table, the components that require the low inductive loops are referenced to the node.

TABLE 2 - Inductive Loop Component to Node Designation

Node	Components
1	C_{in}, S_m, S_a, D_x, D_y, C_{r1}
2	S_m, L_r, C_{r2}, D_m
4	S_a, D_y, L_r, D_1
5	D_1, D_2
6	C_{in}, D_2, D_m, C

The resonant capacitors C_{r1} and C_{r2} and the input capacitor C_{in} should be high-frequency non-electrolytic capacitors to minimize ESR and ESL. A ceramic capacitor would be a good choice since these capacitances will be lower than 1uf for switching frequencies in excess of 20kHz. The output capacitance should be a combination of high-quality electrolytic capacitors for bulk capacitance and ceramic capacitors for noise and high-frequency spikes. The ceramic portion of C needs to be included in the low inductive loop path as listed in Table 2. However, it is not important for the electrolytic portion of C to be included in the low inductive path. As shown in the schematic, the input should be bypassed with an LC-network at minimum to decouple the line from the load. A standard off-the-shelf filter can be used if power levels are sufficiently low (<1500W). However, node 1 is a low inductive path so C_{in} will need to be used even if a standard filter is chosen.

Further, if S_m does not contain an internal fast recovery antiparallel diode (D_x) an external diode will need to be added. Even though the switches are supposed to be under low switching stress because of the resonant operation, an MOV with very short lead lengths should be connected to each switch to prevent any unintentional or unforeseen voltage spikes from destroying the switches.

Additionally, S_m must be protected against unintentionally discharging C_{r1}. Although the on-time for the auxiliary switch may be set to a constant, it is recommended that a lock-out circuit be used to prevent the main switch from turning on if $V_{cr1}>0$. If any charge exists on the C_{r1}, S_m would likely be stressed or destroyed. This lock-out may be accomplished most easily with the use of a cross-over detector connected in parallel with Sm.

Another area of interest is component ratings. Component voltage and current ratings are best chosen via simulation. However, for any specified topology some general guidelines can be established. For this design all semiconductors, transistors and diodes, should have a voltage rating $>V_{dc}$ plus margin. The average current ratings should be $>I_R$ plus margin and the peak current ratings should be $>I_{L,max}$ plus margin. As expected the input capacitance, C_{in}, must be able to handle the source voltage along with any variation in the source voltage. The output capacitance, C, must have a minimum rating of V_c. Further, the most critical specifications for the main inductance, L, are its dc current rating and frequency capability. L should maintain its rated inductance at full current and not saturate.

The last topic in this section to be considered is placement of sensors for the purposes of monitoring and control. For control purposes it would be most useful to have voltage sensors at node 1 and node 2 to obtain the input and output voltages. This will allow a feedforward loop if desired and the use of a voltage loop. Further, current sensors on the main inductor L and the load will allow for a current loop as well as estimating the transient and switch currents. The transient current can be used to speed up response and the peak inductor current to assure that switch ratings are not exceeded. All sensors should be optically or magnetically isolated and the control board as well as the power section should have good ground planes. The two isolated ground planes should be connected electrostatically via a high impedance to prevent static discharge (~1MΩ).

The final section of the report documents a PSPICE simulation of the candidate network. The PSPICE simulation is intended to validate the ACSL model and provide further device-level guidance.

VI. PSPICE Simulation

PSPICE is a simulation package which allows the designer to model a circuit at the component level. That is, diodes and transistors are represented in detail and not simply approximated as short-circuits or open-circuits as was done in the ACSL simulation. These device nuances are often times critical to circuit operation, especially for high-power and circuits employing high switching frequencies. Therefore in this effort, it was deemed important to assemble a PSPICE model of the proposed circuit [17] to both validate the ACSL representation and to focus in on the non-ideal aspects of the switching elements. In addition, PSPICE facilitates the determination of the circuit efficiency which is of primary interest in a resonant converter.

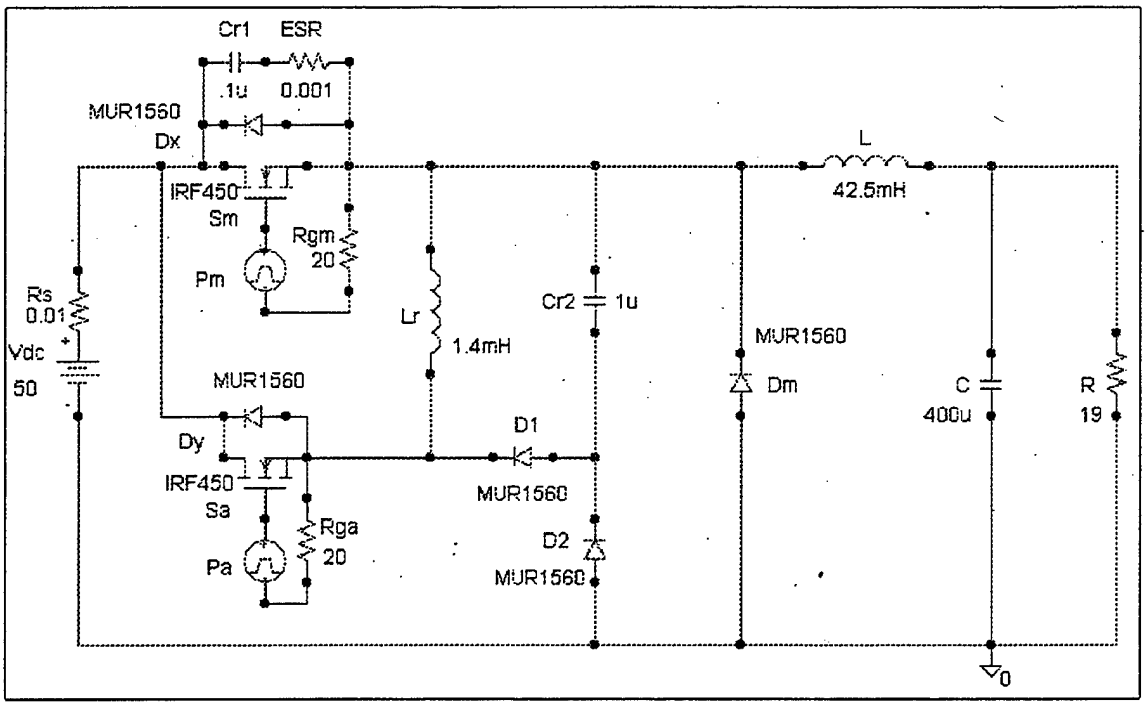


Figure 30 - PSPICE Model of the Chosen Circuit

The basic PSPICE circuit is assembled using the schematic capture facilities of the program. The schematic for the low-voltage 2kHz circuit is illustrated in Figure 30. Note that pulse generators are used to drive the MOSFETS and a small series resistance is inserted to limit the current drawn. A small resistance is inserted in series with C_{r1} to model ESR effects. The circuit diodes are fast-recovery diodes selected from the parts library. A study was structured identical to the one reported on in the ASCL Simulation

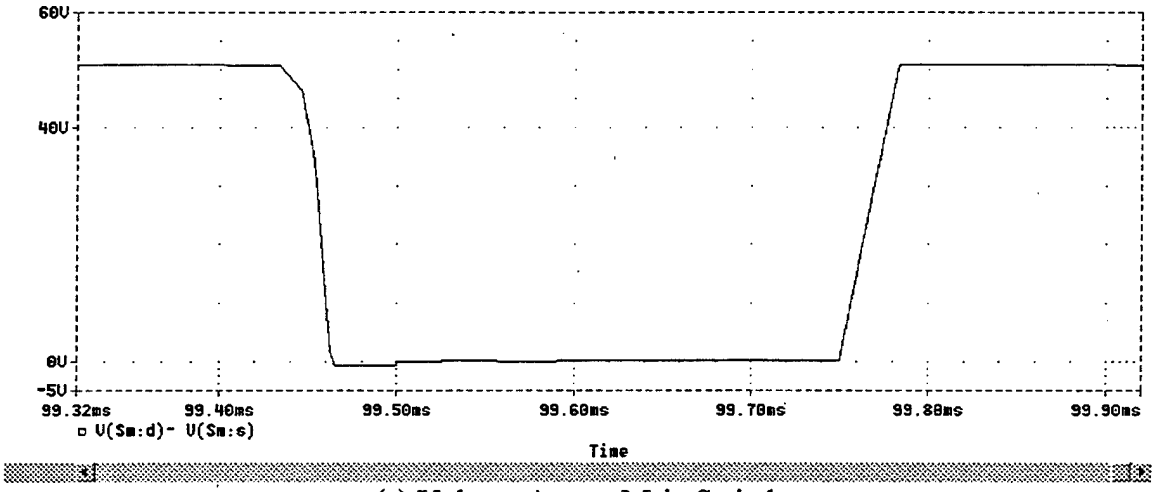
section of this report. As is clear from Figure 30, the same component parameters were used and the same open-loop switch actuation signals were programmed. The results for the 19Ω load are documented in Figures 31-33.

The resonant current i_r in Figure 31 appears to closely match the ACSL result of Figure 22. The principle differences are the slight slope at the peak and the fact that the current goes negative for a brief amount of time. During this interval, diode D_y is carrying the current. The rates of rise and fall of the two resonant capacitor voltages are very similar to those portrayed in Figure 22. In Figure 32, the startup characteristics are illustrated showing how the output capacitor voltage and the main inductor current build to their steady-state values. Note that the final values are in strong agreement with those from Figure 22. In addition, a plot of efficiency was included to illustrate how the circuit operates above 92% efficiency. Figure 33 shows a steady-state cycle of the output voltage and main inductor current, once again in tight agreement with the ACSL results.

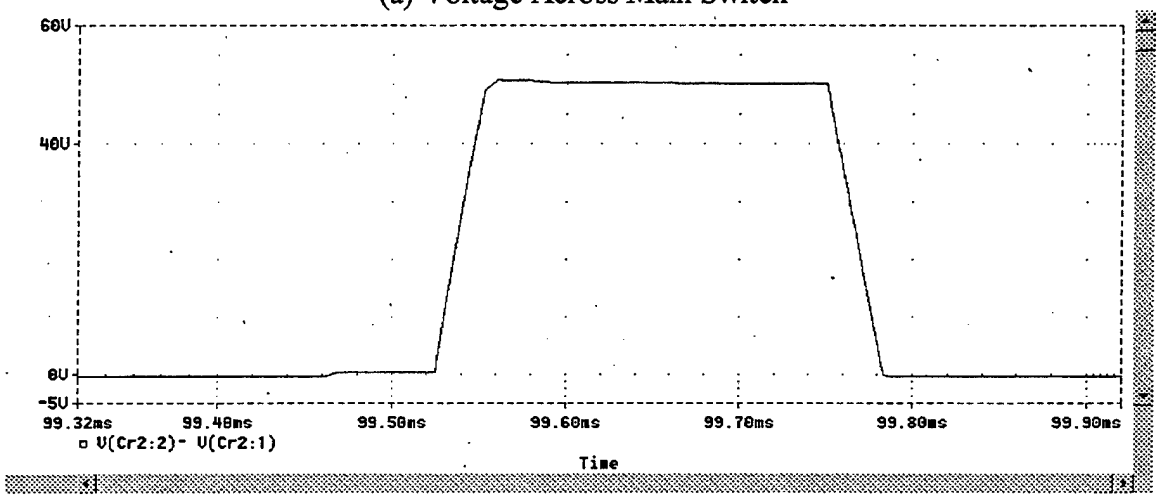
The next set of curves document operation of the same circuit with the load resistance changed to R=95Ω. The data is recorded in Figures 34-36. The voltage V_{cr2} is shown to not rise to V_{dc} and the shape is remarkably similar to the waveform of Figure 24. The amplitude of the resonant inductor current is also close to the ACSL simulation, modulus the differences mentioned above. The dual positive slope on the V_{cr1} waveform appears in the PSPICE results as it did in the ASCL study. From these results, it appears that the ACSL representation is a valid tool at the low frequency and input voltages. Figure 35 documents the startup waveforms for the capacitor voltage, main inductor current and the circuit efficiency. The circuit efficiency is noticeably lower at the light load; however, the system has not yet settled to a quiescent point. Note that the converter remains in the continuous conduction mode and, as noted in Figure 36, the level and ripple content of the waveforms established by the PSPICE model closely match those predicted by ACSL. Any deviations are due to the fact that PSPICE is representing voltage drops and losses that are not accounted for in the ACSL model.

With the low-frequency, low-voltage circuit validated with the ACSL representation, the next step was to convert the model to the 20kHz 300V-in circuit. The result is depicted in Figure 37. Initially, MOSFETS were used as the switching components. Figures 38-40 document the results. The main switch appears to be soft-switching but an

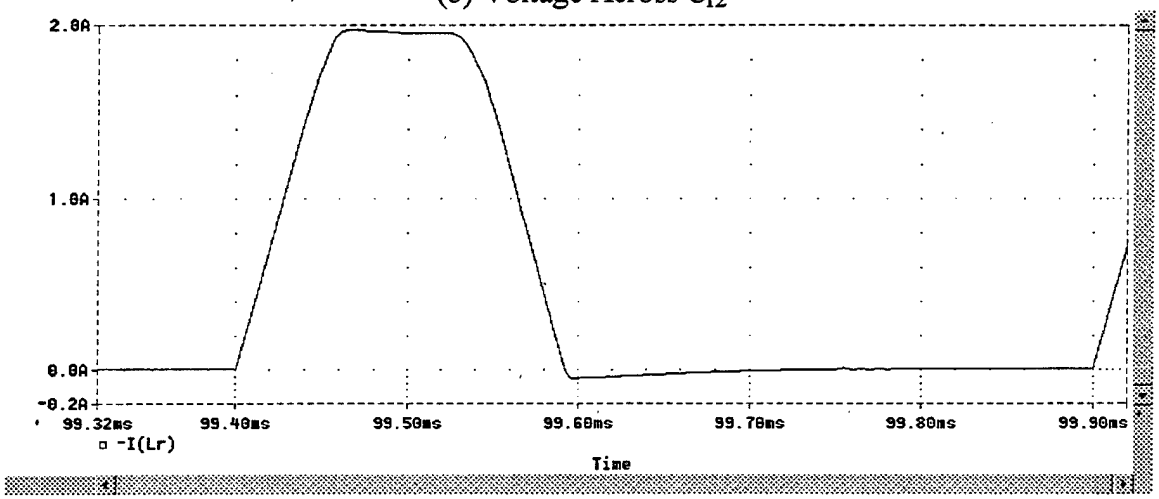
anomaly was observed with regards to the resonant inductor current. It appears that the body capacitance of S_a is maintaining the voltage at node 4 (Figure 29) while the voltage at node 2 drops due to S_m opening. This induces a positive current in the resonant inductor which is maintained through the loop consisting of D_1, D_2, and D_m. In actuality, it is displacing current that is flowing through D_m into the load. It is unclear that this would occur with actual hardware and would require further study. If problems are evidenced with the MOSFET switches, a lower body capacitance device may need to be substituted and investigated in the circuit (such as an IGBT).



(a) Voltage Across Main Switch

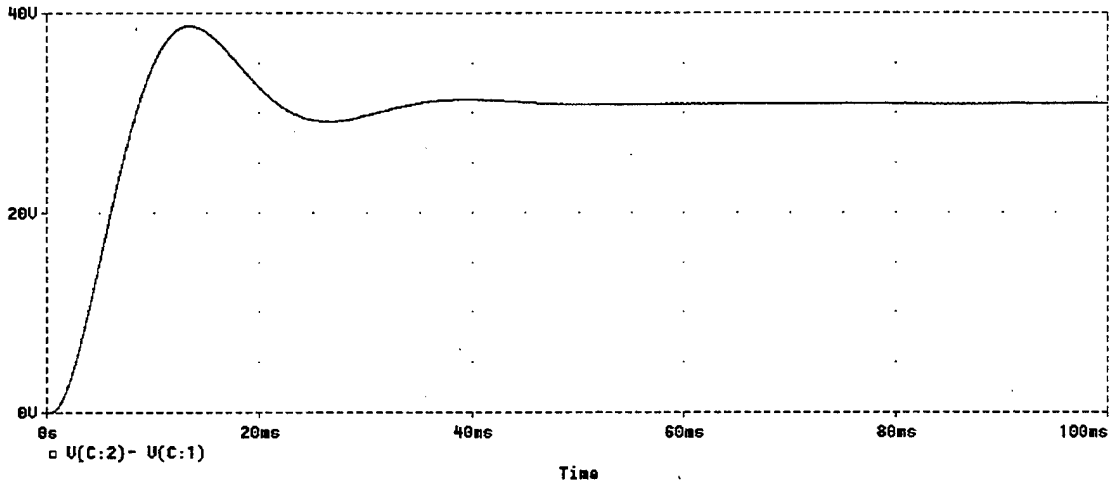


(b) Voltage Across C_{r2}

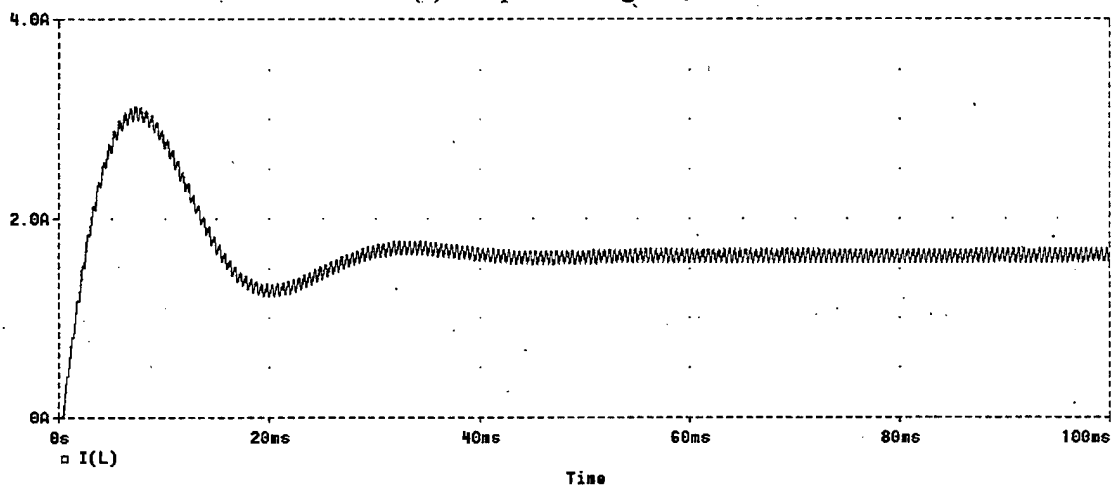


(c) Current Through Resonant Inductor L_r

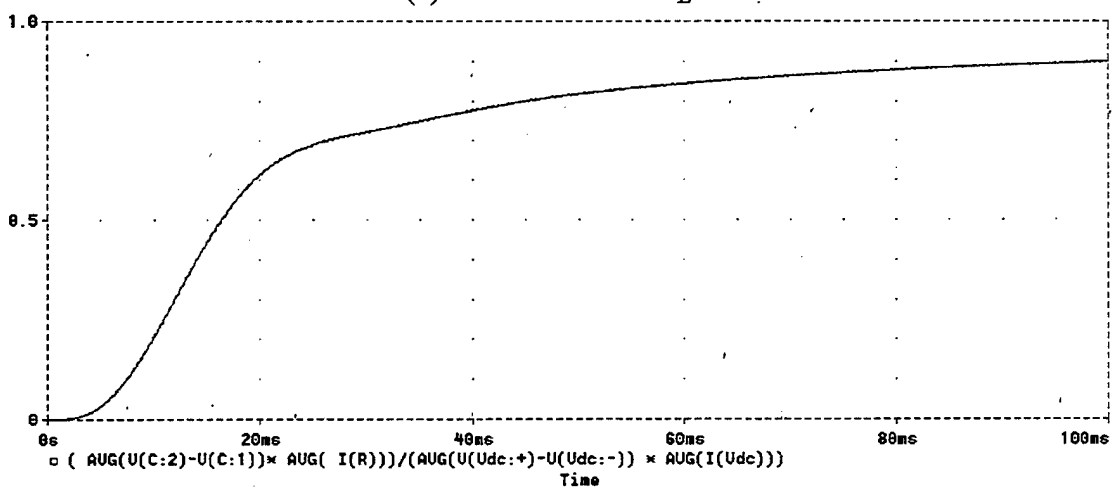
Figure 31 - V_{dc}=50V, R=19Ω, 2kHz



(a) Output Voltage V_c

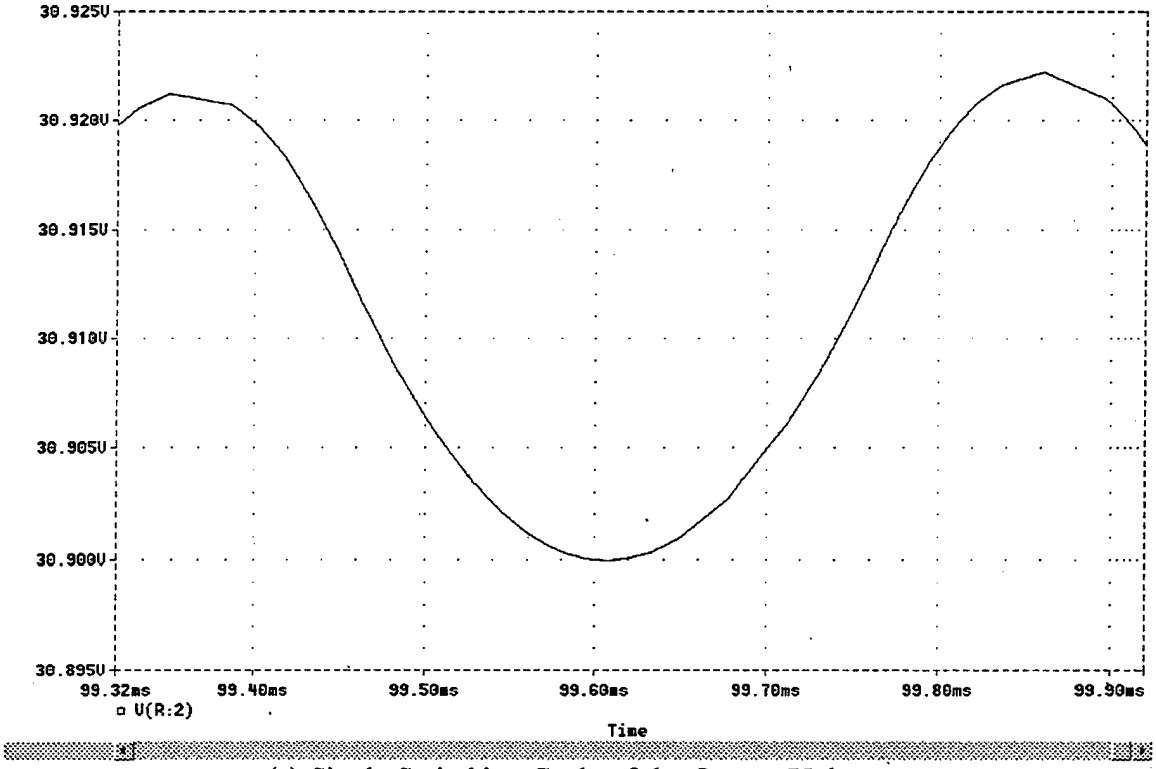


(b) Inductor Current i_L

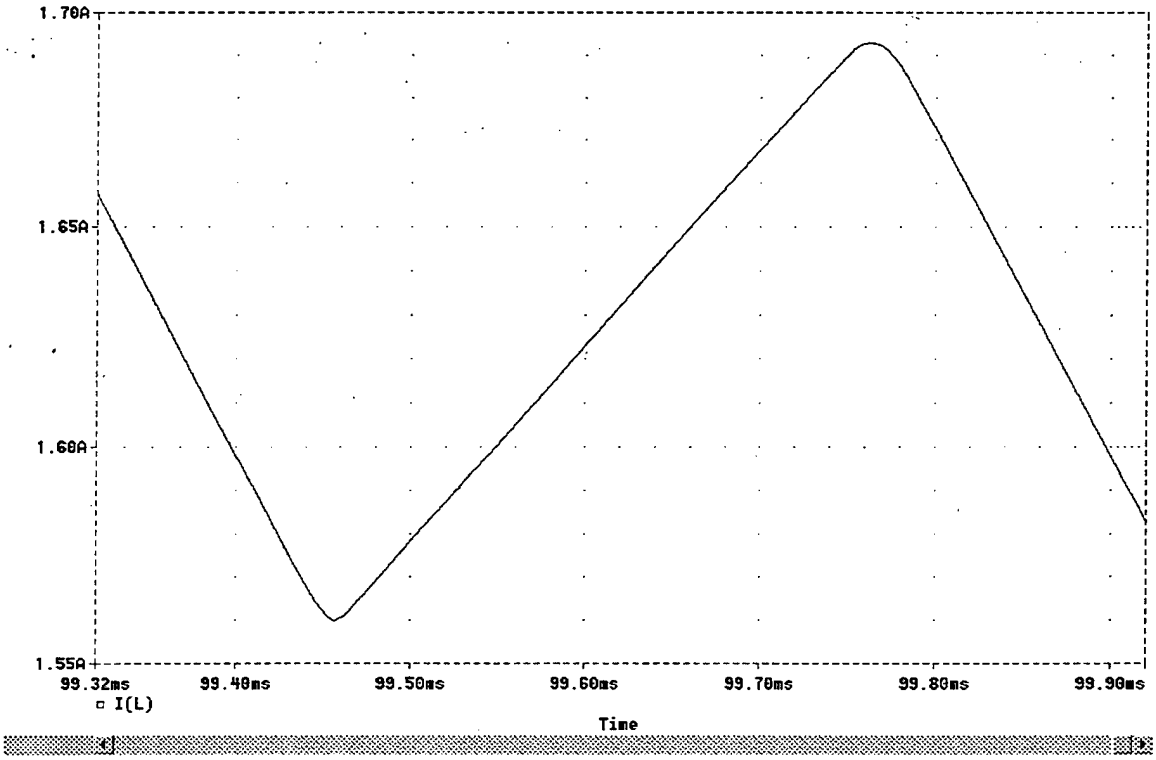


(c) Efficiency

Figure 32 - V_{dc}=50V, R=19Ω, 2kHz

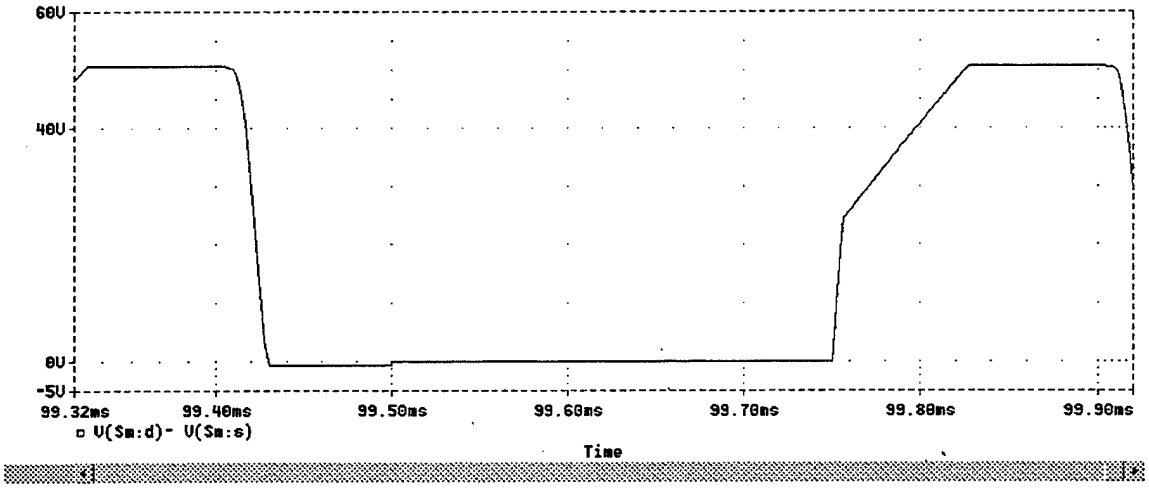


(a) Single Switching Cycle of the Output Voltage

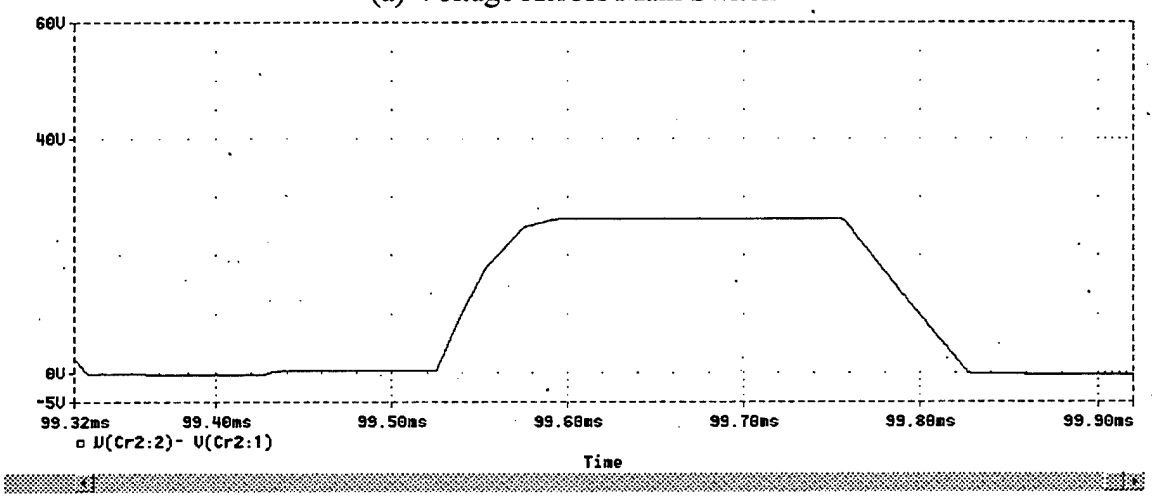


(b) Single Switching Cycle of the Inductor Current

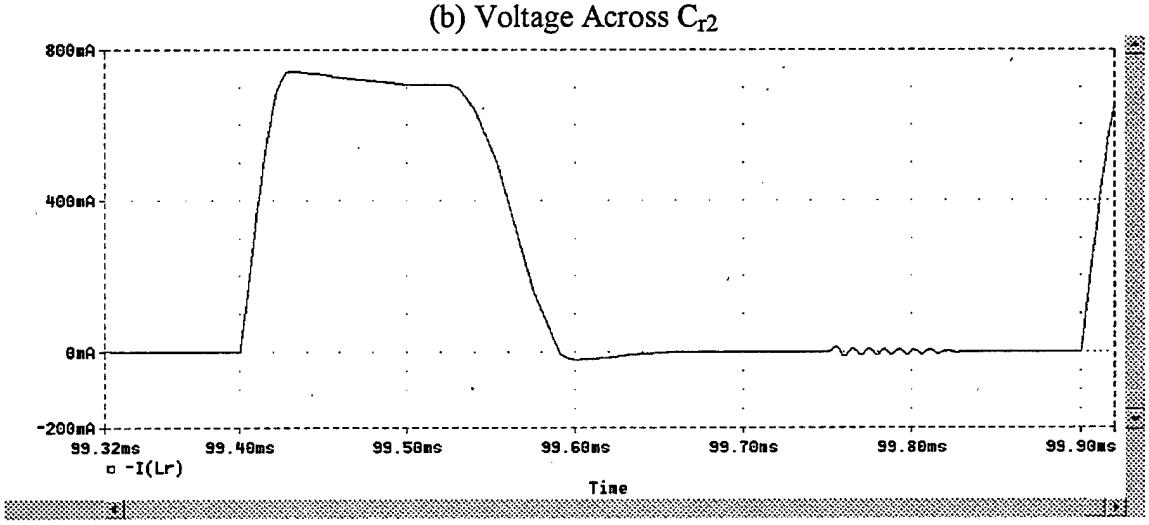
Figure 33 - V_{dc}=50V, R=19Ω, 2kHz



(a) Voltage Across Main Switch

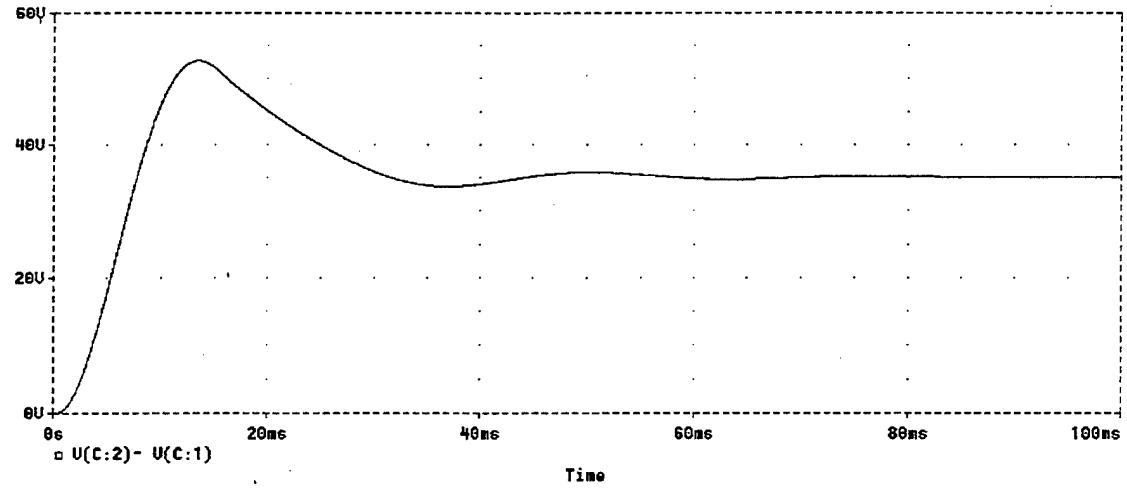


(b) Voltage Across C_{r2}

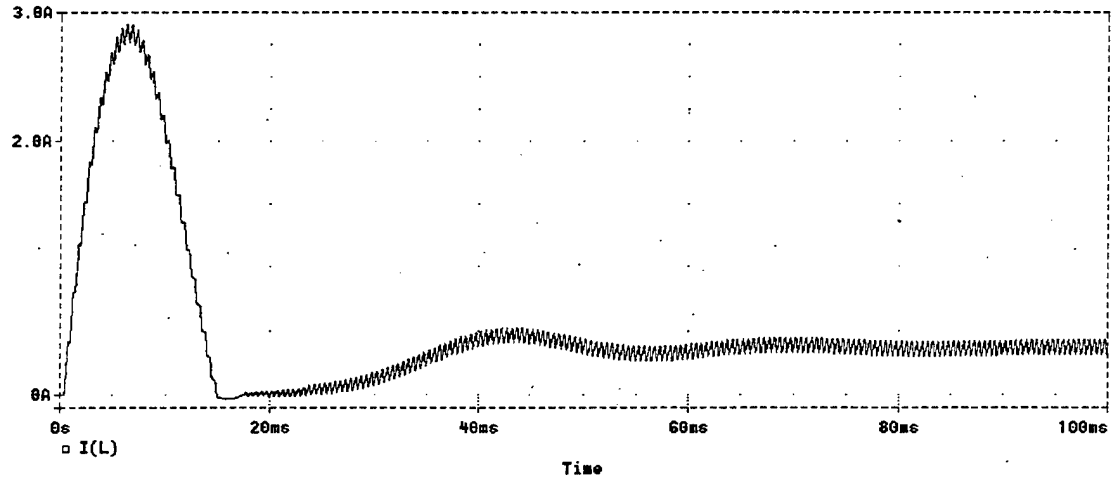


(c) Current Through Resonant Inductor L_r

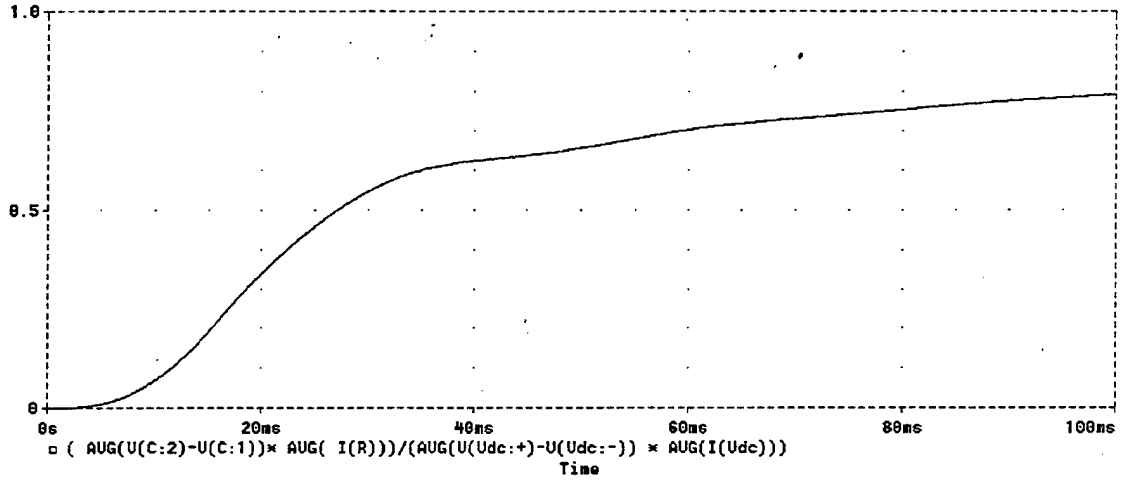
Figure 34 - V_{dc}=50V, R=95Ω, 2kHz



(a) Output Voltage V_c

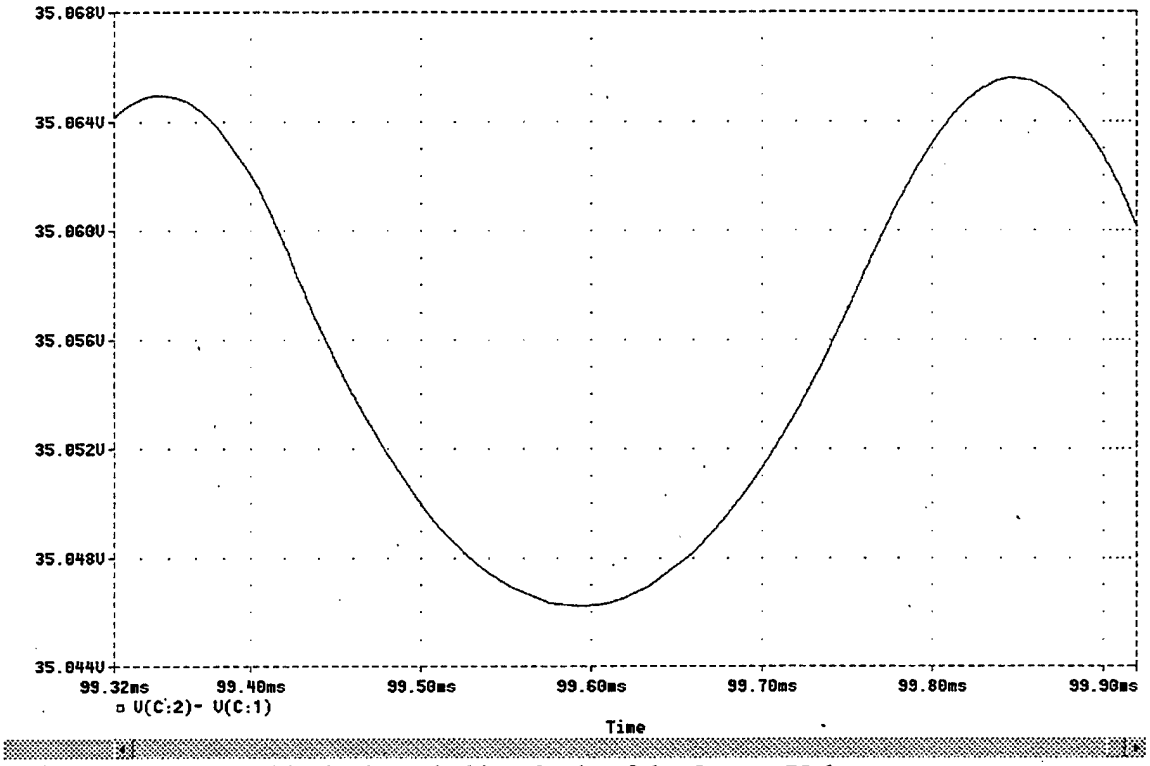


(b) Inductor Current i_L

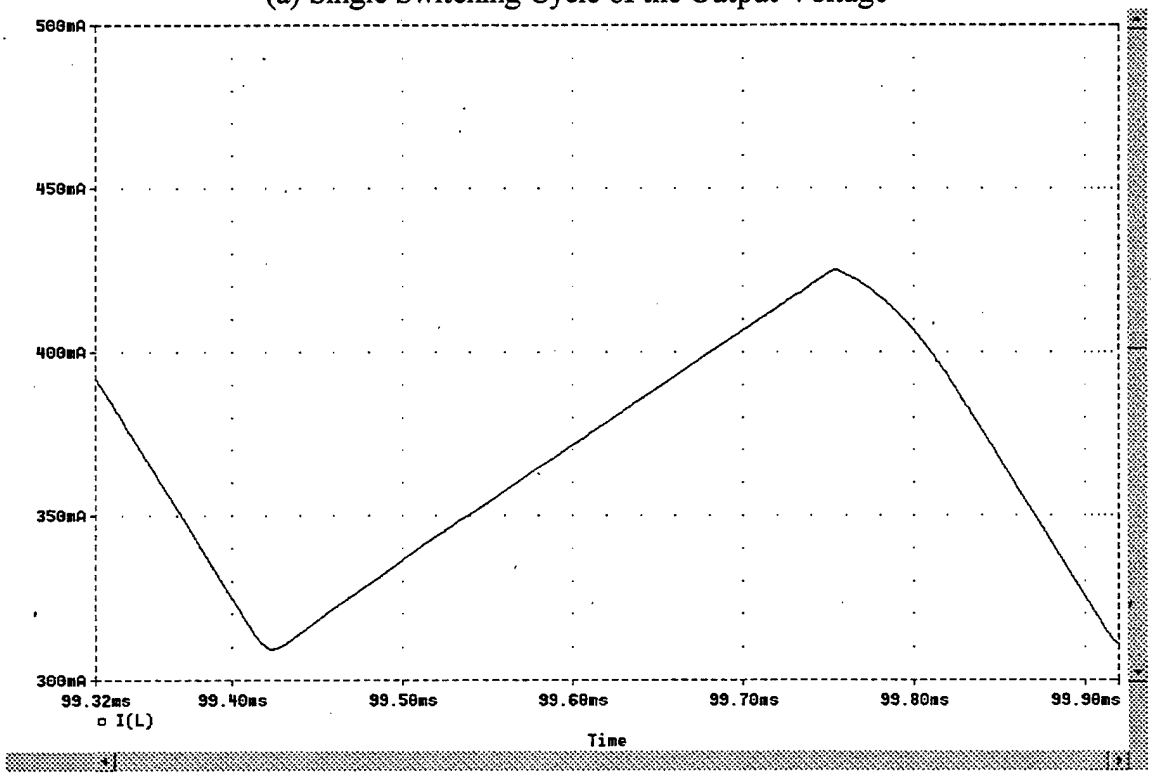


(c) Efficiency

Figure 35 - V_{dc}=50V, R=95Ω, 2kHz



(a) Single Switching Cycle of the Output Voltage



(b) Single Switching Cycle of the Inductor Current

Figure 36 - V_{dc}=50V, R=95Ω, 2kHz

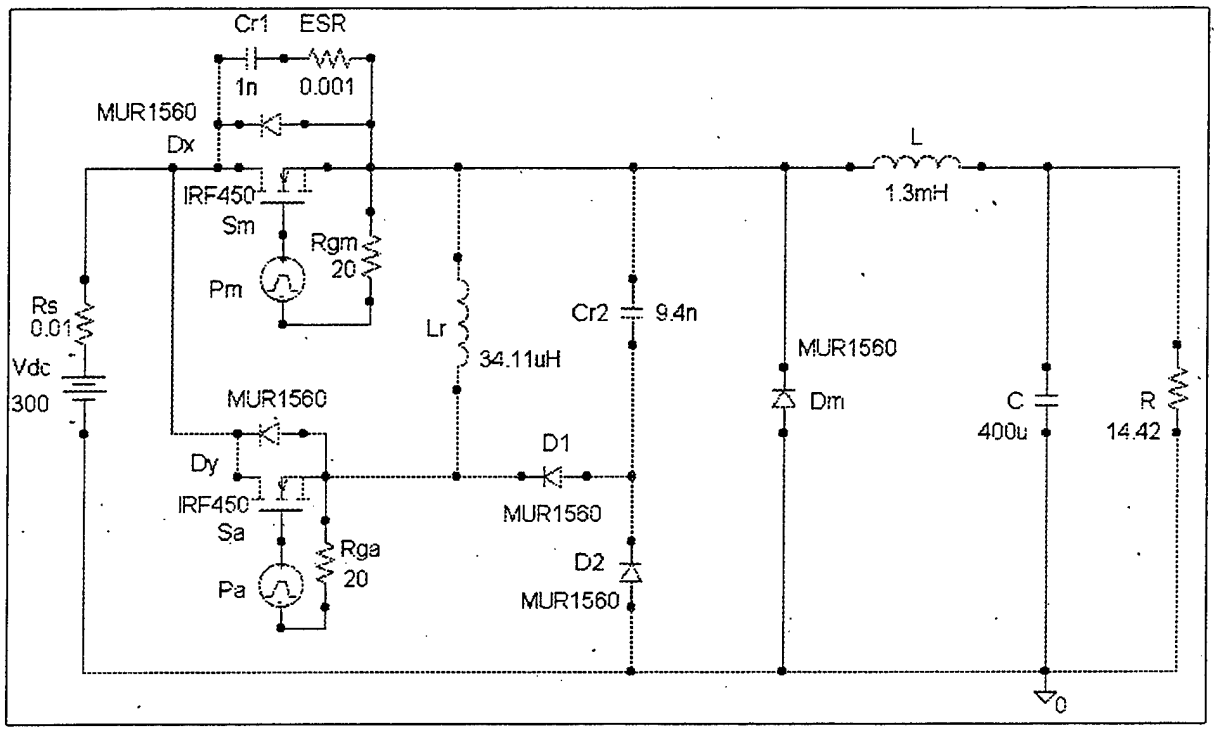
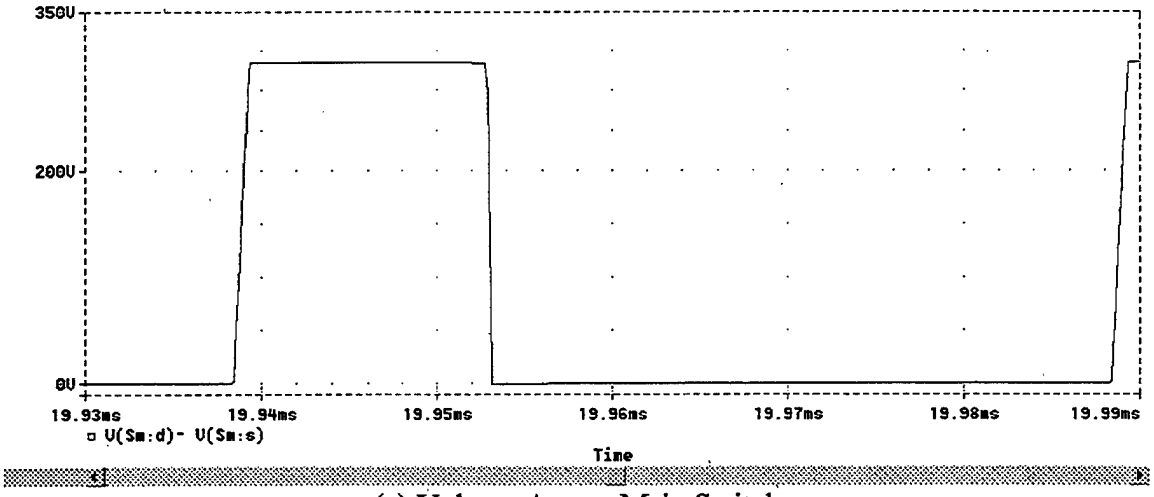
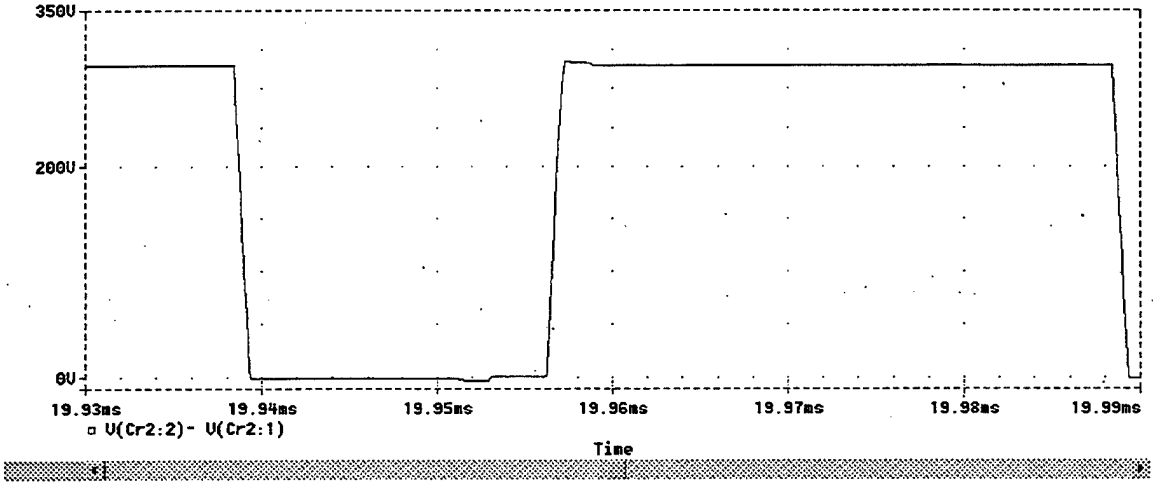


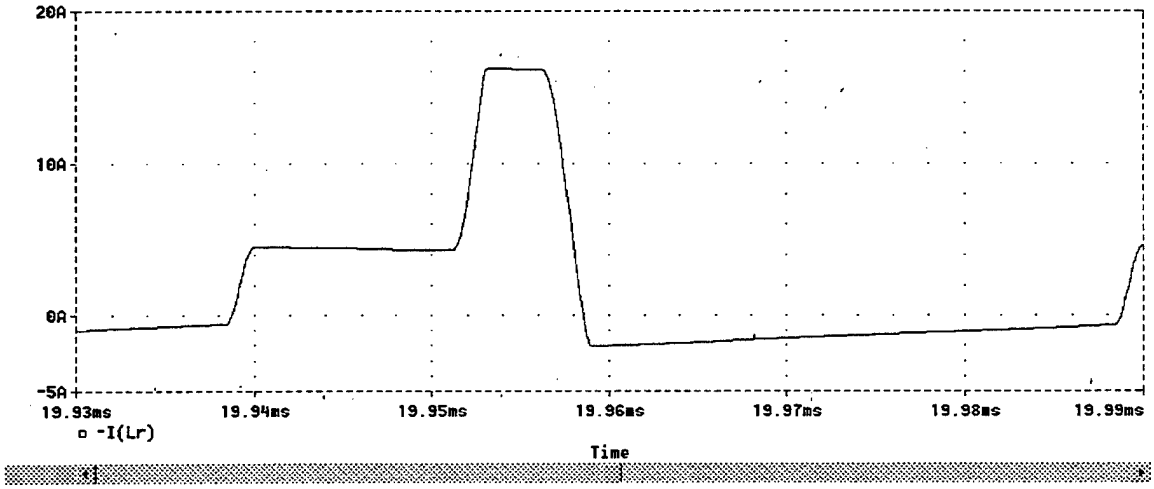
Figure 37 - High Power PSPICE Model



(a) Voltage Across Main Switch



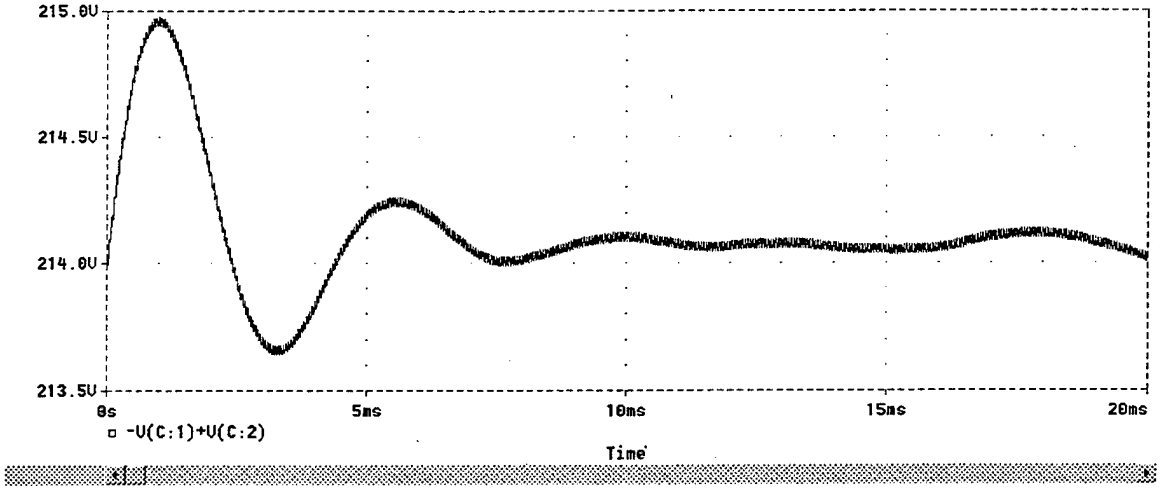
(b) Voltage Across C_{r2}



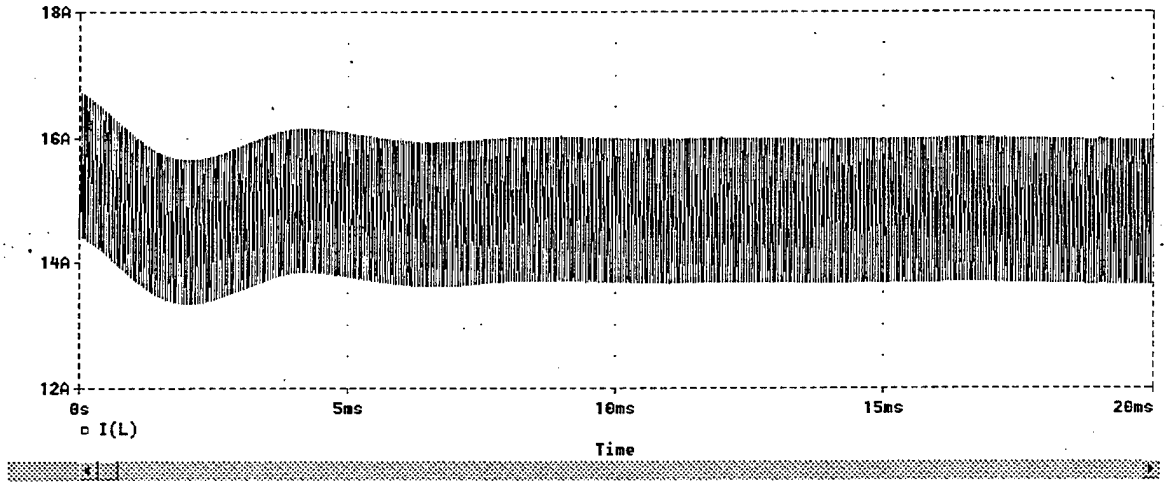
(c) Current Through Resonant Inductor L_r

Figure 38 - V_{dc}=300V, R=14.42Ω, 20kHz

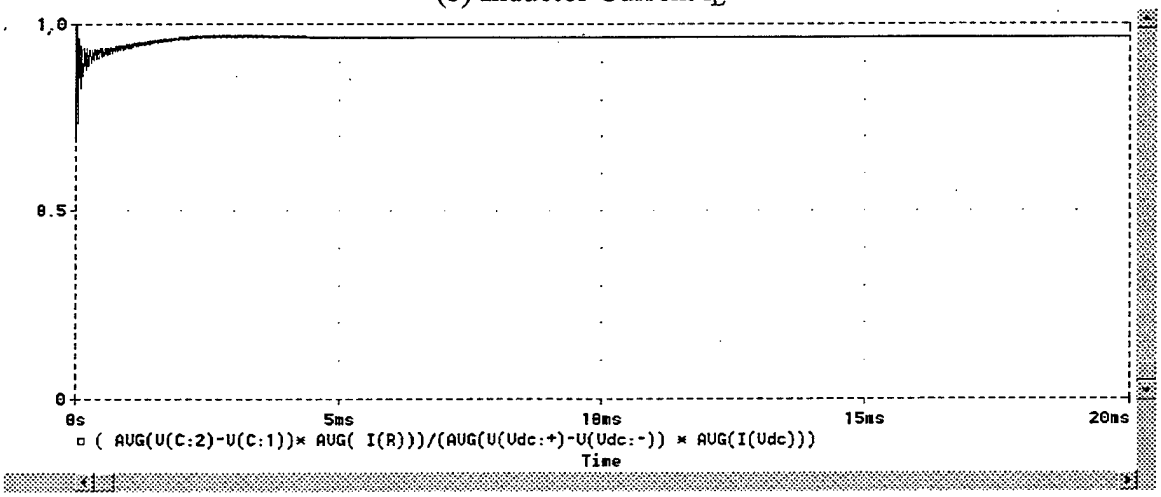
Initial Conditions: V_{cr1}=300, I_L=15A, V_c=214V



(a) Output Voltage V_c

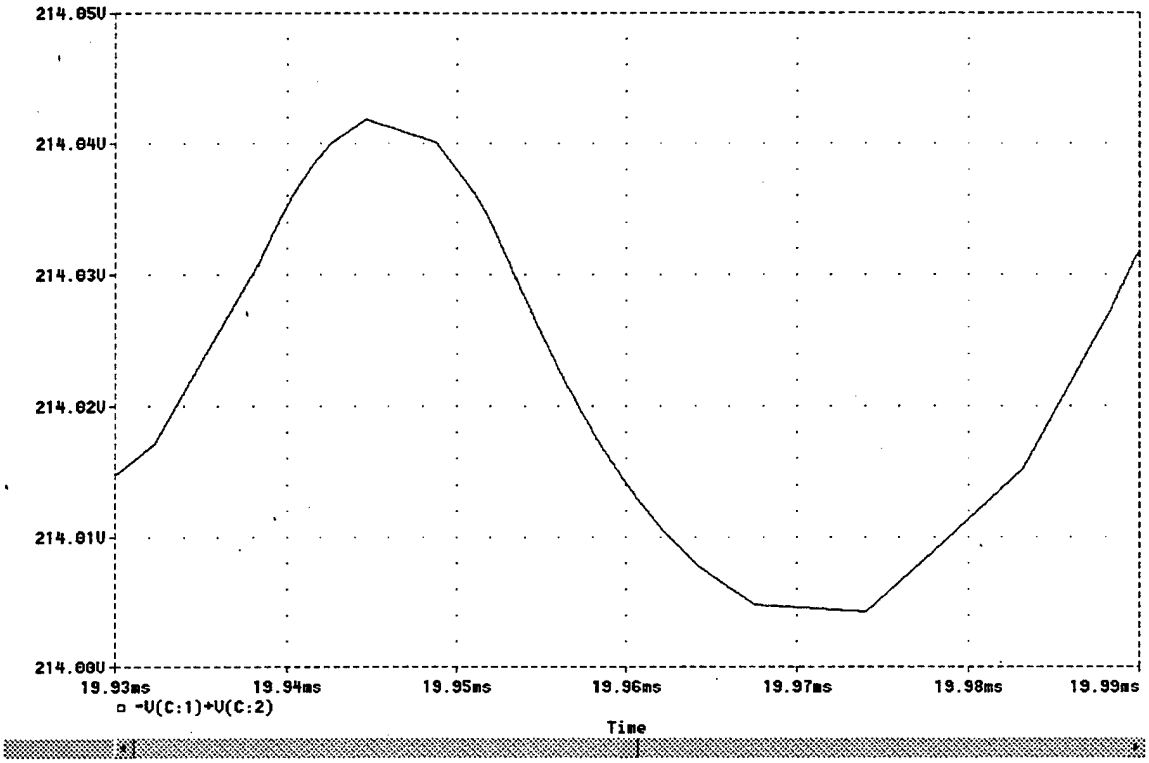


(b) Inductor Current i_L

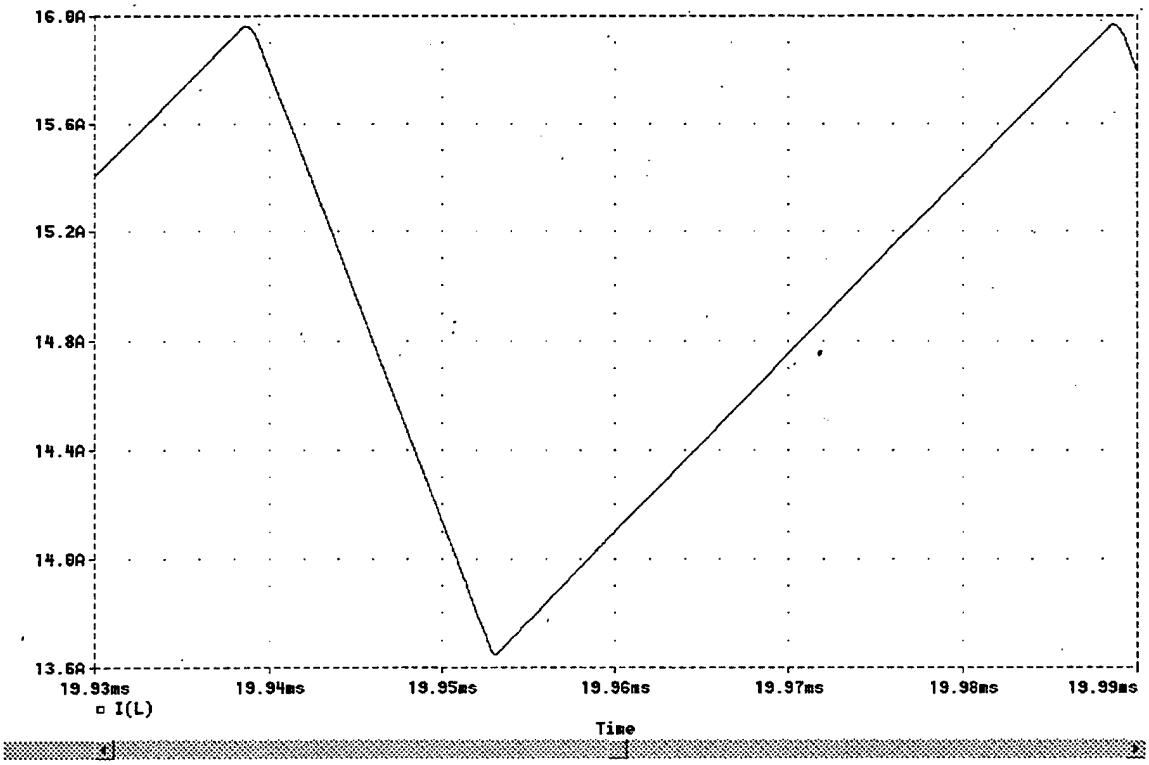


(c) Efficiency

Figure 39 - V_{dc}=300V, R=14.42Ω, 20kHz



(a) Single Switching Cycle of the Output Voltage



(b) Single Switching Cycle of the Inductor Current

Figure 40 - V_{dc}=300V, R=14.42Ω, 20kHz

Conclusion

The Navy's interest in implementing a DC Zonal Electric Distribution System (DC ZEDS) in the next generation of surface combatant (SC-21) has lead to considerable research work into both dc-dc converters and dc-ac inverters. The dc-dc converters, coined Ship Service Converter Modules (SSCMs), are intended to be multi-functional units containing the power section, sensing components and the requisite DSP control hardware and software. The SSCM requirements are somewhat unique as compared to most other dc-dc converter power supply applications. First off, the SSCM will be high power, with unit ratings on board ship exceeding 100kW. It is also desirable that the switching frequency of the SSCM be maximized to facilitate a compact design with the highest possible control bandwidth. The SSCM is a step-down converter and must be very efficient to reduce distribution losses. The construction must be rugged to ensure a high degree of reliability in the hostile environment of a surface combatant. Finally, the SSCM must be capable of parallel operation so that multiple such units can be combined to source larger loads while sharing the output current proportionately.

Currently, SSCM prototypes are hard-switched converters. Each time the switching elements are turned on or off, a switching loss is encountered. Therefore, the fast switching frequencies required for a rapid transient response are ultimately limited by the maximum admissible switching losses imposed by the switch, heat sink and cooling process. In addition, the abrupt circuit changes in a hard-switched converter leads to considerable EMI that contributes further design complications. Thus, switching losses, switch stresses and EMI concerns have motivated the consideration of a relatively new class of converters called resonant converters.

Several resonant converter topologies were briefly introduced in the Background section of this report. There is a variety of different circuits. Some operate with a fixed switching frequency while some require the switching frequency to be varied in order to exert regulation over the output voltage. The bulk of the circuits described operate under Zero-Voltage-Switching (ZVS) or Zero-Current-Switching (ZCS) conditions. There are quasi-resonant converters and multi-resonant converters. Fortunately, there are no quasi-multi-resonant converters. From the list of candidate topologies, one circuit emerged with several attractive features and with no over-riding negative concern. In particular, the candidate circuit was such that existing hardware could be easily modified to accommodate the additional auxiliary circuit components. Also, the control is very straightforward and will not require significant re-engineering. The circuit does not exhibit any large voltage or current stresses and the auxiliary circuit does not introduce any significant losses. Finally, the soft-switching characteristics of the converter can be extended over a large load range, down to light load.

This report has sought to accomplish the following six tasks as pertained to the selected circuit. First, the modes of operation were identified in the sequence of a normal steady-state cycle. Next, the differential equations governing each mode were identified and the transition conditions between the various modes clarified. Third, an ACSL simulation was structured and then studies conducted to illustrate the converter operating modes. The fourth task involved laying out some approximate governing equations for the resonant modes and using these equations to infer a synthesis procedure for the converter parameters. Fifth, a section was devoted to design nuances and important issues regarding circuit realization. These suggestions are intended to guide the designer in fabricating an operational unit. Last, a PSPICE simulation was structured in order to validate the ACSL simulation and to provide further design guidance. In particular, the PSPICE simulation facilitates the inclusion of actual device characteristics which are particularly important for low-voltage designs and high-frequency designs.

The final aspect of the analysis of this converter involves prototyping. The particular circuit under consideration was built in the NPS Power Systems Lab and some data and waveforms were collected. The implementation was at low voltage (50V) and low switching frequency (2kHz) but the data did confirm soft-switching operation. The next step is to fabricate a unit at higher voltages and a higher switching frequency. The unit should then be evaluated for startup, load dump, load cycling (10%-100%-10%-%100), and over-current conditions. The data of interest includes efficiency, output voltage regulation, current regulation and noise.

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