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THESIS

THE CLOSED-LOOP CONTROL OF A THREE-PHASE
INVERTER USING A DSPACE DS1102 DSP BOARD

by

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December 1998

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13. ABSTRACT *(maximum 200 words)*

Due to enhanced reliability, reductions in cost, and ease of maintenance, the U.S. Navy has decided to shift from radial electrical distribution to DC zonal distribution for shipboard use. Correspondingly, the construction of newer classes of combatant vessels will replace bulky transformers with semiconductor switching DC-DC converters and DC-AC inverters. Electrical Control Units, ECUs, control these converters and inverters. Development of an ECU begins with a prototype design, used by the engineer to test the ability of an experimental algorithm to control a physical system. This thesis research examines the use of the DSPACE DS1102 DSP board as a prototype ECU for a three-phase inverter. A DS1102 monitored currents at the output of a three-phase power MOSFET bridge, performed the signal processing, and accordingly provided the MOSFET gating signals. This research compared several different algorithms, time steps and integration methods implemented by the DSP board. In the experiments, the inverter powered a simple RL load and an induction motor. For the closed-loop control of the induction motor, a speed control algorithm provided command inputs to the previously tested inverter. This thesis research demonstrates that the DS1102 can quickly and effectively prototype the signal processing and control units of the electrical power distribution systems of future U.S. Navy ships.

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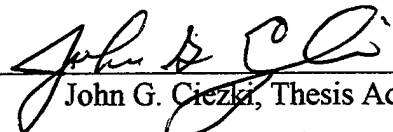B.S., United States Naval Academy, 1990

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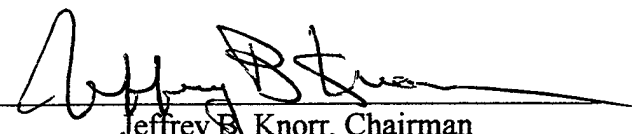
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ABSTRACT

Due to enhanced reliability, reductions in cost, and ease of maintenance, the U.S. Navy has decided to shift from radial electrical distribution to DC zonal distribution for shipboard use. Correspondingly, the construction of newer classes of combatant vessels will replace bulky transformers with semiconductor switching DC-DC converters and DC-AC inverters. Electrical Control Units, ECUs, control these converters and inverters. Development of an ECU begins with a prototype design, used by the engineer to test the ability of an experimental algorithm to control a physical system. This thesis research examines the use of the DSPACE DS1102 DSP board as a prototype ECU for a three-phase inverter. A DS1102 monitored currents at the output of a three-phase power MOSFET bridge, performed the signal processing, and accordingly provided the MOSFET gating signals. This research compared several different algorithms, time steps and integration methods implemented by the DSP board. In the experiments, the inverter powered a simple RL load and an induction motor. For the closed-loop control of the induction motor, a speed control algorithm provided command inputs to the previously tested inverter. This thesis research demonstrates that the DS1102 can quickly and effectively prototype the signal processing and control units of the electrical power distribution systems of future U.S. Navy ships.

TABLE OF CONTENTS

I. INTRODUCTION

A. U.S. NAVY SHIPBOARD ZONAL ELECTRICAL DISTRIBUTION SYSTEM

For several advantageous reasons including enhanced survivability and reduced platform cost [1], the U.S. Navy intends to shift from radial electric power distribution to zonal distribution in its next generation surface combatants. In this arrangement, a starboard and a port main bus supply high voltage DC power to each zone within the ship. The anticipated voltage levels range from 1200V to 2000V, as dictated by available semiconductor switch technology. A power converter buffers the main bus and the intra-zone electrical loads, as it steps down the voltage to a DC level between 850V and 950V. Within the zone, additional converters and inverters adjust the DC voltage to the level and the form needed to supply the particular loads within the zone. Isolation of shipboard power requirements into zones and implementing a zonal distribution architecture offers significant reductions in the size, weight and cost of the platform.

For robustness, each individual converter and each inverter has its own Electrical Control Unit, ECU, performing the monitoring and controlling functions. To evaluate algorithms for possible implementation in ECUs, a German company, DSPACE GmbH, manufactures a very versatile DSP controller board, the DS1102 [2]. The controller board plugs into the AT/PCI slot of a host personal computer. Along with Matlab's Simulink application software, the host computer becomes a means to devise a system controller. The host computer compiles the Simulink file representation of the proposed controller, then downloads executable code into the DS1102 DSP controller board. Through the DS1102 Input/Output (I/O) ports, the controller

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board can monitor and control the sensors and actuators of systems, including power converters and inverters. The ease of programming the DS1102 allows the controls engineer to test the effectiveness of any control algorithm within the limitations of the DS1102. From the insight obtained through this thesis research, the DS1102 allows the engineer to create a prototype controller for shipboard inverter and converter systems.

B. THESIS OBJECTIVES

The main objecitve of this research is to evaluate the utility of the DS1102 DSP board to the Navy. An investigation into the operation and capabilities of the DS1102 controller board system would ascertain its capacity to prototype a control system for shipboard electrical power applications. Clearly, ease of programming the DS1102 through Simulink allows an engineer to rapidly adjust and optimize an algorithm. The dual microprocessors and I/O suite allow considerable complexity in an algorithm. A thesis study of the performance of this versatile DSP board as a controller for a three-phase inverter would provide insight into realization and implementation issues. Two secondary objecitves support the main objective.

1. To implement the closed-loop control of a three-phase inverter.

The DS1102 provides an avenue to realize, with equipment readily available in the Electrical and Computer Engineering (ECE) Power Systems Lab at the Naval Postgraduate School (NPS), the closed-loop control of a three-phase inverter. Since the DS1102's host computer has the capability to record sensor outputs, along with control algorithm variables, it allows the control engineer the opportunity to optimize a control algorithm by running multiple tests to reveal cause-and-effect relations between the control algorithm and the physical plant.

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2. To develop a robust physical plant interface for the signal processing equipment.

The design of the interface between the I/O subsystem and the sensors and actuators deserves some careful consideration. For the three-phase inverter, two Hall effect current sensors monitor the plant, while six power MOSFETs function as actuators, whose control regulates the physical plant activity. Sensitive components at the interface require over-current, over-voltage, and ground-loop protection. The Hall effect current sensor requires calibration in order to shift and scale the output to appropriate levels that the DS1102 can read through its Analog-to-Digital (A/D) converter input port.

C. EXAMPLES OF USE OF DSPACE BOARDS

The ECE Power Systems Lab at NPS currently holds two DS1102 controller boards in its inventory. Three students in the ECE Power Systems option have previously implemented the DS1102 in their thesis research projects. LT Mark Oberley used it to control one phase of an auxiliary resonant commutated pole converter [2]. LT Brian Tait assembled a slip energy recovery system and implemented a speed control loop [3] . LCDR Homer Blalock applied the DS1102 in the feedback control of buck-configured DC-DC converters [4].

Universities and industry have demonstrated many uses for DSPACE controller boards. In the automotive field, Delphi Chassis Systems in Dayton, Ohio tests algorithms for braking systems with DSPACE equipment. Toyota Motor Corporation uses the DSPACE toolset in the design of fuel injection control. Audi engineers developed an engine simulator for virtual test drives of a load panel with real engine components. At the Technical University of Ilmenau, Germany, an interdisciplinary team used a DSPACE control system to develop a prototype of a

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planar multi-coordinate drive with a precision of 0.2 μm for applications in microassembly. Prof. Huang in the aerospace department at NPS currently conducts research on vibration and dampening systems using a DS1102. The diverse nature of systems controlled by DSPACE equipment attests to its capabilities as a tool in the design of control units.

D. THESIS CHAPTER OVERVIEW

Chapter II introduces the DS1102 DSP board and the capabilities of the two microprocessors and various I/O devices contained within the board. The software required to operate the DS1102 also receives some attention in this chapter. Chapter III contains a discussion of the interface between the DS1102 and the sensors and actuators through which it monitors and regulates the operation of the inverter system. Chapters IV and V document the performance of the inverter system powering a simple RL load using open-loop and closed-loop control algorithms, respectively. Chapter VI explains the addition of an induction motor speed control algorithm to the inverter algorithm and presents the laboratory implementation. Chapter VII contains several observations and an enumeration of the work completed.

II. DSPACE

A. DS1102 OVERVIEW

The DSPACE DS1102 Digital-Signal-Processing (DSP) controller board and its associated software, in conjunction with Matlab Simulink, provides a very quick and accurate means for developing control systems. The following eleven step procedure illustrates the development process:

1. Identify plant control objectives.

2. Select actuator and sensor components.

3. Model the plant/actuator dynamics in Simulink.

4. Select a control architecture.

5. Model and integrate controller with plant/actuator.

6. Establish required control gains through simulation.

7. Develop interface between DS1102 and hardware.

8. Extract desired control structure from Simulink.

9. Develop DS1102 I/O with DSPACE software.

10. Compile and download program into DS1102.

11. Conduct hardware studies.

During the initial investigations of this thesis, a balanced three-phase wye-connected resistor-inductor (RL) load represented the physical plant, a three-phase bridge inverter was the actuator, and a proportional-integral (PI) controller regulated the three-phase current supplied to the RL load. The Simulink model of the physical plant along with its controller facilitated initial

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testing of the controller design, the establishment of control gains, and the validation of transient performance. The real-time (RTI31) application software later translated the controller design into code which the DS1102 executed.

Once satisfied with the Simulink model's system response, the engineer may turn to the DS1102 tools available to continue the controller design. The DS1102 controller board performs two separate functions in the design process: rapid control prototyping (RCP) and hardware-in-the-loop simulation (HIL).

During RCP, the engineer programs the DS1102 controller board to perform the functions of a controller which he has already successfully tested in Simulink. Sensors and actuators connect to the input/output (IO) ports of the DS1102 controller board to allow it to control the physical plant. If the controller design operates correctly, the engineer may build a dedicated Electronic Control Unit (ECU), based on the design programmed into the DS1102. RCP bridges the gap between the initial Simulink computer model and the physical plant, permitting the evaluation of the effects of quantization, sample rate, and the performance of algorithms prior to incurring the cost of building an ECU. RCP may uncover glitches in the design at an early stage, prior to the commitment of expensive hardware resources.

After production of the ECU, the engineer may resort to the DS1102 controller board to conduct HIL simulations that rigorously test the robustness of the new ECU, without having to arrange costly experiments involving the physical plant. Opposite of RCP testing, where the DS1102 controller board emulates the ECU, HIL simulation employs the DS1102 to emulate the physical plant, so the engineer can evaluate the performance of the new ECU as it executes control of the physical plant model programmed into the DS1102. Beyond reducing costs and

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speeding up development, HIL testing can simulate the performance of a physical plant under severe conditions.

For example, to test a new ECU, the designer of an anti-lock braking system may model the characteristics of an automobile braking over wet pavement using a DS1102 controller board. The designer can run multiple tests under any conceivable scenario without ever having to mount the new ECU on an automobile. He also would not have to wait for the first snow of winter to test the ECU performance on an icy road.

To conduct an HIL simulation for the testing of the three-phase inverter's ECU, the DS1102 simulates the behavior of a wye-connected three-phase RL load while the dedicated ECU regulates the current supplied to the load. With the DS1102 simulating the physical plant, the engineer does not need to worry about jeopardizing expensive equipment. The testing can safely reach extreme conditions, such as evaluating the new ECU's performance in overcurrent conditions, which might exceed the current limits of power MOSFET switches or other sensitive devices. HIL simulation provides a simple method to test a new ECU under worst case conditions.

B. HARDWARE

1. Architecture

The DS1102 DSP controller board plugs into the Industry Standard Architecture (ISA) slot of the host IBM-PC/AT compatible computer. Inside the core of the DS1102 lies the Texas Instruments TMS320C31 floating-point microprocessor [2]. The TMS320C31 receives its program from the host computer in object code form. To accelerate the TMS320C31, a

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TMS320P14 slave-DSP handles certain computationally heavy digital I/O functions, such as the pulse-width-modulation (PWM) routine employed by the three-phase inverter. A bit-selectable 16-bit I/O port governed by the slave-DSP can satisfy digital I/O requirements. A total of 4 analog-to-digital (A/D) converters and 4 digital-to-analog (D/A) converters encompass the analog I/O capabilities. Two incremental phase encoders, intended for use in conjunction with optical sensors, can perform speed monitoring functions with rotating machinery.

2. Board Installation

As with any sensitive electrical component, one must take precautions against electrostatic discharge while handling the DS1102 by grounding oneself. In addition, the host must have no power during the plugging and unplugging of the board.

The DS1102 plugs into the host IBM-PC/AT compatible computer's 6.2" (ISA) slot. The host must deliver 2A on the 5V line and 100mA on the ± 12V lines. To meet set-up and hold times in the DS1102 access registers, the host clock frequency must not exceed 8.33MHz during expansion bus access. Prior to plugging in the DS1102, one must set the appropriate port address.

The host must have available ten unused consecutive 8-bit I/O ports (ten unassigned port addresses) in the host 64K I/O space. The host will then use the ten ports to read and write to the primary registers in the DS1102. The host computer incorporates the addresses of the ports corresponding to the DS1102's primary registers into its I/O address space table in accordance with a manual 8-bit switch on the bottom of the board. One may have to manually change the address on the 8-bit switch if it conflicts with the addresses for other devices on the bus, such as

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the printer. From left to right, the bits on the switch correspond to address bits A15, A14, A9, A8, A7, A6, A5 and A4. Bits A13 and A12 are "don't care" bits, and A11 and A10 are always treated as binary zero. The base address corresponds to the switch settings of A15 thru A4 plus zero for A3 thru A0. The board arrives from the factory set to 0300H, so the ten consecutive addresses 0300H thru 030AH port to the DS1102.

3. Execution key

Also known by its German name, dongle, the execution key connects to the parallel printer port of the host computer. The matching correct license entry resides in the text file *C:\dsp_cit\citfiles\license.dsp*. Appendix A shows the license file.

Line	Source
INT0	user defined external port input
INT1	incremental encoder
INT2	incremental encoder
INT3	host computer

Table 2-1. TMS320C31 interrupt request lines.

4. Texas Instruments TMS320C31 DSP

The TMS320C31 floating-point DSP can perform several operations during its 50 ns single cycle instruction execution time. In addition to the real-time interface to Simulink (RTI31) method of generating object code for the TMS320C31, other compilers allow the use of high-level languages for application development. The bus arbitration feature makes all off-chip

memory directly accessible to the host for fast download operations. The TMS320C31 has four interrupt request lines. Table 2-1 lists the sources which may issue interrupts along with their respective lines in order of priority. Line INT0 has the highest priority.

5. A/D and D/A Subsystems

The DS1102 DSP controller board contains two 16-bit A/D converters and two 12-bit A/D converters with conversion times of 10 μs and 3 μs, respectively. The four 12-bit D/A converters have a 4 μsec settling time. The A/D converters have a ± 10V span at the external (input) end, and a dimensionless signal with a range of ± 1 at the internal (output) end. The D/A converters on the controller board have a ±1 dimensionless internal (input) span and a ± 10V external (output) span. The use of separate ground return lines for each sensor connected to an A/D or D/A converter isolates sensor grounds and prevents the formation of ground loops.

The A/D converters introduce a scaling factor which divides the input signal by 10, so 1/10th of the value of the input voltage appears in the converter's data register. For example, an A/D converter will produce a value of -0.5 for an input signal with a value of -5V. Conversely, D/A converters introduce a scaling factor which multiplies by 10 the value in the data register, so a voltage 10 times the value in the converter's data register appears at the output of the D/A converter. The control engineer programming the DS1102 for an application must take this peculiarity into consideration, particularly in the selection of feedback control gains.

6. Pulse-Width-Modulation (PWM) / Frequency Generation Subsystem.

The TMS320P14 slave-DSP handles PWM functions. Similar to the D/A converter, its

input value must range from -1 to +1 to produce a 0 % to 100% duty cycle. A 0 input produces a 50 % duty cycle. The subsystem can generate up to six outputs with a selection of 8, 10, 12 or 14- bit resolution. Double-clicking on the Simulink PWM unit icon brings up a menu for selecting the PWM unit's resolution. The resolution parameter governs the accuracy of the output duty cycle. Table 2-2 shows the frequency-to-resolution correlation.

freq. (kHz)	resolution (bits)	resolution (nsec)
100	8	$1/(2^8 \text{x} 100\text{k}) = 39$
25	10	$1/(2^{10} \text{x} 25\text{k}) = 39$
5.7	12	$1/(2^{12} \text{x} 5.7\text{k}) = 42$
1.6	14	$1/(2^{14} \text{x} 1.6\text{k}) = 38$

Table 2-2. PWM unit resolution settings.

The frequency generation module can generate square wave signals from 0.01Hz up to 10kHz. For vibration and dampening testing applications, the frequency generator may produce a signal to trigger a transducer to pulse at a particular frequency. This module cannot operate simultaneously with PWM.

C. SOFTWARE

1. Requirements

The 1994 version of the DS1102 controller card available presently in the ECE Power Systems Lab at NPS requires a host computer installed with the following software versions:

    a. Texas Instruments C Compiler Version 4.50. The C compiler converts C code into object code that the DS1102 can execute. This Texas Instrument software

should reside in the hard drive *C:\c30tools* directory. Several batch files in the

DSPACE software expect to find the Texas Instrument files in this directory.

b. Matlab Version 4.2.

c. Simulink Version 1.3.

d. Real-Time Workshop (C code generator) Version 1.1.

e. MS-DOS Version 5.0 or newer.

The host should have at a minimum 8 Mbytes of physical memory and a permanent

Windows swap file of at least 12 Mbytes.

2. Program Loader (LD31)

The LD31 utility program loads the object code into the DS1102 controller board and

enables the execution of object code. Upon installation, the LD31 distribution diskette creates

the directories *C:\dsp_cit\exe* and *C:\dsp_cit\citfiles* in the hard drive. The *citfiles* directory

holds the system setup file containing the I/O-port base address of the DS1102 controller board.

Upon initial invocation, the LD31 program requests the user to enter the start address of the

selected I/O port address range, determined by the 8-bit switch on the bottom of the board.

Since the LD31 program accesses the DS1102 system setup file via the environment variable

citfiles, the *autoexec.bat* file should contain the line

   set citfiles = C:\dsp_cit\citfiles

As a matter of convenience, to allow invocation of the LD31 program from any directory, the

path command line in the *autoexec.bat* file should include the path *C:\dsp_cit\exe*.

To invoke LD31 from the DOS prompt, the user should type *ld31*. The LD31 menu

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offers 6 options:

     a. Load object file - downloads an executable object file to the DS1102.

     b. Restart DSP - initiates execution of the object file.

     c. Reset DSP - suspends execution of the object file.

     d. Select slave application - loads an object file into the TMS320P14 slave DSP

only.

     e. Quit LD31 and disable DSP

     f. Quit LD31 - terminates LD31 without changing the operating state of the

DS1102. This option frees the host to execute other applications after it has

downloaded and started execution of the DSP, such as TRACE31, which

monitors the variables defined in the Simulink model.

After LD31 completes a download, it invokes the program CHCKER31 to check proper

operation of the application program and brings up an error message if it detects an overload

condition in the DSP. Should an overload occur, reducing the step size of the integration

algorithm might solve the problem without resorting to modifying some more fundamental

aspect of the Simulink model. The complexity of the controller model for the three-phase

inverter allows a minimum step size of 0.0002 s for the Euler integration algorithm.

3. Real-Time Interface to Simulink (RTI31).

The DSPACE Real-Time Interface transforms a Simulink model into an object code

module that the DS1102 controller board hardware can execute.

From the Simulink toolbar, selecting the *code* menu, then the *real-time options* brings up

the real-time options dialog box. Here the user may set the integration options. The rest of the

blocks in the dialog box should read:

     a. *Output File:* - should remain blank.

     b. *Template Makefile: rti31.tmf* .

     c. *Target Makefile: $model.mk* .

     d. *Build Command: make_rt* .

Clicking on the *Build* button on the dialog box invokes the Real-Time Workshop, which

begins the conversion process by generating C code from the Simulink model. Then RTI31

executes the Matlab m-file *make_rt* to create an application specific makefile called

model_name.mk, based on the RTI31 template makefile *rti31.tmf.* Here *model_name* represents

the original name of the Simulink model. The *make* utility then invokes *model_name.mk,* which

sequentially calls the following:

     a. The RTI Model Postprocessor, which modifies the generated C code of the

     model for implementation on DSPACE hardware. The postprocessor generates

     all application-specific setups and I/O function calls.

     b. The Texas Instruments Compiler/Linker which compiles the model and the

     DSPACE real-time simulation frame, and combines the object files and libraries

     into an executable image of the model.

     c. The loader program, LD31, which automatically downloads and initiates

     execution of the object file.

     d. The error check program, CHCKER31.

D. RAPID CONTROL PROTOTYPING EXAMPLE

1. Create controller block diagram using Simulink on host computer.

2. At the Matlab prompt, type
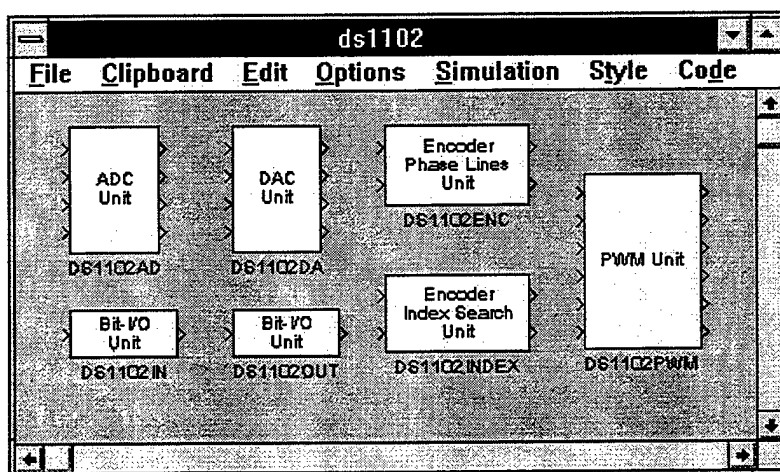
    > *ds1102*

followed by

    > *plugs*

Figure 2-1. DS1102 I/O.

3. From the window shown in Figure 2-1 click and drag selected I/O devices into the controller block diagram window. Of course, only bit-I/O units may appear more than once (up to 16 units per controller block diagram).

4. Click and drag I/O plugs shown in Figure 2-2. Connect the necessary plugs to the external side of the used channels in the I/O devices. The plugs represent the external pins of the DS1102; however, the generic plug icons themselves have no pin numbers. Consult Appendix B for DS1102 I/O device pinout. The ribbon cable provides a convenient connection to the port in the back of the host computer.
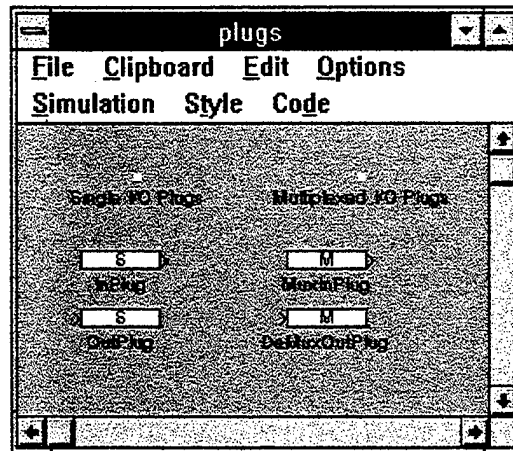
Figure 2-2. DS1102 plugs.

5. When ready to compile and download a Simulink block diagram, select *Code* from

the menu bar at the top, followed by *Real Time Options* from the submenu, to bring up

the *Real-Time Options* window shown in Figure 2-3.
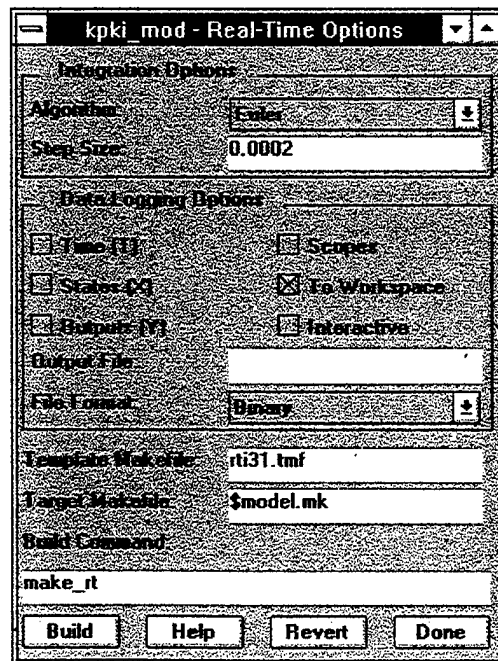

Figure 2-3. Real-Time Options.

6. Except for *Step Size*, the *Real-Time Options* prompts should read as shown in Figure

2-3. The minimum step size allowed depends on the complexity of the block diagram. If

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the requested step size is too small for the block diagram, a *processor overload error* message will appear. Increasing the step size solves this problem but slows down the microprocessor. For the fastest signal processor performance, choose the minimum step size possible and the default integration algorithm, *Euler*. Other integration algorithms can slow the signal processing considerably. Later chapters address this point.

7. Select *build* to initiate the compiling and downloading of the Simulink block diagram. A DOS window appears, showing status messages. The messages *download succeeded* and *DSP started* indicate that the DS1102 has begun its signal processing implementation the algorithm of the Simulink block diagram.

8. Stopping, resetting and reloading the DS1102 requires invoking the program loader application (LD31) from a DOS prompt

     C:ld31

and selecting the respective command from the LD31 menu.

9. Once the DS1102 starts signal processing, invoking the TRACE31 application software allows the option to record the value at the output of any block in the Simulink block diagram. The sampling rate will depend on the step size chosen in the Real-Time Options menu. After saving the sampled data in *.mat* format, it becomes available for further analysis with Matlab.

III. INTERFACE SUBSYSTEMS

A. INTERFACE OVERVIEW

Direct connection of the DS1102 DSP board to the sensors and the actuators could result in exceeding the voltage and current limitations of the I/O components in the board. The interface subsystems protect the board from these conditions. Furthermore, the sensors used in this research generate very low voltage levels, within a range that compromises the resolution of the A/D converters. Part of the sensor interface consists of amplifiers that boost the sensors' signals to optimum levels for the DS1102 A/D converters. The actuator interface protects the DS1102 from overcurrent and prevents short circuits in the MOSFET actuators.
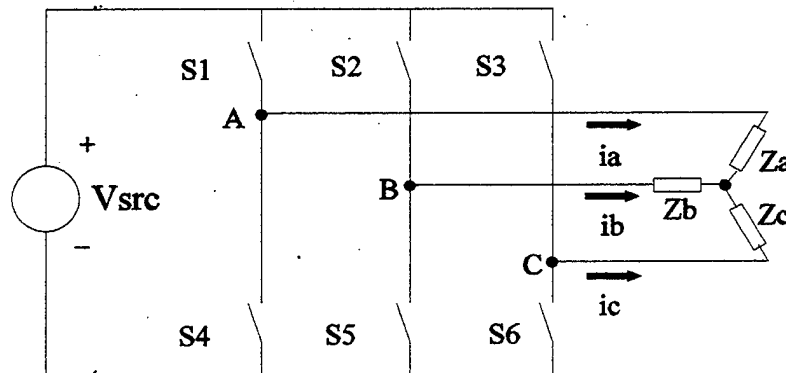

Figure 3-1. Inverter bridge topology.

B. ACTUATOR INTERFACE

The DS1102 generates three PWM signals, corresponding to each leg in the three-phase MOSFET inverter bridge topology, shown in Figure 3-1. Each leg in the bridge has one pair of MOSFET switches. Each MOSFET has a fast recovery diode connected between the drain and

source. The upper rail switches, S1, S2 and S3, connect the load to the high voltage terminal of the DC power source. The lower rail switches, S4, S5 and S6, connect the load to the ground terminal of the DC power source. The state of a switch depends on the PWM signal corresponding to its leg. When a PWM signal goes hi, its corresponding upper rail switch closes and the lower opens, when it goes lo, the upper opens and the lower closes. Also, the PWM signals, directly from the DS1102 PWM unit, cannot simultaneously drive the gates of both MOSFETs in one leg. Should a direct connection exist between the PWM unit and a pair of MOSFETs, the DC power supply would experience a short circuit, large currents would flow, damaging the semiconductor devices. An interface circuit must create a brief time period between the turn-off and turn-on of the upper-rail and lower-rail MOSFET in a leg, referred to as dead time, to eliminate the potential momentary short-circuit state.
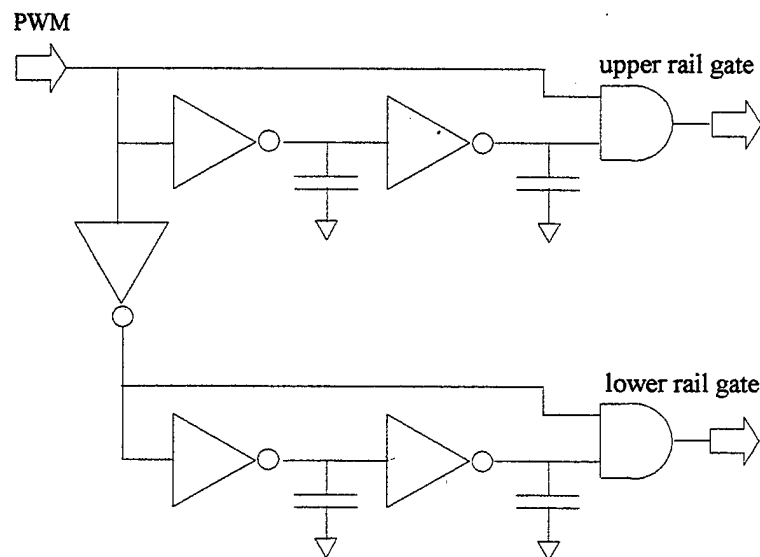

Figure 3-2. Short-circuit-protection-isolation-buffer circuit.

Use of the short-circuit-protection-isolation-buffer circuit shown in Figure 3-2 precludes the possibility of both MOSFETs in one leg being 'on' or 'partially on' during changes in the value of the PWM signal. The circuit guarantees that the upper rail MOSFET remains 'off' whenever the lower rail MOSFET is conducting. Conversely, the lower rail MOSFET remains 'off' whenever the upper rail device is 'on'. As illustrated in Figure 3-1, the PWM signal drives directly one input of the upper-rail AND gate; it also drives an inverter-capacitor-inverter-
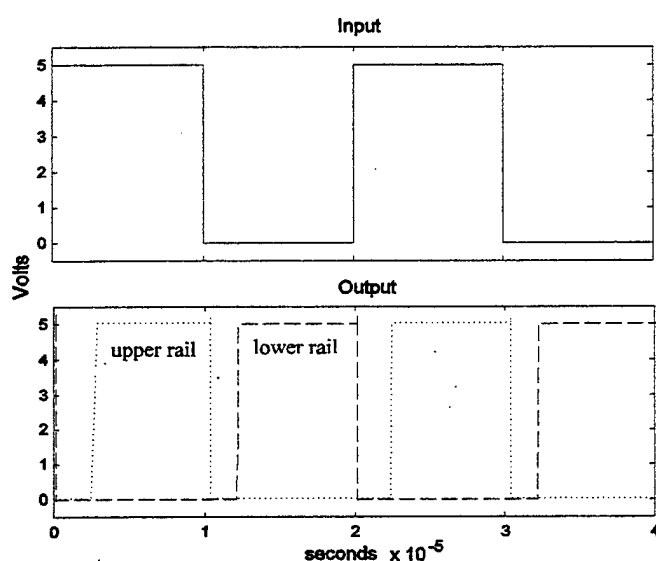

Figure 3-3. Buffer circuit traces.

capacitor sequence at the other input of the same AND gate. The sequence introduces a time delay in the state transitions of the AND gate which has the net effect of reducing the time that the AND gate spends in the hi state, compared to a topology in which both inputs to the AND gate are directly connected to the PWM input, bypassing the inverter-capacitor sequence. A complementary circuit produces a signal to drive the bottom-rail MOSFET. The SPICE file listed in Appendix C was used to simulate the buffer circuit. The signals generated in the SPICE simulation appear in Figure 3-3. The traces show a 2 μsec dead time between the turn-off of one

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transistor and the turn-on of its counterpart on the same bridge leg.

The Lab-Volt power MOSFET module (EMS 8837) houses the six power MOSFETs and corresponding free-wheeling diodes. A toggle switch configures the MOSFETs in a three-phase bridge topology, connecting together the drains of the three upper rail MOSFETs, and separately, the sources of the three lower rail MOSFETs. The module contains circuitry which isolates the gate of each MOSFET and protects the transistors against overvoltage (350V), overcurrent (3A), and overheating (100°C) [5]. The Lab-Volt EMS 8525 power supply console provides power to the isolation and protection circuits through a 24VAC input jack on the power MOSFET module panel.

The inputs to the MOSFET gates require 5V for turn-on and 0V for turn-off. The use of CMOS LSI components to implement the short-circuit-protection-buffer circuit provides the appropriate signal levels to drive the gates.

The buffer circuit schematic shows adequate loading at the output of the DS1102's PWM unit. Each one of the utilized channels in the PWM unit drives one CMOS AND and two CMOS inverters, requiring roughly 15µA, well below the overcurrent limits of the unit (5mA).

C. SENSOR INTERFACE

Hall effect current sensors generate an output current proportional to the monitored current. Appendix D contains specifications for the F. W. Bell CLN-50 (50 A rms) Hall effect current sensors utilized in this laboratory exercise. For a monitored current value of 1 A, the sensor will generate an output current on the order of 1 mA. A 150 Ω resistor between the output of the current sensor and ground produces a linear sensor input/output relation for the

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anticipated current levels of the three-phase inverter, ± 2A maximum. For the anticipated values

of sensor output current and the 150 Ω resistance, the sensor produces output voltages on the

order of tenths of a volt. An operational amplifier in a non-inverting configuration amplifies

these voltage levels while presenting a high input impedance to the sensor output. The

amplifiers have a gain setting such that the maximum peak current in the three-phase inverter,

± 2A, generates the maximum voltage level discernible by the DS1102 A/D converter, ± 10 V.

The non-inverting amplifiers require gain settings of approximately 100 to produce a 10 V

output for 2A through the three-phase inverter lines. Differences between individual current

sensors will cause these settings to vary by about 10%; therefore, the non-inverting amplifiers

have variable resistors which facilitate the calibration of the gain.
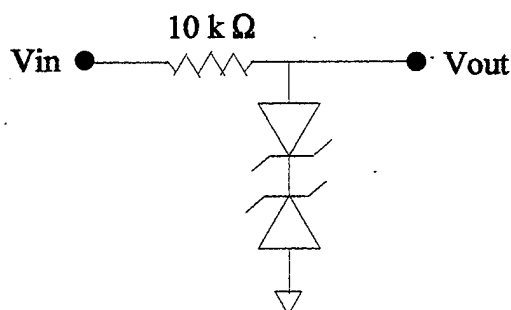
Figure 3-4. Overvoltage protection.

Two zener diodes with a breakdown voltage of 12 V and a 10 kΩ resistor, arranged as

shown in Figure 3-4, protect the DS1102 A/D converter against overvoltage. This arrangement

at the input to the A/D converter limits the levels to ± 12 V, preventing costly damage to the

DS1102.

D. RIBBON CABLE

A ribbon cable in the ECE power lab provides a convenient connection to the DS1102

I/O pins on the back of the host PC. Appendix B contains a table for the ribbon cable pinout [3].

E. SYNOPSIS

The DSPACE RCP setup consists of a DS1102 DSP board and its associated software, including Simulink installed on the host computer. Supported by an adequate interface between the I/O ports and sensors and actuators, the setup provides the means to control a physical plant. The next three chapters document exercises in system control where the physical plant consists of a three-phase inverter supplying current to a simple resistive-inductive (RL) load and an induction motor.

IV. OPEN-LOOP EXERCISE

A. OPEN-LOOP CONTROL METHOD

The control of an open-loop three-phase inverter consists of three 60Hz sinusoidal control signals, for phases A, B, and C, driving three PWM units. The 60Hz sinusoidal signals are displaced by 120°. The output of each PWM unit controls the switch pair in one of the legs in the inverter bridge shown in Figure 3-1. The digital logic complements of the S1, S2 and S3 signals drive the S4, S5 and S6 switches, respectively. For the studies conducted, each leg of the wye-connected load has a 56.5Ω resistor in series with a 30.4mH inductor. With proper control signals gating the switches, the inverter bridge supplies three-phase current to the load.

Simulink serves two purposes in these exercises. Initially, a Simulink block diagram is assembled on a host computer, then used to simulate the performance of an entire system, load/actuator and control. Subsequently, a Simulink control block diagram serves as the code that, after compiling, programs an algorithm into the microprocessor onboard the DS1102. A Simulink model does not contain any DS1102 I/O blocks. A Simulink control block diagram does.
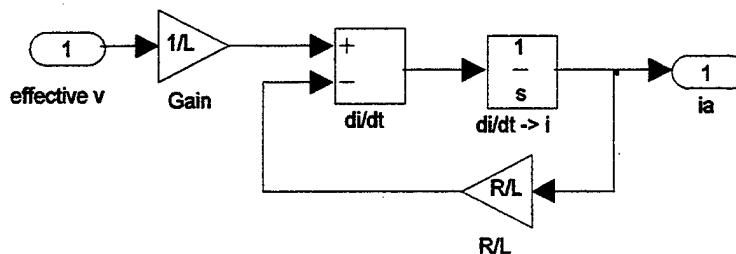

Figure 4-1. R-L load subsystem Simulink block diagram model.

B. SIMULATION

The Simulink subsystem block diagram model shown in Figure 4-1 determines the load current for a given voltage applied to a resistive-inductive (R-L) load. Three of these R-L load subsystem block diagrams within the Simulink model are used to evaluate the current flowing through each leg of the three-phase wye-connected load. The load subsystem block diagram implements the solution for i_a from the following ordinary differential equation

$$V_a \quad = \quad L\frac{di_a}{dt} + i_a R \qquad\qquad \text{(Eqn. 4-1)}$$

S1	S2	S3	S4	S5	S6	Van	Vbn	Vcn
1	0	0	0	1	1	2/3	-1/3	-1/3
1	1	0	0	0	1	1/3	1/3	-2/3
0	1	0	1	0	1	-1/3	2/3	-1/3
0	1	1	1	0	0	-2/3	1/3	1/3
0	0	1	1	1	0	-1/3	-1/3	2/3
1	0	1	0	1	0	1/3	-2/3	1/3

Table 4-1. Effective voltages at load per phase.

To determine the values of the effective line-to-neutral voltages for a balanced wye-connected load in Figure 3-1, consider the valid switch combinations in Table 4-1. A '1' denotes a closed switch, while a '0' denotes an open switch. The fractions correspond to fractions of Vsrc, the DC input voltage to the inverter. For example, the switch combination on the first row of Table 4-1 arranges Zb and Zc in parallel, and the Zb∥Zc pair in series with Za. Consequently, the effective voltage inputs to the load subsystem block diagrams become (2/3)*Vsrc for Za, and (-1/3)*Vsrc for Zb and Zc.

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To generate the switch actuation PWM signal at the input to the switches, the sine-triangular PWM (STPWM) method [7] requires three sinusoidal modulating signals and a high-frequency carrier triangular signal. Three comparators arranged as shown in the model illustrated in Figure 4-2 determine the state of its corresponding pair of switches for one leg the three-phase inverter bridge. For example, if the phase A comparator determines that the phase A 60 Hz sinusoidal control signal is greater than the reference triangular carrier signal, S1 closes and S4 opens; otherwise, S1 opens and S4 closes.
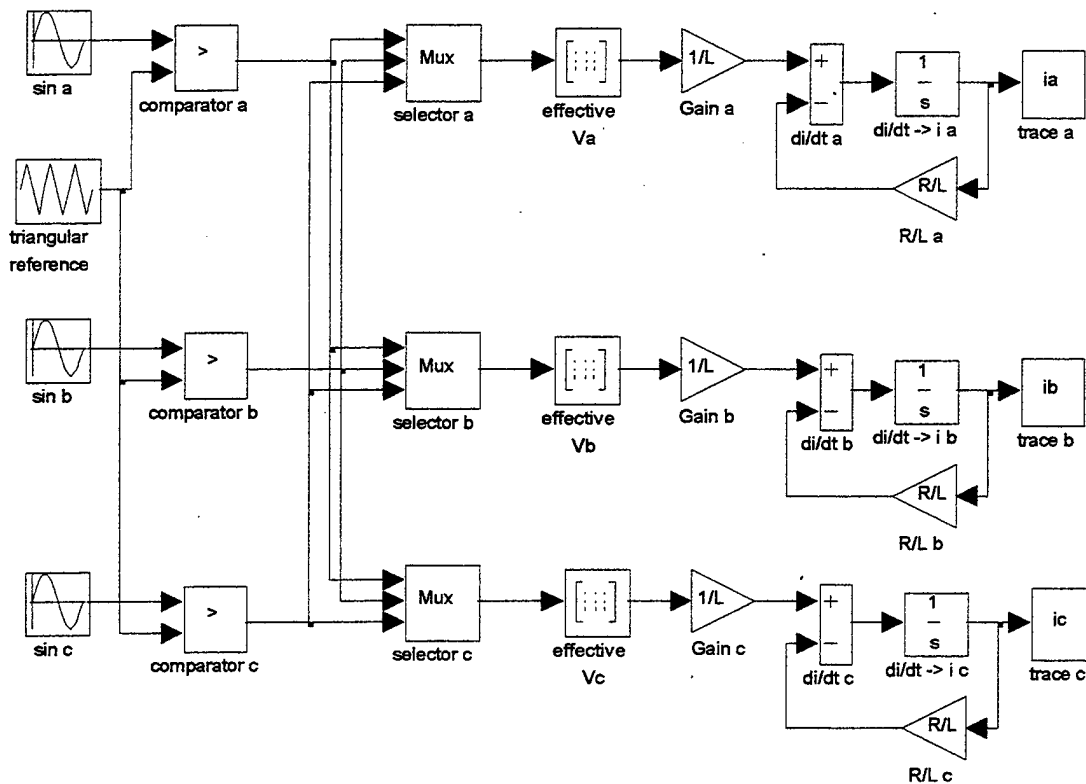

Figure 4-2. Open-loop block diagram model.

Implementation of PWM in Simulink via STPWM requires a triangular waveform generator. The peak value of the carrier, set at ± 1, matches the valid range at the input end of the PWM unit in the DS1102 board. To further imitate the performance of the DS1102 PWM

unit through the simulation, the triangular waveform has the same frequency as the DS1102

PWM unit, 1.6 kHz. Three comparators determine if the ia control, ib control, and ic control

signals exceed the value of the triangular reference. If the control signal for ia, ib, or ic exceeds

the triangular reference, S1, S2, or S3 turn 'on' respectively; otherwise, S4, S5, or S6 turn 'on'

respectively. The STPWM offers outstanding harmonic performance [7]. The DS1102 literature

guarantees 14-bit resolution at a switching frequency of 1.6kHz. A 14-bit resolution translates

into a $1/(2^{14} \times 1600)$=38 nsec resolution, so transitions in the logic level of the PWM output occur
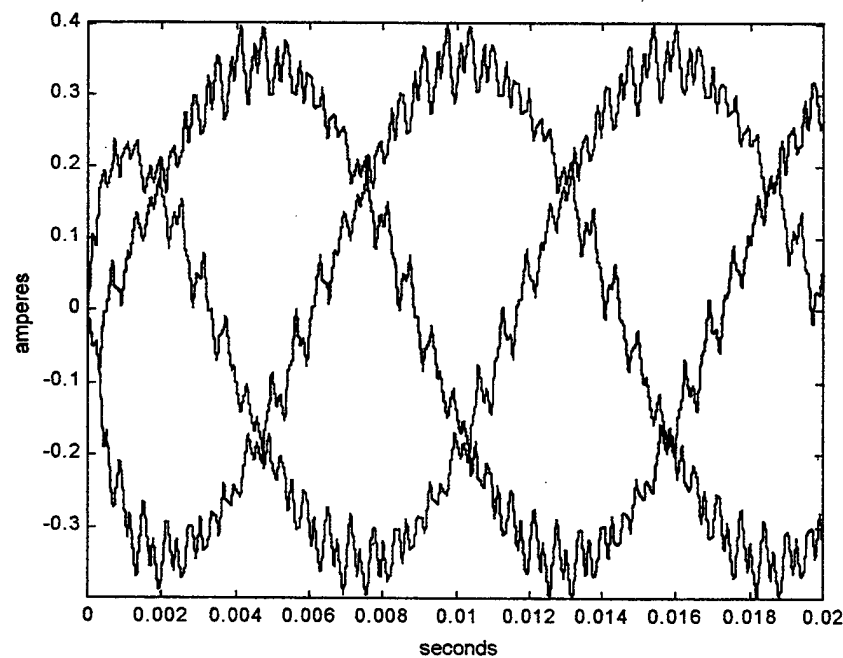
within a ±38 nsec window of error.

Figure 4-3. Open-loop simulation current traces.

The Simulink model of the open-loop controlled three-phase inverter in Figure 4-2

produced the current traces shown in Figure 4-3. The input to the inverter was fixed at 50 VDC.

The three 60 Hz sinusoidal control signals' amplitude remained constant with the peak set at

± 0.8, maintaining the control in the linear modulation region and also avoiding unrealizable

switch times. The simulation predicted peak currrents of ± 0.35A for the system parameters in

source	50 VDC
R	56.17 Ω
L	30.4 mH

Table 4-2. Open-loop system parameters.

Table 4-2. A Fourier transform of the current traces, generated using the Matlab *fft* function,

appears in Figure 4-4, revealing a small loss component at 1600 Hz corresponding to the

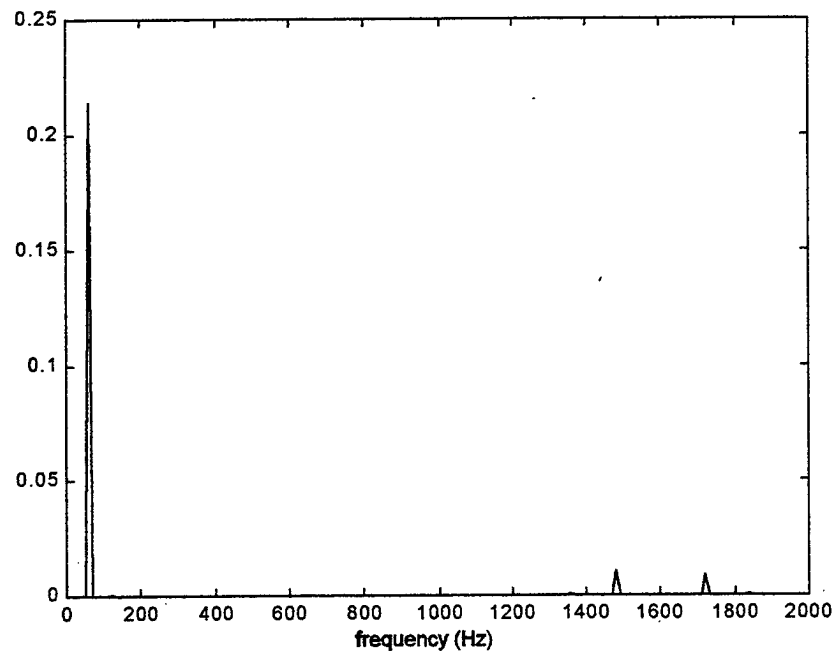frequency of the triangular reference wave.

Figure 4-4. Open-loop simulation Fourier transform.

C. HARDWARE IMPLEMENTATION

Figure 4-5 shows the current traces produced in the implementation of an open-loop controlled three-phase inverter using the DS1102 controller board. The Simulink control block diagram presented in Figure 4-6 programmed the DS1102 to generate three sinusoidal control signals identical (60 Hz, ± 0.8, displaced120°) to the ones used in the simulation of the block diagram model. The sinusoidal control signals drive the PWM unit, which in turn create the gating signals for the power MOSFETs. Note, the hardware implementation does not require a high-frequency carrier triangle signal.
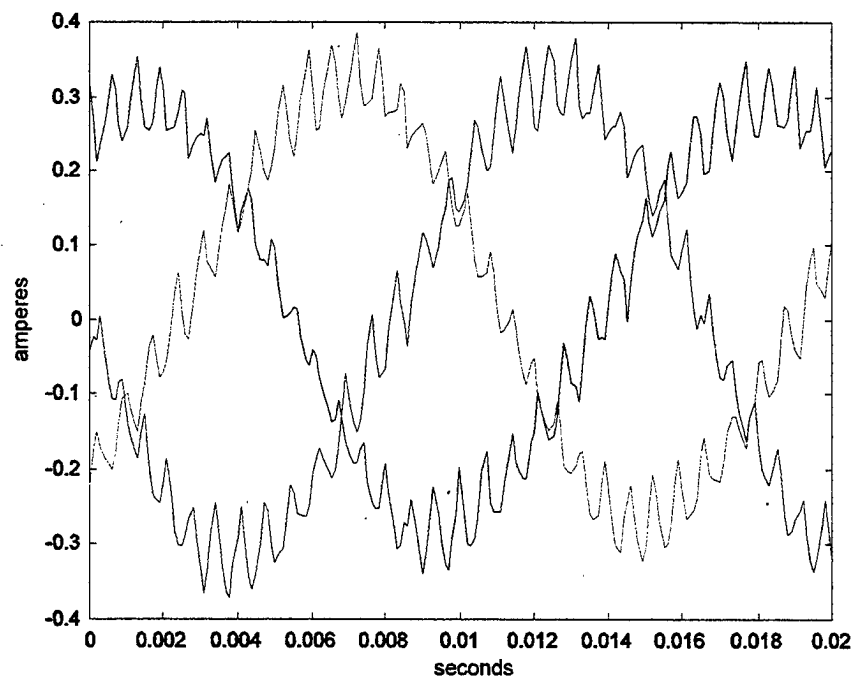

Figure 4-5. Open-loop hardware current traces.

Except for a slight amplitude discrepancy, the simulated current and the actual current traces seem very similar. The actual current reaches a peak of ± 0.3A, a 16.7% decrease from the simulation current trace. The 1.6kHz ripple on the current trace appeared due to the 1.6kHz
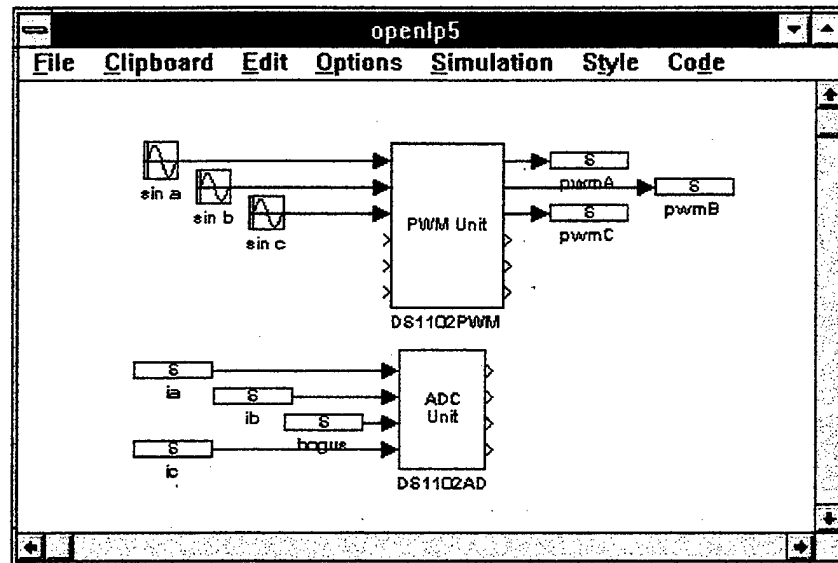
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Figure 4-6. Open-loop control block diagram.

frequency setting of the PWM unit. Hard-switching in the power MOSFETs and other losses

result in smaller amplitudes when compared with the simulation. The Fourier transform of the

actual current trace in Figure 4-7 validates the accuracy of the simulation.
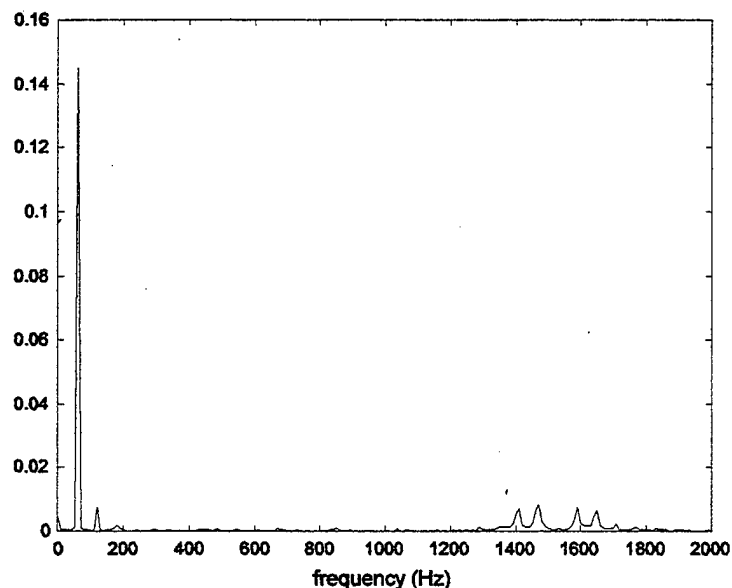
Figure 4-7. Open-loop hardware Fourier transform.

The Fourier transform reveals a small 120Hz component in the three-phase current, which did not appear in the simulation. The DC voltage supply source at the input to the inverter introduced this component. In the ECE Power Systems Lab, to obtain high DC voltages, the three-phase voltage supplied to the Lab must pass through a rectifier circuit which introduces a 120Hz component.

D. SYNOPSIS

The open-loop exercise illustrated the basics of RCP. The DS1102 executed a simple algorithm that demonstrated the compatibility of the PWM unit, the MOSFET actuators and their interface. A more complex algorithm, presented in the next chapter, incorporates a sensor subsystem for closed-loop control.

V. CLOSED-LOOP EXERCISE

A. CLOSED-LOOP CONTROL METHOD

Closed-loop control of the three-phase inverter compensates for circuit non-idealities and improves current tracking. In the simulation exercise the STPWM's modulating signals are functions of the actual load currents. Analogously, in the hardware exercise, the modulating signals at the input of the PWM unit are functions of actual load currents.
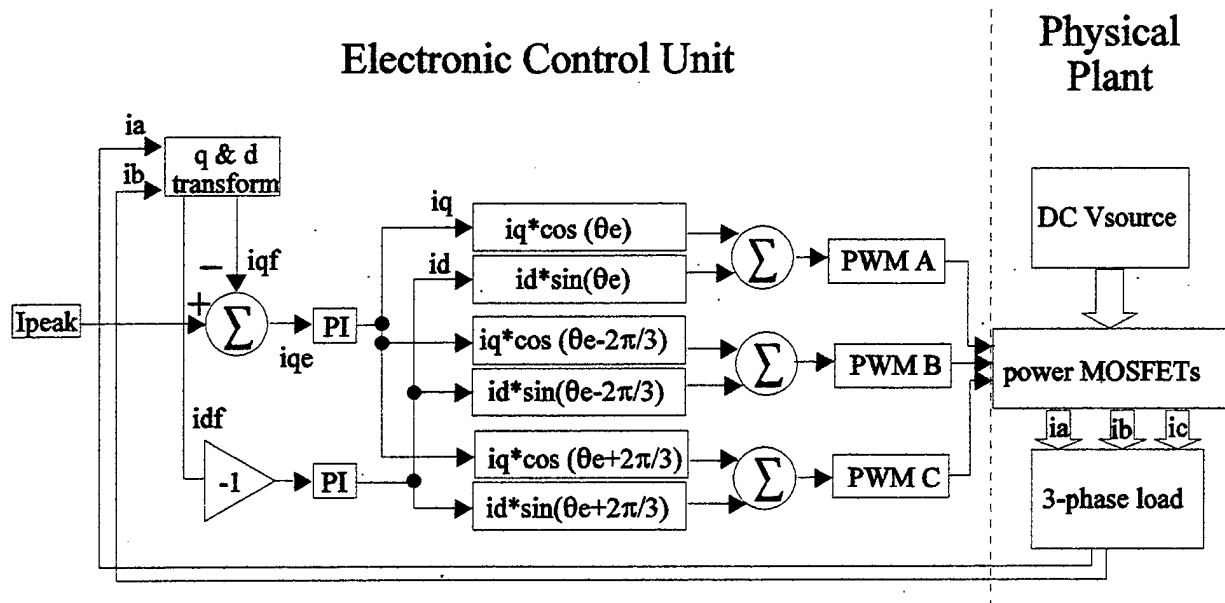
Figure 5-1. Closed-loop overview.

For current control of the three-phase inverter, two Hall effect current sensors provide two feedback signals. These feedback signals are proportional to the instantaneous current in phase A and phase B. Since the load is wye-connected and the sum of the phase currents is zero, measurement of the phase C current is redundant. Application of the q and d synchronous reference frame (SRF) transformations [8] to the current sensor signals produces the feedback

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signals i_q^f and i_d^f. Subtracting the feedback i_q^f and i_d^f signals from the desired I_q and I_d values results in two error signals, i_q^e and i_d^e. Each error signal passes through a proportional-plus-integral (PI) controller to produce i_q and i_d. Finally, transforming i_q and i_d back to the abc-reference frame generates the signals that control the PWM units as shown in Figure 5-1. The angle θ_e is the synchronous reference frame angle that varies at the desired output frequency.

The application of reference frame theory offers the advantage that steady-state quantities are constants in the synchronous reference frame. As a result, the PI controller can guarantee zero steady-state error. The following development illustrates this point. It begins with the desired sinusoidal currents:

$$i_a^* = \sqrt{2} I_s \cos(\theta_e + \phi_s) \qquad \text{(Eqn. 5-1)}$$

$$i_b^* = \sqrt{2} I_s \cos(\theta_e - \tfrac{2\pi}{3} + \phi_s) \qquad \text{(Eqn. 5-2)}$$

$$i_c^* = \sqrt{2} I_s \cos(\theta_e + \tfrac{2\pi}{3} + \phi_s) \qquad \text{(Eqn. 5-3)}$$

where ϕ_s is an arbitrary steady-state phase angle. The q & d reference frame transformation produces:

$$i_q = \tfrac{2}{3}\cos(\theta_e)i_a^* + \tfrac{2}{3}\cos(\theta_e - \tfrac{2\pi}{3})i_b^* + \tfrac{2}{3}\cos(\theta_e + \tfrac{2\pi}{3})i_c^* \qquad \text{(Eqn. 5-4)}$$

$$i_d = \tfrac{2}{3}\sin(\theta_e)i_a^* + \tfrac{2}{3}\sin(\theta_e - \tfrac{2\pi}{3})i_b^* + \tfrac{2}{3}\sin(\theta_e + \tfrac{2\pi}{3})i_c^* \qquad \text{(Eqn. 5-5)}$$

which upon substitution yields:

$$i_q = \sqrt{2} I_s \cos(\phi_s) \qquad \text{(Eqn. 5-6)}$$

$$i_d = -\sqrt{2}I_s \sin(\phi_s) \qquad\qquad \text{(Eqn. 5-7)}$$

from which it can be shown that:

$$\sqrt{i_q^2 + i_d^2} = \sqrt{2I_s^2 \cos^2\phi_s + 2I_s^2 \sin^2\phi_s} = \sqrt{2}I_s \qquad \text{(Eqn. 5-8)}$$

Note that setting the angle $\phi_s = 0$ leads to

$$i_q = \sqrt{2}I_s \qquad\qquad \text{(Eqn. 5-9)}$$

Application of this property in the algorithm equates to setting I_d to zero and setting I_q to the

desired peak current, $\sqrt{2}I_s$.

Conversely, the application of an inverse q and d transformation recovers i_a, i_b, and i_c

from the i_q and i_d variables:

$$i_a = i_q \cos(\theta_e) + i_d \sin(\theta_e) \qquad\qquad \text{(Eqn. 5-8)}$$

$$i_b = i_q \cos(\theta_e - \tfrac{2\pi}{3}) + i_d \sin(\theta_e - \tfrac{2\pi}{3}) \qquad\qquad \text{(Eqn. 5-9)}$$

$$i_c = i_q \cos(\theta_e + \tfrac{2\pi}{3}) + i_d \sin(\theta_e + \tfrac{2\pi}{3}) \qquad\qquad \text{(Eqn. 5-10)}$$

Assuming a balanced load, equations 5-8, 5-9 and 5-10 may simplify by observing that:

$$i_a + i_b + i_c = 0 \qquad\qquad \text{(Eqn. 5-11)}$$

$$i_c = -i_a - i_b \qquad\qquad \text{(Eqn. 5-12)}$$

substituting for i_c :

$$i_q = \tfrac{2}{3}[\cos(\theta_e) - \cos(\theta_e + \tfrac{2\pi}{3})]i_a + \tfrac{2}{3}[\cos(\theta_e - \tfrac{2\pi}{3}) - \cos(\theta_e + \tfrac{2\pi}{3})]i_b \quad \text{(Eqn. 5-13)}$$

$$i_d = \tfrac{2}{3}[\sin(\theta_e) - \sin(\theta_e + \tfrac{2\pi}{3})]i_a + \tfrac{2}{3}[\sin(\theta_e - \tfrac{2\pi}{3}) - \sin(\theta_e + \tfrac{2\pi}{3})]i_b \quad \text{(Eqn. 5-14)}$$

which, through trigonometric identities [8], simplify to:

$$i_q = i_a \cos\theta_e + (\tfrac{\sqrt{3}}{3}i_a + \tfrac{2\sqrt{3}}{3}i_b)\sin\theta_e \qquad \text{(Eqn. 5-15)}$$

$$i_d = (-\tfrac{\sqrt{3}}{3}i_a - \tfrac{2\sqrt{3}}{3}i_b)\cos\theta_e + i_a \sin\theta_e \qquad \text{(Eqn. 5-16)}$$

Signal	Description
I_q , I_d	desired SRF currents
$i_q^{\;f}$, $i_d^{\;f}$	actual currents in SRF
$i_q^{\;e}$, $i_d^{\;e}$	current error in SRF
i_q , i_d	output of PI controller (SRF)
ia_cont, ib_cont, ic_cont	PWM modulating signals

Table 5-1. Current-control signal descriptions.

Figure 5-2. Closed-Loop Simulink block diagram model.
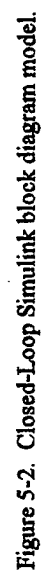
B. SIMULATION

The complete Simulink model of the closed-loop control of a three-phase inverter appears in Figure 5-2. The generation of the i_q and i_d signals in the closed-loop model follows the previous discussion on the q & d synchronous reference frame transformation. Table 5-1 lists descriptions of circuit variables. The difference between the desired current, Ipeak, and the i_q^f term generates the i_q^e error signal. The $-i_d^f$ term by itself becomes the i_d error signal due to the assumption in the q & d derivation that $\phi_s = 0$. The i_d and i_q signals are multiplied by the sine and cosine blocks, respectively.

The closed-loop model simulates the balanced RL load in a manner identical to the open-loop exercises. Both use the same subsystem block from Figure 4-1, and both employ the STPWM method.
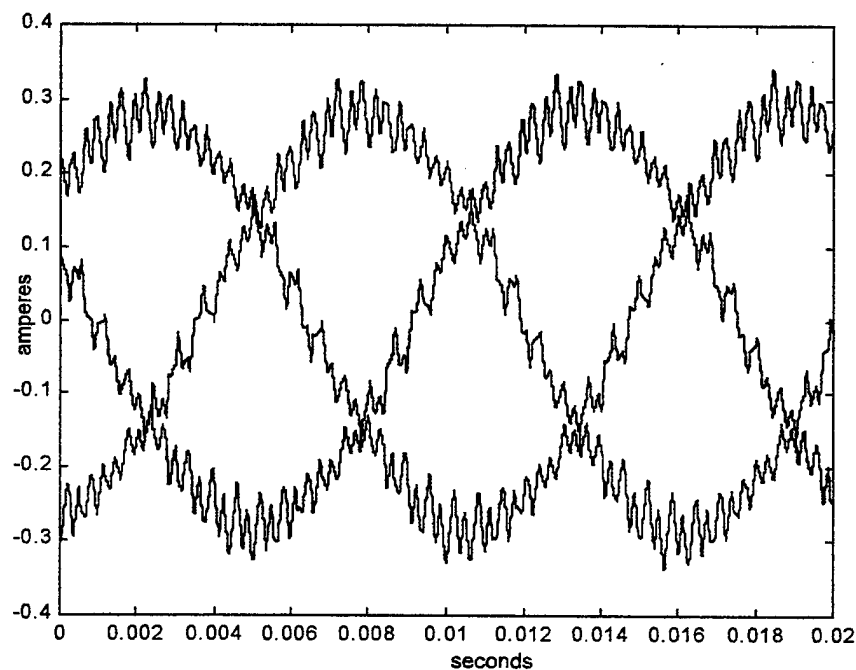

Figure 5-3. Closed-loop simulation current traces.

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The closed-loop simulation resulted in the current traces shown in Figure 5-3. The

Fourier frequency spectrum of the current traces, shown in Figure 5-4, shows the main

component at 60 Hz and small losses near 1600 Hz, corresponding to the frequency of the

triangular wave. The simulation produced the expected current traces.

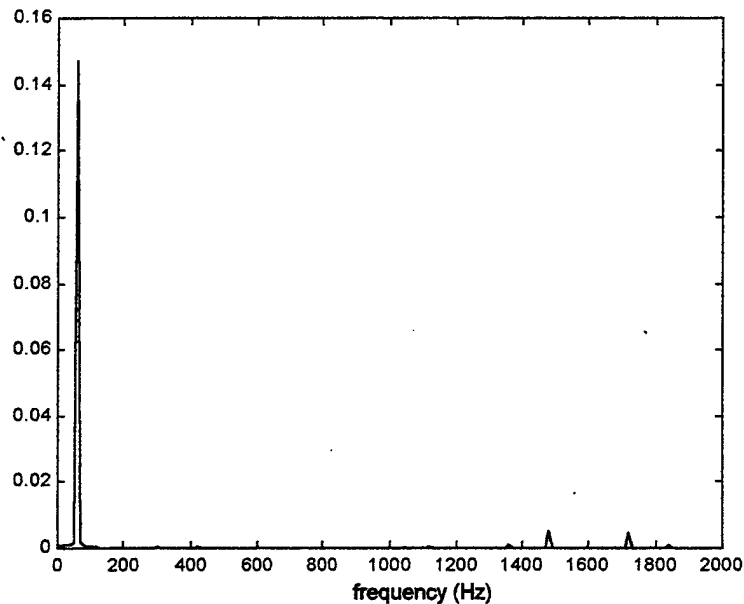Figure 5-4. Closed-loop simulation Fourier transform.

C. HARDWARE IMPLEMENTATION

For DS1102 implementation of the closed-loop control of a three-phase inverter, the

output of a variable gain operational amplifier regulates the peak current, I_q (Ipeak), as shown in

Figure 5-5. Due to the $\pm$ 10V input of the range A/D converter, the user may adjust I_q to any
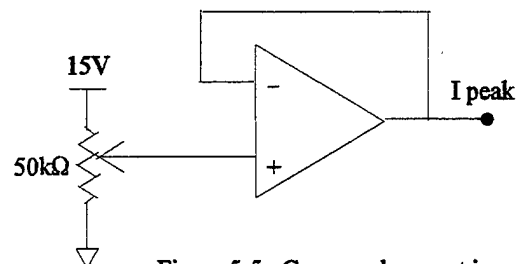
Figure 5-5. Command current input.

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value from 0 to 10V. The inverter system interprets one volt equal to one-tenth of an ampere, so that setting I_q to 5V causes the peak AC current output of the inverter to reach $\pm$ 0.5A.

The scaled outputs of two Hall effect current sensors, i_a and i_b, provide feedback. As with I_q, each volt in these signals represents one tenth of an ampere.

Figure 5-6 shows the control block diagram that programs the DS1102 board for closed-loop control. It uses the same q & d transformation subsystem blocks and PI controller subsystem blocks as in the closed-loop simulation. However, note that to adjust the peak

Figure 5-6. Closed-loop control block diagram.

current, an externally generated input signal I_q or Ipeak has replaced the fixed I_q from the simulation. Since the DS1102's hardware contains a dedicated PWM unit, the triangular reference signal and comparison subsystem blocks do not appear in the hardware

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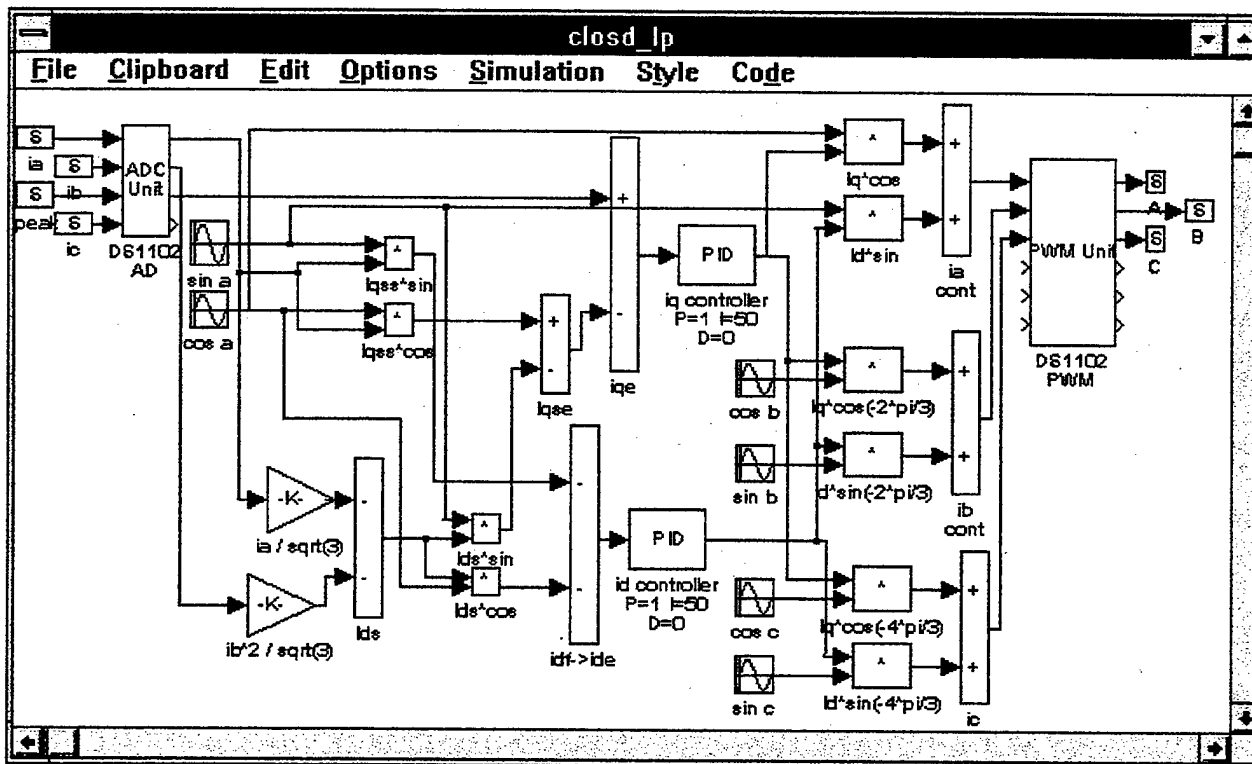implementation. Hall effect current sensors provide feedback, replacing the simulation model of the three-phase wye-connected RL load.

The gains Kp = 1 and Ki = 50 for the q and d PI controllers provided the best system response. Numerous experiments using different gains confirmed this. These gains minimized steady-state error, kept the system stable and provided the fastest response. The experimentation consisted of manual changes to the variable resistor which governs the commanded current input to the system (Ipeak) and visual observation of the effects on the current traces on an oscilloscope. The simulation model was much less sensitive than the actual system to adjustments of Kp and Ki. The model's settling time seemed to be the only parameter that varied with these adjustments. This observation on the difference in gain sensitivities emphasizes the importance of rapid-control-prototyping (RCP). A computer simulation
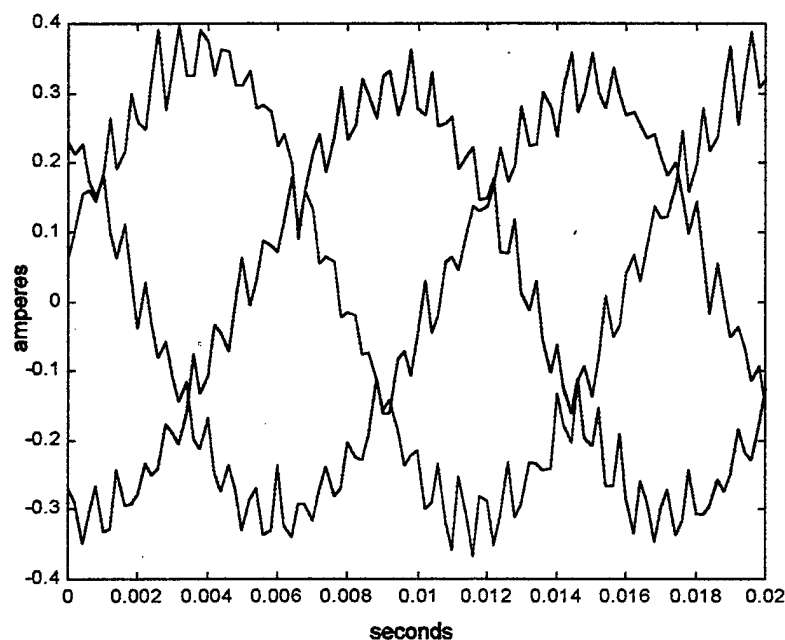
Figure 5-7. Closed-loop hardware current traces.

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indicated that a wide range of gain values could provide adequate system response; however, RCP exercises demonstrated that noise and laboratory equipment inaccuracies reduce the range of acceptable gain values.

The steady-state current traces generated by hardware implementation, in Figure 5-7, appear similar to the current traces from the simulation in Figure 5-3. The amplitude of the simulation is smaller by about 0.02A (6.7%). The Fourier transforms in Figures 5-4 and 5-8 also closely match, and they show a small harmonic component at 1600Hz, the switching frequency of the PWM unit. Again, for the same reasons as in the open-loop hardware exercise, a small component at 120Hz appeared in the Fourier transform. Overall, the physical system controlled by the DS1102 board behaved in a manner analogous to the simulated system.

Figure 5-8. Closed-loop hardware Fourier transform.

Only one major difficulty arose during the closed-loop exercise. Initially, a polarity reversal of the current sensors created a positve feedback loop and caused improper operation.

After reversing the direction of current flow through the current sensor the system operated correctly.

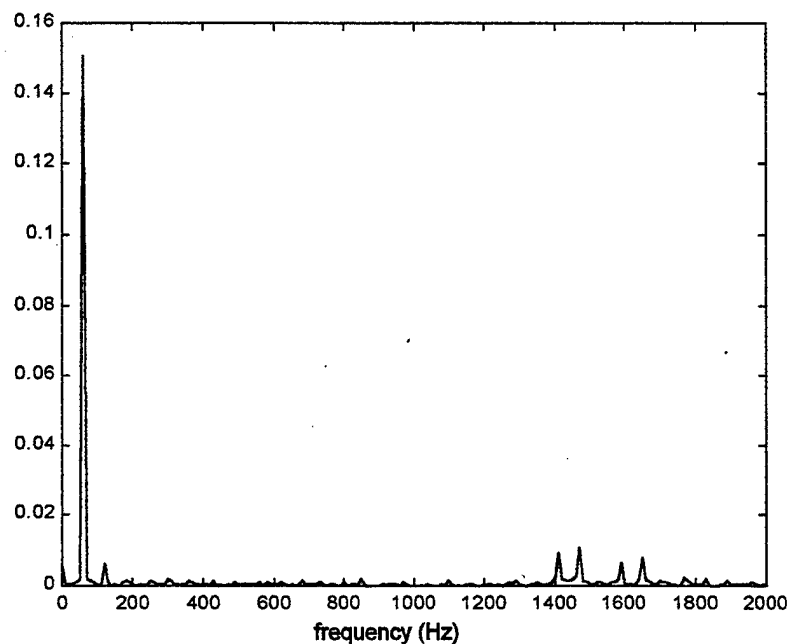The choice of integration methods for the compiling of the Simulink block diagram into executable code affects the minimum executable time step. Complex integration methods, such as Runge-Kutta, require larger time steps, resulting in slower signal processing speeds, compared to simpler methods, such as Euler. For the executable code of the closed-loop inverter control Euler's method allowed a minimum time step of 0.0001 s. Attempts using the Runge-Kutta integration method slowed the signal processing speed by a factor of five, for a minimum time step of 0.0005 s. Decreasing the time step below 0.0001 for Euler and 0.0005 for Runge-Kutta caused the CHECKER31 program to bring up an error message in the download window of the host computer.

The system behavior did not change noticeably with the use of different integration methods. For the three-phase inverter powering an RL load, the 500% slowdown in signal processing did not affect the system response significantly; however, a 500% slowdown in signal processing for the induction motor system presented in Chapter VI had detrimental consequences.

VI. INDUCTION MOTOR CONTROL

A. INDUCTION MOTOR CONTROL METHOD

In the Navy's proposed DC Zonal Electrical Distribution System, many of the inverter modules must power induction machines. Consequently, this chapter will document how the DSPACE system can serve to develop a closed-loop speed control system.

Closed-loop current-control of a three-phase inverter provides two distinct advantages in the control of an induction motor. First, it prevents a large current in-rush during start-up. Second, it can keep the magnetizing current from saturating the machine iron. To remain below saturation while providing adequate torque, an induction-motor-control algorithm provides a peak current command input, Ipeak, and a frequency command input, ω_e. These signals then enter the previous closed-loop current control, as illustrated in Figure 6-1. The slower speed-
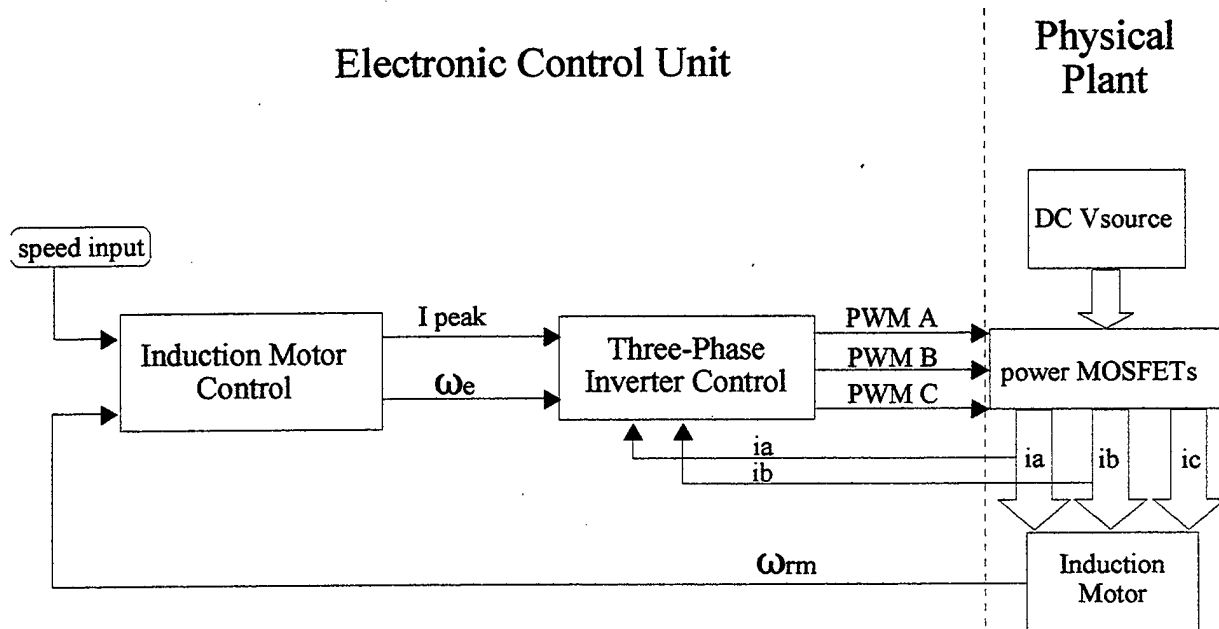

Figure 6-1. Induction motor control overview.

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control loop runs on top of the faster current-control loop to control the speed and torque of the induction motor.
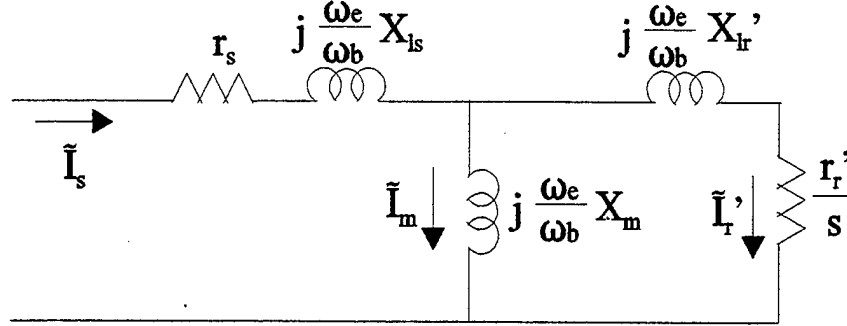
Figure 6-2. Induction machine equivalent circuit.

Figure 6-2 illustrates the standard per-phase steady-state equivalent circuit of the induction machine [9]. The parameters r_s and r_r' are the resistances of the stator winding and the referred rotor winding (referred to have the same number of turns as the stator). The reactances X_{ls} and X_{lr}' are associated with the leakage flux produced by the stator and referred rotor windings. The reactance X_m accounts for the production of the flux which couples both the stator and the rotor, the air-gap flux. The current $\tilde{I}_s$ is the current programmed into a stator phase by the controlled inverter. The current flowing down through the center branch is termed the magnetizing current $\tilde{I}_m$ and is directly related to the air-gap flux.

The machine slip parameter s affects the current flow through the magnetizing current branch and the referred rotor branch of Figure 6-2 due to the r_r'/s resistance element in the referred rotor branch. The difference between the fundamental frequency of the current provided by the inverter ω_e and the rotor electrical speed ω_r determines machine slip, so

$$s = \frac{\omega_e - \omega_r}{\omega_e}$$
(Eqn. 6-1)

The number of pole pairs P in the induction motor relates the actual rotor speed ω_{rm} to the rotor electrical speed ω_r by

$$\omega_r = \frac{P}{2}\omega_{rm} \qquad\qquad \text{(Eqn. 6-2)}$$

In the case of the 4-pole induction motor used in this laboratory exercise, multiplying tachometer readings of actual rotor speed by a factor of 2 produces the rotor electrical speed.

If the inverter merely acts as a constant three-phase current source, then the stator phase current $\tilde{I}_s$ remains fixed, allowing the value of the machine slip to dictate how much of the phase current divides into the magnetizing current and into the rotor-referred current. Optimally, the magnetizing current should remain slightly below the stator iron saturation limit without exceeding it; however, any change in slip would alter the amount of the stator phase current flowing into the referred rotor windings, consequently affecting the magnetizing current through the parallel branch. To overcome this problem, the induction-motor-control algorithm evaluates the amount of slip, then commands the current-control inverter to adjust the phase current magnitude to the appropriate level so that the magnetizing current remains slightly below saturation. Maintaining the optimum level of magnetizing current allows the induction motor to maximize the torque developed. A drop below the rated magnetizing current $\tilde{I}_{m,rat}$ decreases the air-gap flux, decreasing maximum torque capacity. Also, exceeding saturation introduces losses, waveform distortion and harmonics, and airborne noise and vibration [9].

The speed-control algorithm realizes the objective of preserving the level of magnetizing current by solving for the currents in the equivalent circuit of Figure 6-2, then commanding the appropriate stator phase current levels into the motor to maintain the optimum level of

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magnetizing current. The current divider equation

$$\tilde{I}_m = \frac{\dfrac{r_s'}{s} + j\dfrac{\omega_e}{\omega_b} X_{lr}'}{\dfrac{r_s'}{s} + j\dfrac{\omega_e}{\omega_b} X_{rr}'} \tilde{I}_s \qquad \text{(Eqn. 6-3)}$$

where

$$X'_{rr} = X_m + X'_{lr} \qquad \text{(Eqn. 6-4)}$$

solves for the magnetizing current in terms of the slip, the electrical angular frequency ω_e, and

obtainable motor parameters, including the rated frequency ω_b. Solving for the magnitude of the

stator current [9], and replacing the variable mag($\tilde{I}_m$) for the constant mag($\tilde{I}_{m,rat}$), uncovers the

magnitude of the stator phase current that the inverter must supply to the motor to maintain $\tilde{I}_{m,rat}$

through the magnetizing current branch of the circuit,

$$\text{mag}(\tilde{I}_s) = \sqrt{\frac{(X'_{rr}\,\omega_{sl})^2 + (r_r'\,\omega_b)^2}{(X'_{lr}\,\omega_{sl})^2 + (r_r'\,\omega_b)^2}}\,\text{mag}(\tilde{I}_{m,rat}) \qquad \text{(Eqn. 6-5)}$$

where

$$\omega_{sl} = \omega_e - \omega_r \qquad \text{(Eqn. 6-6)}$$

Figure 6-3 illustrates the flow of the speed control algorithm. The difference between the

commanded speed and the actual motor speed results in an error signal that becomes the

commanded slip ω_{sl}* signal. Based on Equation 6-5, the commanded slip establishes the

optimal stator phase current magnitude, which then replaces Ipeak in the current control

algorithm presented in Chapter V. Finally, adding the commanded slip signal to the rotor

electrical speed sets the fundamental frequency for the current control algorithm.

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$$\sqrt{\frac{(X'_{rr}\,\omega_{sl}*)^2 + (r'_r\,\omega_b)^2}{(X'_{lr}\,\omega_{sl}*)^2 + (r'_r\,\omega_b)^2}}\,mag(\tilde{I}_{m,rat})$$
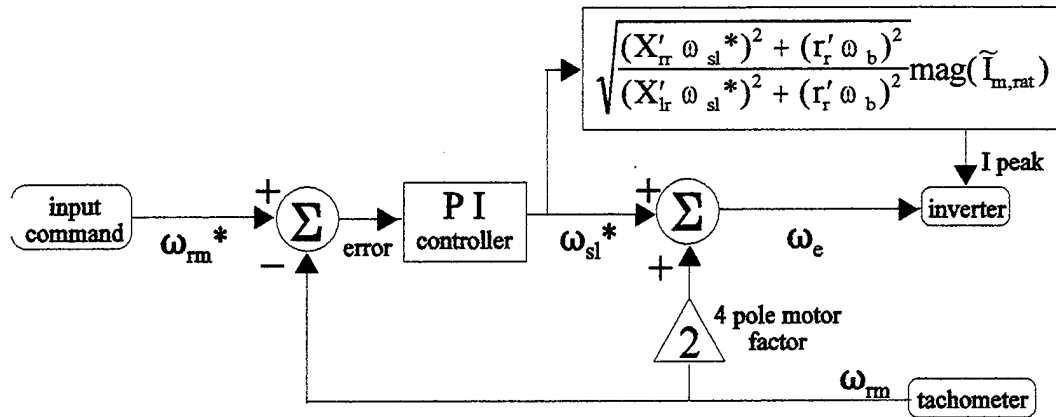
Figure 6-3. Speed control algorithm.
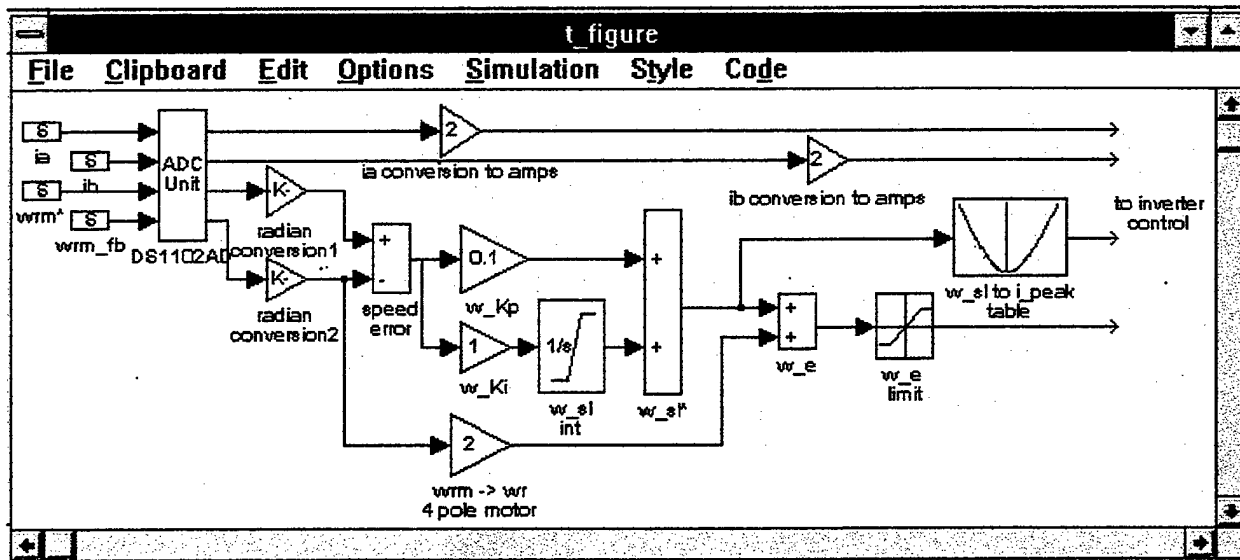
Figure 6-4. Speed control block diagram.

B. HARDWARE IMPLEMENTATION

The Simulink block diagram in Figure 6-4 implements the speed control algorithm. The speed control block diagram generates the Ipeak and frequency signals that regulate the inverter control block diagram. A variable resistor arrangement as shown in Figure 6-5 provides an adjustable speed control input to the system. A tachometer connected to the induction motor

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shaft produces a voltage proportional to the speed of the motor. The tachometer has an operating range from 0 to 2500 rpm and a scaling factor of 2V/100rpm. Two gain blocks in the diagram convert the variable resistor and the tachometer voltages to radians/sec. A look-up table determines the amplitude of the stator phase current from the commanded slip frequency in accordance with Equation 6-5. Table 6-1 summarizes the parameters for the squirrel-cage induction motor used in the laboratory exercise.

$r_s = 11.78\ \Omega$	$X_{ls} = 10.84\ \Omega$	$X_m = 149.0\ \Omega$	$X_{lr}' = 10.84\ \Omega$
$r_r' = 8.83\ \Omega$	$R_c = 2097\ \Omega$	$P = 4$	$J = 0.0024\ kg/m^2$

Table 6-1. Squirrel-cage induction motor parameters.

The motor has rated rms phase voltages of 120 V, rated rms phase currents of 1.2 A, and a rated speed of 1670 rpm. A summing block adds the commanded slip to the rotor electrical speed to generate the electrical frequency of the stator phase currents. This signal generates the synchronous reference frame angle θ_e required for the current-control transformations..

The version of the current control-loop used for motor speed control has one slight modification from the original 60Hz three-phase inverter presented in Chapters IV and V. The current-control loop must now accept frequency command inputs. So rather than using 60Hz
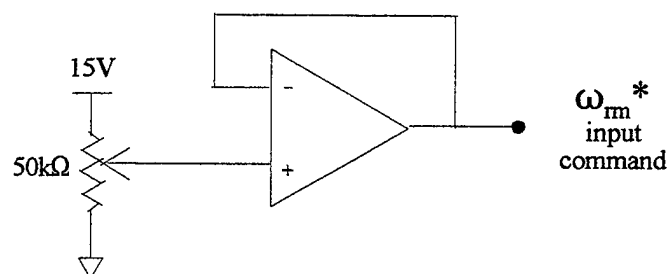

Figure 6-5. Command speed input.

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sine wave generators, an integrator block accepts the electrical angular frequency input ω_e and provides the electrical angle θ_e. The integrator block cyclically resets to zero when the electrical angle reaches 2π. Sine and cosine look up tables then produce the signals that enter the current loop at the positions formerly occupied by the 60Hz generators in the original current-control loop.

The Simulink control block diagram, programmed into the DS1102 board, successfully controlled the squirrel-cage induction motor. The motor speed consistently tracked the commanded speed input with $\pm$ 8% error for commanded values ranging between 250 and 1000 rpm. Above 1000 rpm, the DC power supply levels required to sustain the commanded levels of stator current magnitude approached the voltage limit of the power MOSFETs. Beyond this operating point, the speed control subsystem would command a current magnitude that the available DC power supply could not provide. The standard per-phase steady-state equivalent circuit shows that the dependence on ω_e/ω_b causes the input impedance to increase with electrical frequency.

To satisfy the current demand of the motor, the DC power supply must overcome two obstacles which worsen as the speed (frequency) increases. First, some impedances in the equivalent circuit increase as a function of ω_e/ω_b. Second, a faster speed increases friction losses, subsequently increasing slip. More slip causes the proportion of rotor referred current to magnetizing current to increase, due to the r_r'/s element in the referred rotor branch. So unless the power source supplies more stator phase current, the referred rotor branch will rob the magnetizing branch of the current it needs to remain at its optimum level. The speed-control algorithm performs the function of increasing the current demand to the inverter subsystem in

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accordance with the amount of slip in the motor.

The following table summarizes observations in the lab.

rpm	VDC supply	error (rpm)	error (%)
250	65	20	8
500	123	35	7
750	182	60	8
850	200	65	8
1000	252	79	8
1200	330	125	10

Table 6-2. Laboratory observations.

The error column shows the difference between the commanded rpm and the steady-state rpm.

Since the speed-control algorithm generates the commanded input to the current-control algorithm, the current-control algorithm must have a faster response time. To attain this objective, the PI controller gains in the current algorithm have a higher setting (Kp = 0.5, Ki = 5) than the speed algorithm's PI controller gains (Kp = 0.1, Ki = 1). Laboratory experimentation determined that these settings resulted in the lowest steady-state error and most acceptable dynamic response. Future research efforts may investigate optimizing these gains thru further simulation studies.

. , The RTI31 software application allowed a minimum integration time step of 0.001 s for the control block diagram of the induction motor control algorithm. The motor algorithm's larger control block diagram caused a tenfold slowdown compared to the minimum signal

processing speed allowed for the inverter algorithm (0.0001 s).

Attempts to use the Runge-Kutta method of integration for the speed algorithm resulted in failure. The integration time step had to slow down to 0.005 s for RTI31 to download; otherwise, the processor overload message would appear on the host computer screen. Slowing down the signal processing at first caused the system to become unstable, then the motor stopped. Throughout these exercises, the Euler method of integration performed best because it allowed the use of the smallest time step for signal processing.

No significant difficulties arose during the hardware exercise, other than a minor wiring error in the buffer circuit at the input to the A/D converter. The limited resolution of the tachometer probably caused most of the tracking error. Use of an optical sensor, such as the one employed by Tait [3], would reduce this error.

VII. CONCLUSION

A. OBSERVATIONS

The DSPACE DS1102 DSP board successfully implemented the closed-loop control of a three-phase inverter. The inverter powered a simple three-phase wye-connected RL load, maintaining the commanded current through the load with no discernible fluctuations in the current levels in the steady state. The inverter also successfully powered a squirrel-cage induction motor. The speed control algorithm ran on top of the original inverter algorithm. The speed control algorithm provided peak current and electrical angle commands to the inverter algorithm. The induction motor rpm remained within 8% of the commanded rpm under steady-state conditions.

The DS1102 can handle algorithms of formidable complexity with speed and accuracy; however, the easy method of programming ingratiates the DS1102 among control engineers. The debugging software, TRACE31, simplifies troubleshooting greatly by monitoring in real-time the value of any block in the Simulink block diagram. Probably, the limited number of I/O device channels constitutes the DS1102 board's most significant limitation. Some creativity may allow an engineer to work around the I/O limitation. For example, in the closed-loop inverter control, knowing that the three phase currents add to zero, the algorithm uses only two out of three phases for feedback.

B. SUMMARY OF SIGNIFICANT ACCOMPLISHMENTS OF THIS WORK

1. Developed Simulink model of closed-loop controlled three-phase inverter using

current control.

2. Installed DS1102 board and software in host PC.

3. Designed short-circuit protection buffer circuit and modeled it in SPICE 3f4.

4. Assembled short-circuit protection buffer circuit on printed circuit board.

5. Wired Hall effect current sensors and associated amplifier circuits on breadboard.

6. Powered three-phase wye-connected RL load with closed-loop, current-controlled inverter.

7. Powered squirrel-cage induction motor with closed-loop, current-controlled inverter.

C. UTILITY TO THE NAVY

The capabilities of the DS1102 allow an engineer to easily test complex algorithms for system control. This thesis has demonstrated a viable method for control of a three-phase inverter on U.S. Navy ships using DC zonal distribution. A previous thesis [4] demonstrated a control method for a DC-DC converter using the DS1102. Another thesis [2] developed the control for a single-phase resonant inverter resulting in very low power losses. The DS1102 can serve as a valuable tool for Navy engineers in signal processing problems in the power electronics arena.

D. FUTURE WORK

This thesis research, along with the three previous DS1102 related efforts in the NPS ECE Power Lab [2, 3, 4], demonstrated some powerful capabilities of the controller board. Yet, the next step for research into shipboard DC zonal distribution demands even greater capacity

from a controller board, in terms of signal processing speed and I/O ports. The four DS1102 theses have dealt with single converter and inverter systems. Further DC zonal distribution research into the performance of multiple systems in parallel exceeds the capacity available in the DS1102. A more capable signal processor would greatly facilitate research into paralleling multiple converters and inverters. Access to the most recent signal processing tool from DSPACE, the DS1103, would enhance further research activity. The board features 333 MHz processor speed, 16 A/D channels, and several other upgrades.

Advances in signal processor technology have a profound impact in the way the Navy powers its ships and how effectively its Sailors harness this power. They deserve the best systems our country can provide.

APPENDIX A. DS1102 LICENSE FILE

TRACE31W : FULL,, 1, 9EFD1FE9F914AF8C, #132, Vs.2.0
RTI   : FULL,, 1, 14046544624AD7C0, #132, Vs.2.2

APPENDIX B. RIBBON CABLE PINOUT [4]

Signal	DS1102 Pin	Ribbon Cable Port
ADC 1	1	1
Analog Ground	22	2
ADC 2	2	3
Analog Ground	23	4
ADC 3	3	5
Analog Ground	24	6
ADC 4	4	7
Analog Ground	25	8
IOP1 (2)	7	9
IOP3 (4)	8	10
IOP5 (6)	9	11
IOP7 (8)	10	12
IOP9 (10)	11	13
IOP11 (12)	12	14
IOP13 (14)	13	15
IOP15 (16)	14	16
Digital Ground	15	17
DAC 1	43	18
Digital Ground	26	19
DAC 2	44	20
Digital Ground	60	21
DAC 3	45	22
Digital Ground	47	23
DAC 4	46	24

Phi90 2	16	25
Phi0 2	17	26
Index 2	18	27
/Phi90 2	37	28
/Phi0 2	38	29
/Index 2	39	30
IOP0 (1)	28	31
IOP2 (3)	29	32
IOP4	30	33
IOP6	31	34
IOP8	32	35
IOP10	33	36
IOP12	34	37
IOP14	35	38
CAP0 / PWM4	50	39
CAP1 / PWM5	51	40
CAP2	52	41
CAP3	53	42
CMP0 / PWM0	54	43
CMP1 / PWM1	55	44
CMP2 / PWM2	56	45
CMP3 / PWM3	57	46
Vsupply	61	47
Vsupply	62	48

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APPENDIX C. SPICE FILE

ISOLATOR-BUFFER CIRCUIT FOR POWER MOSFET CONTROL

```
.MODEL CMOSN NMOS LEVEL=2 PHI=0.700000 TOX=4.0800E-08 XJ=0.200000U TPG=1
+ VTO=0.8309 DELTA=3.2570E+00 LD=3.2850E-07 KP=6.2842E-05
+ UO=742.5 UEXP=1.9200E-01 UCRIT=2.1830E+04 RSH=6.1490E+00
+ GAMMA=0.5612 NSUB=6.7970E+15 NFS=9.0930E+10 VMAX=5.7540E+04
+ LAMBDA=4.2800E-02 CGDO=4.1704E-10 CGSO=4.1704E-10
+ CGBO=3.4581E-10 CJ=1.2204E-04 MJ=6.3602E-01 CJSW=5.5150E-10
+ MJSW=2.5691E-01 PB=4.4514E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09


.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=4.0800E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9891 DELTA=1.2110E+00 LD=3.7130E-07 KP=1.7503E-05
+ UO=206.8 UEXP=2.8220E-01 UCRIT=1.1030E+05 RSH=1.0210E-01
+ GAMMA=0.7803 NSUB=1.3140E+16 NFS=7.1500E+11 VMAX=1.2110E+05
+ LAMBDA=5.3880E-02 CGDO=4.7138E-10 CGSO=4.7138E-10
+ CGBO=3.5113E-10 CJ=3.2670E-04 MJ=6.2773E-01 CJSW=3.7671E-10
+ MJSW=1.9873E-01 PB=9.0000E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.3340E-08


.SUBCKT INV 2 3
VDD 1 0 5
M1  3 2 1 1 CMOSP W=6U L=2U
M2  3 2 0 0 CMOSN W=3U L=2U
.ENDS INV


.SUBCKT NAND2 2 3 5
VDD  1 0 5
MPA  5 2 1 1 CMOSP W=6U L=2U
MPB  5 3 1 1 CMOSP W=6U L=2U
MNA  5 2 4 0 CMOSN W=3U L=2U
MNB  4 3 0 0 CMOSN W=3U L=2U
.ENDS NAND2


VIN 1 0 0 PULSE(0 5 1NS 1NS 1NS 10US 20US)

* top rail delay
X1 1 2 INV
```

```
Ct 2 0 350P
X2 2 3 INV
X3 1 3 4 NAND2
X4 4 5 INV

* bottom rail delay
X5 1 6 INV
X6 6 7 INV
Cb 7 0 350P
X7 7 8 INV
X8 6 8 9 NAND2
X9 9 10 INV

.TRAN 1NS 40US
.END
```
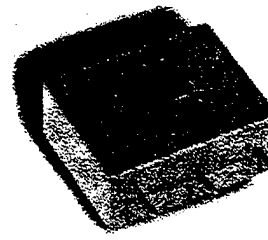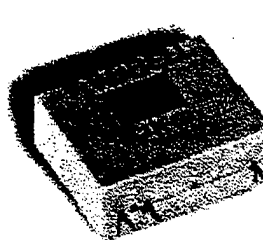
Model CLN-50/100 **Closed Loop Hall Effect**

Description
Models CLN-50 and CLN-100 are closed loop Hall effect current sensors that accurately measure dc and ac current and provide electrical isolation between the current carrying conductor and the output of the sensor.

Current Sensors

Electrical Specifications	**CLN-50**		**CLN-100**	
Nominal current (I_N)	50 A rms		100 A rms	
Measuring range	0 to ± 90 A		0 to ± 150 A	
Sense resistor	R. min.	R. max.	R. min.	R. max.
with ± 12 V at ± 70 A peak	50 ohms	90 ohms	n/a	n/a
at ± 100 A peak	n/a	n/a	30 ohms	55 ohms
at ± 150 A peak	n/a	n/a	10 ohms	25 ohms
with ± 15 V at ± 90 A peak	70 ohms	100 ohms	n/a	n/a
at ± 100 A peak	n/a	n/a	30 ohms	85 ohms
at ± 150 A peak	n/a	n/a	30 ohms	40 ohms
Nominal analog output current	50 mA		100 mA	
Turns ratio	1:1000		1:1000	
Overall accuracy at 25 °C and ± 12 V	± 0.9% of I_N		± 0.9% of I_N	
Overall accuracy at 25 °C and ± 15 V	± 0.5% of I_N		± 0.5% of I_N	
Supply voltage (Vdc)	± 12 to ± 15 (± 5%)		± 12 to ± 15 (± 5%)	
Dielectric strength	3 kV rms/50 Hz/1 min.		3 kV rms/50 Hz/1 min.	
(between the current carrying conductor and the output of the sensor)				

Accuracy-Dynamic Performance

	CLN-50	**CLN-100**
Zero current offset at 25 °C	± 0.2 mA max.	± 0.2 mA max.
Offset current temperature drift		
between 0 °C and +70 °C	± 0.3 mA typ., ± 0.6 mA max.	± 0.3 mA typ., ± 0.6 mA max.
between -25 °C and +85 °C	± 0.3 mA typ., ± 0.8 mA max.	± 0.3 mA typ., ± 0.8 mA max.
Linearity	better than ±0.1%	better than ±0.1%
Response time	less than 500 ns	less than 500 ns
di/dt accurately followed	better than 100 A/µs	better than 100 A/µs
Bandwidth	0 to 150 kHz (-1 dB)	0 to 150 kHz (-1 dB)

General Information

	CLN-50	**CLN-100**
Operating temperature	-40 °C to +85 °C	-40 °C to +85 °C
Storage temperature	-40 °C to +90 °C	-40 °C to +90 °C
Current drain (plus output current)	10 mA (at ± 15 V)	14 mA (at ± 15 V)
Coil resistance		
at + 70 °C	30 ohms	30 ohms
at + 85 °C	35 ohms	
Package	Flame retarded plastic case	
Weight	18 grams	21 grams
Mounting	Designed to mount on PCB via thru hole connection pins	
Aperture	0.530" x 0.390" (13.5 mm x 10 mm)	
Output reference	To obtain a positive output on the terminal marked "O/P", aperture current must flow in the direction of the arrow (conventional flow)	

Notes: - The temperature of the current carrying conductor should not exceed 90°C
- Contact F.W. Bell for other models
- Due to continuous process improvement, specifications subject to change without notice.

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