APPENDIX 18

TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION
FINAL SOFTWARE REPORT
DATA ITEM NO. A005

INTEGRATED ELECTRONIC WARFARE SYSTEM
ADVANCED DEVELOPMENT MODEL (ADM)

7800987-18

PREPARED FOR
NAVAL AIR DEVELOPMENT CENTER
WARMINGSTON, PENNSYLVANIA

RAYTHEON ELECTROMAGNETIC SYSTEMS DIVISION

1 OCTOBER 1977

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APPENDIX 18

TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION
FINAL SOFTWARE REPORT
DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)
ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:
Naval Air Development Center
Warminster, Pennsylvania

Prepared by:

RAYTHEON COMPANY
Electromagnetic Systems Division
6380 Hollister Avenue
Goleta, California 93017

1 OCTOBER 1977
UNIT SOFTWARE DEVELOPMENT SPECIFICATION

TITLE OF SPEC

COMPUTER PROGRAM DESIGN SPECIFICATION FOR IEWS TECHNIQUES GENERATOR

<table>
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<tbody>
<tr>
<td>WRITER</td>
<td>H. McQuillen</td>
<td>8/5/76</td>
<td></td>
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REVISIONS

<table>
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<tr>
<th>CHK</th>
<th>DESCRIPTION</th>
<th>REV</th>
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<tr>
<td>A</td>
<td>9/13/76 Update Some Addresses In Flow HRM Charts &amp; Add List III</td>
<td></td>
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<tr>
<td>B</td>
<td>12/20/76 Changes are made in two modules, SC Technique-Channel Assignment, and SC Technique-Channel Parameter Change or Dismiss. The updated flow charts are: Figure 7: Pg. 1-Added temporary storage (clear) for CFN. Pg. 2-Added insertion of CHAN in word 9, and insertion of CFN in word 12. Pg. 3-Added insertion of FN into CFN. Pg. 4-Added restore of FM generator status when RR/RGPO Gen. unavailable. Figure 8: Pg. 1-No change. Pg. 2-No change. Pg. 3-Added dismiss for RR/RGPO Gen., and for FM Gen. Pg. 4-Added Insertion of CHAN in word 9, and of FM Gen no.</td>
<td></td>
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in word 12.

Table A gives address and data for eight Technique programs to be stored in the Techniques Program memory. These are selected samples used during TGU integration and test.

REV STATUS OF SHEETS

<table>
<thead>
<tr>
<th>REVISION</th>
<th>SHEET NO.</th>
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1.0 **SCOPE**

The computer program specified herein shall be entitled IEWS Techniques Generator Controller Program. The Techniques Generator Unit is part of the Integrated Electronics Warfare System, IEWS, being developed for test and evaluation to determine operational usefulness for advanced combat aircraft.

2.0 **APPLICABLE DOCUMENTS**

The following documents, form a part of this specification to the extent specified herein. In the event of conflict, the requirements of this specification shall govern.

- **AETD-XAV-1000**
  - Experimental and Developmental Specification IEWS (Integrated Electronic Warfare System)

- **WS-3506**
  - Requirements for Digital Computer Program Documentation

**RAYTHEON SPECIFICATIONS**

- **53959-HM-0410**
  - Unit Hardware Development Specification - IEWS Hardware Spec. - Techniques Generator

- **53959-HM-0411**
  - Unit Hardware Development Specification - IEWS Hardware Spec. - Transmitter Control - MAAS

- **53959-CD-1401**
  - Interface Control Document Spec. - Daisy Chain Bus ICD

- **53959-JK-1003**
  - Interface Control Document Spec. - Auxiliary Bus ICD
Eqpt. Division I
RP-16 Microprocessor

Eqpt. Division II
Computer Program Package Specification
Raytheon RP-16 Relocatable Macro
Assembler Functional Specification

3.0 REQUIREMENTS

3.1 FUNCTION/ALLOCATION DESCRIPTION

The IEWS Techniques Generator Controller Program shall be the software portion of Techniques Generator. It shall run in the T.G. Controller/Processor hardware which is implemented with an RP-16 Microprocessor. Together with the hardware, the program shall provide the overall T.G. functions described in paragraph 3.1.1, and the Controller/Processor functions described in paragraph 3.1.2.1, both of applicable document 53959-HM-0410, T.G. hardware specifications.

The TG Controller Program shall be structured in the modules and relationships as shown in Figure 1. Basically, once initialized, the program shall be interrupt-driven. The two hierarchy modules are Initilize (INLZ), and Loop (LOOP). At power up or as required, the System Controller, SC, or a Local Control Panel, LCP, shall be able to put the program to start of INLZ. Either of the two shall be able to command run.

INLZ shall initialize all variables, assignments and generators and transfer to LOOP. LOOP shall basically enable interrupts and run in an idle loop awaiting interrupts. All service routines shall return to LOOP to await further interrupts.

There shall be twelve types of interrupt service modules as shown in Figure 1 and Figure 2, VIZ.,

SC Write Fault (SCWF)
SC Assignment - Frequency, ACN (SCAFA)
**Fig. 1. TECH GEN UNIT CONTROLLER SOFTWARE**

*see Fig. 2*

-intr. lVL Priority-

HIGH−LOW = 8 → 2

Hardware wired.
See Fig. 1 for module relationships to remainder of program.

Fig. 2 RR/RSPD module types
SC Technique-Channel Assignment (SCTA)
SC Technique-Channel Parameter Change, Dismiss (SCTCC)
SC Program Control (Currently Growth) (SCPC)
Channel-VCO Frequency Set-On (CVFSO)
Auxiliary Bus-Frequency (ABFR)
RAN-RAP Cover (RRC)
RAN-RAP Cover and Early (RRCE)
RAN-RAP Cover and Late (RRCL)
RAN-RAP Cover, Early, Late (RRCEL)
Range Gate Pull-Off (RGPO)

Note in Figure 1 that the last five module types shall service four RAN-RAP RGPO Technique Generators. Interrupt level selects the general service. Within the interrupt level the three least significant bits, LSB's, of the hardware interrupt vector shall identify a particular service module. Within any of these levels, the device requesting service determines the vector, only one vector per service request.

Interrupt services have horizontal modularity, i.e., service routines are independent of one another.

Finally, there are three subroutines:
Frequency Update (FUP)
Convert and Load Tuning (CLT)
RAN RAP - A Version (RRA)

Relationships of subroutines to service module users are shown in Figures 1 and 2.
At the end of any service-routine execution, the program shall return to LOOP. For this development the software shall enable interrupts only during LOOP. Nesting of interrupt services is a software growth capability. The hardware is capable of supporting such nesting.

3.2 FUNCTIONAL DESCRIPTIONS

Each IEWS T.G. Controller Program module shall implement the corresponding flow diagram given herein. Each flow diagram shows the fixed hardware addresses involved. Externally interchanged word formats shall be as specified in the referenced, associated document, 53959-HM-0410, "Unit Hardware Development Specification - IEWS Hardware Spec. - Techniques Generator". Programmable variables within programs shall have the values given on the diagrams. Some of these modules might change as a result of development tests. Internal word formats can vary from those herein if more practical. Program Tables are given in paragraph 3.3

3.2.1 Initialize (INLZ) Module

INLZ shall be as given in Figure 3. Controls and address to set and run INLZ are given in notes thereon. INLZ clears all assignments, if any, and flags. It initializes all internal tables.

3.2.2 Loop (LOOP) Module

LOOP shall be as given in Figure 4. Background testing can be added to this at any time as growth software.

3.2.3 SC Write Fault (SCWF) Module

SCWF shall be the interrupt routine of Figure 5. Hardware interrupt vectors and addresses are given. This routine endeavors notify the SC if a write is attempted to T.G. instruction memory during times of memory-protect. The T.G. RP-16 4K word memory is two-port, one for the Daisy Chain (DC) bus, and the other for the T.G. RP-16. The memory is
**Initialize**

INL is address of INLB program.

CT is cumulative TEST-Count Reg.

For loop entries - a development check

CR5 is start of CHAN/RESOURCE $\text{Table II}$

CH is CHAN.

---

**Notes:**

1. Initialize Address 0000 is set for any:
   
   a. SC Daisy Chain Master Clear-DECALC
   
   b. LCP Master Clear-MTDC
   
   c. SC TCE External Control "Initialize"
   
   d. LCP Control "STOP" and by inputting Addr. 0000.

2. Subsequent Jump to Initialize Run either:
   
   a. SC TCE External Control "NEWSTART"
   
   b. LCP Control "START" (Q2: Addr. 0000)
Fig. 3 (cont'd) Initialize
Added 1/20/72

SFS is START OF FM GEN PRE-OPER.
STATUS TABLE IIA

SFA is START OF FM GEN ALLOCATION
(OPER.) TABLE IIA

FN is FM GEN NO.

A/1

LOAD: SFS ← B
LOAD: SFA ← X

LOAD: 2 ← FN

FN = 0

2

NO

LOAD: B + FN ← A
STORE: A ← X + FN

B/3

DECNT: FN−1 ← FN

1/25/72
Howard McQuillen
FIG. 3 (cont'd) INITIALIZE

PAGE 3 OF 3

SRS is start of RA/RRP
Gen. Pre-operation
Status TABLE II

SRA is start of RR/RAP
Gen. Allocation (Operation)
TABLE II

RN is RR/RAP
Gen. NO. or ZERO

LOAD:
SRS → B
LOAD:
SRA → X

LOAD:
4 → RN

RN = 0 ?

YES

FUBL RPTHI

LOAD:
B + RN → A
STORE:
A → X + RN

JUMP:
LOOP → RC

 unconditional jump TO LOOP

EXIT TO LOOP

NO

DECRNT:
RN - 1 → RN

7/29/76

H. McDaniel
**Fig. 4 LOOP**

CT is cumulative test

![Diagram of LOOP with ENCRMT: CT+1→CT, IDLE, ENBL ATOLO, JUMP UNKN: IDLE→PC]

**NOTES:**
1. LOOP is entered with:
   - Jump from:
     a. INITIALZ (INLE),
     b. Return from any other interrupt routine module

2. Cumulative Test is
   count of loop entries subsequent to INLE.
   This is a check during development tests

---

H. M. H: 7/28/76
**FIG. 5 SC WRITE FAULT**

```
SC WF

DISABLE RPT20
STORE STATE

STORE: 16 bit 1s DATA
STORE: 20 bit 1s DATA
ZERO DS: 20 bit 1s DATA
STORE: 16 bit 1s DATA

RESTORE STATE

RETURN
```

**NOTE:**

1. 1753773 addr 32 to SC
   INTR(8) on the Daisy Chain Bus. The bus has no
   INTR Ack. Hence -
2. The INTR RPS (8) remains
   until:
   a) SC addresses 0057758, or
   b) SC issues DE MCR, or
   c) If programmed, TG RP is "RESET XTRNA", i.e.
   OPRST.
partitioned with T.G. instructions, data, and working space in all but 8 locations. It is the bulk of this memory except the 8 locations for SC messages that is at times protected to DC writes. An SC Daisy Chain Master Clear, DCMCL always opens all memory to DC write. Any time a message is transferred through any of the 8 message locations the bulk of memory is protected from DC writes. If while protected a DC write is attempted, DC ACKnowledge is hardware returned to prevent hanging the bus, even though data is not written. The T.G. RP-16 receives the interrupt and in turn attempts to notify the SC as shown in Figure 5. The 4K memory is open to DC read all the time. The two port is used to facilitate loading T.G. RP-16 program directly from the DC bus.

3.2.4 SC Assignment-Frequency, ACN (SCAFA)

SCAFA shall be the interrupt routine of Figure 6. Note that the Frequency Update Subroutine (FUP) is used in this service. Return to LOOP is from FUP.

3.2.5 SC Technique-Channel Assignment (SCTA) Module

SCTA shall be the interrupt routines of Figure 7. This module retrieves all generator parameters from T.G. Techniques Program memory and loads the proper generators. Where the limited number of RAN-RAP/RGPO generators are needed, the routine performs a resource management allocation by finding an unused generator for the current program. It remembers to which channel the generator is assigned.

3.2.6 SC Technique-Channel Parameter Change or Dismiss (SCTCC) Module

SCTCC shall be the interrupt routines of Figure 8. This module changes any parameters of a currently assigned Technique Program per the SC message. The Technique Program stored in Technique Program memory remains as originally loaded. If the change is in use of the Auxiliary Bus for Frequency and/or ACN, the routine fills in the balance of the word as stored in Techniques
**SC ASSIGNMENT - FREQ, ACN**

**SCAFR**

1. **INTR 030101**
2. **DISABLE RFILO, STORE STATE**
   - LOAD FREQ \( \rightarrow \) FREQ
   - LOAD SAC \( \rightarrow \) AC
3. **CLEAR MSY FLAG** \( = (bit15) \rightarrow 0 \) \( \rightarrow \) STATE
   - \( 005770 \) \( \rightarrow \) STATUS
4. **CH IS CHAN**
5. **AN IS ACN**
6. **START OF XACN MEN** \( \rightarrow \) SN = 1753008
   - STORES ACN

**FUP**

- **FREQ UPDATE SUBROUTINE**
- **JUMP UNCONDITIONAL**

**RETURN**

- **INCLUDED IN FUP**

---

**Notes:**
- Register state must be appropriate to FUP
- 1/24/76
- H.R. McEwen
FIG 7 SC TECHNIQUE CHANNEL ASSIGNMENT

TO ADD TWO FM GEN'S.

CFM IS CONNECTED MEMORY FM GEN NO.
TEMP STORAGE LOCATION

0057738
TW IS TECH WORD
BIT 15 ZERO START 0057778
CLR SC MSG
FLAG BIT 15

CH IS CHANNEL
TN IS TECH NO. X2

TECH NO. 8
PS IS TECH PROG START 006008
GL IS GEN LOAD ADDR 175008

PW IS PARAMETER WORD

D/2

CD IS GEN CODE

CD = 8

CD = 10

FM GEN NEEDED

8/3

RE/RESA GEN
NEEDED

8/3

A/2
FIG. 7 SC TECH-CHAN ASSRT (CONT'D)

REDOONE 12/10/76

\[
\begin{align*}
\text{A/1} & \quad \text{2ND WORD OF FM GEN.} \\
\text{CD=9} & \quad \text{OR: PW VCHAN → PW} \\
\text{CD=12} & \quad \text{OR: PW VGEN → PW} \\
\text{D/1} & \quad \text{STORE: PW → X} \\
\text{INC NXT: Tn+1 → Tn} & \quad \text{CHECK FOR LAST WORD OF PROGRAM} \\
\text{CD=13} & \quad \text{RESTORE STATE} \\
\text{YES} & \quad \text{GOOD EXIT} \\
\text{NO} & \quad \text{RESPONSE ASSIGNED} \\
\end{align*}
\]
FN is FM GEN No.

SFA is START OF FM GEN

ALLOCATION (OPERATION) TABLE/FIA

CRS is CHANNEL RESOURCE STATUS BASE ADDR./TABLE

\[ \text{FN} \rightarrow \text{STORE: } 2 \rightarrow \text{FN} \]

\[ \text{LOAD: } \text{x'0888'} \rightarrow \text{SFA+FN+FA} \]

\[ \text{FA=0?} \]

\[ \text{YES} \rightarrow \text{STORE: } \text{FN} \rightarrow \text{bits 8,7 of CFN} \]

\[ \text{FA<0?} \rightarrow \text{FN<0?} \]

\[ \text{YES} \rightarrow \text{STORE: } \text{FN} \rightarrow \text{bits 15, 14 of CR5+CH} \]

\[ \text{G/4} \rightarrow \text{X'0888'} \]

\[ \text{STORE: } 1 \rightarrow \text{SFA+FN} \]

\[ \text{SUBTRACT: } \text{FN} \rightarrow \text{FN, } \text{rotate & store, FN} \rightarrow \text{FA, FA plus} \]

\[ \text{RESTORE STATE} \]

\[ \text{ERROR EXIT} \]

\[ \text{TECH/CHAN NOT ASSIGNED} \]

\[ \text{RETURN} \]

\[ \text{FORMAT FOR WD CODES, CONNECTION MEMORY} \]

\[ \text{FN ASSIGNED RIGHT JUSTIFIED UNTIL LAST STEP HERE} \]

\[ \text{FORMAT FORA} \]

\[ \text{GOOD BRANCH FM GEN ASSIGNMENT} \]

\[ \text{ERROR EXIT} \]

\[ \text{TECH/CHAN NOT ASSIGNED} \]

\[ \text{RETURN} \]

\[ \text{FORMAT FORA} \]

\[ \text{GOOD BRANCH FM GEN ASSIGNMENT} \]

\[ \text{RETURN} \]
**FIG. 8 SC TECHNIQUE - CANCEL PARAMETER CHANGE OR DISMISS**

**PASS 1 OF 4**

1. **SCTC** → INTR. 000103B
   - **DISABLE RPT20**
   - **STORE STATE**

2. **TW 15 THEN WIND**
   - **TA is Tech and Assignment**
   - **PA is Param. Change**

3. **LOAD:**
   - **STA → TW**
   - **SPA → PA**

4. **STORE:**
   - **ZERO → STAT**
   - **005773B = STATUS**
   - **Clears Miss FLG**

5. **AD is Aux(Assign) Detect**
   - **CH is CHAN**

6. **GEN LOAD(ADDR) GL = 175000B**

7. **AD=FO01H**
   - **YES**
   - **Change Aux Freq/Addr**
   - **A/2**

8. **PA=FO01H**
   - **YES**
   - **Dismiss Assignment**

9. **NO**
   - **A/4**

**NOTE:**
1. **PA = FO00H** dismisses the assignment.
2. **PA ≠ FO00H and AD ≠ FO01H** change current GEN parameters. If in proper code, PA does not change parameters in Tech Proc. Memory.
3. See format of PARAM.
4. **CHNL or other control (Fig. 3)**
5. TO INLB DISMISSES ALL CHANNEL ASSIGNMENTS.

**Signature:** R. McElroy

**Date:** 7/23/76
TN is Tech No. x 2 —
TN is Tech No. x 8 —
(Tech) Pos Start - PS = 00000008 —

PW is Param Word
CD is (Gen) Code

INC NXT; TN+1 → TN

No

CD = 15

Yes

RC is Response Command
AUX (Bus) Command - AC

MASK 1-3 of PW → RC
MASK R = 0
PA → AC

LOAD: RC & PA
LOAD: A → X + CH

RESTORE STATE

RETURN

This Wait mem changes Aux Bus
As; MT - ACM or FRET
For this channel
PFR SC command

Fetch Techn Mem END word.

Combine Techn Mem XOR, XOR, 4 CH bits & END word with new
Aux Bus Assignment as PA
This routine dismisses a channel assuming resources R&R2/R3 and/or FM GEN IF assigned.

**Figure 8: SC TECH-CNAM PARAM, CHG OR DISMISS**

**32C2 (CONT'D)**

**REDATE 12/19/76**

**CRS is CHAN-RESOURCE**

**STATUS ADDR BASE TABLE II**

**RN is R&R2/R3 GEN NO. ASSIGNED TO THIS CHAN**

**SRA is R&R2/R3 GEN ALLOCATION TABLE II**

**OR, DISMISS R&R2/R3 GEN AND EQUALS X'8000'**

**FN is FM GEN NO. ASSIGNED TO THIS CHANNEL**

**SFA is FM GEN ALLOCATION TABLE II A**

**DF is DISMISS FM GEN AND EQUALS X'8000'**

**SIGN STORE**

**LOAD: CRS 13 LOAD BL 2,10 B+CH 2 RN**

**STORE: ZERO 3,10 B+CH**

**STORE: SRA + RN X08ED**

**STORE: RN NO. HP RSS OR: XVRN 2 X**

**STORE: DF 2 X+CH**

**LOAD BIT 15H CR$7CH 2 FN**

**STORE: ZERO +B15H CR$7CH**

**STORE: SFA + FN X0881**

**SUB: FN 2 FN # 8, ROTATE LF 11**

**OR: FN VDF 2 DF STORE: DF 2 X+CH**

**Signed Dismissed: 12/19/76**
FIG. 8 5C TECH-CARD PARAM. CHG OR DISMSS
5C50 (CONT'D)

REDUM 12/19/76

CD IS REDUM CODE

crs IS CARD-RESOURCE STATUS ADDR. BASE TABLE II

FN IS FN RGN. NO. ASSIGNED TO THE CARD.

RN IS RR/RCPG GEN. NO. ASSIGNED TO THE CARD.

LOAD Bits 16-12
OF CR5-CH → RN
ROTATE RN LEFT 4 PLACES → RN

OR:
X OR RN = X

RR/RCPG GEN.
PARAM. CHANGE

LOAD Bits 15-14
OF CR5-CH → FN
ROTATE FN LEFT 11 PLACES

OR:
PAV FN → PA

NOTE: CHANGE FOR:
ANGLE TECHN'S.
RGN TECHN'S.
ARE SERVICED WITHOUT
DATA OR ADDR.
MODIFICATIONS

STORE:
PA → X+CH

RESTORE STATE

RETURN

Howard 12/19/76
Program memory. This module alternatively dismisses a particular Channel-Technique assignment. See notes of Figure 8 for codes. The routine for channel-technique dismissal also performs the resource management update of RAN-RAP/RGPO generator allocations.

3.2.7 SC Program Control (SCPC) Module

This module is a growth module to allow great flexibility to enable the TG RP-16 to execute instructions sent by the SC. The hardware is designed to accommodate this, but currently the SC External Control via hardware address is sufficient. See Figure 10 of 53959-HM-0410.

3.2.8 Channel-VCO Frequency Set-on (CVFSO) Module

CVFSO shall be the interrupt routines of Figure 9. This routine is requested every 0.1 second by each channel-technique assigned. It currently is a linear integration of error correction. Growth software could provide other correction to include even a transfer table for VCO tuning command to frequency output. The routine calls subroutine Convert and Load Tuning (CLT) to select VCO subband and tuning, within subband.

3.2.9 Auxiliary Bus Frequency (ABFR) Module

ABFR is the interrupt routine of Figure 10. This routine services frequency assignment updates for response-assigned channels, whose assignment includes Auxiliary bus update enable. The module uses the Frequency Update (FUP) subroutine which exits directly to LOOP.

3.2.10 RAN-RAP Cover (RRC) Module

RRC is the interrupt module of Figure 11. As noted thereon, this function is performed for each of the four RAN-RAP/RGPO generators. List I of paragraph 3.3 gives the priority level and least significant octal addresses for each generator service module. This module uses RAN-RAP A version (RRA) subroutine and generates a single element RAN-RAP. Internal
FIG. 9  CHANNEL-VCO FREQUENCY SET-ON

**CV** is CHAN-VCO

**FM** is FREQ MSMT

**CH** is CHAN

**SF** is FREQ ADDR of FREQ TABLE

**FE** is FREQ ERROR

**ST** is FREQ ADDR of TUNING TABLE

**SB** is Subind Indicator

**AT** is Absolute Tuning

**CLT** is CONVERT AND LOAD Tuning to Tuning Memory

**INR. 0000708**

**LOAD:**

ICV → CV

IFM → FM

**MASK:**

X'3FF '

CH

**LOAD:**

SF → B

(LB+CH)*-MA+FE

**LOAD:**

ST → X

X+CV → A

**ADD:**

AT+FE → AT

**USE JS48 CALL**

**DISA8L RPTZ0, STORE STATE**

**LOAD:**

ICV → CV

IFM → FM

**MASK:**

X'003F'

CH+4

CH

**MASK:**

X'0003'

**LOAD:**

SF → B

(LB+CH)*-MA+FE

**LOAD:**

ST → X

X+CV → A

**ADD:**

AT+FE → AT

**USE JS48 CALL**

**RETURN**

**NOTE:** See Table for Freq & Tuning Table Structures.
Fig. 10 Aux Bus Frequency

ABFR INTR: 0000602

DISABLE ROUTS
STORE STATE

LOAD:
ACN \to CH
AFREQ \to FREQ

CH is CHANNEL
17537
17537

FUP is FREQ UPDATE
SUBROUTINE
(see SC ASSMT-
FREQ ACN PAGE 2)

FUP

JUMP UNCOND.

RETURN included in FUP

Note: Register states must be appropriate to FUP

J. McDowell
7/27/76
Fig. 11. RAN RAP COVER

Notes:
1. There is one of these programs for each of
   4 RRA/RSPA Gen 3
2. See List II for
   LIV, even odd asserts

WA is word A
WB is word B

RRA is RAN RAP -
A version

CC is cell-count set
by RRA subroutine

PL is pulse storage
start addr

CC is relative storage
cell location of
a pulse delay

EG is EARLY COMMIGATE
DELAY

LG is LATE COMMIGATE
DELAY

See Table III

*
pulse delay storage shall be as in Table III.

3.2.11 RAN-RAP Cover and Early (RRCE) Module

RRCE is the interrupt module of Figure 12. The description of paragraph 3.2.10 is generally the same except these routines generate a two-element RAN-RAP.

3.2.12 RAN-RAP Cover and Late (RRCL) Module

RRCL is the interrupt module of Figure 13. This is another two-element RAN-RAP similar to paragraph 3.2.11.

3.2.13 RAN-RAP Cover, Early and Late (RRCEL) Module

RRCEL is the interrupt module of Figure 14. This is a three-element RAN-RAP built up from the single element of paragraph 3.2.10. Note that growth software can have many variations in delay pulse configurations for this RRCEL as well as for RRC, RRCE, and RRCL.

3.2.14 Range Gate Pull Off (RGPO) Module

RGPO is the interrupt module of Figure 15. As noted thereon this function shall be performed for each of four RR/RGPO generators. List I gives the priority levels and addresses.

3.2.15 Frequency Update (FUP) Subroutine

FUP is the subroutine of Figure 16. As noted thereon frequency assignment modules SCAFA and ABFR shall use the subroutine. Internal tables used are those of Table I. Essentially this subroutine shall update the tuning of each of four VCO's by the same amount the channels assigned frequency is changed. Growth software can have a more complex tuning update if tests with MAAS equipment indicate a need. FUP uses the subroutine Convert and Load Tuning (CLT).
Fig. 12 Ran Rap Cover and Early

Notes: 1. There is one of these programs for each of 4 RR/Rapo gens
2. See Table III for LVL, EVEN, ODD ASSMS

WA is word A
WB is word B 1753H(EVEN)\textsubscript{A}
1753H(ODD)\textsubscript{B}

RRA is Ran Rap A Version

CC is Cell Count, Set by RRA
{PL is pulse storage start addr. \* \*
CC is also relative storage cell location of pulse delay
EG is Early Commit Gate Delay
LG is Late Commit Gate delay
EO is Early (Element) Offset, currently 4.4 usec

\* See Table III
Fig. 13  RAN RAP COVER AND LATE

Notes: 1. There is one of these programs for each of 4 RRA/RG85 gen.
2. See LIST I for LVL EVEN, ODD ASSMT.

WA is word A
WB is word B 17534(EVEN) 8
17534(ODD) 8

RRA is RAN RAP
A VERSION

USE JS48 CALL

CC is Cell Count set by RRA

PL is pulse storage start addr.

CC is also relative storage cell location of pulse delay

EG is Early Commit Gate delay
LG is Late Commit Gate delay

LO is Late (Element) Offset, currently 4 = 6 µsec.

RS is RGEN Pulse delay mem. addr.

* see TABLE III

1/30/75
J. R. McCallum
Fig. 14 Ran RAP-Cover, Early and Late

Notes: 1. There is one of these programs for each of 4 R8/R8P3 gens.
2. See list Z for LUL, EVEN, ODD ASSIGN

WA is word A
WB is word B

RRA is RAN-RAP
A Version

17534(ENV)
17534(ODD)

RRCA

A

RRCel

DISRBL RAP20
STORE STATE

LOAD:
RWA → WA
RNB → WB

INTR. 0000 (LYL) B
CC is cell count set by RRA

Pulse storage start addr

CC is relative storage cell location of pulse-delay

EG is Early Commit Gate delay

LG is Late Commit Gate delay

EO is Early (Element)
Offset, currently in use.

LO is Late (Element)
Offset, currently in use.

RS is RRSFn pulse delay mem addr.

* See Table III

FLG 14 RAN RAP COVER Early and Late (Cont'd) PAGE 20

X'083F'

YES

X'0830'

LOAD: PL+CC→A
STORE: A→RS

SUB: A-EO→A
STORE: A→RS

ADD: A+EO+LO→A
STORE: A→RS

DECRT: CC-1→CC

X'08E4'

LOAD: EG→A
SUB: A-EO→A

STORE: A→RG

LOAD: EG→A
SUB: A-EO→A

STORE: A→RG

LOAD: LG→A
ADD: A+LO→A

STORE: A→RG

RESTORE STATE

RETURN

RG is RRSF commit gate mem addr.

AR. McQuillen
7/30/78
**FIG 15  RANGE GATE PULL OFF**

Note: 1. There is one of these programs for each of HRR/REP GEN's.

2. Sec 2.1.5 for LWL, EVEN, ODD ASSETS

WB is word B

WA is word A

PW is Pulse Width

PWJ is start of pulse with conversion table, \( x'OBES \)

RD is pre trigger,

Currently \( 25.6 \mu \text{sccs} \)

LSB = 62.5 nanosecs, \( x'OBES' \)

CV is Cover Pul Delay

PD is Pull-off Delay

SS is Scratch-Pul. Delay

\( RG \) is GEN

**DISABLPUL\( \rightarrow \) STORE STATE**

\( RGPO \) \( \rightarrow \) INTR. SOCC(OOD)\( \rightarrow \)

LOAD:

\( RWB \rightarrow WB \)

LOAD:

\( RWA \rightarrow WA \)

LOAD:

\( RWJ \rightarrow PWJ \)

LOAD:

\( PWJ \rightarrow B \)

LOAD:

\( 8 + PWJ \rightarrow PD \)

LOAD:

\( PD \rightarrow CV \)

LOAD:

\( CV \rightarrow PD \)

LOAD:

\( A \rightarrow SS \)

ADD:

\( 2 \times \frac{PD + A}{2} \)

STORtED:

\( A \rightarrow RG \)

\( \frac{17534(OOD)}{8} \)

**STORES DATA END OF COMMIT GATE**

HR. McKinley

7/26/76
FIG. 15  RANGE GATE PULL-OFF  (CONT'D)

TH is Threshold Delay
for Cover Start and
AMI check, currently ~ 2 / 12 sec
LSB = 62.5 nanosec.

TD is Tuning Delay, currently
> 10 / 12 sec.
LSB = 63.5 nanosec.

bit 11 of WB is
AMI bit
1 → AMI
0 → AMI

MASK bit of
WB → A
FOR:
A VSS → A

PD > TH

STORE:
CV → RS
STORE:
CV - TD - A

17534 (EVEN) / 8
STORES COVER PULSE

STORE:
A → RG
STORE:
17534 (ODD) / 8
STORES EARLY
(STARTUP) GATE
PULSE

STORES EARLY
(STARTUP) COMMIT
GATE

548:
A - TD → A
STORE:
17534 (ODD)
A → RG

STORE:
A - TD → A
STORE:

RESTORE STATE

RETURN
Fig. 16 Frequency Update Subroutine

1. **FIP**

   - **ENTRITED FROM**
     - **SUBSNDJ, JSUBP**

2. **LOAD**
   - SF → B
   - FREQ → B+CH + DF

3. **STORE**
   - FREQ → B+CH

4. **LOAD**
   - ST → X
   - L → V

5. **ROTATE CH D FE 2 PLACES**

6. **ADD**
   - CH + V → CV

7. **LOAD**
   - X + CV → A

8. **MASK**
   - H → A & bit 0

9. **ADD**
   - AT + DF → AT

10. **CLT**

11. **A**

**Note:** This subroutine is entered from **SUBSNDJ** or **ABFP**, so the same register states are anticipated. This subroutine returns directly to **LOAD**.

- Grows: 3 → V
- To handle four VCO's
- MASK has only two 0's

**CV & CHAN-VCO**

**SB** is **SUBBD INDICATOR**
- 0 = Lower
- 1 = Upper

**AT** is **Absolute Tuning**

**CLT** is **CONVERT AND LOAD TUNING TO TUNING MFM.**

---

*See TABLE I for Freq & Tuning Tables Structures.*
Fig. 16 FREQUENCY UPDATE SUBR. (CONT'D)

A

DECREASE V.

V < 0?

NO

YES

RESTORE STATE

RETURN

B

REALLY A JUMP TO "LOOP"
3.2.16 Convert and Load Tuning (CLT) Subroutine

CLT is the subroutine of Figure 17. This subroutine shall convert the calculated absolute tuning frequency to tuning frequency by subband designation and relative subband tuning command. This routine assumes an upper subband VCO in the MAAS transmitter. It includes hysteresis for overlap of subbands, and assumes subband tuning is proportional above a lower value for each subband. The overlap and the lower values of each subband are programmable.

3.2.17 RAN-RAP A Version (RRA) Subroutine

RRA is the subroutine of Figure 18. This subroutine sets up the basic element pulse delay patterns for all RAN-RAP programs. It also sets up the basic commit gate start and end.

3.3 STORAGE AND PROCESSING ALLOCATION

The Technique Generator RP-16 Controller memory allocations are given in Figure 15 of reference 53959-HM-0410. Of the 4K-word memory, the upper 1K is currently allocated to T.G. Techniques Program memory. Within the remaining 3K, the software instructions and data objects of this CPDS are to fit. All other addresses are given in the cited reference and listed herein where needed.

Tables I through III are the important internal data-object tables for the T.G. Controller Program. Use of these tables is given in the appropriate functional description of paragraph 3.1. List I gives the RR/RGPO Generators priority and address assignments. List II summarizes important program data objects. List III allocates total RP-16 addresse space, including programs and data.

3.4 COMPUTER PROGRAM FUNCTIONAL FLOW

Program flow is described in paragraph 3.1 and Figure 1, and 2. Interrupt levels and assignments are given therein.
**Fig. 17** Convert and Load Tuning (To Tuning Memory) Subroutine

- **LOAD:** TM→B  
  - TM is start of tuning memory  
  - 175200

- **SB is Subadd Indicator:**  
  - 0 = Lower  
  - 1 = Upper

- **LL is Limit of Lower Subadd, currently ≤ 12 GHz  
  - LSB = 1.25 MHz

- **AT is Absolute Tuning:**  
  - x'OBDE'
  - From Caller

- **A < 0?**  
  - YES: Go to Upper Subadd  
  - NO: Stay in Lower Subadd

- **C/2**  
  - LT (Lower Subadd)  
  - Threshold: currently ≤ 8 GHz  
  - LSB = 1.25 MHz

- **STORE:**  
  - AT+CV  
  - AT-LT→A

- **STORE:**  
  - A→B+CV  
  - B/2

- **Note:** AT has SB=0.

- **STORES Relative Tuning & General Flag—Exit**

---

**Note:** This subroutine can be expanded to include VCO tuning curves if later VCO tests so indicate.
FIG 17 Convert and Load Tuning Subroutine (Cont'd)

UT is upper Sub8d THREE.
Should be ± MHz
LSB = ± 0.25 MHz

UT @
X'DBDF'

A < 0?

Yes
Go to lower Sub8d

No
Stay in upper Sub8d

STORE:
A → TR

TOR:
SB V AT → A
STORE:
A → X + CV

ROTATE:
SB RV 3 places
TOR:
SB V TR → A

D/1

X is from caller
X = 3I

Page 2 of 2
Upper Sub8d Test

TR is a temporary register for upper Sub8d relative tuning.

STORE absolute tuning and Sub8d flag.

Moves flag from bit 15 to bit 12, and includes rel. tuning for storage in tuning mixing.

AI: 7/4/77

1/12/77
**Fig. 18 RAN RAP A Version**

**Subroutine**

**RRA**

- **Enter From**: Caller Routines
  - RRC, RRCF, RRCL
  - RRCFL
  - Needs Correct Register States.

- **PW** is Pulse Width
- **PWS** is Start of Pulse Width Conversion Table

**PR** is Pretrigger
- Currently = 25.6 usec
- 1.93/2.5 nanoseconds

**CV** is Cover Pulse Start

**CC** is Cell Count

**PD** is Primary Delay

**PP** is Primary Pulldown Direction

**FG** is Fixed Gate Delay

**PL** is Pulse Storage Start × 0810

**EP** is Early Primary Pulse Delay

**LP** is Late Primary Pulse Delay

**References**

- Mask: X'0E00'
- Mask: RPN of WA → PW
- Load: PW → B
- B + PW → B
- Sub: PR - PW → A
- Load: A → CV
- Store: CV → EL
- Mask: R-byte of WA → PD
- Mask: Bit 8 of WA → PD
- Mask: From WA
- Sub: FG → FG
- Shift FG Left 3 bits → FG

**Flowchart**

1. **ADD**: CV + FG → A
2. **SUB**: CV - FG → A
3. **ADD**: PW + A → A
4. **ADD**: A + EP → A
5. **ADD**: CV + EP → A

**Conditions**

- **FG < PD**
- **PP = 1**
- **FG ≤ PD**

**Instructions**

- **STORE**:
  - A → PL + CC
- **STORE**:
  - A → PL + CC
- **STORE**:
  - A → PL + CC
- **STORE**:
  - A → EP

**Notes**

- Store Delay PLs Prim Neg
- Store Delay PLs Prim Pos

**Signature**

[Signature]
Fig. 18
RUN-RAP AVERSION
SUBR. (CONT'D)

AD is Altern. Delay
AP is Altern. Pull direction

ADD:
CV+FG → A
STORE:
A → PL+CC

STORES
DROP PLUS
+ ALT.

INC/MT:
CC+1 → CC

MASK R- bytes of
WB → AD
MASK A- bytes of
WB → AP

SUB:
CV- FG → A
STORE:
A → PL+CC

STORES
DROP PLUS
- ALT.

INC/MT:
CC+1 → CC

ADD:
CV-AD → A
STORE:
A → PL+CC
STORE DEAY
PLUS ALT.

EA is Early Altern. 
PULSE 
DELAY

LA is Late Altern. 
PULSE 
DELAY

ADD:
2×BY+ A → A

STORE:
A → LA
STORE:
CV → EA

LOAD:
EA → A

LOAD:
EP → A

SUB:
A-7D → A
STORE:
A → EG

STORE EARLY
(START OF) COMMIT GATE

TD = X'08F2'
T.D. is Tuning Delay
Currently = 10.415SEC.
LSB = 63.5 microsec
EG is Early Commit Gate
Delay @ X'6B3D'

NOTE:

J.R. McDowall
7/29/78
LG is Later Commit Gate Delay @ X'OB3E'

FIG. 1B
RAN-RAP  A VERSION
SUBR (CONT'D)

Page 3 of 3

STORE:
LP → LG

LP < LA

STORE:
LA → LG

STOP
LATE (END OF)
COMMIT GATE

RESTORE STATE

RETURN TO CALLER
### TABLE I FREQUENCY AND TUNING LOCAL DATA STRUCTURES

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$SF + OH$</td>
<td>FREQ ($C_H$) 1481/3</td>
</tr>
<tr>
<td>$SF + F_H$</td>
<td>FREQ ($F_H$)</td>
</tr>
</tbody>
</table>

**ASSIGNED FREQUENCY TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ST + O_{1,0}$</td>
<td>TUN ($O_{2,0}$)</td>
</tr>
<tr>
<td>$ST + O_{1,1}$</td>
<td>TUN ($O_{2,1}$) 617.15</td>
</tr>
<tr>
<td>$ST + O_{2,2}$</td>
<td>TUN ($O_{2,2}$) 0 → SUBBD 1-Lower</td>
</tr>
<tr>
<td>$ST + O_{2,3}$</td>
<td>TUN ($O_{2,3}$) 1 → SUBBD 2-High</td>
</tr>
<tr>
<td>$ST + F_{H,0}$</td>
<td>TUN ($F_{H,0}$)</td>
</tr>
<tr>
<td>$ST + F_{H,1}$</td>
<td>TUN ($F_{H,1}$)</td>
</tr>
<tr>
<td>$ST + F_{H,2}$</td>
<td>TUN ($F_{H,2}$)</td>
</tr>
<tr>
<td>$ST + F_{H,3}$</td>
<td>TUN ($F_{H,3}$)</td>
</tr>
</tbody>
</table>

**TUNING TABLE**

**Also see List III**

*Note: These are used in FSP UPDATE (FSPD) subroutine, and CHANNEL-VCO PREP DETON (CVPDD) module.*

[Handwritten note: AP, 7/30/96]
# TABLE II CHANNEL-RESOURCE, AND RESOURCES
LOCAL DATA STRUCTURES

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA: 8:15</th>
<th>13 - 3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRS + OH</td>
<td>FN</td>
<td>ZERO</td>
<td>RN</td>
</tr>
<tr>
<td>CRS + FH</td>
<td>FN</td>
<td>ZERO</td>
<td>RN^T</td>
</tr>
</tbody>
</table>

**CHANNEL-RESOURCE TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA: 8:15</th>
<th>13 - 3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRS + 18</td>
<td>0005H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRS + 48</td>
<td>0005H</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**RR/RSPO GENERATOR PRE-OPERATION STATUS TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA: 8:15</th>
<th>13 - 3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRA + 18</td>
<td>000AH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRA + 48</td>
<td>000AH</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**RR/RSPO GENERATOR ALLOCATION (OPERATION) TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA: 8:15</th>
<th>13 - 3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRA + 18</td>
<td>000AH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRA + 48</td>
<td>000AH</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SRA IS RR/RSPO GEN Alloc Address**

**SRS IS RR/RSPO GEN Status Addr.**

**Used by**
INITIALIZATION (CENLZ) Module,
SC TECH ASMT (SCTA) Module,
AND SC TECH-CH FRM, CHS OR DISMISS Module (SCTEC).

**WP - OCTAL**
0 - NONE
1 - GEN #1
2 - GEN #2

**RN - OCTAL**
0 - NONE
1 - GEN 1
2 - GEN 2
3 - GEN 3
4 - GEN 4

**ALSO SEE LIST III**
### Table A: Resources Local: Data Structure Continued

<table>
<thead>
<tr>
<th>ADDR #</th>
<th>DATA HEX</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFS + 1</td>
<td>0000 SHA</td>
<td>0</td>
</tr>
<tr>
<td>SFS + 2</td>
<td>0000 SHA</td>
<td>1</td>
</tr>
</tbody>
</table>

**FM GENERATOR PRE-OPERATION STATUS TABLE**

<table>
<thead>
<tr>
<th>ADDR #</th>
<th>DATA HEX</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFA + 1</td>
<td>0000 SHA</td>
<td>0</td>
</tr>
<tr>
<td>SFA + 2</td>
<td>0000 SHA</td>
<td>1</td>
</tr>
</tbody>
</table>

**FM GENERATOR ALLOCATION (OPERATION) TABLE**

---

Handwritten note:

Howard W. G. 11/9/76
**TABLE III** | **RAN-RAP PULSE DELAY STORAGE AND PULSE WIDTH CONVERSION TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc</td>
<td>cell count</td>
</tr>
<tr>
<td>PL is pulse storage start</td>
<td>PL + 0</td>
</tr>
<tr>
<td>CC is cell count</td>
<td></td>
</tr>
<tr>
<td>Used by all RAN-RAP modules and subroutine</td>
<td>PL + 5</td>
</tr>
</tbody>
</table>

**RAN-RAP PULSE DELAY TABLE**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA - ( \frac{PW}{2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>PW is pulse width code</td>
<td>bits 5-0</td>
</tr>
<tr>
<td>PWS + 18</td>
<td>1.5 ( \mu \text{sec} = 308 )</td>
</tr>
<tr>
<td>+ 38</td>
<td>1.0 ( \mu \text{sec} = 208 )</td>
</tr>
<tr>
<td>+ 58</td>
<td>0.6 ( \mu \text{sec} = 108 )</td>
</tr>
<tr>
<td>+ 68</td>
<td>0.25 ( \mu \text{sec} = 48 )</td>
</tr>
</tbody>
</table>

**PULSE WIDTH CONVERSION TABLE**

**ALSO SEE LIST III**

H.R. McDuffie
1/30/74
List II: RR/KSPD GENERATORS -
PRIORITY LEVEL, AND ADDRESS
LSB ASSIGNMENTS

<table>
<thead>
<tr>
<th>GEN#</th>
<th>(Priority)</th>
<th>LVL 8</th>
<th>EVEN 8</th>
<th>ODD 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>6</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

* PULSE STROBE DELAY MEMORY
II COMMIT GATE DELAY MEMORY

[Handwritten note: HR. Y. [Signature] 7/30/76]
### List II  Important Data-Objects and Users

<table>
<thead>
<tr>
<th>REF.</th>
<th>Description</th>
<th>Using Module(s) or Subroutine(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT</td>
<td>Count - No. LOOP entries after INLB</td>
<td>INLB, LOOP</td>
</tr>
<tr>
<td>C5S</td>
<td>Channel Resource Table Start</td>
<td>INLB, SCTA, SCTCC</td>
</tr>
<tr>
<td>SRS</td>
<td>Start of RR/RAP Status Table - Programmable</td>
<td>INLB</td>
</tr>
<tr>
<td>SRA</td>
<td>Start of RR/RAP Allocation Table - During Run</td>
<td>INLB, SCTA, SCTCC</td>
</tr>
<tr>
<td>PS</td>
<td>(Technique) Program Start - 0080008 Program</td>
<td>SCTA, SCTCC</td>
</tr>
<tr>
<td>SF</td>
<td>Start of Frequency (Assignment) Table</td>
<td>CVF30, FUP</td>
</tr>
<tr>
<td>ST</td>
<td>Start of Tuning (Absolute) Table</td>
<td>CVF30, FUP</td>
</tr>
<tr>
<td>PL</td>
<td>Pulse Storage - Start</td>
<td>RRLE, RRLE</td>
</tr>
<tr>
<td>EG</td>
<td>Early (Commit) Gate - start</td>
<td>RRLE, RRLE, RRCE</td>
</tr>
<tr>
<td>LG</td>
<td>Late (Commit) Gate - end</td>
<td>RRLE, RRLE, RRCE</td>
</tr>
<tr>
<td>TD</td>
<td>Tuning Delay</td>
<td>Pre-Run, Programmable</td>
</tr>
<tr>
<td>PR</td>
<td>Pretigger Delay</td>
<td>Pre-Run, Programmable</td>
</tr>
</tbody>
</table>

NR McBride 1/30/76
### LIST II (CONT'D) IMPORTANT DATA-OBJECTS AND USERS

<table>
<thead>
<tr>
<th>REF.</th>
<th>DESCRIPTION</th>
<th>DATA ITEM</th>
<th>USING MODULE(S) OR SUBROUTINES</th>
</tr>
</thead>
<tbody>
<tr>
<td>EO</td>
<td>Early (Element) Offset</td>
<td>Pre-Run Programmable</td>
<td>RRCE, RRCEL</td>
</tr>
<tr>
<td>LO</td>
<td>Late (Element) Offset</td>
<td>Pre-Run Programmable</td>
<td>RRCL, RRCEL</td>
</tr>
<tr>
<td>PWS</td>
<td>Pulse Width Conversion Table Programmable</td>
<td>Pre-Run Table Fixed</td>
<td>RRA</td>
</tr>
<tr>
<td>CH</td>
<td>Channel Variable 0 thru 15</td>
<td>VARIABLE</td>
<td>INLE, S2AFA, SC7CC, CVS2, 400ER</td>
</tr>
<tr>
<td>RN</td>
<td>RR/AGPO, GA. No. Variable 1 thru 4</td>
<td>VARIABLE</td>
<td>INLE, SC7TA, SC7CC</td>
</tr>
<tr>
<td>AN</td>
<td>Angle Cell No. Variable 0 thru 31</td>
<td>O thru 31</td>
<td>SCAFA</td>
</tr>
<tr>
<td>TNX8</td>
<td>Technique No. Var. 0000 thru 1779</td>
<td>TABLE</td>
<td>SC7TA, SC7CC</td>
</tr>
<tr>
<td>CC</td>
<td>Cell Count- Run-RAP Delay Pulse No. Variable</td>
<td>Pre-run</td>
<td>RRG, RRA, RRAF, RRCE, RRCL, RRCEL</td>
</tr>
<tr>
<td>TH</td>
<td>Threshold Delay for Cover Insert/Remove Programmable</td>
<td>Pre-run</td>
<td>RGPO</td>
</tr>
<tr>
<td>LL</td>
<td>Lower Subband Limit Time HighThreshold Programmable</td>
<td>Pre-run</td>
<td>CLT</td>
</tr>
<tr>
<td>LT</td>
<td>Lower Subband Threshold Time Low Programmable</td>
<td>Pre-run</td>
<td>CLT</td>
</tr>
<tr>
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<td>Pre-run</td>
<td>CLT</td>
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3.5 PROGRAMMING GUIDELINES

Object program shall be machine code suitable for loading from the System Controller (SC) via the Daisy Chain (DC) bus. During development object program shall be available on paper tape for loading via a TTY terminal directly into the T.G. The latter includes an Asynchronous Line Control Module (ALCM) for TTY interface and a Hardware Loader program to accept inputs. Word formats and addresses are given in Figures 15, 16 and 17 of reference 53959-HM-0410.

Source programming can be in assembly language. The source program can be converted to object program using either the RP-16 Assembler, reference Equipment Division II, or the ESD Nova Cross-Assembler for the RP-16. RP-16 instructions and functions are described in reference Equipment Division I.
### List III: TGU RP16 Address Space Page 10 of 4

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<th>Data Type</th>
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<td>START OF RAM MEM DEFINED 10</td>
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<td>Interrupt Vector Addr's</td>
<td>DEFINED DURING CODING &amp; ASSEMBLY 111</td>
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<td>Current &amp; Growth</td>
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<td>006F</td>
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**Estimated Limit of 0.3FF** - Prog. Instr./Data

- Stack: 1853
  - Stack -1 = 083C
  - Top of Stack Used - VAR

**Total = 2877**

9/18/76
### List III - TSU RS-15 Address

**Space (Cont'd) Page 274**

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<td>Freq (Absolute) for Channel Assignments</td>
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*Note: TSU can handle 3, i.e., four VCO's.

VCO's are numbered: 0, 1, ...
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<td>RR LATE OFFSET</td>
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