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THESIS

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**THE OPERATION AND INTERACTION OF THE
AUXILIARY RESONANT COMMUTATED POLE
CONVERTER IN A SHIPBOARD DC POWER
DISTRIBUTION NETWORK**

by

Mark J. Oberley

December, 1996

Thesis Advisor:

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Lieutenant, United States Navy
B.S., Colorado School of Mines, 1989

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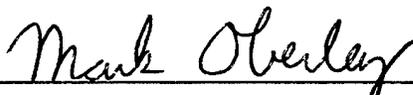
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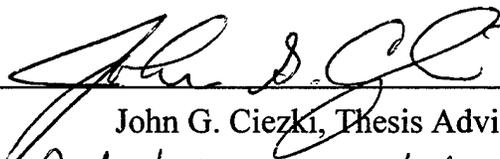
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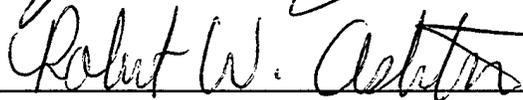


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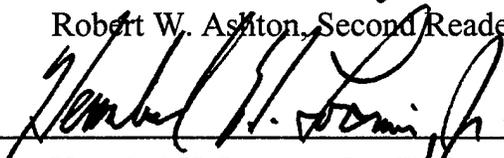
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ABSTRACT

The objective of this thesis is to investigate the use of the Auxiliary Resonant Commutated Pole Converter (ARCP) as a DC-to-AC power converter. The advantages and disadvantages of resonant converters over non-resonant, or hard-switched converters, are investigated. Basic ARCP circuit operation is modeled, with emphasis placed on examining the commutation between high and low voltage states. Detailed ARCP converter operation is modeled in software and compared to a software model of a hard-switched converter. Comparisons are made using total harmonic distortion calculations, to establish the reliability of using the hard-switched model to perform control synthesis for the ARCP.

Several control algorithms are tested through simulation and the results analyzed. The advantages of performing control in the synchronous vice stationary reference frame are shown. Testing on a reduced-scale circuit model using a digital signal processing system (dSPACE) to implement control algorithms is used to validate the control algorithm simulations. A new method of waveform modulation, Space Vector Control, is introduced and compared with conventional methods. Finally the operation of a prototype ARCP unit is discussed, and recommendations for improvements in future designs are presented.

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I. INTRODUCTION

Current naval shipboard power requirements are satisfied using classical AC power distribution employing transformers and three-phase transmission cables. As the Navy moves toward the "more electric" initiative for propulsion, electromechanical actuation and high power weapons systems on ships, submarines and aircraft, there is a need to capitalize on electric power developments [Ref. 1]. Improvements in semiconductor technology, specifically increased current density capabilities, have made advanced shipboard power distribution schemes using semiconductor devices realizable. Critical requirements for Naval electrical systems include reduction in size and cost, increase in power density, and the inclusion of intelligence within power devices that can provide electric power control, conditioning, and very high-speed switching [Ref. 1].

A. PROPOSED SHIPBOARD DC POWER SYSTEM

In order to best take advantage of the power electronics revolution, a new architecture for shipboard power distribution has been proposed [Ref. 2]. In this new distribution scheme the main feeders are DC. The ship is divided into zones, each zone containing common energy conversion devices fed from the DC busses. As shown in Figure 1-1, DC is distributed via port and starboard busses from the source(s) into the separate zones [Ref. 3]. Each zone contains a number of Ship Service Converter (SSCM) and Inverter Modules (SSIM). The SSCM is used in each zone to step-down the distribution bus voltage to a regulated level for use in the zone. In this way the SSCM

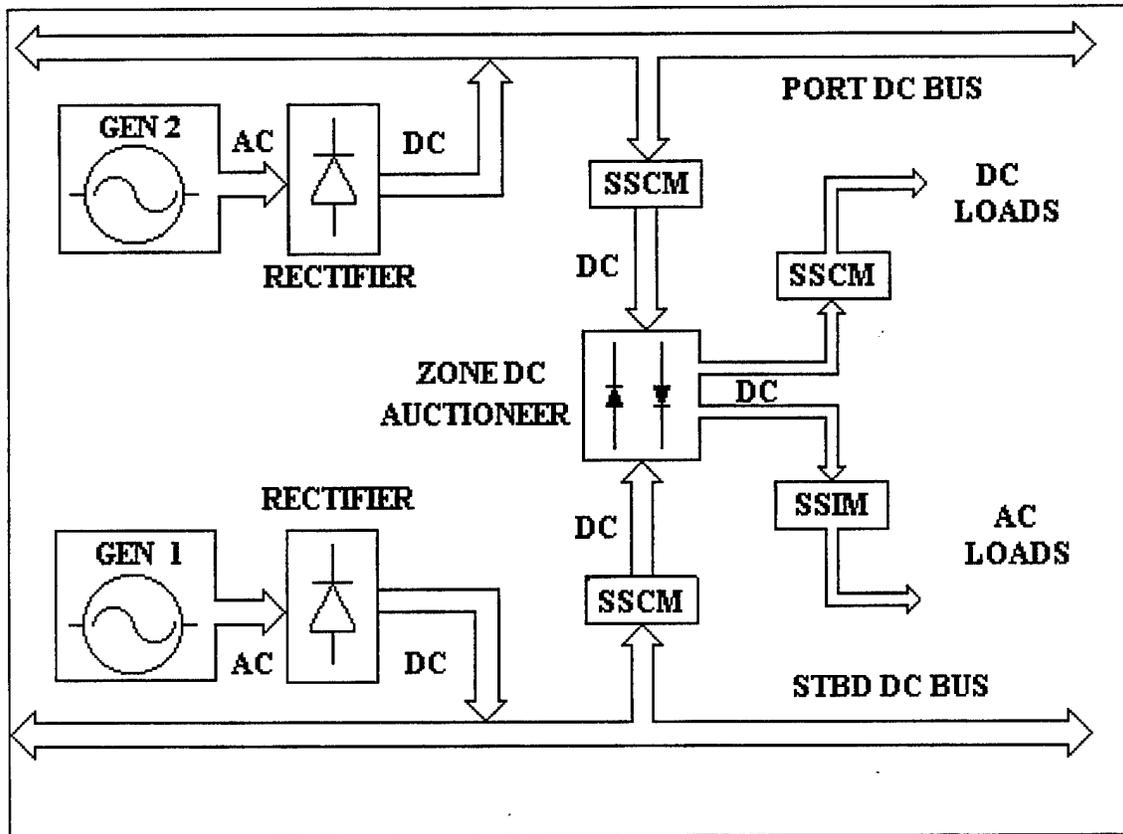


Figure 1-1 - Integrated Power System (from [Ref. 3])

inserts intelligence into the system by acting as a buffer, preregulator and fault protection for each zone. Electric loads within the zone are fed by either SSCM's or SSIM's depending on the load's requirement for DC or AC power.

The focus of this thesis is on the SSIM. Traditionally DC-to-AC converters have been uni-directional power flow, non-resonant type devices. Allowing bi-directional (DC-to-AC and AC-to-DC) power transfer improves the efficiency of the system since energy that would be unrecoverable in a uni-directional system, such as during motor braking, can now be captured and returned to the system. Resonant converters have lower losses and emit less electromagnetic interference. It is proposed to use a resonant

converter, specifically an Auxiliary Resonant Commutated Pole (ARCP) converter, as a SSIM.

The remainder of this chapter discusses the inherent advantages and disadvantages of resonant converters. In Chapter II the basic operation of the ARCP is presented and the equations governing circuit behavior are developed. Chapter III deals with simulation of single-phase and three-phase converters and the comparison of hard-switched (non-resonant) and ARCP converter simulations. Control of converters with various loads and with various control designs is investigated in Chapter IV. A new pulse-width-modulation technique (Space Vector Control) which provides advantages over sine-triangle control is presented in Chapter V. Testing of control algorithms using a hard-switched converter and digital-signal-processing hardware is covered in Chapter VI. The operation and physical characteristics of a prototype ARCP converter are discussed in Chapter VII, together with suggestions for improving the circuit implementation. The final chapter, contains a summary of the research work, notable conclusions and recommendations for future work.

B. ADVANTAGES OF RESONANT CONVERTERS

Examining a typical switch in a power converter provides insight into the advantages of resonant converters. In the ideal situation with a switch closed and conducting a current I_{Load} , the voltage across the switch is zero volts. When the switch is gated off the current falls off linearly to zero and the voltage rises linearly to some final value which is based on the circuit topology. For purposes of illustration, the final value

of the voltage across the switch will be called V_{cc} . The power loss during switching will be the voltage times the current. Figure 1-2 shows idealized waveforms for turn on and

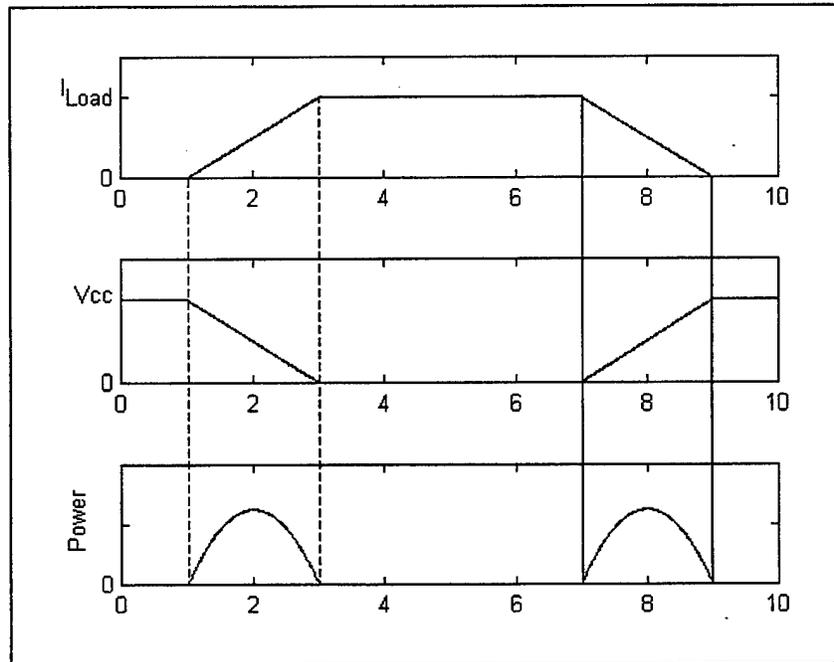


Figure 1-2 - Power Loss During Switching

turn off in the case of a resistive load. The current rise and fall times are controlled by the type of devices and the drive current used. For a typical 150 amp/1200 volt Insulated Gate Bipolar Transistor (IGBT) (POWEREX CM150DY-24E), the rise and fall times are 400 nsec [Ref. 4]. Most IGBT rise and fall times are on this order of magnitude, with larger current ratings having longer rise and fall times.

Each time the switch changes state a specified amount of energy is lost. Some of the energy is dissipated as heat and some goes to the generation of electro-magnetic-interference (EMI). The short rise and fall times cause significant energy to be generated in the radio frequency (RF) region [Ref. 5]. The more frequently the switch changes state the more energy is lost, thus the power loss is proportional to the switching frequency.

For high-frequency pulse-width-modulation techniques switching losses can be quite significant. This not only lowers the efficiency of the overall system, it also places stress on the devices used for switches. The ability of a semiconductor device to remove heat is limited. As the heat load increases, temperature rises which, in turn, degrades performance.

To reduce the stress on the devices used for switches and limit EMI, snubbers can be used. The goal of a snubber during device turn-off is to provide zero voltage while the current dies off. During device turn-on the snubber tries to maintain a zero current while the voltage drops off to zero. In this way current and voltage are not present in the switch simultaneously and thus ideally no power is lost in the switch. Additionally snubbers limit the di/dt and dv/dt of the switches which reduces the EMI emissions.

Figure 1-3 shows a typical turn-off snubber attached to a transistor [Ref. 5]. To analyze the snubber it is assumed that the transistor is initially gated, the voltage across it is zero and it is conducting a current I_{Load} . When the transistor is turned off the current will drop at a rate determined by the fall time of the device, and the voltage will rise as the snubber capacitor begins to charge. With the snubber capacitor in the circuit, the

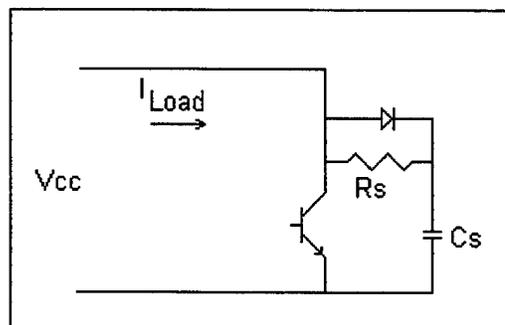


Figure 1-3 - Turn-Off Snubber

voltage rise is slower than the current fall off (depending on the value of the capacitor) and the energy lost in the switch is smaller than without the snubber. Figure 1-4 illustrates the waveforms for transistor turn off.

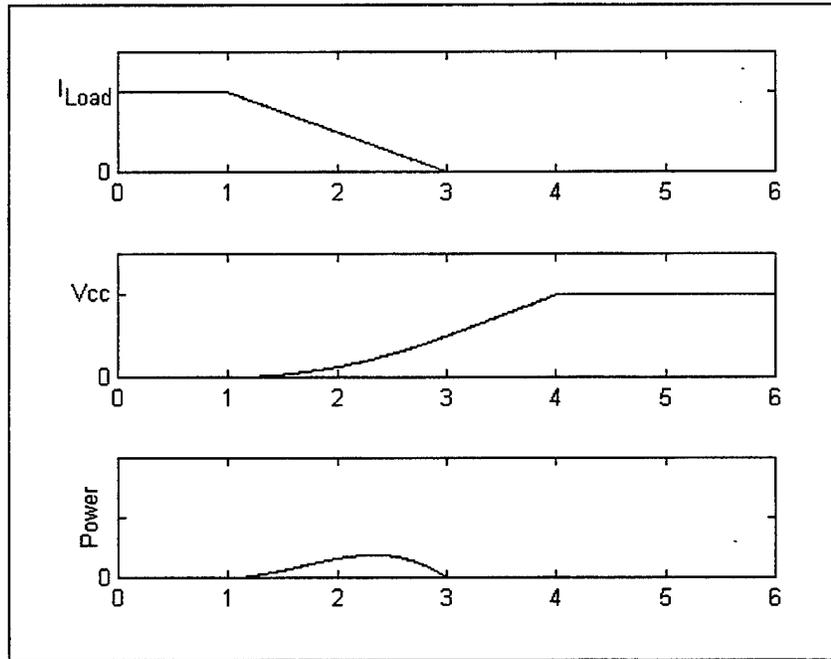


Figure 1-4 - Turn-Off Snubber Waveforms

The energy stored in the capacitor after turn off is dissipated in the resistor when the switch is turned on, thus the snubber does not improve the overall efficiency of the circuit but simply limits the stress on the transistor.

A turn-on snubber [Ref. 5] and the waveforms associated with it are shown in Figures 1-5 and 1-6. The snubber inductor limits the current build up until the voltage across the switch has died down. This limits the current loss in the switch. However, during the off time of the switch the energy stored in the inductor is dissipated in the snubber resistor, so the overall efficiency of the circuit is not improved. Since the

inductor is required to carry the entire load current, it is expensive and is seldom used alone.

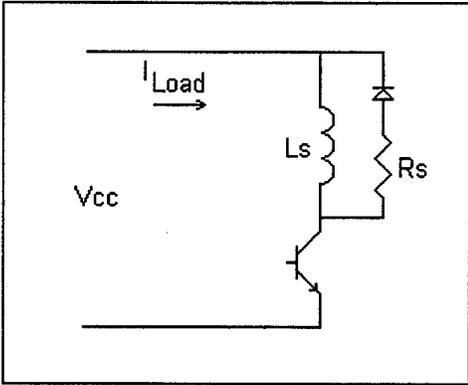


Figure 1-5 - Turn-On Snubber

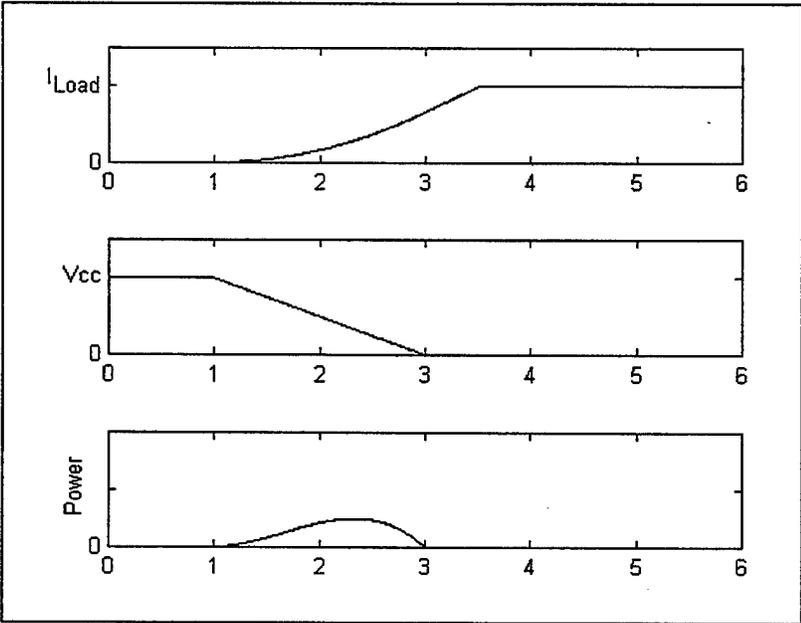


Figure 1-6 - Turn-On Snubber Waveforms

The previous discussion has shown that switch stress and EMI can be reduced by the use of snubbers but that the overall efficiency of the circuit is not improved. To improve the efficiency of the overall system the switching losses must be reduced and the energy saved in reduced switching losses must be somehow returned to the system.

Resonant converters attempt to accomplish this by using some type of LC resonance. As the voltage and current resonate, switches are turned on and off at either zero voltage (zero voltage switching) or zero current (zero current switching), thus avoiding power loss. Since the circuits resonate, the energy used to drive the circuit to a zero state is returned to the system avoiding energy loss. Electro-magnetic interference is also eliminated since no power is lost during switching.

Resonant converters are generally more complex than non-resonant converters. As a result, resonant converters are not normally used in low-power or low-frequency applications where the added cost and complexity outweigh the benefits of improved efficiency, lower switch stresses and reduced EMI. Higher power and frequency converters are more likely to be of the resonant type since the efficiency improvements begin to become significant. In general the decision to use a resonant converter is a tradeoff between complexity and efficiency and between increased initial cost and continued savings.

II. BASIC OPERATION OF ARCP CIRCUIT

This chapter contains a detailed analysis of the basic operation of the ARCP converter. A single-phase converter is used to explain the dynamics involved in commutation and how ARCP commutation differs from that occurring in a hard-switched inverter. Three different commutation situations are explained in detail, and the extension to three-phase power applications is demonstrated. The majority of the material presented on the ARCP is derived from DeDoncker [Ref. 6].

A. BASIC COMMUTATION

Operation of the Auxiliary Resonant Commutated Pole (ARCP) inverter is similar to that of a hard-switched inverter. The difference lies in the commutation between states. For the hard-switched inverter, commutation involves opening one switch and closing another. Thus, the inverter leg output voltage changes instantaneously, in the ideal case, from V_{DC} to zero, or vice-versa. In the ARCP in order to reduce switching losses, commutation is accomplished through additional auxiliary circuitry in a finite amount of time.

The basic single-phase ARCP circuit is shown in Figure 2-1. It consists of two main switches, S1 and S2, with associated free-wheeling diodes, D1 and D2; two auxiliary switches, A1 and A2; two DC supply capacitors, labeled $2C_{dc}$; two resonant capacitors, labeled $C_r/2$; a resonant inductor, L_r ; and a filter inductor L_f . The main switches operate much the same as in a classical hard-switched inverter. When the output voltage, V_f , is desired to be high switch S1 is closed and when the output voltage is

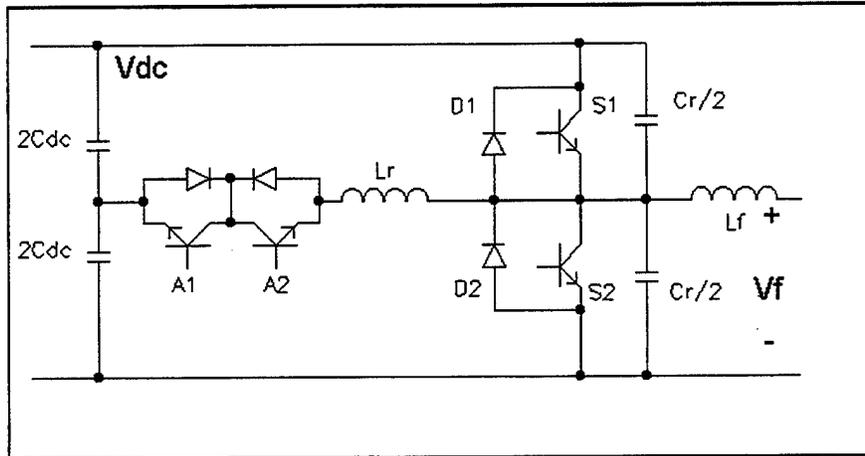


Figure 2-1 - Single-Phase ARCP

desired to be zero switch S2 is closed. Switches A1 and A2 along with the resonant inductor, L_r , make-up the *auxiliary circuit*. Auxiliary switches A1 and A2 are not required to turn off with current present and can be SCR's, GTO's, ZTO's or MCT's. The main switches S1 and S2 must be turn-off devices and can be GTO's, MCT's or IGBT's.

The auxiliary circuit is involved in commutation as is explained in the following sections. The resonant inductor along with the resonant capacitors determine the resonant frequency of the converter and thus define the speed at which the converter can be switched. The DC supply capacitors are large capacitors which provide a voltage equal to half of the source voltage at the center of the two capacitors. If the negative rail of the load is connected to this midpoint, an AC voltage with no DC offset is applied to the load. The filter inductor is normally several orders of magnitude larger than the resonant inductor and helps maintain the load current constant during commutation.

In order to implement an ARCP inverter in the laboratory, additional circuitry is required to monitor signals, gate-on the switches and provide necessary protection. This additional circuitry is not considered in the forthcoming discussion to focus attention on the commutation process. The auxiliary circuit and all of its attendant additional circuitry substantially increase the parts count of an ARCP inverter as compared to a hard-switched inverter and is one of the drawbacks that must be considered.

In a classical hard-switched inverter, shown in Figure 2-2, commutation involves simply turning off one switch and turning on another. In an ideal circuit the turn-on and turn-off can take place simultaneously; however, in a real circuit the time delays involved can result in a direct short across the source. As a consequence a time delay is typically implemented into the commutation process. Even with the time delay issue, the commutation and circuitry involved are much simpler than that associated with the ARCP.

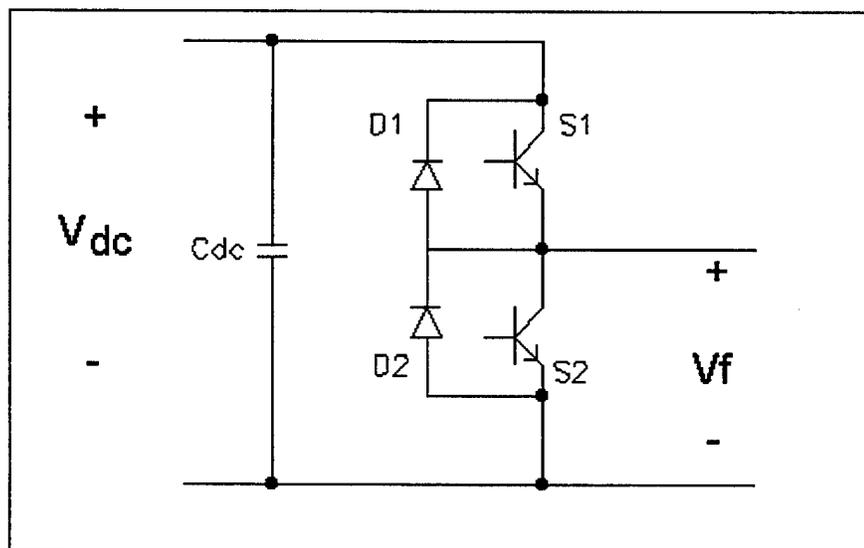


Figure 2-2 - Single-Phase Hard-Switched Converter

There are three basic cases for commutation in the ARCP inverter. In a steady-state switching state either the upper or lower switch (S1 or S2) will be closed at a given instant, and either the diode (D1 or D2) or the switch will be carrying the current (depending on the polarity of the load current). When it is desired to change states from the upper to the lower switch, the direction of current flow and hence the device in conduction must be determined. For example, if the output voltage, V_f is V_{DC} and the current flow is into the inverter, then diode D1 is conducting the load current.

The three commutation cases are explained in detail in the following sections. The first of the three cases occurs when either diode D1 or D2 is conducting. In this case commutation is accomplished using the auxiliary circuit to add additional energy into the circuit. Additional energy is required to overcome the losses in the circuit. For example, if no additional energy were added to the circuit during commutation from $V_f = 0$ to $V_f = V_{DC}$, the output voltage would never quite reach the upper rail voltage while resonating and the upper switch would have to be turned on with a non-zero voltage present. The second and third cases occur when either of the main switches are conducting. In the second case the magnitude of the current is below some threshold level, and the auxiliary circuit is used in commutation. This threshold level is chosen to limit the peak current seen in the main switches. The third case occurs when the magnitude of the current is above a threshold level. In this final case the auxiliary circuit is not used in commutation; the main switch is simply turned off and after the voltage swings to the opposite state the other main switch is gated on.

In summary, commutation from a diode always involves the auxiliary circuit and commutation from a switch does not always involve the auxiliary circuit.

B. CASE 1 - COMMUTATION FROM DIODE

The starting point for Case 1 is shown in Figure 2-3. Initially diode D2 is assumed to be conducting the full load current and the output voltage, V_f , is zero. Switch S2 remains gated on. A DC source voltage is continuously applied across the two capacitors, $2C_{dc}$. The mid-point of these capacitors is at a voltage $V_{DC}/2$. It is assumed that the commutation process occurs at a much faster rate than the fundamental of the output quantities is changing. Thus, it is reasonable to assume that the load current is effectively constant during the commutation interval.

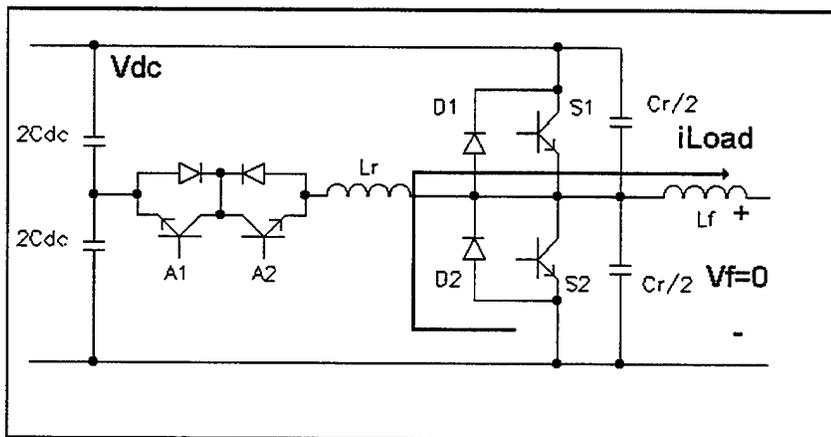


Figure 2-3 - Initial Condition, D2 Conducting S2 Gated On

To start the commutation process, switch A2 is gated on. With the voltage drop across conducting devices assumed to be zero, this introduces a forcing potential of $V_{DC}/2$ across the filter inductor L_r , as shown in Figure 2-4. The *ramp-up* phase begins as the auxiliary current, i_r , increases at a linear rate of $V_{DC}/(2L_r)$, dictated by the relationship

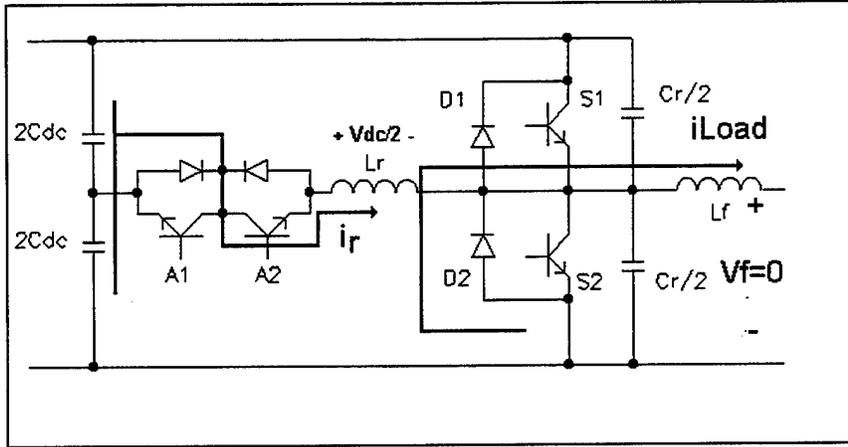


Figure 2-4 - Ramp-up A2 - Gated On

$V = L \frac{di}{dt}$. Switch S2 remains gated on and the auxiliary current begins to displace the load current flowing through D2.

When i_r exceeds i_{load} , assumed to be approximately constant throughout commutation, the *boost* phase, shown in Figure 2-5, begins. The amount of auxiliary current in excess of the load current flows through switch S2, and is defined as $i_{boost} = i_r - i_{load}$. This boost current adds energy of an amount equal to $\frac{L_r i_{boost}^2}{2}$ to the circuit. This additional energy is used to overcome the losses in the circuit during the resonant

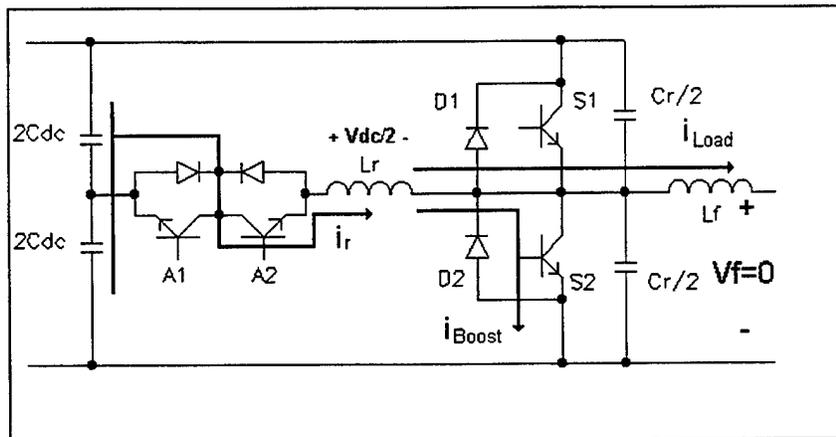


Figure 2-5 - Boost, i_r exceeds I_L and I_{boost} flows through S2

commutation phase. The boost current adds to the magnitude of the voltage resonance such that the overall magnitude is large enough to reach the upper rail voltage during commutation. Since i_{boost} is increasing at a linear rate, the boost phase can be controlled by a simple time delay. At this point, the auxiliary circuit is carrying the entire load current plus the boost current. Also of note in this boost interval is that the recovery current in D2 is in the direction of the boost current, and thus adds additional boost energy which assists in commutation.

When the required boost energy has been added (as specified by the control), S2 is gated off beginning the *resonant* commutation phase. The current in S2 at shut-off is diverted into the resonant capacitors, $C_r / 2$, as shown in Figure 2-6. Some switching losses will occur in switch S2 at turn-off but the resonant capacitors will act as snubbers to limit these losses. The auxiliary current and output voltage now resonate at a frequency determined by the values L_r and C_r . The auxiliary current will rise to a peak and then drop while the output voltage swings towards the upper rail voltage.

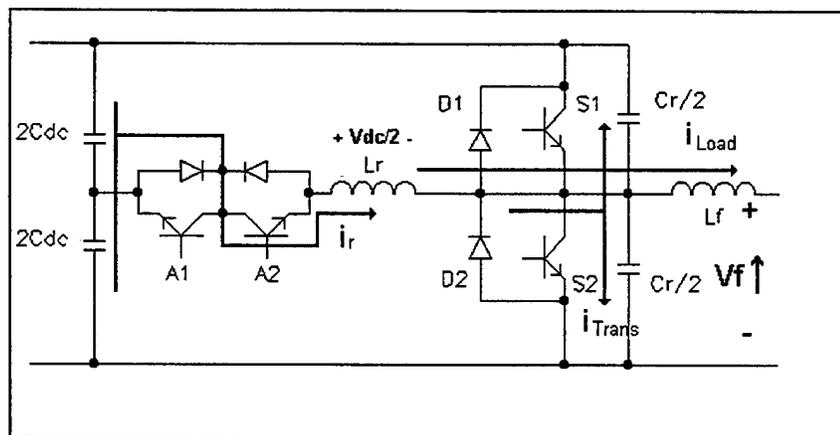


Figure 2-6 - Resonant, S2 Gated Off

In analyzing the resonant commutation interval, the load current can be considered constant, since $L_f \gg L_r$, and the front-end capacitors can be modeled as voltage sources with a value of $V_{DC}/2$, since $2C_{DC} \gg C_r/2$. Details of the analysis of the resonant phase are provided in Appendix A. Assuming ideal circuit elements, the maximum current in the auxiliary circuit can be approximated by:

$$i_{r,max} = i_L + i_{boost} + \frac{V_{dc}}{2} \sqrt{\frac{C_r}{L_r}} \quad (\text{Eq. 2-1})$$

This value is used to size the auxiliary branch devices.

When the output voltage becomes equal to the DC input voltage, zero voltage exists across S1. At this point S1 is gated on with no switching losses, clamping the output voltage at the high state (Figure 2-7).

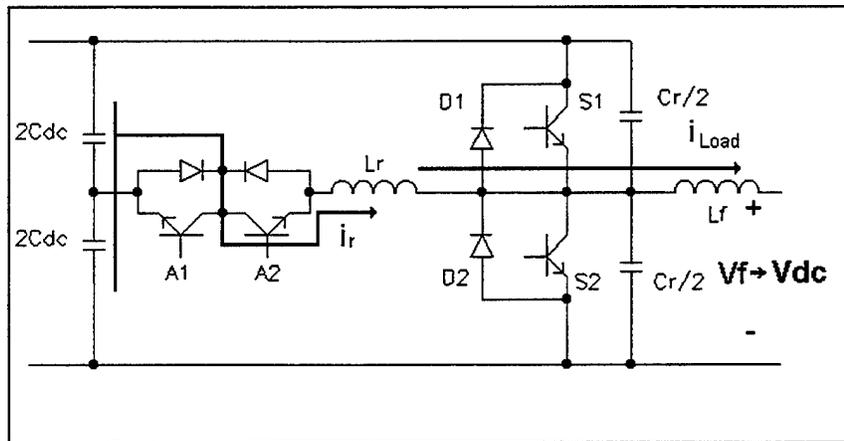


Figure 2-7 - Clamp, S1 Gated On

When S1 is closed in order to clamp the output voltage at the upper rail, a forcing potential of $V_{DC}/2$ is locked across the resonant inductor L_r as shown in Figure 2-8. This causes the auxiliary current to drop off linearly at a rate of $\frac{-V_{DC}}{2L_r}$. As the auxiliary current drops off, load current shifts to switch S1.

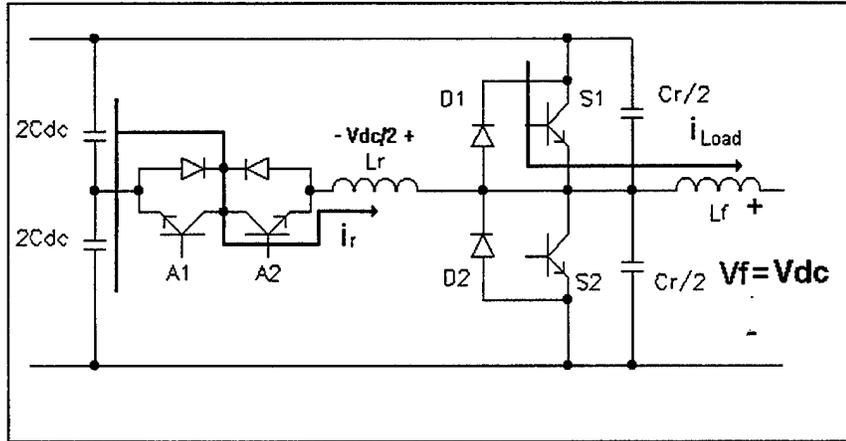


Figure 2-8 - Ramp-Down, S1 Picks-up Load, Auxiliary Current Falls Off

As auxiliary current falls to zero, A2 is gated off with no current flowing through it; therefore, there are no switching-off losses. In actuality A2 will be gated off in anticipation of the current crossing zero so that the crossover point can be accurately predicted. The diode shunting A1 will stop the current from resonating back negative, but some losses will occur if the diode blocks the current due to reverse recovery losses. A snubber is normally added across the auxiliary devices to eliminate the possibility of damaging the switches due to a small timing error.

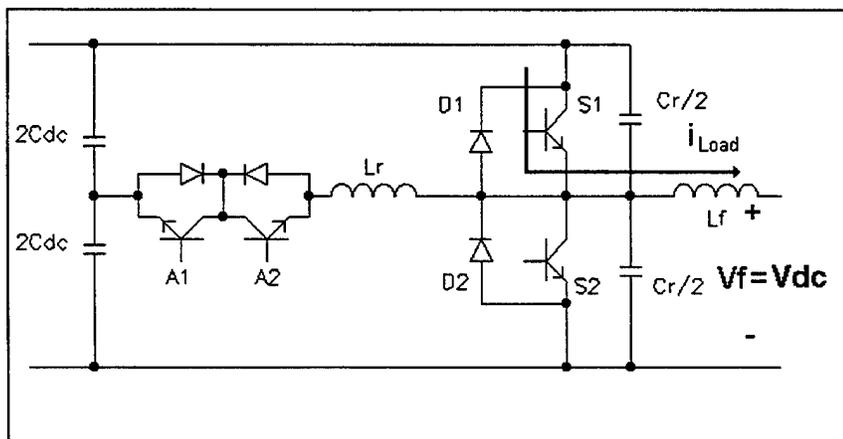


Figure 2-9 - Completion, A2 Gated Off

Figure 2-10 shows the output voltage and auxiliary circuit current for Case 1 commutation. Initially the auxiliary current is zero, the output voltage is zero and diode D2 is conducting the load current. The devices in conduction are indicated below the

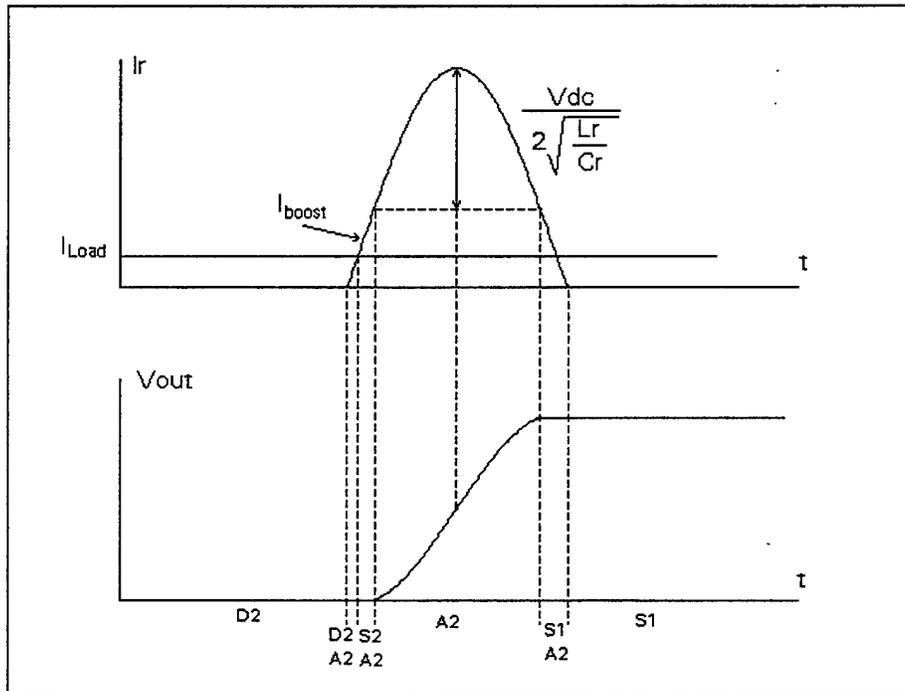


Figure 2-10 - Case One Waveforms, Vout and Ir

voltage graph in Figure 2-10. When the auxiliary device A2 is switched on, the *ramp-up* phase begins and the auxiliary current begins to rise, and both D2 and A2 are conducting. As the auxiliary current increases above the level of the load current, diode D2 stops conducting and current begins flowing through the lower main switch S2, initiating the *boost* phase of commutation. After the boost current reaches the desired level S2 is switched off commencing the *resonant* phase. Throughout the resonant phase auxiliary switch A2 is conducting the entire load current in conjunction with the auxiliary current. The output voltage swings high and the auxiliary current peaks and begins to swing low.

When the output voltage reaches the DC voltage the upper main switch (S1) is gated on. In the diagram this occurs just as the auxiliary circuit current drops to the boost plus load current level. In an actual circuit the voltage would not reach this level until slightly after the auxiliary current passed below the boost plus auxiliary current level due to losses. Figure 2-10 is generated assuming no losses. Once S1 is gated on the auxiliary current drops off at a linear rate. When the auxiliary current drops below the level of the load current, S1 begins to conduct. As the auxiliary current drops to zero, A2 is gated off completing the commutation.

C. CASE 2 - SWITCH CONDUCTING, CURRENT BELOW THRESHOLD

Commutation for Case 2 is similar to Case 1 except that there are no ramp-up or ramp-down phases involved.

Initially switch S1 is assumed to be conducting the full load current, and the output voltage is equal to V_{DC} , as illustrated in Figure 2-11.

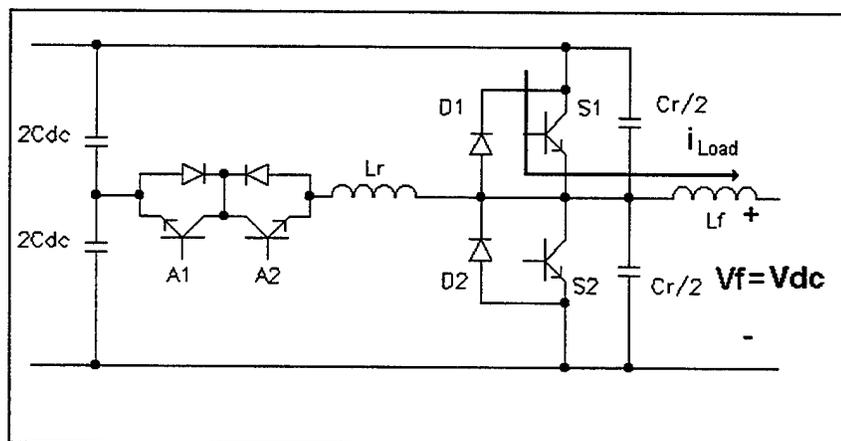


Figure 2-11 - Initial Condition, S1 Conducting

Switch A1 is gated on to start the commutation process. This introduces a forcing potential of $V_{DC}/2$ across the filter inductor L_f . The current flow through the auxiliary

circuit is in a direction to increase the current flow through S1 as shown in Figure 2-12.

Thus no ramp-up phase is needed as the auxiliary current immediately initiates a boost of the load current.

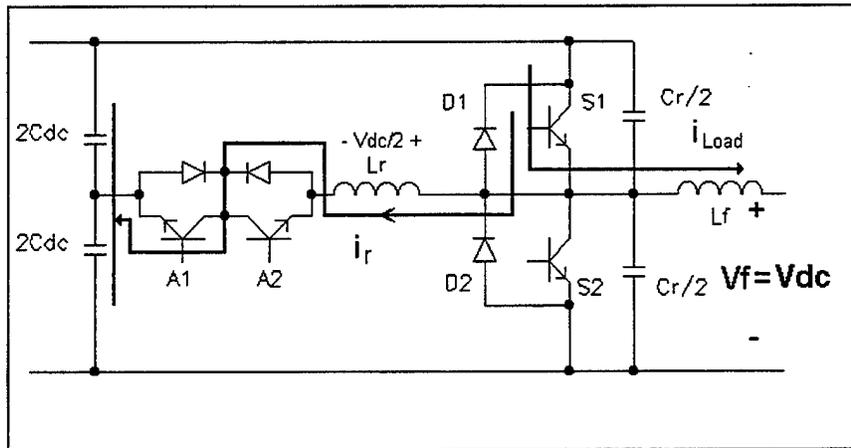


Figure 2-12 - Boost, I_r Flows through S1

When the boost current reaches the desired level, the *resonant* commutation phase is started by switching S1 off. The output voltage begins to fall while the current through S1 is diverted to the resonant capacitors. This action is depicted in Figure 2-13. Ideally, the auxiliary current consists of a half-sinusoid superimposed upon the boost current level, and the output voltage falls as the sum of cosine and ramp waveforms.

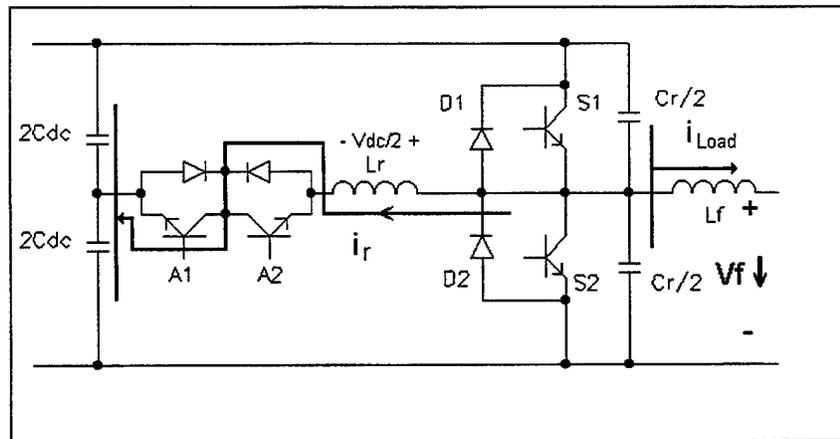


Figure 2-13 - Resonant, S1 Gated Off

As the output voltage continues to fall it will attempt to drop below zero. At this point diode D2 becomes forward biased and begins to pick up load current. Switch S2 is turned on at this point to clamp the voltage to zero. Energy remaining in the resonant inductor is returned to the DC bus capacitors as the potential across the inductor is now of opposite polarity as at the initiation of the *resonant* phase.

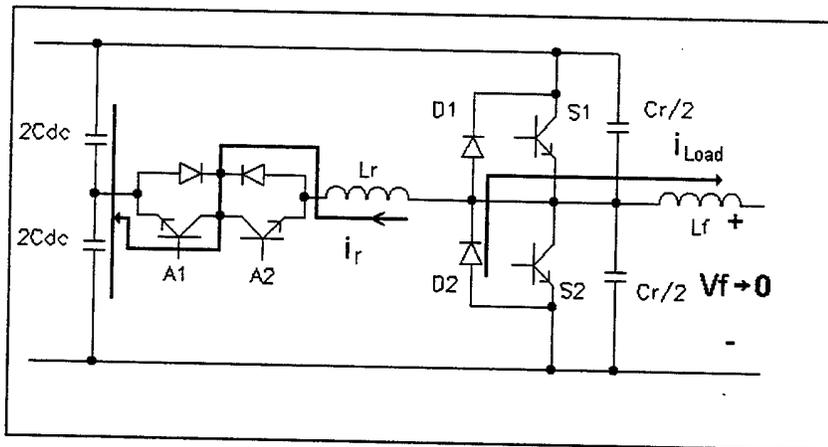


Figure 2-14 - Clamp, S2 Gated On

When the auxiliary current falls to zero A1 is gated off. Diode D2 is now conducting all of the load current and commutation is complete.

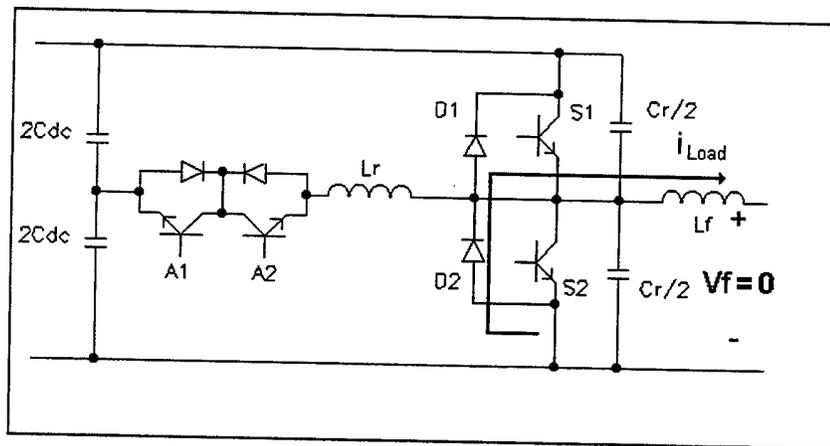


Figure 2-15 - Completion, A1 Gated Off

Figure 2-16 illustrates the output voltage and auxiliary current waveforms for Case 2 commutation. Initially the output voltage is high, auxiliary current is zero and the upper main switch S1 is conducting all of the load current. Auxiliary switch A1 is gated on to start the commutation process; this immediately initiates the *boost* phase. The

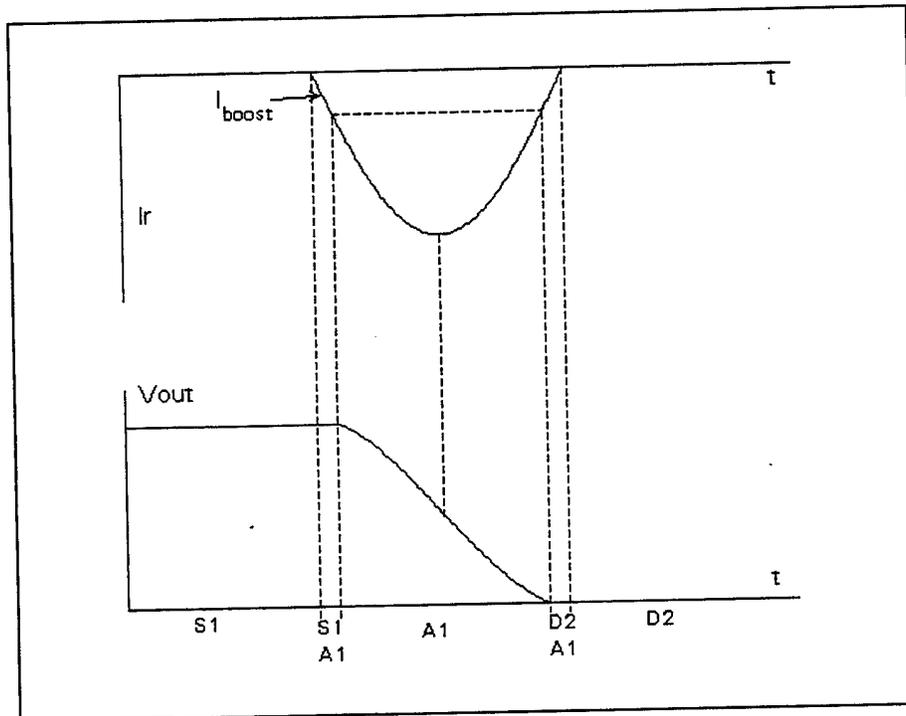


Figure 2-16 - Case Two Waveforms, V_{out} and I_r

boost current increases to a specified level, then the upper main switch S1 is gated off initiating the *resonant* phase. The output voltage swings low and the auxiliary current peaks in magnitude and begins to decrease. When the output voltage reaches zero, diode D2 begins conducting and S2 is gated on with a zero voltage differential. When the auxiliary current drops to zero, A1 is gated off completing the commutation. It can be noted that in Figure 2-16 the output voltage reaches zero just as the auxiliary current

drops to the boost level. If losses are considered, the time at which the output voltage reaches zero would be shifted past this point.

D. CASE 3 - SWITCH CONDUCTING, CURRENT ABOVE THRESHOLD

When the load current exceeds a pre-defined threshold level, the auxiliary circuit is not used when commutating from a conducting switch. To determine the threshold current level, the maximum commutation time, T_{max} , (i.e. the time required for a Case 1 commutation at full-load current) must first be computed. It is desired to maintain the Case 3 commutation time less than or equal to the maximum commutation time for Case 1. In Case 3 the change in output voltage is governed by Equation 2-2.

$$\frac{dV_{out}}{dt} = \frac{I_{Load}}{C_r} \quad (\text{Eq. 2-2})$$

The larger the load current, the faster the output voltage will change; therefore, a small output current will cause commutation to take longer. To determine the smallest current at which the Case 3 commutation time will be less than or equal to T_{max} , Equation 2-2 is used with $dV_{out} = V_{DC}$ and $dt = T_{max}$. This current, defined as the threshold current, takes on the following value

$$I_{th} = \frac{C_r V_{DC}}{T_{max}} \quad (\text{Eq. 2-3})$$

In component selection the threshold current should be selected to be sufficiently below the peak load current. Thus, $I_{th} + I_{boost} \leq I_{load-peak}$. If this criteria is met, then the primary switches do not have to turn off any higher current than if a hard-switched converter were used.

Case 3 commutation is described as follows. Initially switch S1 is assumed to be conducting the full load current, and the output voltage is equal to V_{DC} . This is the same initial condition as given for Case 2.

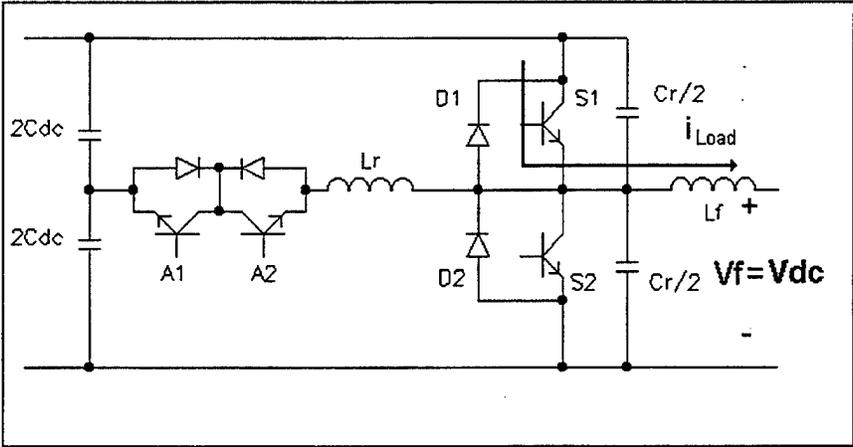


Figure 2-17 - Initial Condition, S1 Conducting

Switch S1 is gated off to begin commutation. This causes the load current to be shunted into the two resonant capacitors as shown in Figure 2-18. The output voltage falls at a rate proportional to the output current following the relationship $i = C \frac{dV}{dt}$.

When the output current attempts to fall below zero, diode D2 becomes forward biased

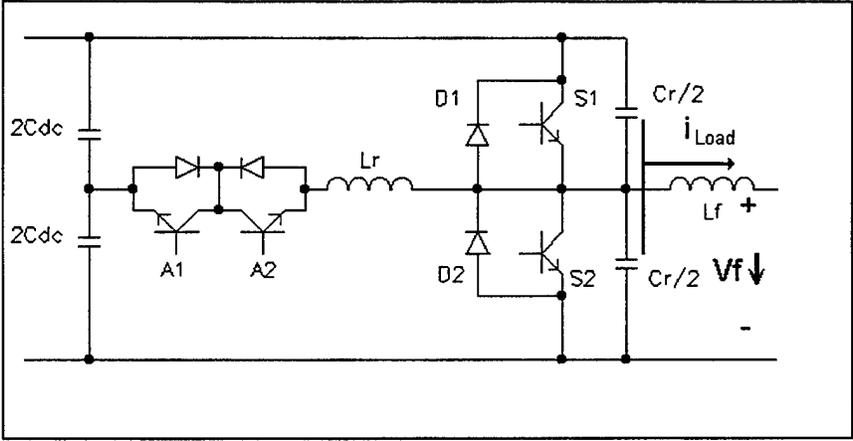


Figure 2-18 - Commutation, S1 Gated Off

and picks up the load current. Switch S2 is gated on at this point, with no losses, completing the commutation.

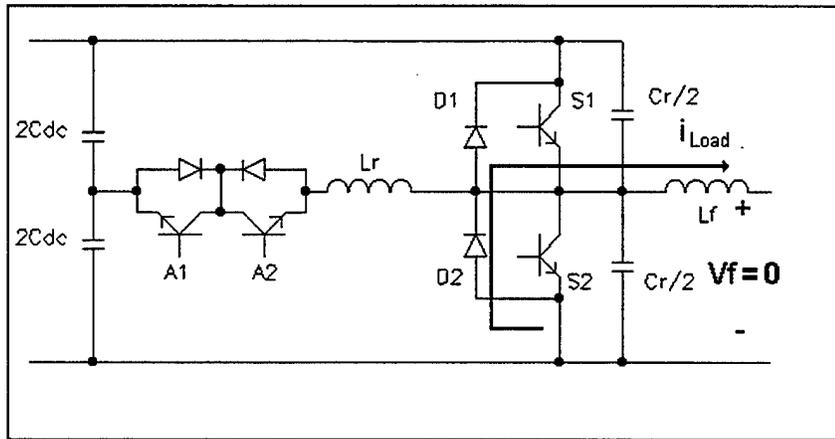


Figure 2-19 - Completion, D2 Begins Conducting, S2 Gated On

Figure 2-20 illustrates the output voltage and auxiliary current waveforms for Case 3 commutation. Initially the output voltage is high, auxiliary current is zero and the upper main switch S1 is conducting all of the load current. S1 is gated off, dumping the

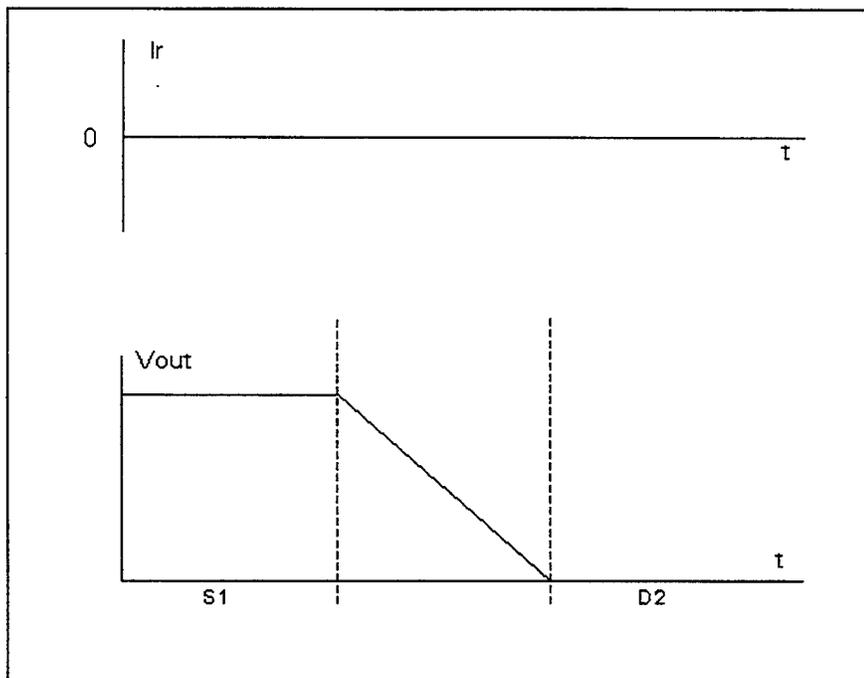


Figure 2-20 - Case Three Waveforms, Vout and Ir

load current into the resonant capacitors. The output voltage falls linearly following the constitutive capacitor relationship $i_{load} = C_r \frac{dV_{out}}{dt}$. Once the voltage falls to zero, diode D2 begins conducting and S2 is gated on, completing the commutation.

E. THREE-PHASE APPLICATIONS

To integrate the ARCP into a three-phase power system is a relatively simple task of connecting three single-phase ARCP units into a correct configuration. A common DC voltage bus is used for all three units and the AC sides are connected in the desired configuration, either Y or Δ . A Y-connected configuration is shown in Figure 2-21.

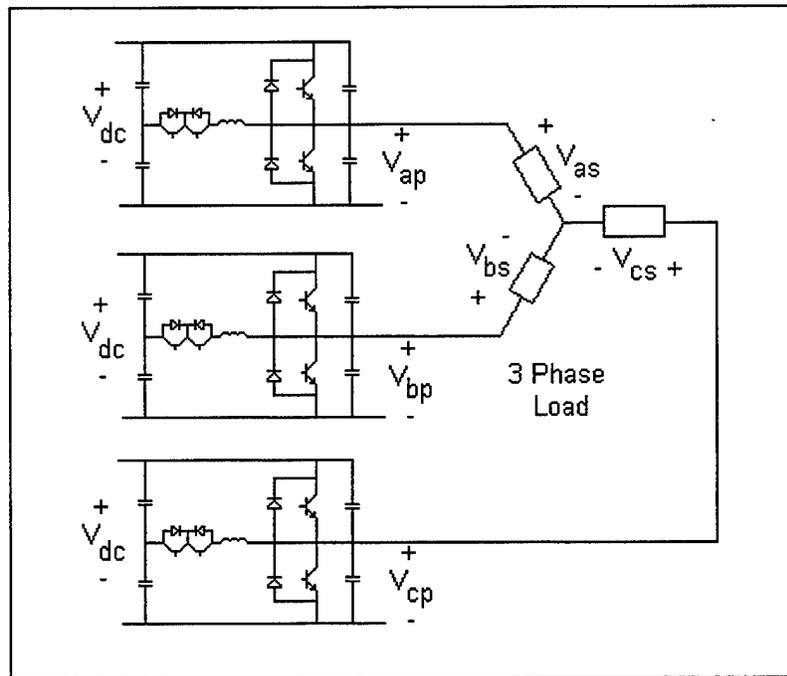


Figure 2-21 - Three-Phase ARCP, Y-Connected Load

One consequence of the above configuration is that the neutral point of the Y-connected load will be at the same potential as the average DC input voltage. To avoid an offset at the neutral point the DC voltage can be made bi-polar with the positive and

negative voltages of equal value, thus the average value will be zero. This problem is avoided in a Δ -configuration since no neutral point exists.

Power flow can be in either direction, DC to AC or AC to DC. No additional modifications are necessary in the ARCP to accommodate the bi-directional power flow. However, the load and source must be capable of sourcing and sinking power.

III. SIMULATION

This chapter documents the approach and issues related to the simulation of a number of structures considered in this work. Initially a digital-based simulation of a single-phase hard-switched inverter is developed with sine-triangle voltage control. Next, the details required to model a single-phase ARCP converter with sine-triangle control are examined. Finally the simulations of the three-phase versions of both the hard-switched and ARCP converters are obtained. Comparison of the converters using total harmonic distortion calculations shows that the hard-switched inverter can be used as a practical reduced-order model of the ARCP. This facilitates faster simulation of controllers and the convenient investigation of system load transients. In addition, the effect of a minimum switching time on high-frequency modulation will be explored.

A. SIMULATION LANGUAGE

Simulations described in this chapter are performed using the Advanced Continuous Simulation Language (ACSL). ACSL, pronounced 'axle', is a Fortran based language which uses a free format which is not as restrictive as Fortran. Programs are compiled after being translated into Fortran by the ACSL translator. Once compiled, the program is linked with the ACSL run-time library to allow user interface.

Models are constructed from state space descriptions of systems. Discrete-event blocks and if-then-else constructs are used to switch from one set of equations to another. The general construction of a program is shown in Figure 3-1 [Ref. 7]. The derivative

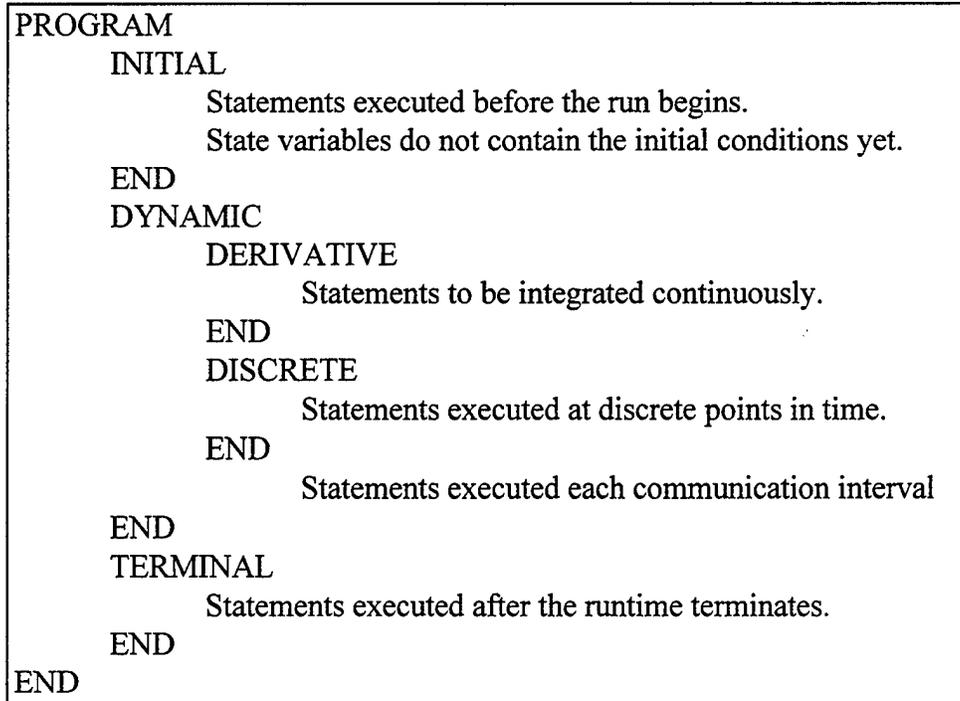


Figure 3-1 - ACSL Program Outline (from [Ref. 7])

section is sorted so that as long as the inputs and outputs of various subsystems are compatible, no specific sequential ordering of statements is required by the programmer.

The ACSL language was selected over SIMULINK for several reasons. First, ACSL programs are compiled so they run faster. ACSL also handles switching-type networks far more easily and provides more options for solving algebraic loops. Overall the major advantage over SIMULINK is the speed at which ACSL provides in the simulation of complex systems.

B. SINGLE-PHASE HARD-SWITCHED CONVERTER

In simulation it is assumed that the hard-switched inverter can change states instantaneously. As soon as one switch is opened, the other is closed with no delay. In

practice some delay must be introduced, as switches do not turn off instantly, to avoid both switches being shut simultaneously causing a short across the source.

A sine-triangle method of modulation was used to generate the control signal [Ref. 8]. A control sinusoid at the desired output frequency is generated and superimposed on a high-frequency triangle wave. The two waves are compared and when the sinusoid is greater than the triangle wave, a control signal to switch the particular leg of the inverter to the high state is generated. When the control sinusoid is less than the triangle wave, a control signal for the low state is generated. Figure 3-2 shows graphically how sine-triangle modulation generates an output voltage scheme.

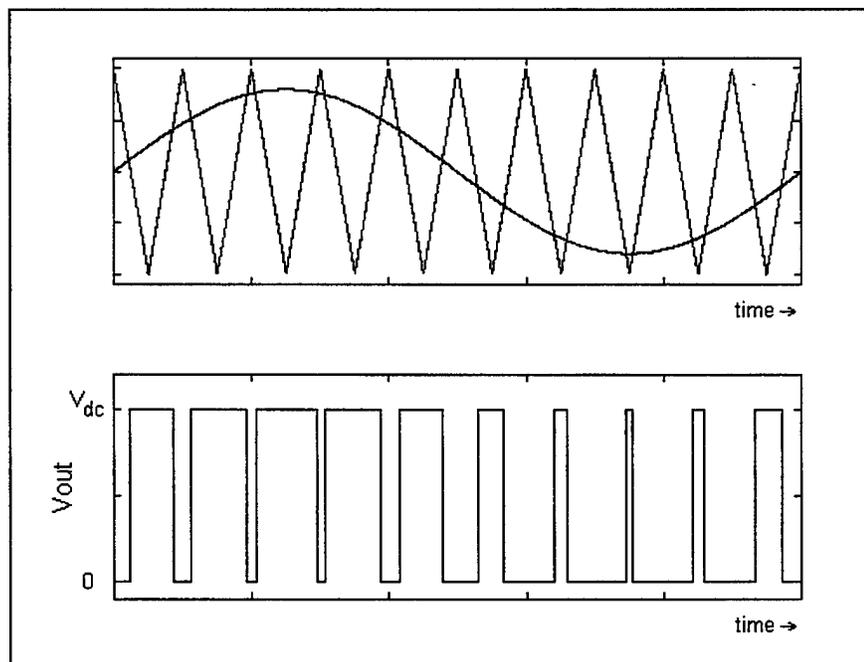


Figure 3-2 - Sine-Triangle Modulation

The output voltage waveform is a square wave which contains many harmonic components. To reduce the lower-order harmonics the frequency of the triangle wave is increased in relation to the frequency of the control sinusoid. In the simulations

considered, the frequency of the control sinusoid is 60 Hz while the frequency of the triangle wave is 6 kHz.

Appendix B (pp 127-128) lists the ACSL code for the single-phase hard-switched converter. A resistor with an LC filter is the assumed load.

C. SINGLE-PHASE ARCP CONVERTER

The first step in simulating the ARCP was to generate a control signal for switching. As in the hard-switched converter, sine-triangle modulation was considered.

Establishing the switching states for the ARCP is much more complicated than in the hard-switched converter. How the ARCP changes states is described in detail in Chapter II. To simplify modeling the switching dynamics six situations encompassing all possible ways of changing states were identified. Three situations involved a positive load current, and three a negative load current. Each situation corresponds to a commutation sequence described in Chapter II. Table 3-1 shows all the possible commutation states for the ARCP. Figure 3-3 illustrates the decision cycle that must be implemented in the ACSL code. The load current sign and magnitude, as well as the initial output voltage, are the quantities which dictate the commutation case.

Table 3-1 - ARCP Commutation Possibilities

State #	Type of Commutation	Voltage Transition	Load Current	Above/Below Thres Current
1	Case 1	Lo to Hi	Pos	N/A
2	Case 2	Hi to Lo	Pos	Below
3	Case 3	Hi to Lo	Pos	Above
4	Case 2	Lo to Hi	Neg	Below
5	Case 1	Hi to Lo	Neg	N/A
6	Case 3	Lo to Hi	Neg	Above

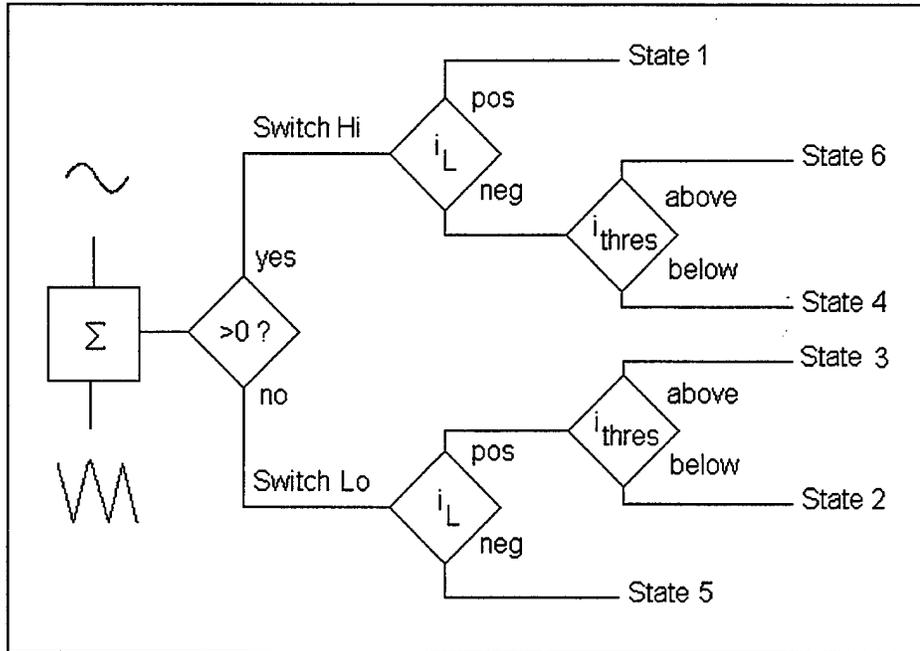


Figure 3-3 - Flowchart for ARCP Commutation

Once the commutation state has been determined, the equations governing the circuit behavior must be found. In Chapter II the Laplace transform solution for the resonant portion of commutation was established. For ease of programming, the Laplace transform solution is not used. Instead, a state space representation is used. State variables of interest are the auxiliary circuit current (i_r), the load current (i_L), the output voltage (V_f), and the load voltage (V_{Load}). The appropriate state space representation depends on the status of both the main and auxiliary switches. These changes are controlled by conditional IF statements in the program. The derivatives of the auxiliary current and output voltage for various switch status combinations are shown in Table 3-2.

Table 3-2 - State Variable Equation vs Switch Positions

A1	off	off	off	off	off	on	on	on	off
A2	off	on	on	on	off	off	off	off	off
S1	off	off	off	on	on	on	off	off	off
S2	on	on	off	off	off	off	off	on	off
$\frac{di_r}{dt}$	0	$\frac{V_{dc} - 2V_f}{2L_r}$	$\frac{V_{dc} - 2V_f}{2L_r}$	$\frac{V_{dc} - 2V_f}{2L_r}$	0	$\frac{V_{dc} - 2V_f}{2L_r}$	$\frac{V_{dc} - 2V_f}{2L_r}$	$\frac{V_{dc} - 2V_f}{2L_r}$	0
$\frac{dV_f}{dt}$	0	0	$\frac{i_r - i_L}{C_r}$	0	0	0	$\frac{i_r - i_L}{C_r}$	0	$\frac{-i_L}{C_r}$

The derivatives of load current and load voltage are independent of the switch status and are given by:

$$\frac{di_L}{dt} = \frac{V_f - V_{Load}}{L_f} \quad (\text{Eq. 3-1})$$

$$\frac{dV_{Load}}{dt} = \frac{i_L - \frac{V_{Load}}{R_{Load}}}{C_f} \quad (\text{Eq. 3-2})$$

Appendix B (pp 129-133) contains the ACSL code for the single-phase ARCP.

D. THREE-PHASE SIMULATIONS

Expansion to three-phase simulation involved combining three separate single-phase inverters and their control signals. Load dynamics were simulated in the stationary reference frame. The control signals consisted of three sinusoids of equal amplitude, phase displaced by 120 degrees. This resulted in a standard three-phase output waveform. Code for the three-phase hard-switched and ARCP converters is listed in Appendix B (pp134 - 148).

E. COMPARISON OF HARD-SWITCHED AND ARCP CONVERTERS USING TOTAL HARMONIC DISTORTION

It should be noted that less simulation code is required for implementing the hard-switched converter as compared to the ARCP. This is due to the ARCP simulation modeling each commutation in detail, while the hard-switched converter simulation takes a simplified view of commutation. Due to this fact the hard-switched simulation runs much faster than the ARCP program. For an integration time step of $0.1\mu\text{sec}$ the ARCP simulation required 133.8 seconds to complete a .032 second real-time simulation on a SPARC 10 workstation. The hard-switched simulation took 63.4 seconds to run an identically structured simulation. Since the hard-switched inverter does not need to model the commutations in detail, the integration step can be changed to a larger value without loss of accuracy. This reduces the run time even further. Given an integration time step of $1\mu\text{sec}$ the same hard-switched simulation run took only 6.6 seconds. For this reason, it is desirable to substitute the hard-switched model for the ARCP when evaluating new control schemes or loads. To verify that this type of substitution is valid a comparison of output waveforms for both converters was undertaken.

To compare the two models the total harmonic distortion (THD) of each model's output voltage was evaluated. Total harmonic distortion is defined as the square root of the sum of the squares of the harmonic components divided by the square of the fundamental, or in equation form:

$$THD\% = 100 \times \sqrt{\frac{V_{s2}^2 + V_{s3}^2 + V_{s4}^2 + \dots}{V_{s1}^2}} = 100 \times \sqrt{\sum_{h \neq 1} \left(\frac{V_{sh}}{V_{s1}}\right)^2} \quad (\text{Eq. 3-3})$$

The method used to calculate THD is described in detail in Appendix C [Ref. 9].

A simulation was run at a switching frequency of 6 kHz to compare the models, harmonic components up to seventh-order were used in calculating THD. Results showed the THD for the hard-switched converter was 0.8537% and for the ARCP was 0.1745%. These are on the same order of magnitude as expected. Total harmonic distortion for the ARCP was lower than for the hard-switched converter. This also was expected since the waveforms for the ARCP were less sharp at the transitions from high to low than for the hard-switched converter which had square transitions and thus more harmonics. For this reason using the hard-switched inverter in simulations will give a conservative result with respect to the amount of distortion created.

F. MINIMUM SWITCHING TIME

Pulse-width-modulation (PWM) schemes such as sine-triangle modulation can require very high-frequency switching. For instance, in sine-triangle modulation with a duty cycle of 95% the highest frequency component will be 20 times the fundamental. At higher switch frequencies this can become a problem because there is a minimum time required for the ARCP to switch states which may be longer than the switching time commanded by the PWM technique. Minimum switching time is commonly referred to as dead time. For the ARCP dead time is on the order of one over the resonant frequency. Hard-switched converters typically have a short dead time also, to allow the switches to completely turn off.

Dead time causes additional distortion in output waveforms. To check the amount of distortion, a simulation using a hard-switched converter with dead time was

implemented. The results in Table 3-3 show a dramatic increase in THD when dead time is incorporated.

Table 3-3 - Simulation Parameters

Dead Time	25 μ sec
Switching Frequency	6 kHz
Maximum Duty Cycle	95%
Method of PWM	sine-triangle
Minimum Switching Time from PWM	8.3 μ sec
Voltage THD - with dead time	1.010%
Voltage THD - w/o dead time	0.039%
Current THD - with dead time	3.584%
Current THD - w/o dead time	0.080%

In an ARCP the dead time can be approximated by Equation 3-4 [Ref. 6].

$$T_{Dead} = 2L_r \frac{(2I_{Load-max} + I_{Boost})}{V_{DC}} + \pi\sqrt{L_r C_r} \quad (\text{Eq. 3-4})$$

Using the values from Table 3-4, a dead time value of 3.44 μ sec is calculated.

Table 3-4 - ARCP Parameters

Resonant Inductance L_r	2.9 μ H
Resonant Capacitance C_r	0.3 μ F
Maximum Load Current	20 Amps
Boost Current	4 Amps

So for a maximum duty cycle of 95 % the highest frequency triangle wave which can be used in sine-triangle modulation is 29 kHz. If the dead time is assumed to be 5 μ sec for a non-ideal ARCP, the highest triangle wave frequency to be used without dead-time distortion is 20 kHz. Although the numbers used in the dead time simulation vary from those of the ARCP, the simulation provides insight to the analyst into the amount of distortion which dead time can introduce.

Using the simulation tools presented here for circuit simulation, the issue of control can be addressed. Various control algorithms can be simulated and joined with the circuit simulations to predict system behavior. The following chapter addresses the control issue in this manner.

IV. CONTROLLERS

Open-loop control of converters can produce satisfactory output waveforms; however, using some type of feedback generally improves the quality of the output response. Feedback helps make the system response less sensitive to parameter variations and exogenous disturbances. In addition, feedback is introduced to improve the transient and steady-state response or make reference signal tracking automatic. To control the output of a three-phase converter, three separate control schemes are proposed. The first uses voltage feedback to control the load voltage, the second uses current feedback to control the load current, and the last uses a combination of current and voltage feedback to control the load voltage. Reference frame theory is used in the control algorithms, and the advantages of implementation in different reference frames are discussed.

A. VOLTAGE FEEDBACK CONTROLLER

A voltage controller, controlling in the stationary reference frame, is presented and analyzed in this section. The controller compares the actual output voltage to the desired voltage, generates an error and passes this error in parallel through proportional and integral amplifiers to generate a control signal. This control signal is used to derive the gating signals for the switches in the converter.

For the purpose of simulation a circuit shown in Figure 4-1, consisting of a three-phase converter driving a resistive load attached to an LC filter, was considered. The

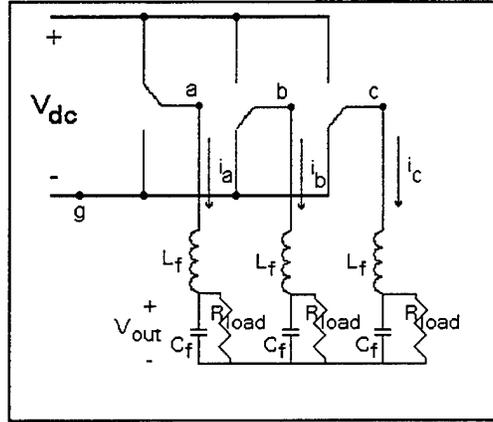


Figure 4-1 - Converter with LRC Load

purpose of the controller is to regulate the voltage across the filter capacitor and load resistor, V_{out} . Possible extensions to machine loads will be apparent.

To begin analysis of the circuit the three phase voltages of the converter are transformed into an equivalent wye-connected source as shown in Figure 4-2. For a balanced load condition, the phase voltages are determined according to the following relationships:

$$V_{as} = \frac{2}{3}V_{ag} - \frac{1}{3}(V_{bg} + V_{cg}) \quad (\text{Eq. 4-1})$$

$$V_{bs} = \frac{2}{3}V_{bg} - \frac{1}{3}(V_{ag} + V_{cg}) \quad (\text{Eq. 4-2})$$

$$V_{cs} = \frac{2}{3}V_{cg} - \frac{1}{3}(V_{ag} + V_{bg}) \quad (\text{Eq. 4-3})$$

where V_{a-b-cs} represents a set of wye-connected phase voltages and V_{a-b-cg} represents phase-to-ground voltages at the converter output. The voltages V_{a-b-cg} are known once the switch status of the inverter is specified. Wye-connected quantities are used in the remainder of the analysis.

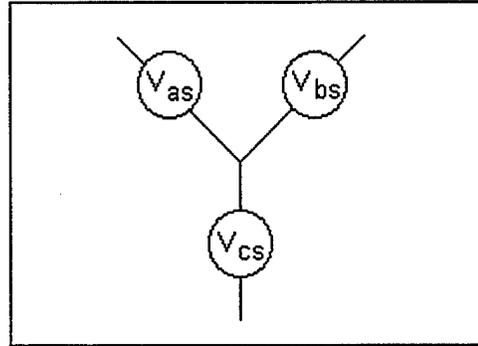


Figure 4-2 - Equivalent Wye-Connected Source

Equations for the circuit are next established for use in the simulation. The state variables include the inductor current and the capacitor voltage. Assuming balanced conditions the center of the wye-connected source and the common point of the resistive load have the same potential. Writing an equation from one common point to the other across phase A gives:

$$V_{as} - L_f \frac{di_a}{dt} - V_{Load-a} = 0 \quad (\text{Eq. 4-4})$$

where i_a is the current flowing through the inductor L_f . Solving for the derivative of the inductor current yields:

$$\frac{di_a}{dt} = \frac{V_{as} - V_{Load-a}}{L_f} \quad (\text{Eq. 4-5}).$$

Summing currents at the common node between the inductor, capacitor and load resistor produces the following equation:

$$i_a - \frac{V_{Load-a}}{R_{Load}} - C_f \frac{dV_{Load-a}}{dt} = 0 \quad (\text{Eq. 4-6}).$$

Solving for the derivative of capacitor voltage gives

$$\frac{dV_{Load-a}}{dt} = \frac{i_a - \frac{V_{Load-a}}{R_{Load}}}{C_f} \quad (\text{Eq. 4-7}).$$

Equations for phases B and C give similar results with the subscript 'a' replaced by 'b' or 'c' as appropriate.

Next the state equations were transformed into the stationary q-d-0 reference frame using the arbitrary reference frame transformation matrix [Ref. 10]

$$\mathbf{K}_s = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (\text{Eq. 4-8})$$

where

$$\theta = \int_0^t \omega dt + \theta_0 \quad (\text{Eq. 4-9})$$

For the stationary reference frame, ω is set to zero and θ_0 is selected to also equal zero for convenience. The transformation matrix then becomes

$$\mathbf{K}_s^s = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (\text{Eq. 4-10}).$$

where the 's' superscript denotes the stationary reference frame.

With balanced conditions the zero-sequence variables must be zero, so they are not considered in the controller analysis. Zero-sequence variables may be used to check

for balanced operation, but for the simulation it is assumed that balanced conditions are maintained.

The transformed state equations, written in vector form, become

$$\frac{d\mathbf{i}_{qd0}^s}{dt} = \frac{\mathbf{V}_{qd0s}^s - \mathbf{V}_{qd0Load}^s}{L_f} \quad (\text{Eq. 4-11}),$$

$$\frac{d\mathbf{V}_{qd0Load}^s}{dt} = \frac{\mathbf{i}_{qd0}^s - \frac{\mathbf{V}_{qd0Load}^s}{R_{Load}}}{C_f} \quad (\text{Eq. 4-12}).$$

A balanced three-phase set of desired voltages is generated and transformed into the stationary reference frame to give the desired q-d-0 voltages.

$$\begin{bmatrix} V_{q-Load}^{s*} \\ V_{d-Load}^{s*} \\ V_{0-Load}^{s*} \end{bmatrix} = \mathbf{K}_s^s \begin{bmatrix} V_{a-Load}^* \\ V_{b-Load}^* \\ V_{c-Load}^* \end{bmatrix} \quad (\text{Eq. 4-13})$$

Again with balanced conditions the zero-sequence voltage will be zero, so it is ignored. Desired q-d voltages are compared with actual q-d voltages to provide error signals, one error signal for the q-quantities and one for the d-quantities. These error signals are next sent through proportional-integral controllers which produce control signals in the q-d frame. The control signals are transformed back into the a-b-c frame to give a commanded control signal to each leg of the converter. Based on beating these control signals up against a high-frequency carrier triangle waveform, the devices in each leg of the inverter are switched to give the required output voltage at the inverter terminals. This voltage drives the load to give the desired voltage across the resistors and capacitors. Signal flow for the controller is illustrated in Figure 4-3. The gain K

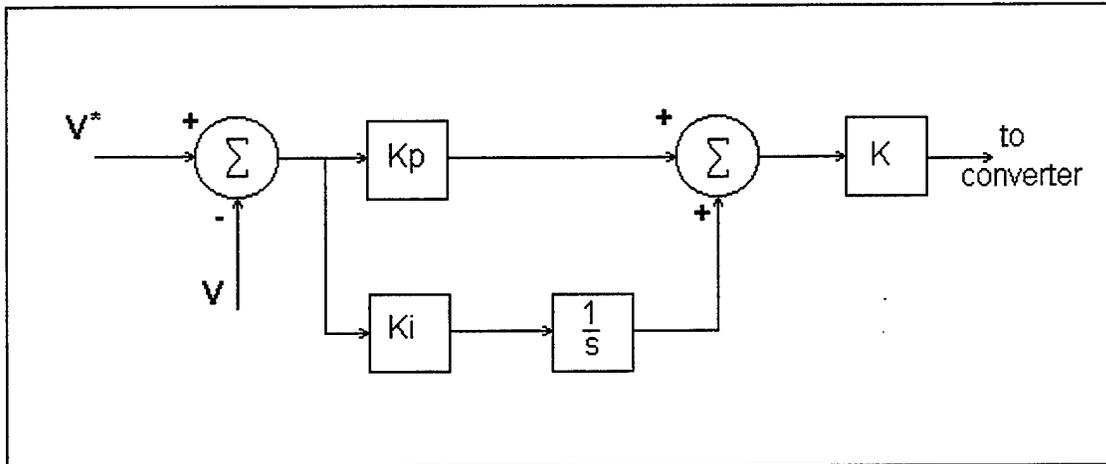


Figure 4-3 - Per-Phase Signal Flow of PI Controller

represents the gain inherent to the sine-triangle PWM process. This gain is a constant in the linear region of operation and decreases in a non-linear fashion in the overmodulation region.

To select gains for the controller the transfer function for the system must be derived. Two methods can be used to find the transfer function, either drawing the block diagram and using Mason's gain formula or by using state space methods. Both methods are considered.

First the classical approach of drawing the block diagram is shown. This is a useful method in visualizing the signal flow of the system. The flow diagram is shown in Figure 4-4. It is assumed that the converter will have a unity gain; that is, the control signal into the converter times the converter gain is the voltage which is given at the output. This simplification ignores nonlinear effects and the impact of harmonics; however, it is mathematically valid as long as the converter is operated in the linear range, with a modulation index of less than one.

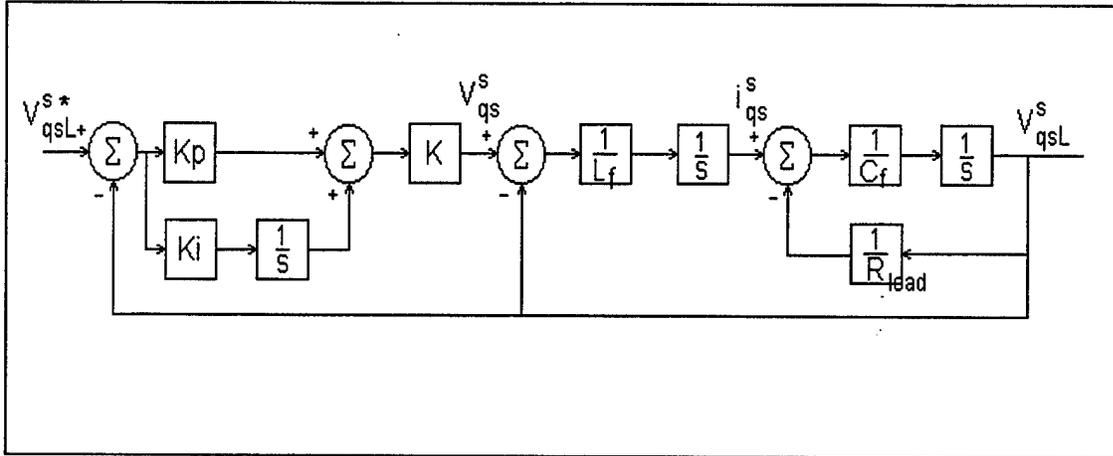


Figure 4-4 - Signal Flow Diagram, q-Quantities Only

In the following discussion only the q-quantities are considered since the q- and d-quantities are independent. Derivation of the d-quantity controller mirror those shown here for the q-quantities.

Mason's rule states that the input-output transfer function associated with the signal-flow graph of Figure 4-4 is given by, [Ref. 11]

$$G(s) = \frac{V_{qsL}^s(s)}{V_{qsL}^{s*}(s)} = \frac{\text{Forward Path Gain}}{1 - \sum \text{Individual Loop Gains}} \quad (\text{Eq. 4-14}).$$

Inserting values and solving, the gain or closed-loop transfer function is given by

$$\frac{V_{qsL}^s(s)}{V_{qsL}^{s*}(s)} = \frac{\left(K_p + \frac{K_i}{s}\right) K \frac{1}{L_f} \frac{1}{s} \frac{1}{C_f} \frac{1}{s}}{1 + \left(K_p + \frac{K_i}{s}\right) K \frac{1}{L_f} \frac{1}{s} \frac{1}{C_f} \frac{1}{s} + \frac{1}{L_f} \frac{1}{s} \frac{1}{C_f} \frac{1}{s} + \frac{1}{s} \frac{1}{C_f} \frac{1}{R_{load}}}$$

$$\frac{V_{qsL}^s(s)}{V_{qsL}^{s*}(s)} = \frac{\left(sK_p + K_i\right) K}{s^3 L_f C_f} \frac{1}{1 + \frac{\left(sK_p + K_i\right) K}{s^3 L_f C_f} + \frac{1}{s^2 L_f C_f} + \frac{1}{s C_f R_{load}}}$$

$$\frac{V_{qsL}^s(s)}{V_{qsL}^{s*}(s)} = \frac{\frac{(sK_p + K_i)K}{s^3 L_f C_F}}{s^3 L_f C_F R_{load} + (sK_p + K_i)KR_{load} + sR_{load} + s^2 L_f}$$

$$\frac{V_{qsL}^s(s)}{V_{qsL}^{s*}(s)} = \frac{(sK_p + K_i)K}{s^3 L_f C_F + s^2 \frac{L_f}{R_{load}} + s(K_p K + 1) + K_i K} \quad (\text{Eq. 4-15}).$$

The characteristic equation is given by the denominator of the closed-loop transfer function

$$s^3 + s^2 \frac{1}{C_f R_{load}} + s \frac{(1 + K_p K)}{L_f C_f} + \frac{K_i K}{L_f C_f} = 0 \quad (\text{Eq. 4-16})$$

An alternative method to solve for the characteristic equation is to use the state equations, Equations 4-11 and 4-12. Additional states are defined to account for the integrators employed in the control as follows

$$\begin{bmatrix} \frac{dx_{qs}^s}{dt} \\ \frac{dx_{ds}^s}{dt} \end{bmatrix} = \begin{bmatrix} V_{qs}^{s*} - V_{qsL}^s \\ V_{ds}^{s*} - V_{dsL}^s \end{bmatrix} \quad (\text{Eq. 4-17})$$

Placing the q-quantities into state space normal form results in Equation 4-18

$$\frac{d}{dt} \begin{bmatrix} x_{qs}^s \\ i_{qs}^s \\ V_{qsL}^s \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 \\ \frac{K_i}{L_f} & 0 & -\frac{K_p}{L_f} - \frac{1}{L_f} \\ 0 & \frac{1}{C_f} & -\frac{1}{R_{load} C_f} \end{bmatrix} \begin{bmatrix} x_{qs}^s \\ i_{qs}^s \\ V_{qsL}^s \end{bmatrix} + \begin{bmatrix} \frac{1}{K_p} \\ \frac{1}{L_f} \\ 0 \end{bmatrix} V_{qs}^{s*} \quad (\text{Eq. 4-18})$$

where the 3x3 system matrix is typically denoted as the system **A** matrix. To find the characteristic equation the determinant of (**sI** - **A**) is found

$$\begin{aligned}
 &= \det \left(\begin{bmatrix} s & 0 & 0 \\ 0 & s & 0 \\ 0 & 0 & s \end{bmatrix} - \begin{bmatrix} 0 & 0 & -1 \\ \frac{K_i K}{L_f} & 0 & -\frac{K_p K}{L_f} - \frac{1}{L_f} \\ 0 & \frac{1}{C_f} & -\frac{1}{R_{load} C_f} \end{bmatrix} \right) \\
 &= \det \begin{bmatrix} s & 0 & 1 \\ -\frac{K_i K}{L_f} & s & \frac{K_p K + 1}{L_f} \\ 0 & -\frac{1}{C_f} & s + \frac{1}{R_{load} C_f} \end{bmatrix} \\
 &= s \left(s \left(s + \frac{1}{R_{load} C_f} \right) - \left(-\frac{1}{C_f} \right) \left(\frac{K_p K + 1}{L_f} \right) \right) - 0 + \left(-\frac{K_i K}{L_f} \right) \left(-\frac{1}{C_f} \right) \\
 &= s^3 + s^2 \frac{1}{R_{load} C_f} + s \frac{K_p K + 1}{L_f C_f} + \frac{K_i K}{L_f C_f} \tag{Eq. 4-19}
 \end{aligned}$$

Note that Equation 4-19 is identical to Equation 4-16, as expected.

With the characteristic equation determined, desired pole locations can be selected and implemented by choice of K_i and K_p and the resultant transient response investigated. Examining the effects of the constants $K_i K$ and $K_p K$ on transient response is most easily accomplished through simulation. A simple MATLAB routine can easily show transient response and pole locations for specific values of $K_i K$ and $K_p K$. It is typically desired to have a quick response with a limited amount of overshoot. In

addition, the gains should not be made too large or else the PWM algorithm is pushed into overmodulation and the aforementioned linear analysis becomes invalid.

To facilitate analysis, the system is transformed into the synchronous reference frame where the desired input voltage is represented by a steady-state constant value. In the synchronous reference frame the q- and d-variables are no longer uncoupled, so all the states must be considered together. The state equation for the system with a stationary controller, represented in the synchronous reference frame, is given by Equation 4-20.

$$\begin{bmatrix} \dot{V}_{Load-q}^e \\ \dot{V}_{Load-d}^e \\ \dot{i}_{L-q}^e \\ \dot{i}_{L-d}^e \\ \dot{xv}_q^e \\ \dot{xv}_d^e \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_f R_{Load}} & -\omega_e & \frac{1}{C_f} & 0 & 0 & 0 \\ \omega_e & -\frac{1}{C_f R_{Load}} & 0 & \frac{1}{C_f} & 0 & 0 \\ -\frac{K_p K + 1}{L_f} & 0 & 0 & -\omega_e & \frac{K_i K}{L_f} & 0 \\ 0 & -\frac{K_p K + 1}{L_f} & \omega_e & 0 & 0 & \frac{K_i K}{L_f} \\ -1 & 0 & 0 & 0 & 0 & -\omega_e \\ 0 & -1 & 0 & 0 & \omega_e & 0 \end{bmatrix} \begin{bmatrix} V_{Load-q}^e \\ V_{Load-d}^e \\ i_{L-q}^e \\ i_{L-d}^e \\ xv_q^e \\ xv_d^e \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & \frac{K_p K}{L_f} \\ 0 & 0 \\ 0 & \frac{K_p K}{L_f} \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Load-q}^{e*} & V_{Load-d}^{e*} \end{bmatrix} \quad (\text{Eq. 4-20})$$

Steady-state values for load voltage in terms of the desired voltages are given by the relationship:

$$V_{Load-qd}^e = \mathbf{A} V_{Load-qd}^{e*} \quad (\text{Eq. 4-21})$$

where the elements of \mathbf{A} (not to be confused with the system matrix) are given by

$$a_{11} = \frac{KR_{Load} \left(K_p^2 KR_{Load} \omega_e^2 + K_i^2 KR_{Load} - K_p \left(R_{Load} C_f L_f \omega_e^4 - R_{Load} \omega_e^2 \right) - K_i R_{Load} \omega_e^2 \right)}{D} \quad (\text{Eq. 4-22})$$

$$a_{12} = \frac{KR_{Load} \omega_e \left(-K_p L_f \omega_e^2 + K_i R_{Load} C_f L_f \omega_e^2 - K_i R_{Load} \right)}{D} \quad (\text{Eq. 4-23})$$

where

$$D = K_p^2 K^2 R_{Load}^2 \omega_e^2 + K_i^2 K^2 R_{Load}^2 + K_p K (2R_{Load}^2 \omega_e^2 - 2R_{Load}^2 C_f L_f \omega_e^4) - 2K_i K R_{Load} L_f \omega_e^2 + R_{Load}^2 \omega_e^2 - 2R_{Load}^2 C_f L_f \omega_e^4 + L_f^2 \omega_e^4 + R_{Load}^2 C_f^2 L_f^2 \omega_e^6 \quad (\text{Eq. 4-24})$$

and

$$\begin{aligned} a_{11} &= a_{22} \\ a_{12} &= -a_{21} \end{aligned} \quad (\text{Eq. 4-25})$$

Examining the diagonal elements of **A**, it can be seen that if the values of $K_p K$ and $K_i K$ are made large enough then the squared terms will dominate and the value will tend towards one. In addition the off-diagonal elements will tend towards zero.

Reducing the steady-state error must be weighed against sending the controller into overmodulation, as large gains will drive the modulation index to be greater than one.

Overmodulation is not necessarily an undesirable phenomenon, but the previous analysis does not hold and therefore the results will not be reliable.

Using the values in Table 4-1 for simulation purposes, a settling time of 25 msec can be achieved with constant values of

$$\begin{aligned} K_i K &= 50 \\ K_p K &= 7. \end{aligned}$$

The controller stayed in the linear modulation range for a 50 Volt step change in commanded voltage amplitude. A larger step change with the gains used would send the controller into overmodulation. The steady-state error was found to be approximately 11%. If a smaller step change were expected then the gains could be increased to further reduce the steady-state error.

Table 4-1 - Simulation Parameters

L_f	10mH
C_f	0.1mF
R_{load}	25 Ohms

Results of the MATLAB program (Appendix D, p153) are shown in Figure 4-5. The waveform is the q-axis load voltage represented in the synchronous reference frame. The STEP function was used, together with the matrices implicit to the state-space description.

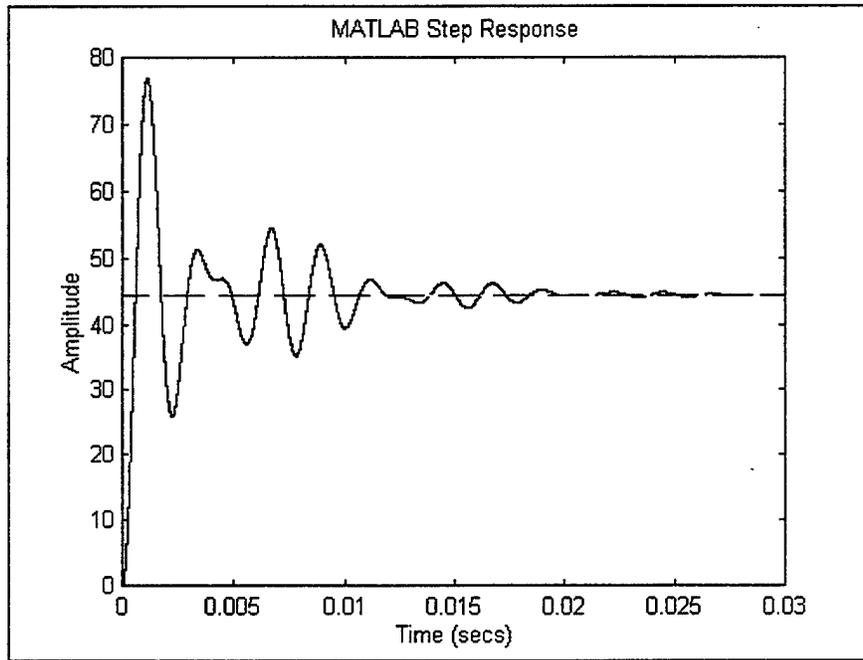


Figure 4-5 - Voltage Controller Transient Response from MATLAB

To verify that the MATLAB simulation provides representative results, an ACSL program (Appendix D, pp154 - 157) incorporating a three-phase hard-switched converter supplying a resistive load through an LC filter was developed. A PI-controller was implemented with the gains from the MATLAB simulation. A transient consisting of a 50 volt step change in the commanded q-axis synchronous load voltage from the ACSL simulation (Figure 4-6) shows a settling time of around 25 msec also. Examining the dynamics of the step change shows an almost identical response to that of the MATLAB simulation, which shows that the controller did not go into overmodulation. A significant

difference between the ACSL and MATLAB results would be evidence of overmodulation, since the ACSL program incorporates the dynamics of the sine-triangle PWM scheme and the MATLAB code simply considers the PWM a constant linear gain regardless of the input magnitude.

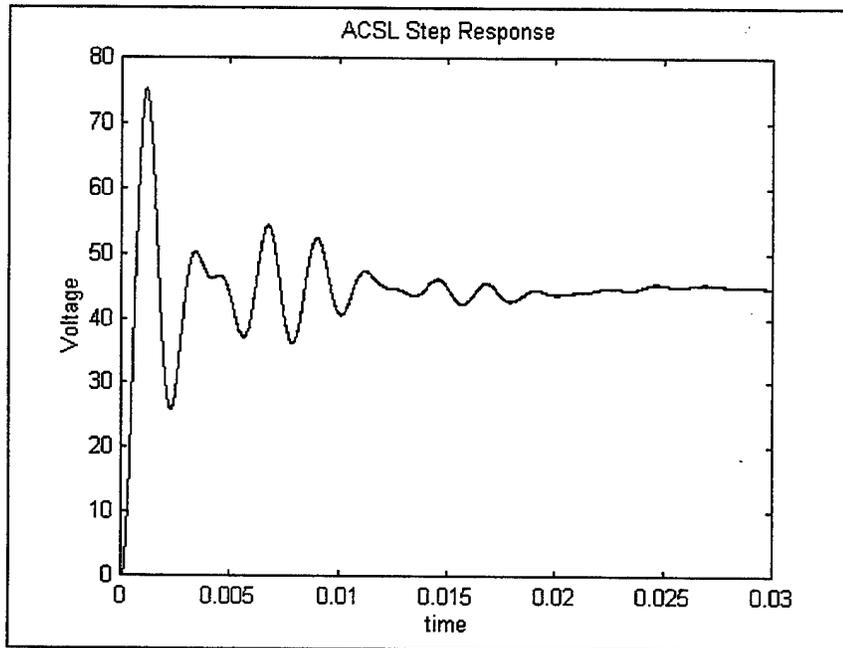


Figure 4-6 - Stationary Voltage Controller Start-up Transient

It is obvious that the steady-state error which exists with the stationary controller can be large. This error is due to the fact that the control is performed in the stationary reference frame and the control quantities are time-varying sinusoids in that frame.

One way to correct for the steady-state error would be to use the A matrix from Equation 4-21, which relates the desired voltages to the steady-state voltages in the synchronous reference frame. The desired voltages would be transformed into the synchronous reference frame, and then be pre-multiplied by A^{-1} , to give a new set of desired voltages. This new set of voltages would be transformed back into the stationary

reference frame to be used by the controller. In this way the steady-state error would be eliminated. The practicality of this method would make it difficult to implement as the delays caused in performing transformations and calculating A^{-1} would introduce additional errors. The steady-state error of stationary controllers will be investigated further in the next section.

B. CURRENT FEEDBACK CONTROLLER

A controller using current feedback together with a commanded output current waveform is considered in this section. This type of set-up can be used as a first-order approximation of an induction machine drive, where the induction machine is modeled as a simple RL load. The circuit diagram is shown in Figure 4-7.

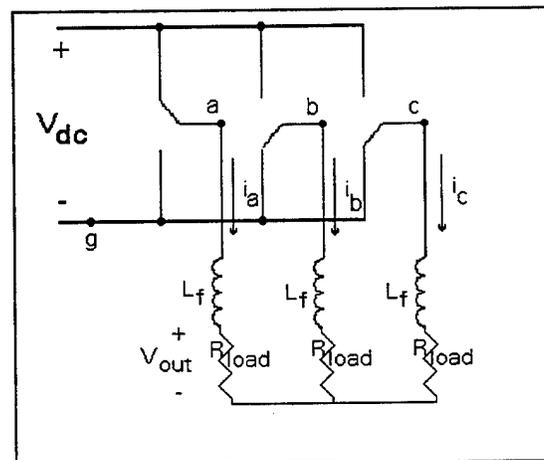


Figure 4-7 - Converter with LR Load

Using the same technique as the voltage feedback controller, the state equation for the current controller with RL load is found and listed as Equation 4-26. The signal flow

$$\frac{di_{qd0}^s}{dt} = \frac{V_{qd0L}^s - R_{load}i_{qd0}^s}{L_f} \quad (\text{Eq. 4-26})$$

diagram for the current feedback controller is illustrated in Figure 4-8 for the q-variables. A similar diagram holds for the d-variables. In the stationary reference frame for the system considered, the 'q' and 'd' variables are not coupled. In Figure 4-8, K is the PWM gain and i_{qs}^{s*} is the desired q-axis current.

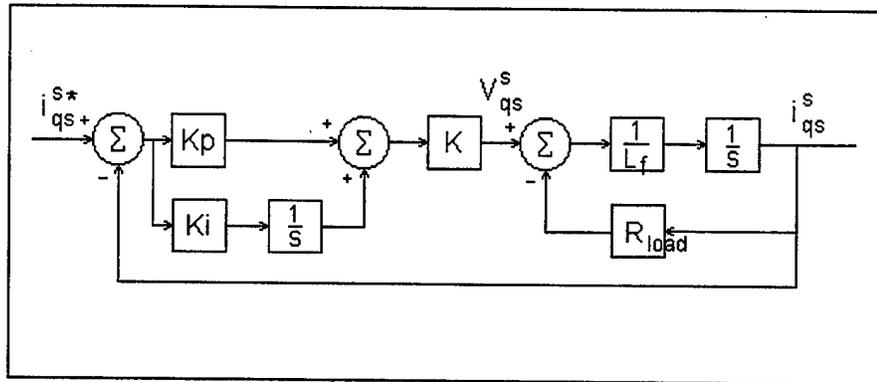


Figure 4-8 - Signal Flow Diagram, q-Quantities Only

Using the same techniques as before the transfer function for the current feedback controller is uncovered and is given in Equation 4-27.

$$\frac{i_{qs}^s}{i_{qs}^{s*}} = \frac{K_p K s + K_i K}{L_f s^2 + (R_{Load} + K_p K) s + K_i K} \quad (\text{Eq. 4-27})$$

Dynamic response can be investigated using simulation as in the voltage feedback converter. One problem encountered is that the control signals are not DC values, instead they vary at the output frequency. This also occurred with the voltage feedback converter in the previous section. To determine the steady-state error, Equation 4-27 is used with 's' set equal to $j\omega$.

$$\frac{i_{qs}^s}{i_{ds}^{s*}} = \left. \frac{K_p K s + K_i K}{L_f s^2 + (R_{Load} + K_p K) s + K_i K} \right|_{s=j\omega}$$

$$i_{qs}^s = \frac{K_i K + j\omega K_p K}{K_i K - L_f \omega^2 + j\omega(R_{Load} + K_p K)} i_{qs}^{s*} \quad (\text{Eq. 4-28})$$

It can be demonstrated from Equation 4-28 that unless the output frequency is zero, a steady-state error will exist. For an output frequency of 60Hz the commanded-to-actual current relationship predicted by Equation 4-28 is: $i_{qs}^s = i_{qs}^{s*} 0.889 \angle -1.36^\circ$.

As the previous analysis has pointed out, one drawback of using stationary reference frame variables in the control is that the steady-state error is non-zero. To facilitate further investigation of the controller, the analysis is shifted to the synchronous reference frame. In this frame the commanded quantities will be DC values and analysis will be simpler. The synchronous reference frame state space formulation of the system with a stationary reference frame controller is given by Equation 4-29. [Ref. 12]

$$\begin{bmatrix} \dot{i}_{qs}^e \\ \dot{i}_{ds}^e \\ \dot{x}_q^e \\ \dot{x}_d^e \end{bmatrix} = \begin{bmatrix} \frac{K_p K + R_{Load}}{L_f} & -\omega_e & \frac{1}{L_f} & 0 \\ \omega_e & -\frac{K_p K + R_{Load}}{L_f} & 0 & \frac{1}{L_f} \\ -K_i K & 0 & 0 & -\omega_e \\ 0 & -K_i K & \omega_e & 0 \end{bmatrix} \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \\ x_q^e \\ x_d^e \end{bmatrix} + \begin{bmatrix} \frac{K_p K}{L_f} & 0 \\ 0 & \frac{K_p K}{L_f} \\ K_i K & 0 \\ 0 & K_i K \end{bmatrix} \begin{bmatrix} i_{qs}^{e*} \\ i_{ds}^{e*} \end{bmatrix} \quad (\text{Eq. 4-29})$$

The relationship between commanded and actual steady-state currents represented in the synchronous reference frame may be derived from Equation 4-29 by setting the derivatives of the state variables equal to zero. Synchronous reference frame quantities

$$\mathbf{i}_{qds}^e = \mathbf{A} \mathbf{i}_{qds}^{e*} \quad (\text{Eq. 4-30})$$

are used because for a desired sinusoidal three-phase input, steady-state DC commanded quantities result. The elements of \mathbf{A} (not to be confused with the system matrix) are given as [Ref. 12]

$$a_{11} = a_{22} = \frac{K'_p(R_{Load} + K'_p) + \frac{K'_i}{\omega_e} \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)}{\left(R_{Load} + K'_p \right)^2 + \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)^2} \quad (\text{Eq. 4-31})$$

$$a_{12} = -a_{21} = \frac{K'_p \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right) - \frac{K'_i}{\omega_e} (R_{Load} + K'_p)}{\left(R_{Load} + K'_p \right)^2 + \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)^2} \quad (\text{Eq. 4-32}).$$

In Equations 4-31 and 4-32 the values for K'_p and K'_i incorporate the pulse-width-modulation gain K . To verify the accuracy of Equations 4-29 through 4-32, an ACSL simulation (Appendix D, pp158 - 161) incorporating a controller in the stationary reference frame with an RL load was developed and investigated. Values used in the simulation are given in Table 4-2.

Table 4-2 - Simulation Parameters

L_f	10mH
R_{load}	25 Ohms
K'_i	3000
K'_p	200
ω_e	377

For the simulation the synchronous reference frame commanded current values for the synchronous quantities were $i_{qs}^{e*} = 5.0$ Amps and $i_{ds}^{e*} = 0.0$ Amps. Using Equations 4-31 and 4-32, a_{11} is computed as 0.889 and a_{12} as -0.019. Thus, the steady-state values for i_{qs}^e and i_{ds}^e are predicted to be

$$i_{qs}^e = a_{11}i_{qs}^{e*} + a_{12}i_{ds}^{e*} = 0.889 * 5.0 - 0.019 * 0.0 = 4.445 \text{ Amps.}$$

$$i_{ds}^e = a_{21}i_{qs}^{e*} + a_{22}i_{ds}^{e*} = 0.019 * 5.0 - 0.889 * 0.0 = 0.095 \text{ Amps.}$$

This corresponds well with the graph of commanded and actual currents during start-up, shown in Figure 4-9.

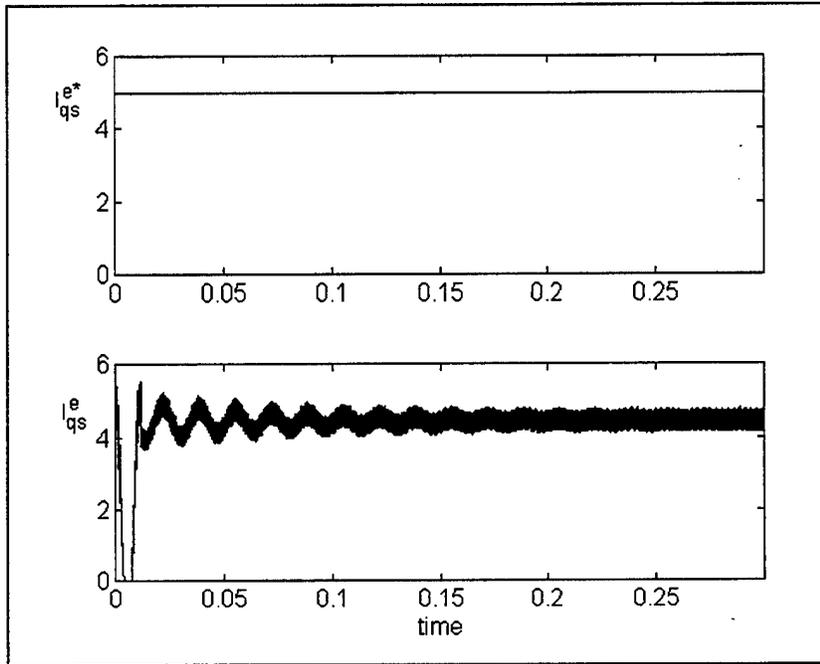


Figure 4-9 - Stationary Current Controller Start-up Transient

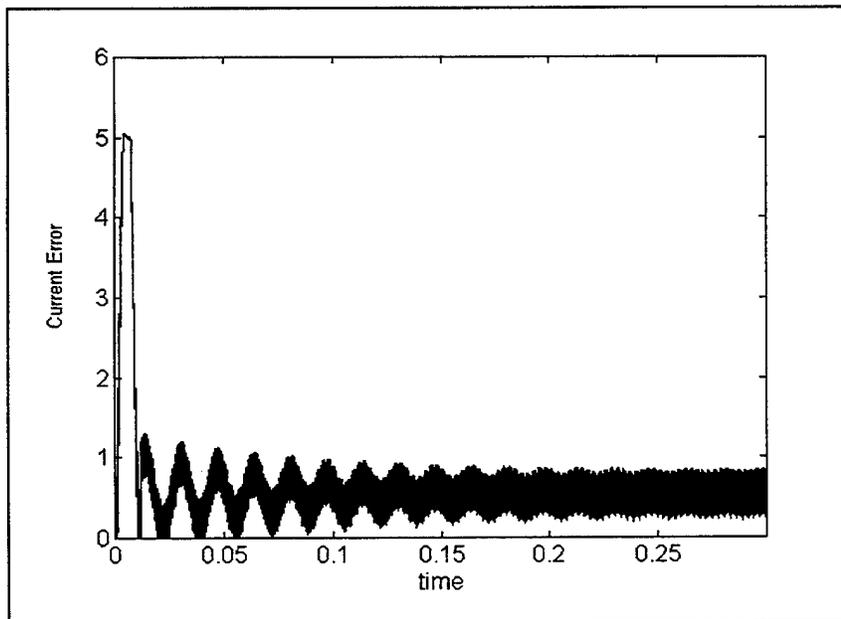


Figure 4-10 - Stationary Current Controller Start-up Error Transient

To overcome the steady-state error, the control can be performed in the synchronous reference frame where the signals being controlled are all DC quantities.

The analysis of such a system results in a state space description given by [Ref. 12]

$$\begin{bmatrix} \dot{i}_{qs}^e \\ \dot{i}_{ds}^e \\ \dot{x}_q^e \\ \dot{x}_d^e \end{bmatrix} = \begin{bmatrix} -\frac{K_p K + R_{Load}}{L_f} & -\omega_e & \frac{1}{L_f} & 0 \\ \omega_e & -\frac{K_p K + R_{Load}}{L_f} & 0 & \frac{1}{L_f} \\ -K_i K & 0 & 0 & 0 \\ 0 & -K_i K & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \\ x_q^e \\ x_d^e \end{bmatrix} + \begin{bmatrix} \frac{K_p K}{L_f} & 0 \\ 0 & \frac{K_p K}{L_f} \\ K_i K & 0 \\ 0 & K_i K \end{bmatrix} \begin{bmatrix} i_{qs}^{e*} \\ i_{ds}^{e*} \end{bmatrix} \quad (\text{Eq. 4-33})$$

Note that the only difference between Equation 4-29 and Equation 4-33 is that elements (3,4) and (4,3) are now zero. The relationship between the actual and commanded qd-currents is now given by, [Ref. 12]

$$\mathbf{i}_{qds}^e = \mathbf{A} \mathbf{i}_{qds}^{e*} \quad (\text{Eq. 4-34})$$

where the elements of \mathbf{A} are

$$a_{11} = a_{22} = 1 \quad (\text{Eq. 4-35})$$

$$a_{12} = a_{21} = 0 \quad (\text{Eq. 4-36})$$

An ACSL simulation (Appendix D, pp 162 - 165) with a controller in the synchronous reference frame was implemented to verify the results. Values for the simulation are as shown in Table 4-2. Results of the simulation are illustrated in Figure 4-11. A zero steady-state error was achieved as desired.

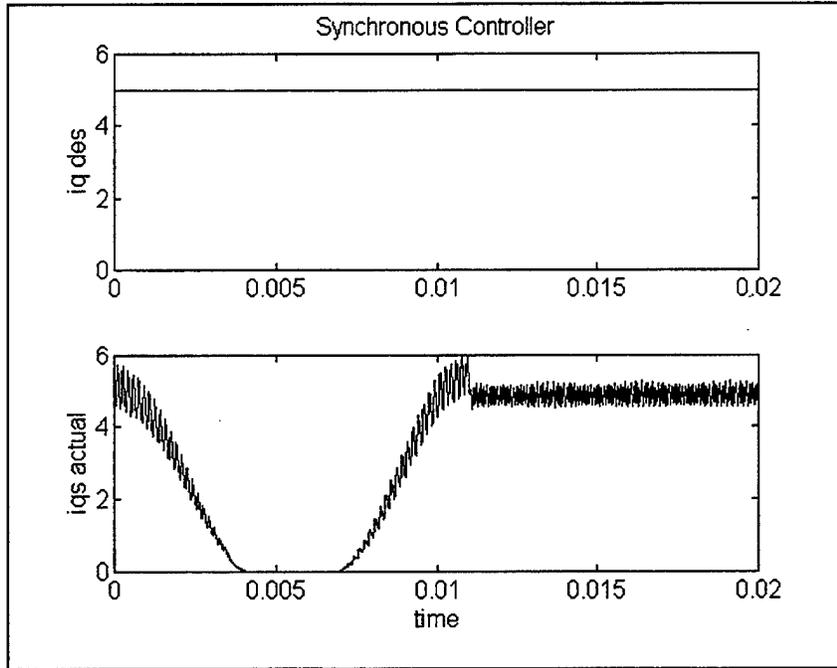


Figure 4-11 - Synchronous Controller Simulation Results

C. A VOLTAGE CONTROLLER WITH INNER CURRENT CONTROL LOOP

A controller which uses current and voltage feedback as well as current and voltage feedforward has been proposed in the literature [Ref. 13]. The input voltage is the line-to-neutral voltage synthesized from a three-phase inverter as described previously. An LC-filter is used to reduce the voltage harmonics across the load. The control is predicated on specifying a desired output voltage and using various feedback and feedforward signals to force the load voltage to track that value. A per-phase representation of the system is illustrated in Figure 4-12.

The state equations for a phase of the system are given by

$$\frac{di_f}{dt} = \frac{V_f - V_{Load}}{L_f} \quad (\text{Eq. 4-37})$$

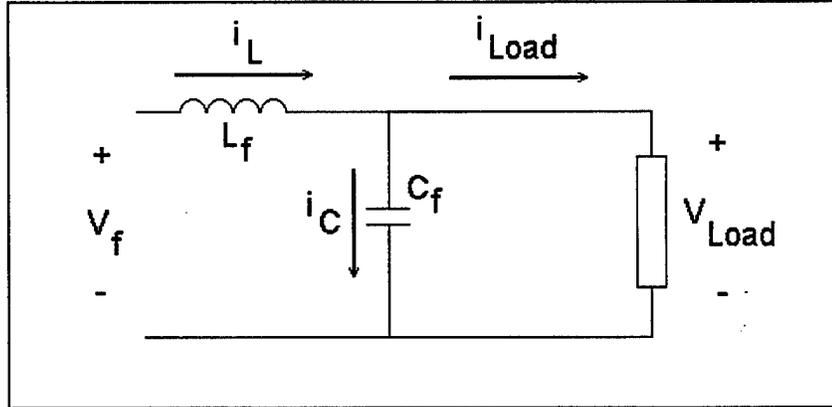


Figure 4-12 - Per-Phase Model

$$\frac{dV_{Load}}{dt} = \frac{i_L - i_{Load}}{C_f} = \frac{i_C}{C_f} \quad (\text{Eq. 4-38})$$

The desired a-phase of the load voltage is specified as

$$V_{Load}^* = V_o \cos(\omega_e t) \quad (\text{Eq. 4-39})$$

where V_o is the desired peak amplitude and ω_e the desired frequency in radians per second. Knowing the desired output voltage the desired capacitor current can be determined from Equation 4-38.

$$i_C^* = C_f \frac{dV_{Load}^*}{dt} = -V_o \omega_e C_f \sin(\omega_e t) \quad (\text{Eq. 4-40})$$

The desired capacitor current is fed forward by adding it to the actual load current to obtain the desired inductor current. This value is then compared with the actual inductor current to obtain a current error, which is passed to a PI controller to generate a control signal for a particular phase of the converter. The current-loop controller is illustrated in Figure 4-13.

Voltage feedback is incorporated by comparing the desired and actual values of load voltage to obtain a voltage error. The voltage error is input to a PI controller to

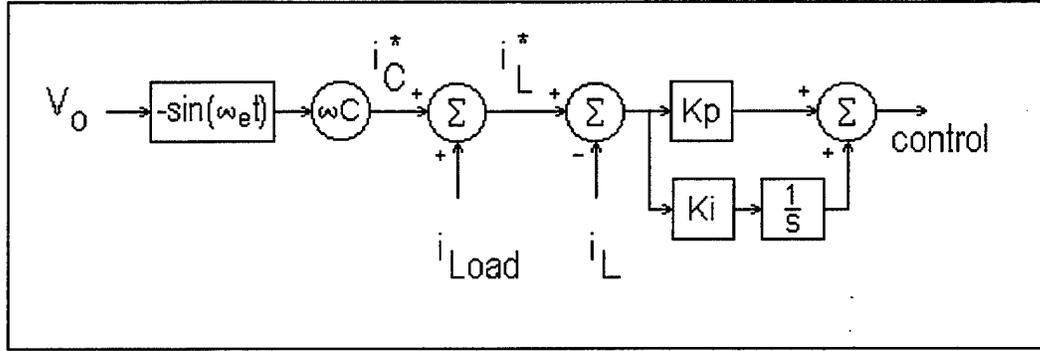


Figure 4-13 - Per-Phase Current-Loop Controller

generate a control signal. Feedforward action is realized by using the desired inductor current and desired load voltage to obtain the desired converter output voltage as specified in Equation 4-41.

$$V_f^* = L_f \frac{di_L^*}{dt} + V_{Load}^* \quad (\text{Eq. 4-41})$$

Equation 4-41 can be simplified by omitting the time derivative of inductor current and re-writing the desired output voltage as:

$$\mathbf{V}_f^{des} = \mathbf{V}_{Load}^{des} + j\omega_e L_f \mathbf{i}_L^* \quad (\text{Eq. 4-42})$$

Because the time derivatives are ignored in Equation 4-42, the feedforward voltage is only correct for sinusoidal steady-state conditions. Feedback loops are necessary to make-up for this shortcoming. Feedback will also correct for discrepancies between the value of inductance used in the controller and the actual value of the circuit filter inductance which may change due to temperature and saturation effects. Figure 4-14 shows the signal flow for the per-phase controller.

Implementation of the controller is accomplished in the synchronous reference frame where sinusoidal quantities become DC quantities. This simplifies the control and

$$\begin{bmatrix} V_{qs}^{e*} \\ V_{ds}^{e*} \\ V_{0s}^{e*} \end{bmatrix} = \mathbf{K}_s^e \begin{bmatrix} V_o \cos(\omega_e t) \\ V_o \cos\left(\omega_e t - \frac{2\pi}{3}\right) \\ V_o \cos\left(\omega_e t + \frac{2\pi}{3}\right) \end{bmatrix} = \begin{bmatrix} V_o \\ 0 \\ 0 \end{bmatrix} \quad (\text{Eq. 4-45})$$

additional detail. The composite controller in the synchronous reference frame is shown in Figure 4-15.

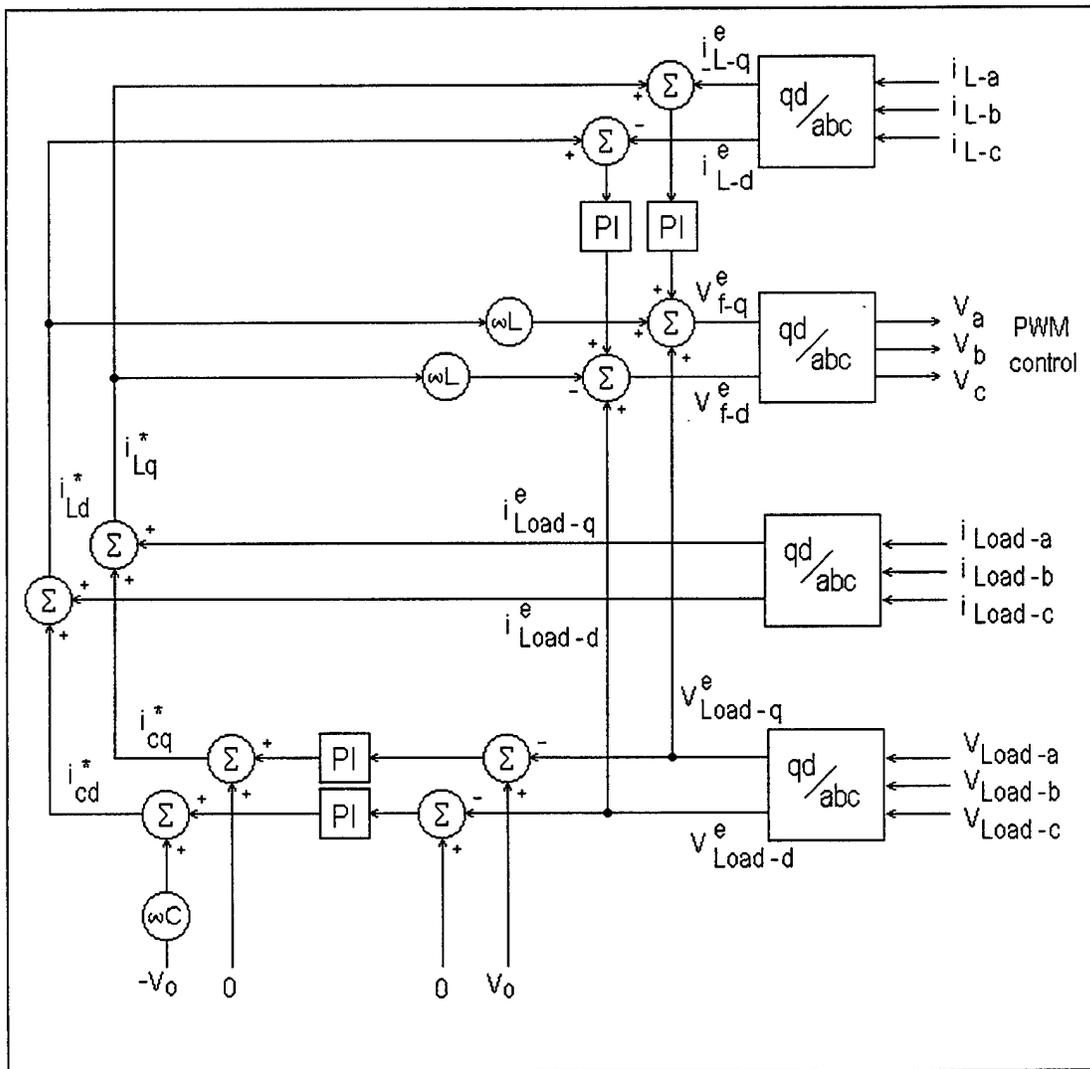


Figure 4-15 - Signal Flow for Synchronous Controller

To choose gains for the PI controllers the transfer function relating the commanded and actual output voltages must be determined. Assuming an RL load, the system state equations in the synchronous reference frame are given by

$$\begin{bmatrix} \dot{V}_{Load-q}^e \\ \dot{V}_{Load-d}^e \end{bmatrix} = \begin{bmatrix} -\omega_e V_{Load-d}^e \\ \omega_e V_{Load-q}^e \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} i_{L-q}^e \\ i_{L-d}^e \end{bmatrix} - \frac{1}{C_f} \begin{bmatrix} i_{Load-q}^e \\ i_{Load-d}^e \end{bmatrix} \quad (\text{Eq. 4-46})$$

$$\begin{bmatrix} i_{L-q}^e \\ i_{L-d}^e \end{bmatrix} = \begin{bmatrix} -\omega_e i_{L-d}^e \\ \omega_e i_{L-q}^e \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} V_{f-q}^e \\ V_{f-d}^e \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} V_{Load-q}^e \\ V_{Load-d}^e \end{bmatrix} \quad (\text{Eq. 4-47})$$

$$\begin{bmatrix} i_{Load-q}^e \\ i_{Load-d}^e \end{bmatrix} = \begin{bmatrix} -\omega_e i_{Load-d}^e \\ \omega_e i_{Load-q}^e \end{bmatrix} + \frac{1}{L_{Load}} \begin{bmatrix} V_{Load-q}^e \\ V_{Load-d}^e \end{bmatrix} - \frac{R_{Load}}{L_{Load}} \begin{bmatrix} i_{Load-q}^e \\ i_{Load-d}^e \end{bmatrix} \quad (\text{Eq. 4-48})$$

In order to incorporate the dynamics of the PI-compensators, the following additional state equations are required

$$\begin{bmatrix} \dot{x}v_q^e \\ \dot{x}v_d^e \end{bmatrix} = \begin{bmatrix} V_O - V_{Load-q}^e \\ 0 - V_{Load-d}^e \end{bmatrix} \quad (\text{Eq. 4-49})$$

$$\begin{bmatrix} \dot{x}i_q^e \\ \dot{x}i_d^e \end{bmatrix} = \begin{bmatrix} i_{L-q}^{e*} - i_{Load-q}^e \\ i_{L-d}^{e*} - i_{Load-d}^e \end{bmatrix} = \begin{bmatrix} K_{pv} V_O - K_{pv} V_{Load-q}^e + K_{iv} x v_q^e + i_{Load-q}^e - i_{L-q}^e \\ -C_f \omega_e V_O - K_{pv} V_{Load-d}^e + K_{iv} x v_d^e + i_{Load-d}^e - i_{L-d}^e \end{bmatrix} \quad (\text{Eq. 4-50})$$

Equations 4-51 and 4-52 show the synchronous reference frame commanded voltages represented in terms of state variables,

$$\begin{aligned} V_{f-q}^{e*} = & (K_{pc} K_{pv} - \omega_e^2 L_f C_f) V_O + K_{pc} K_{iv} x v_q^e + \omega_e L_f K_{iv} x v_d^e + K_{ic} x i_q^e \\ & + (1 - K_{pc} K_{pv}) V_{Load-q}^e - (\omega_e L_f K_{pv}) V_{Load-d}^e + K_{pc} i_{Load-q}^e + \omega_e L_f i_{Load-d}^e - K_{pc} i_{L-d}^e \end{aligned} \quad (\text{Eq. 4-51})$$

$$\begin{aligned} V_{f-d}^{e*} = & -(K_{pc} \omega_e C_f + \omega_e L_f K_{pv}) V_O - \omega_e L_f K_{iv} x v_q^e + K_{pc} K_{iv} x v_d^e + K_{ic} x i_d^e \\ & + \omega_e L_f K_{pv} V_{Load-q}^e + (1 - K_{pc} K_{pv}) V_{Load-d}^e - \omega_e L_f i_{Load-q}^e + K_{pc} i_{Load-d}^e - K_{pc} i_{L-d}^e \end{aligned} \quad (\text{Eq. 4-52})$$

where V_o is the commanded q-axis voltage V_{qs}^{e*} . The actual three-phase source voltages from the converter are the control voltages times the PWM gain, in the synchronous reference frame this is

$$V_{f-q}^e = K_{PWM} V_{f-q}^{e*} \quad (\text{Eq. 4-53})$$

$$V_{f-d}^e = K_{PWM} V_{f-d}^{e*} \quad (\text{Eq. 4-54})$$

Combining Equations 4-46 through 4-54, the state space representation of the system is generated and shown in Equation 4-55.

From the state space representation of Equation 4-55, it is desired to obtain a transfer function relating the commanded voltage to the actual load voltage. With the transfer function known, controller gains can be selected to give the system a desired stable response. As the transfer function will be of tenth-order, an analytical solution was not attempted. Instead, a MATLAB command file was used to obtain transfer functions for various gains. The poles of the system could not all be placed by choosing gains, since there are only four gains to choose and ten system poles. Actual values examined in the analysis are documented in Table 4-3.

Table 4-3 - Simulation Parameters

L_f	10.1 mH
C_f	1.0 mF
ω_e	377 rad/sec
R_{Load}	25 ohms
L_{Load}	1.0 mH
Kpv	0.25
Kpc	10.0
Kiv	1.0
Kic	1.0

The resultant poles and zeros of the transfer function $\frac{V_{Load-q}^e}{V_o}$ are presented in Table 4-4.

Table 4-4 - Poles and Zeros of Transfer Function

Poles	Zeros
-249600±j376	-249800±j433
-419±j1815	-907±j1500
-969±j1060	-3.92±j0.59
-3.92±j0.59	-0.087±j0.033
-0.087±j0.033	

The response of the system to a 50 volt step change in commanded voltage, V_o , was simulated in MATLAB using the STEP function and the state space description of the system given in Equation 4-55. Figure 4-16 illustrates the MATLAB output of the 50 volt step input. The MATLAB program is shown in Appendix D, pp 166 - 167.

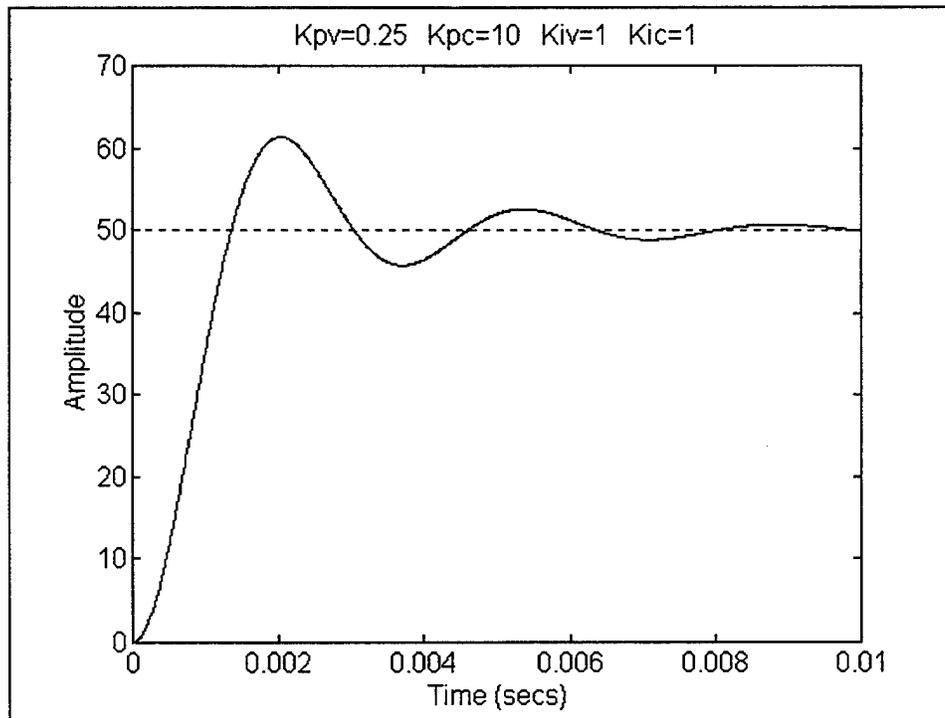


Figure 4-16 - MATLAB Step Response

When considering the poles of the transfer function shown in Table 4-4, the MATLAB step response does not seem to give the correct response. It would appear that the dominant poles would be the set closest to the origin ($-0.087 \pm j0.033$). If this were the case then the settling time for the step response would be much longer than that seen by the simulation. To explain the rapid settling time the zeros of the transfer function must also be examined. Taking the zeros into account, pole-zero cancellation occurs leaving the dominant set of poles as $-419 \pm j1815$. The settling time from Figure 4-17 is

approximately 0.01 seconds. Using the approximation $t_s = \frac{4.6}{\sigma}$, where σ is the negative real part of the dominant pole [Ref. 11], the settling time would be $t_s = \frac{4.6}{419} = 0.011$ sec.

Thus the poles located at $-419 \pm j1815$ are the dominant poles for the system.

To verify that the MATLAB simulation was valid, a detailed simulation of the system and controller using ACSL was performed. The simulation (Appendix D, pp 168 - 171) incorporated the parameter values listed in Table 4-4. A hard-switched converter was used in the simulation with a sine-triangle control scheme. The three modulating sinusoids for the control scheme are the V_a , V_b , and V_c signals illustrated in Figure 4-15. A 50 volt step change in commanded voltage was simulated and the results are shown in Figure 4-17.

Comparing Figures 4-16 and 4-17 shows an almost identical response for the step change. This validates the MATLAB simulation as an accurate model of the system and controller, at least in the linear operating range of the PWM scheme.

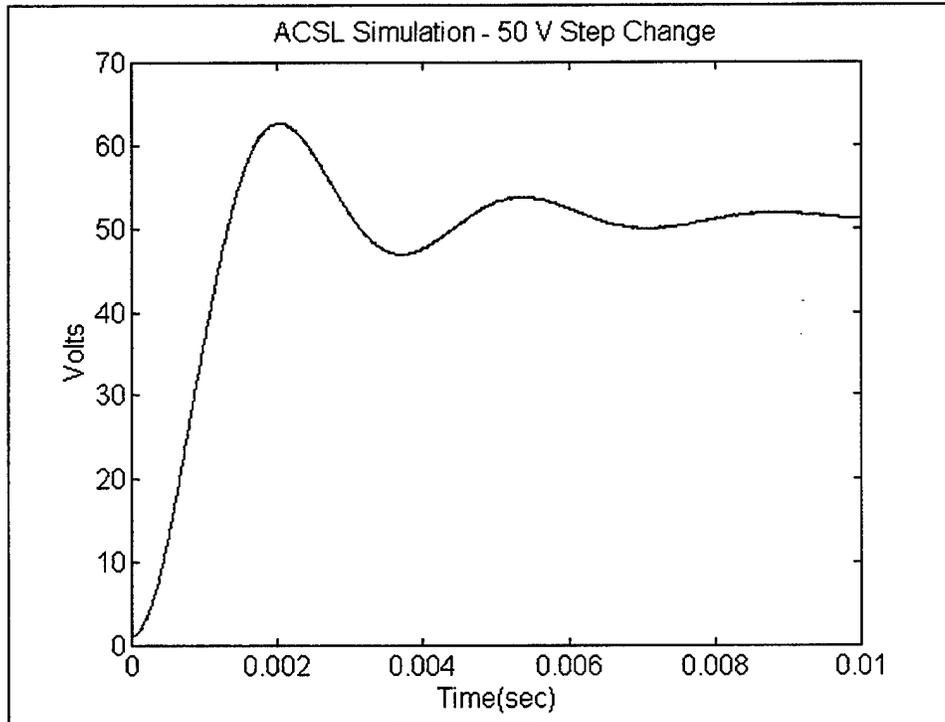


Figure 4-17 - ACSL Step Response

While investigating the effect of controller gains on system response with the MATLAB model, it was noted that larger gains tended to speed up the response. In fact system responses in the order of a few microseconds were achieved using very large gains. When these same gains were used in the ACSL simulation the results showed very erratic and unpredictable outputs. This variation is due to the fact that the state space description used in the MATLAB code assumed that no matter what the commanded signal specified by the controller, the inverter could theoretically produce it. Thus, if the commanded signal was 50000 volts, that is what the system would produce. In reality the system cannot put out a voltage above the source voltage (which was 500 V for the simulations). Thus if the control signal became too large saturation occurred which was not represented by the MATLAB model.

This problem could be overcome by using a source with a very large value, but this is impractical in most realizable systems. Instead the gains were chosen lower so that normal transients would not drive the controller into saturation. This gave a predictable response to transients.

Now that the dominant set of poles has been uncovered for the set of gains chosen, the effect of different gains must be addressed. Specifically, does changing the gains negate the pole-zero cancellation seen earlier and thus shift the dominant poles closer to the origin. To investigate this several sets of gains were simulated and the poles and zeros created were compared. Results for two different sets of poles are listed in Tables 4-5 and 4-6.

Table 4-5 - Poles and Zeros
Gains: $K_{pv}=1.5$ $K_{pc}=15$ $K_{iv}=10$ $K_{ic}=5$

Poles	Zeros
-249600+j376	-249800+j380
-350+j5043	-1046+j4775
-1531+j4288	-6.66+j0.169
-6.66+j0.167	-0.313+j0.0079
-0.313+j0.0079	

Table 4-6 - Poles and Zeors
Gains: $K_{pv}=0.1$ $K_{pc}=1.75$ $K_{iv}=0.01$ $K_{ic}=0.01$

Poles	Zeros
-249600+j376	-249800+j1530
-10.54+j78.66	-10700
-563+j32.0	-590.8
-0.0876+j0.0330	-0.0876+j0.0330
-.000997+j0.00217	-.000997+j0.00217

Inspection of the results shows a pole-zero cancellation for the four poles closest to zero for both sets of gains. All of the other sets of gains investigated showed the same cancellation. It is therefore not a particular set of gains which cause the four poles closest to zero to be canceled, but the system configuration which causes it.

With the knowledge of pole-zero cancellation, the system response can be better optimized. Again using simulation as a tool, several sets of gains were programmed and the responses to a step input analyzed. An optimum set of gains was chosen and is illustrated in Table 4-7 along with the poles and zeros of the transfer function.

Table 4-7 - Optimum Poles and Zeros
Gains - Kpv=0.05 Kpc=10 Kiv=0.05 Kic=0.05

Poles	Zeros
-249600+j376	-249800+j1530
-814.8+j220.1	-1955
-576.8+j534.8	-638.4
-0.632+j0.482	-0.632+j0.482
-0.00437+j0.00166	-0.00437+j0.00166

The MATLAB generated system response to a 50 volt step increase is depicted in Figure 4-18.

To confirm that the controller did not saturate and that the MATLAB code gave realistic results, an ACSL simulation was performed and the results reported in Figure 4-19.

Comparing Figures 4-18 and 4-19 shows an almost identical response with a settling time of about 0.009 seconds. With dominant poles of $-576.8+j534.8$ the predicted settling time is $\frac{4.6}{\sigma} = \frac{4.6}{576.8} = 0.008$ seconds, which corresponds well with the step response plots.

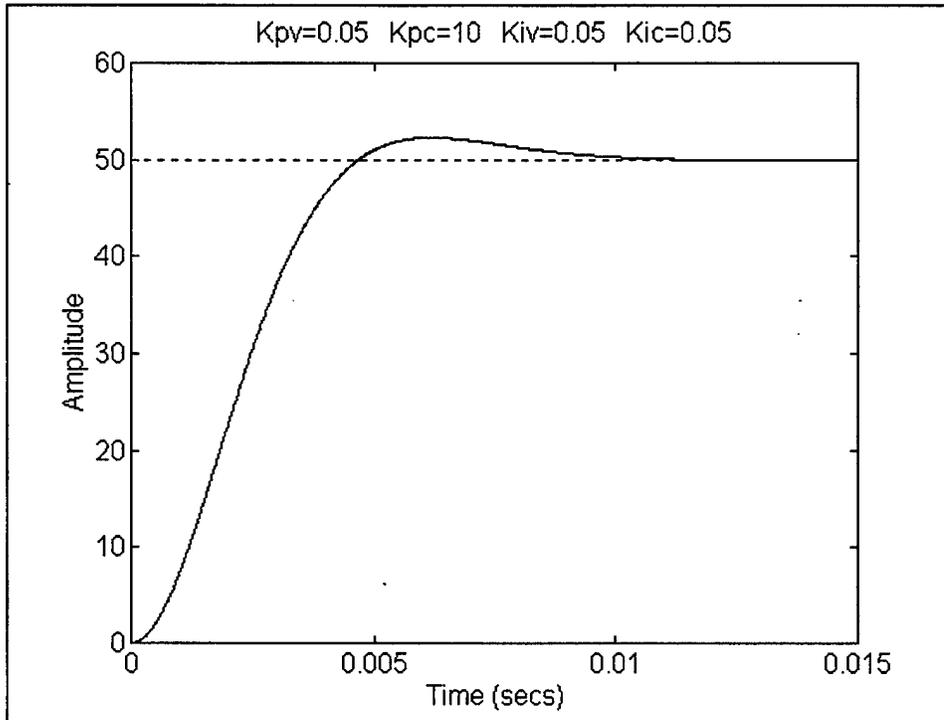


Figure 4-18 - MATLAB Step Response with Optimized Gains

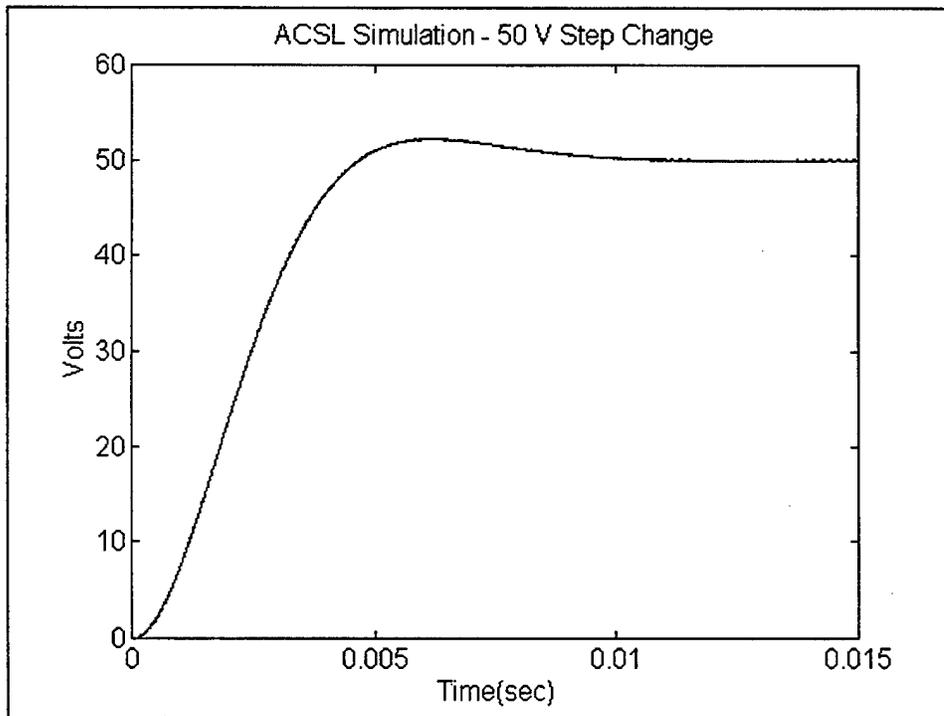


Figure 4-19 - ACSL Step Response with Optimized Gains

If a faster response were desired a bang-bang type of control could be derived where the system would be driven by either the maximum or minimum control effort until the transient was stabilized.

Normally large step changes in commanded values are not encountered. System start-up most likely would be accomplished with manual control or by using a ramp input in commanded voltage. This minimizes the importance of a quick response to step changes and emphasizes the steady-state control for which the controller was designed.

With the control issue addressed, investigation of a new modulation technique is undertaken with a focus on improving the classical sine-triangle modulation method.

V. PRINCIPLES OF SPACE VECTOR CONTROL

A new method of pulse-width-modulation has been introduced recently in the literature [Ref. 14,15]. This chapter explains the basics of this new technique called Space Vector Control (SVC). In addition, a simulation showing the feasibility of the concept is performed, and finally the advantages and disadvantages are discussed.

A. DEVELOPMENT OF SPACE VECTOR CONTROL ALGORITHM

The basic ideas of Space Vector Control have been introduced and discussed in the literature [Ref. 16,17]. The following discussion lays out the steps necessary to implement a SVC-based algorithm. To realize Space Vector Control for three-phase applications, a set of three-phase variables is represented by a single vector. This is accomplished by transforming quantities in the a-b-c reference frame into the stationary q-d-0 frame. The three phase voltages are denoted by the notation

$[V_{an} \ V_{bn} \ V_{cn}]^T = \mathbf{v}_{abcn}$. A transformation matrix is then applied to the voltage vector placing it into the desired reference frame [Ref. 10].

$$\mathbf{v}_{qd0n} = \mathbf{K}_s \mathbf{v}_{abcn} \quad (\text{Eq. 5-1})$$

$$\mathbf{K}_s = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin \theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (\text{Eq. 5-2})$$

$$\mathbf{v}_{qd0n} = \begin{bmatrix} V_{qn} \\ V_{dn} \\ V_{0n} \end{bmatrix} \quad (\text{Eq. 5-3})$$

$$\theta = \int_0^t \omega dt + \theta_0 \quad (\text{Eq. 5-4})$$

For the stationary reference frame, ω is zero and θ_0 is selected to also equal zero for convenience.

Assuming that the load is balanced the zero sequence voltage, \dot{V}_{0n} , will be zero.

The voltages V_{qn} and V_{dn} can be plotted along the stationary q- and d-axes, respectively.

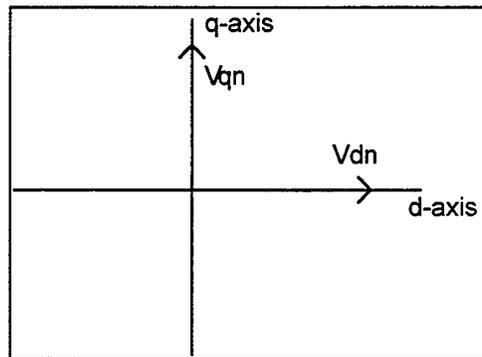


Figure 5-1 - q- and d-axis Voltages

Figure 5-2 illustrates the vector addition of the two instantaneous voltages directed along the q- and d-axes. The resultant V^* provides a vector representation for the three phase voltages, as desired.

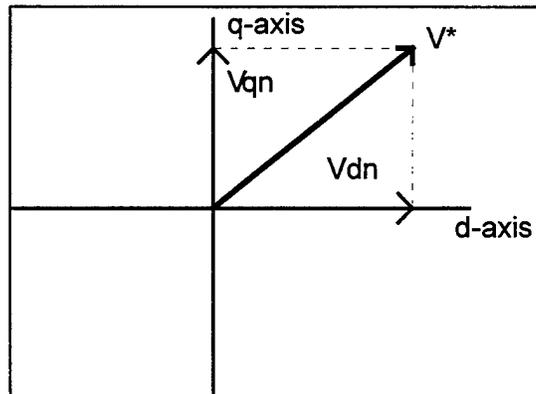


Figure 5-2 - Single Vector Representation

Since the phase voltages are sinusoids and thus time varying, the transformation into the stationary reference frame ($\omega = 0$ and $\theta_0 = 0$) will produce a time-varying resultant vector as well. If the q-axis is viewed as the imaginary axis and the d-axis the real axis, this resultant voltage can be thought of as a phasor representation of the phase voltages. By specifying the magnitude and phase angle of a reference phasor, any desired set of balanced three-phase voltages can be generated and represented conveniently. The space vector method of control uses this reference vector in conjunction with breaking the plane into six sectors to establish the rationale for switching the three-phase inverter used to synthesize the voltages.

In a six-switch inverter there are eight possible switch combinations as shown in Figure 5-3. Note that electrically State 7 and State 8 are identical, both producing zero volts across each phase.

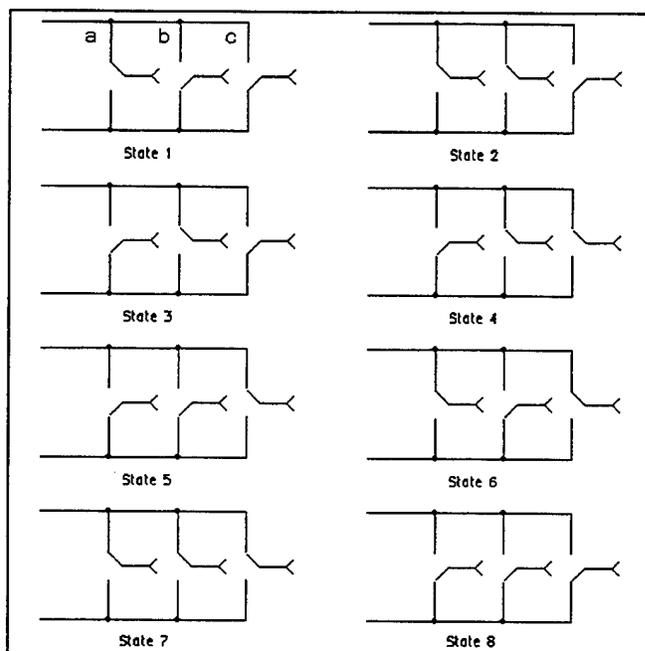


Figure 5-3 - Eight Possible Switch States for Six-Switch Inverter

If it is assumed that the inverter is connected to a balanced three-phase wye-connected load, the line-to-neutral voltages corresponding to each of the above states are summarized in Table 5-1.

Table 5-1 - Phase Voltages

State #	V_{an}	V_{bn}	V_{cn}
1	$2V_{DC}/3$	$-V_{DC}/3$	$-V_{DC}/3$
2	$V_{DC}/3$	$V_{DC}/3$	$-2V_{DC}/3$
3	$-V_{DC}/3$	$2V_{DC}/3$	$-V_{DC}/3$
4	$-2V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$
5	$-V_{DC}/3$	$-V_{DC}/3$	$2V_{DC}/3$
6	$V_{DC}/3$	$-2V_{DC}/3$	$V_{DC}/3$
7	0	0	0
8	0	0	0

Transforming the phase voltages corresponding to each state into the stationary q-d-0 frame results in the mapping illustrated in Figure 5-4. Note that the magnitude of each of the vectors is $\frac{2}{3}V_{DC}$.

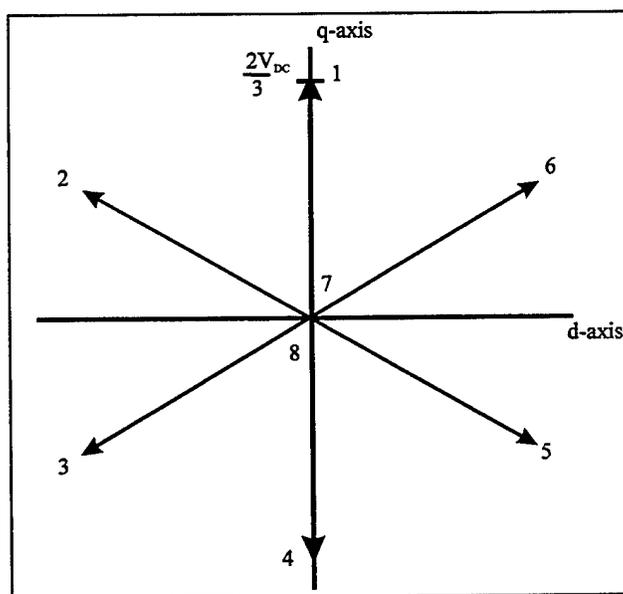


Figure 5-4 - Inverter Voltages in q-d Frame

These states divide the plane into six sectors each spanning 60 degrees, as shown in Figure 5-5.

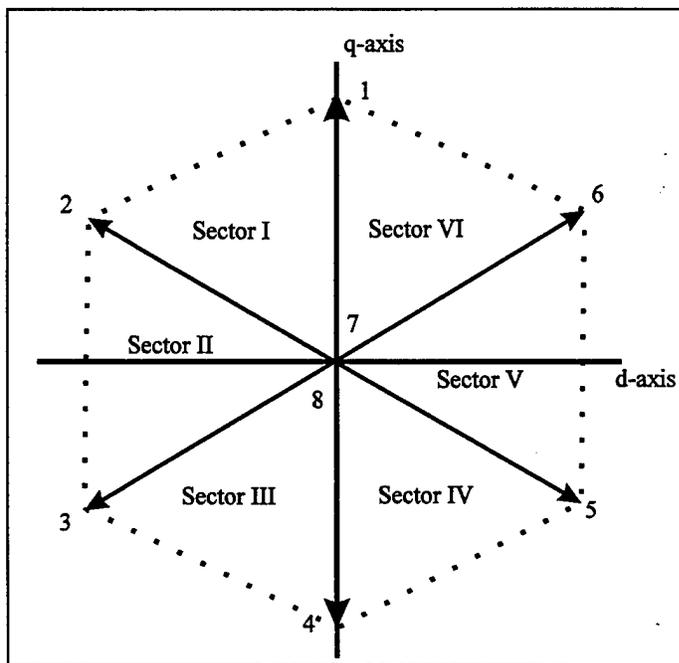


Figure 5-5 - Sectors in the q-d Plane

Next, a 'mean' space vector, \bar{V} , is defined as the weighted average of the line-to-neutral voltages used during a switching period, expressed as a single vector in the stationary q-d-0 frame. A switching period covers the time period it takes to generate the average voltage vector. If four separate switch states are used to create \bar{V} , then the period would cover the time required to switch to all four of these states. In SVC normally only three separate line-to-neutral voltage combinations are used to generate \bar{V} . These line-to neutral voltages are controlled so that \bar{V} tracks the desired voltage vector V^* . The error for one switching period is the mean voltage vector subtracted from the desired voltage vector and integrated over one switching period.

$$error = \int_{t_0}^{t_f} (\mathbf{V}^* - \bar{\mathbf{V}}) dt \quad (\text{Eq. 5-5})$$

where,

\mathbf{V}^* = desired Voltage Vector

$\bar{\mathbf{V}}$ = actual Voltage Vector

t_0 = beginning of switching period

t_f = end of switching period

This error can be maintained small if the cycle time is as short as possible and the ratio of switching frequency to output frequency is large. Both of the previous techniques, maintaining a short cycle time and a large switching to output frequency ratio, operate to keep \mathbf{V}^* approximately constant over a switching period. Since \mathbf{V}^* is rotating in the stationary q-d-0 plane at the electrical output frequency, e.g. 60Hz, if the switching frequency is sufficiently large, somewhere in the kilohertz range, then \mathbf{V}^* can be assumed constant over one switching period. Keeping \mathbf{V}^* constant during a switching period is desirable because the generation of $\bar{\mathbf{V}}$ will not be attempting to hit a “moving target.”

To keep the cycle time short, the three switching states adjacent to the reference vector are only used, and these states are used only once each to generate an average voltage vector equal to the reference vector. For example, if \mathbf{V}^* lies in Sector I then only the states adjacent to Sector I (States 1,2,7,8) will be used to generate $\bar{\mathbf{V}}$. In addition the switching frequency is made as large as practical so that the switching period, $T_s = \frac{1}{f_{switch}}$

the sum of the times at States 1,2,7 and 8, will be small. If the switching frequency were

selected to be 10kHz then the cycle time would be $T_z = \frac{1}{10000Hz} = 0.0001 \text{ sec}.$

The switching sequences are arranged in such a way that a transition from one state to the next is performed by switching only one inverter leg; this minimizes the switching frequency for each inverter leg. It can be seen in the switching diagram that these conditions are met if the inverter legs are switched in a sequence starting at one zero state and ending at the other zero state. Thus, both zero states must be used. For example, if the reference vector lies in Sector I then the switching sequence would be . . . 8,1,2,7,2,1,8,1,2,7,2 . . . Starting at State 8, phase A is switched high to arrive at State 1. From State 1, phase C is switched high to arrive at State 2. To arrive at State 7 phase C is switched high. Note that the switching sequence is 8,1,2,7... and not 8,2,1,7... . This is to minimize the number of switchings required. To go from State 8 to State 2 both phase A and phase B must be switched; however, to go from State 8 to State 1 only phase A must be switched. The times spent at each state are variables to be calculated and are used to force the average voltage equal to the desired voltage. This process repeats until V^* rotates into a new sector. The transition to the next sector is accomplished when the sequence is at a zero state, since the zero states are used in every sector. Table 5-2 lists the switching sequence to be used for each sector.

The average voltage generated for one cycle of switching from states 1-2-7 is then

$$V_{avg_{1-2-7}} = \frac{V_{state1}t_{state1} + V_{state2}t_{state2} + V_{state7}t_{state7}}{t_{state1} + t_{state2} + t_{state7}} \quad (\text{Eq. 5-6})$$

Table 5-2 - Switching Sequence

Sector	Sequence
I	...8,1,2,7,2,1,8...
II	...8,3,2,7,2,3,8...
III	...8,3,4,7,4,3,8...
IV	...8,5,4,7,4,5,8...
V	...8,5,6,7,6,5,8...
VI	...8,1,6,7,6,1,8...

Upon determining t_{state7} , half of the time will be used for State 7 and half of the time will be used for State 8. Since these two states are electrically equivalent, the average voltage will not be affected. This average voltage value is equal to \bar{V} , which is approximately the desired voltage vector, \mathbf{V}^* .

Defining variables as :

$$T_z = \frac{1}{f_{switch}} = t_{state1} + t_{state2} + t_{state7}$$

$$\mathbf{V}_1 = \mathbf{V}_{state1}$$

$$\mathbf{V}_2 = \mathbf{V}_{state2}$$

$$t_1 = t_{state1}$$

$$t_2 = t_{state2}$$

it is clear from Equation 5-6 that

$$\mathbf{V}_1 t_1 + \mathbf{V}_2 t_2 = \bar{\mathbf{V}} T_z \quad (\text{Eq. 5-7})$$

Describing the space vectors of Figure 5-6 in rectangular coordinates, $\begin{bmatrix} x \\ y \end{bmatrix}$, the above equation becomes:

$$t_1 \frac{2}{3} V_{DC} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + t_2 \frac{2}{3} V_{DC} \begin{bmatrix} \cos(60^\circ) \\ \sin(60^\circ) \end{bmatrix} = T_z \frac{2}{3} V_{DC} a \begin{bmatrix} \cos(\gamma) \\ \sin(\gamma) \end{bmatrix} \quad (\text{Eq. 5-8})$$

where $\gamma = \omega t$ and $a = \frac{|\bar{\mathbf{V}}|}{V_{DC}}$

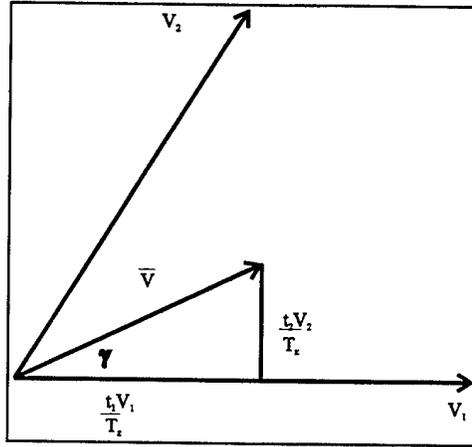


Figure 5-6 - Determination of Switching Times

Equation 5-8 is solved for t_1 and t_2 , as shown in Equations 5-9 and 5-10. Knowing t_1 and t_2 , the zero state time, t_7 , can be easily found from Equation 5-11.

$$t_1 = T_z a \frac{\sin(60^\circ - \gamma)}{\sin(60^\circ)} \quad (\text{Eq. 5-9})$$

$$t_2 = T_z a \frac{\sin(\gamma)}{\sin(60^\circ)} \quad (\text{Eq. 5-10})$$

$$t_7 = T_z - (t_1 + t_2) \quad (\text{Eq. 5-11})$$

Since the voltage is zero at both State 7 and State 8, it is found to be beneficial in terms of symmetry to allocate half of the zero voltage time to State 7 and half to State 8. By redefining t_7 as T_0 (time at zero state) and dividing by two, the desired zero state times are generated. Thus, states seven and eight are both at zero for $\frac{T_0}{2}$ seconds. This leads to the pulse pattern shown in Figure 5-7. Switching in other sectors follows the same general rules as in Sector one.

A situation may arise where the reference vector is so large that it cannot be generated in one cycle i.e. $V^* > V_1 + V_2$ (Figure 5-6). This problem can be handled by

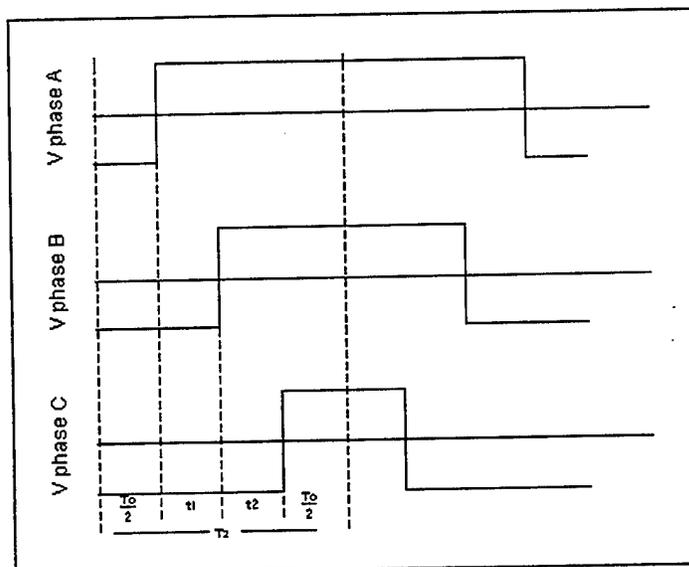


Figure 5-7 - Voltage Pattern, Sector One

limiting the control vector to $2/3$ of the DC line voltage, if a value larger than this is required the q- and d-components of the control must be scaled to achieve a smaller magnitude while maintaining the same relative proportions. This is accomplished by limiting the value of $a = \frac{|\bar{V}|}{V_{DC}}$ to $\frac{2}{3}V_{DC}$. Additionally, the time to switch from a zero state to an intermediate state must be considered. A minimum switching time exists, this may vary depending on the type of inverter in use. Thus the largest voltage which can be generated in one cycle becomes

$$|\bar{V}|_{Max} = \frac{2}{3}V_{DC} \frac{T_z - 2T_{Min}}{T_z} \quad (\text{Eq. 5-12})$$

B. SIMULATION

Simulation of a six-switch inverter controlled by space vector modulation was accomplished using Advanced Continuous Simulation Language (ACSL). An initial open-loop simulation without voltage or current feedback shows the feasibility of the

control scheme. The circuit used in the simulation is shown in Figure 5-8. The program (listed in Appendix E) implements the LC output filter and the resistive load shown in the circuit diagram. Values used in the simulation are reported in Table 5-3, and the flowchart for the simulation is shown in Figure 5-9.

Table 5-3 - Simulation Parameters

V_{DC}	500V
L_f	10mH
C_f	1mF
R_{load}	25 Ohms
f_{switch}	6kHz
V_{l-n}	140V
f_{out}	60Hz

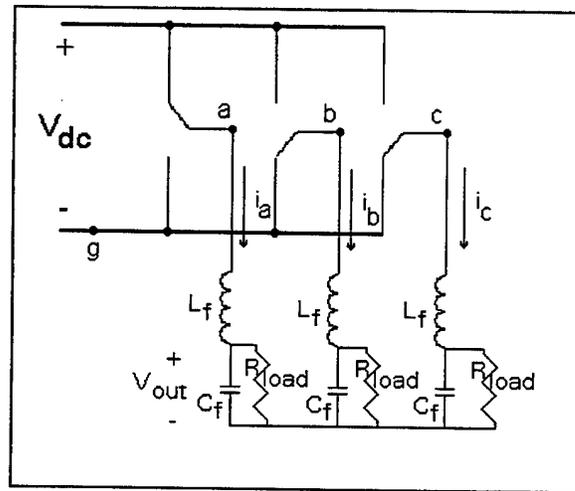


Figure 5-8 - Circuit Diagram for Simulation

The initial section of the ACSL code sets up the integration algorithm and constants for use by the rest of the program. The main body of the program, the derivative section, begins by generating a desired three-phase voltage waveform and converts it into the stationary q-d-0 frame. Next the sector of operation is determined from the q-d-0 voltage values. Switching times are calculated using angles from the

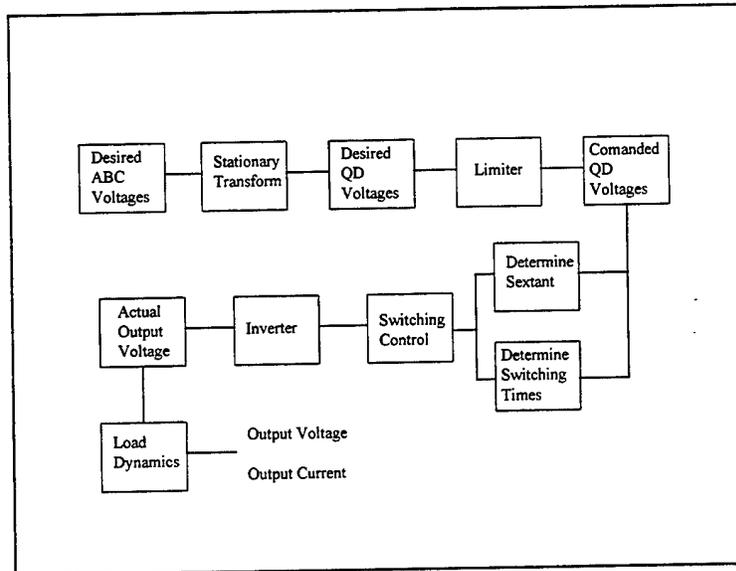


Figure 5-9 - Simulation Flowchart

q-d-0 values, a maximum limit is placed on the switching times by using an if statement to limit the magnitude of \bar{V} (V_{bar}) to V_{DC} . A minimum switching time is incorporated by the use of a bound statement in the generation of the switching times. Schedule statements perform the switching by calling appropriate subroutines located in discrete blocks at the end of the derivative section. These subroutines generate the appropriate output voltages for the switch configuration. The remainder of the derivative section transforms the output voltages into q-d-0 quantities, calculates state variables, and then transforms quantities back into the a-b-c reference frame.

Figure 5-10 shows the output voltage across a single phase of the load resistance and the current output from a single phase of the converter. As expected the current and voltage are out of phase and are both sinusoidal.

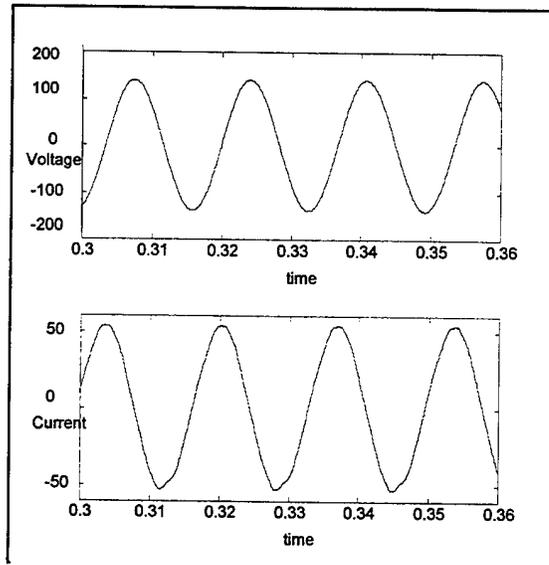


Figure 5-10 - Output Voltage and Current - Phase A

The voltage pattern for two complete switching cycles is shown in Figure 5-11.

As expected each phase changes polarity only once per cycle.

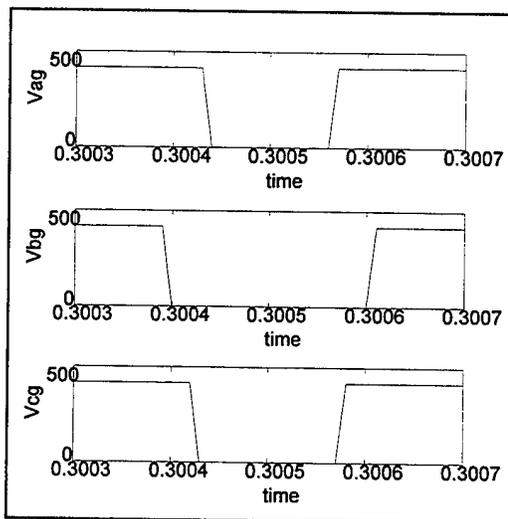


Figure 5-11 - Voltage Pattern - Sector Six

C. ADVANTAGES OF SPACE VECTOR CONTROL

With the advent of the microprocessor Space Vector Control (SVC) has become a very practical control method to implement. A simple look-up table based on the

magnitude, phase angle and sector location of a reference phasor can be used by a microprocessor to generate an SVC switching sequence. Traditional sine-triangle modulation, where a sinewave is superimposed on a high-frequency triangle wave, is much simpler to implement using analog methods than SVC. As most modern controllers are microprocessor based, in which case both sine-triangle and SVC are implemented using look-up tables, this analog disadvantage of SVC is lost.

To compare the maximum output amplitudes possible with sine-triangle and SVC the modulation indices must be studied. The modulation index for sine-triangle modulation, m_{ST} , is defined as the fraction of possible maximum pulse width. The line-to-neutral voltage for sine-triangle modulation in terms of the modulation index is given as:

$$V_{l-n} = m_{ST} \frac{V_{DC}}{2} \quad (\text{Eq. 5-13})$$

For SVC the modulation index, m_{SVC} , can be obtained by referring to Figure 5-6 as:

$$V_{l-n} = m_{SVC} \frac{2}{3} V_{DC} \quad (\text{Eq. 5-14})$$

In sine-triangle modulation when the modulation index becomes larger than one the overmodulation region is entered. This is normally undesirable since the output waveform becomes more distorted and lower order harmonics are generated.

Comparing Equations 5-13 and 5-14, a relationship between m_{ST} and m_{SVC} can be uncovered.

$$m_{ST} = \frac{4}{3} m_{SVC} \quad (\text{Eq. 5-15})$$

Further investigation shows that the largest line-to-line voltage possible without distortion for SVC is the DC source voltage V_{DC} . Using Equation 5-14 this gives the maximum modulation index for nondistorted waveform from SVC as:

$$V_{l-l\max} = V_{DC} = \sqrt{3}V_{l-n} = \sqrt{3}m_{svc} \frac{2}{3}V_{DC}$$

$$m_{svc} = \frac{\sqrt{3}}{2}. \quad (\text{Eq. 5-16})$$

Relating this back to sine-triangle modulation gives a modulation index of

$$m_{ST} = \frac{4}{3}m_{SVC} = \frac{4}{3} \frac{\sqrt{3}}{2} = \frac{2}{\sqrt{3}} = 1.155. \quad (\text{Eq. 5-17})$$

Comparing Equations 5-16 and 5-17 it can be seen that the peak amplitude non-distorted waveform which can be generated by SVC is approximately 15% higher than the maximum sine-triangle generated waveform.

When comparing the switching frequency of individual devices using SVC with that of sine-triangle modulation, it is noted that for one cycle of SVC each of the three legs of a six-switch converter change state once. So each switch is operated once. However for sine-triangle modulation each leg of the converter changes state twice during one cycle, so each switch is operated twice. Therefore when comparing waveforms generated by each of the modulation techniques this relationship, Equation 5-18, must be taken into account.

$$f_{\text{switch sine-triangle}} = \frac{1}{2} f_{\text{switch SVC}} \quad (\text{Eq. 5-18})$$

The previous chapters have dealt entirely with circuit description and system simulation. It is desired to test the previous findings on an actual circuit model. This will validate the findings and give greater confidence to the simulation results. The next chapter focuses on comparing simulated and actual circuit performance under various conditions.

VI. IMPLEMENTATION AND TESTING OF CONTROL ALGORITHMS

In order to test the control algorithms a hard-switched inverter was constructed using lab components. Control algorithms were realized with a real-time interface system consisting of a 486 computer and a Digital Signal Processor (DSP). This system allowed the control algorithm to be programmed in SIMULINK, automatically translated into C-code and then downloaded into the DSP. This chapter includes a brief description of the system used for testing, a discussion of the process of implementing control schemes, a presentation of test results, and a correlation of the test results with theory.

A. d-SPACE SYSTEM DESCRIPTION

The dSPACE (digital signal processing and control engineering) system is a technology which allows for real-time processing, analysis and control of digital signals. The specific hardware used is the dSPACE-DS1102 controller board, which is built around a TMS320C31 floating point DSP. The DS1102 contains two DSP's. The first is the main processor, a TMS320C31, which executes the main user application. The second is the TMS320P14 slave-DSP used for many different digital I/O functions.[18] SIMULINK is normally used to generate the main user application. However, for the DSP to be able to read the program it must be in C code. To solve this problem the system incorporates an automatic C code generator which converts the MATLAB code generated from SIMULINK into C and downloads it into the main processor. Figure 6-1 illustrates a flowchart for the dSPACE system.

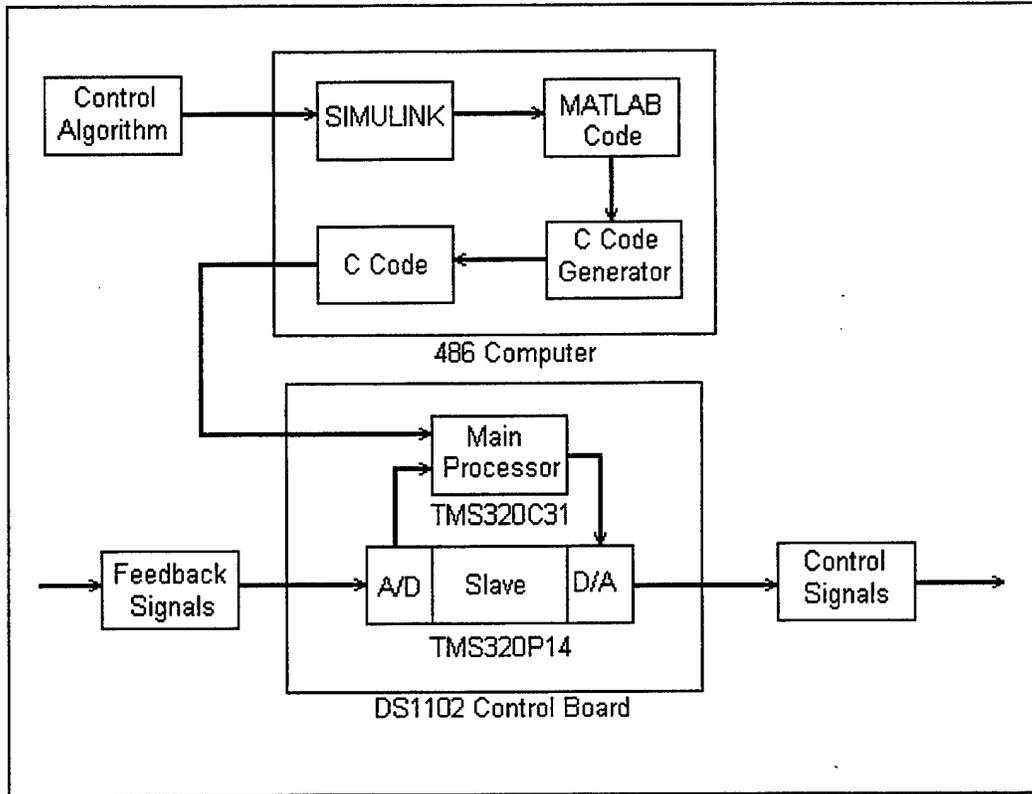


Figure 6-1 - dSPACE System Flowchart

B. SYSTEM USED FOR TESTING

A hard-switched inverter was constructed using a Transistor Voltage Source Inverter manufactured by INVERPOWER Controls Ltd. It consists of six transistor/diode pairs arranged for use in three-phase applications as illustrated in Figure 6-2. Darlingon power transistors are used for the switches. Gating signals for the transistors are supplied by the output of the d-SPACE board, which is passed through a pulse amplifier module (also built by INVERPOWER) as the d-SPACE output is not appropriate to directly drive the six transistors.

Source power for the circuit was provided by a three-phase rectifier connected to a large capacitor bank (a total of 30mF). This provided a stable DC voltage. A varic was

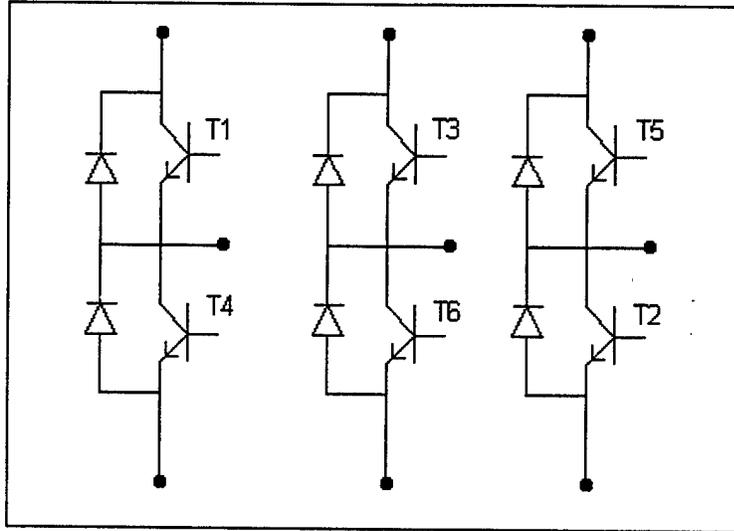


Figure 6-2 - Inverter Arrangement

connected between the three-phase source and the rectifier. This arrangement allowed the DC voltage to be varied from zero to 220 volts.

A three-phase RL-load was built with standard laboratory equipment. The resistor banks used are also manufactured by INVERPOWER and consist of six $116 \Omega/500$ Watt resistors which can be easily arranged in series or parallel as required. The inductors used are 43.5 mH/10 Amp reactors, built by INVERPOWER, and have taps at 5% increments from zero to full inductance. The load used for testing was arranged as a three-phase Y-connected load with an open neutral. Hall effect sensors were used to provide current feedback. These sensors provide an output current which is 1/1000 th of the measured current. By using a load resistor this current was converted to a voltage signal, which is more easily handled by the dSPACE system. The hall effect sensors require an external grounded voltage supply. This fact must be considered when connecting to the feedback lines to avoid ground loops.

C. SIMULINK IMPLEMENTATION OF CONTROL ALGORITHM

The stationary reference frame current control algorithm discussed in Chapter IV was programmed in SIMULINK. Figure 6-3 shows the block diagram for the code.

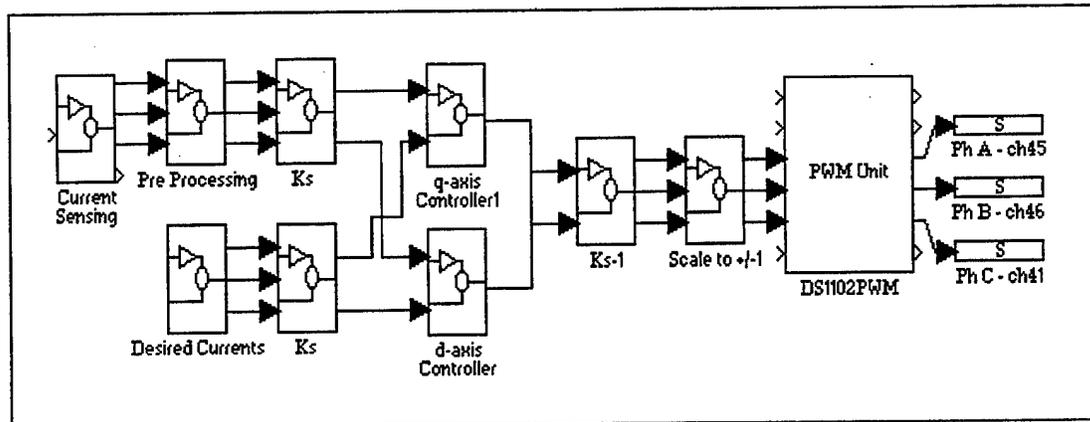


Figure 6-3 - SIMULINK Flowchart for Stationary Current Controller

The Current Sensing block contains the A/D conversion of the feedback signals from the Hall Effect sensors. Signals from -10 to 10 volts are accepted by the A/D converter, outside this range the unit saturates. These -10 to 10 volt analog values are scaled to a digital signal in the range -1 to 1. As stated before care must be taken to ensure that a ground loop does not exist between the feedback signals and the power for the DS1102 board. To protect the A/D converter from overvoltage two 10 volt zener diodes were used to limit the feedback signal to ± 10 volts. The PreProcessing block scales the current signals so that the digital signal matches the analog value of current seen by the circuit and removes any bias in the signal. Digital filtering can be performed in this block, if required, by using any one of the built-in SIMULINK filters. One must be careful when introducing a filter in that the filter will introduce an amplitude scale and phase shift. For this testing a filter was not necessary. In the Desired Currents block the

desired sinusoidal a-b-c phase currents are generated and a ramp-up signal is generated for use in start-up. The ramp causes a linear increase in the desired signal from 0 to 100%. For testing, the duration of the ramp-up was 10 seconds. The Ks and Ks-1 blocks perform the algebraic transformation into and from the stationary reference frame. Both the q- and d-axis controller blocks contain proportional-integral controllers. Limited integrators are used to prevent wind-up. The Scale to ± 1 block limits the input to the PWM to ± 1 and also scales the incoming signal so that a maximum commanded value corresponds to +1 input to the PWM block. The PWM unit requires a ± 1 signal. A -1 corresponds to a duty cycle of zero and +1 to a duty cycle of 100%. The unit uses the slave DSP chip to generate a modulating signal with a duty cycle specified by the input. The frequency of this modulating signal can be set to one of four values; 1.5kHz, 6kHz, 25kHz or 100kHz. The output is directed through channels 45, 46 and 41. These channels are electrical connections within the DS1102 board. By use of a ribbon cable connected to the board these signals are brought to an external interface where they can be used by the converter. At this point the possibility of a ground loop between the external circuit and the DS1102 board exists also. Some type of isolation amplifier is normally used to protect the DSP board. The details of each block are included in Appendix F.

Once the modulation signals were passed out of the DS1102 board a time delay was introduced to allow one switch to turn off before the opposite switch was turned on. This delay is necessary to prevent both switches being closed simultaneously causing a short across the source. This was implemented in hardware using dual input AND and

NOR gates (with an RC network on one of the inputs) and LM311 comparators. The value of the time delay was approximately $8\mu\text{sec}$, this seemed to work well with the INVERPOWER switches.

D. TESTING OF STATIONARY REFERENCE FRAME CONTROLLER

Values used for testing are shown in Table 6-1. The value of switching frequency was selected based upon the limitations of the switches used in the INVERPOWER unit.

Table 6-1 - Testing Parameters

L_f	42.5mH
R_{load}	29 Ohms
K_i	30
K_p	2
ω_e	377 rad/sec
f_{switch}	1.5 kHz
V_{DC}	100 V

From Chapter IV, it is known that a steady-state error will exist between the commanded and actual currents due to the control being performed in the stationary reference frame. To predict the error a simulation using the ACSL code for the current controller was performed. Figure 6-4 shows one of the phase currents from the simulation with a commanded current amplitude of one amp peak (two amps peak-to-peak).

As can be seen in Figure 6-4 a substantial steady-state error exists. A phase current plot from the hardware, Figure 6-5, verifies this error.

Figures 6-4 and 6-5 show a very good correlation. The simulation shows a current value of ± 0.5 Amps and the circuit produced a value of about ± 0.55 Amps. The

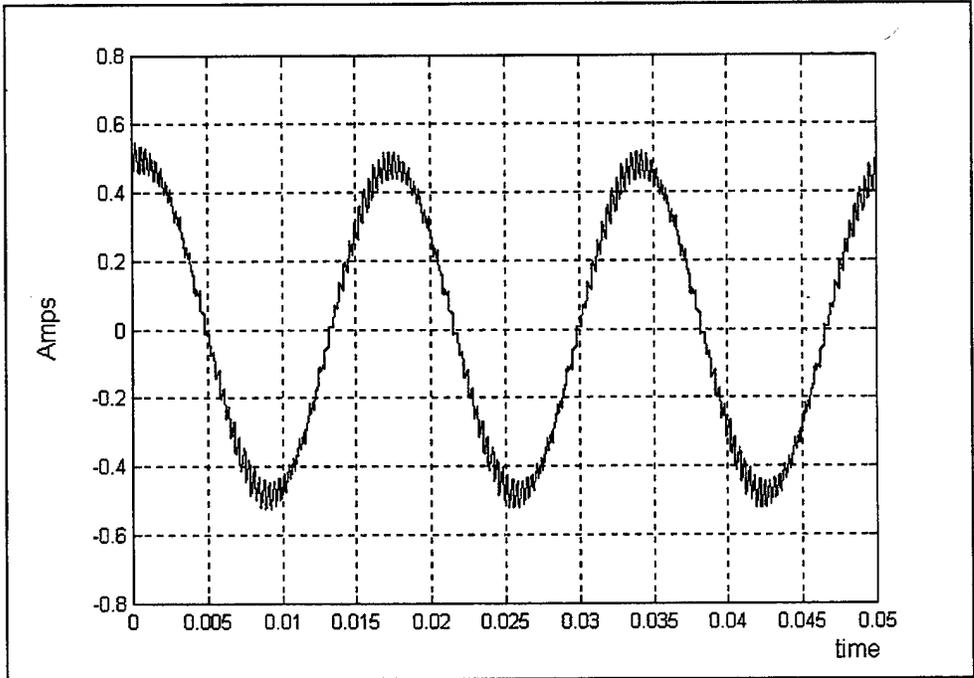


Figure 6-4 - ACSL Output for 1 Amp Commanded Current

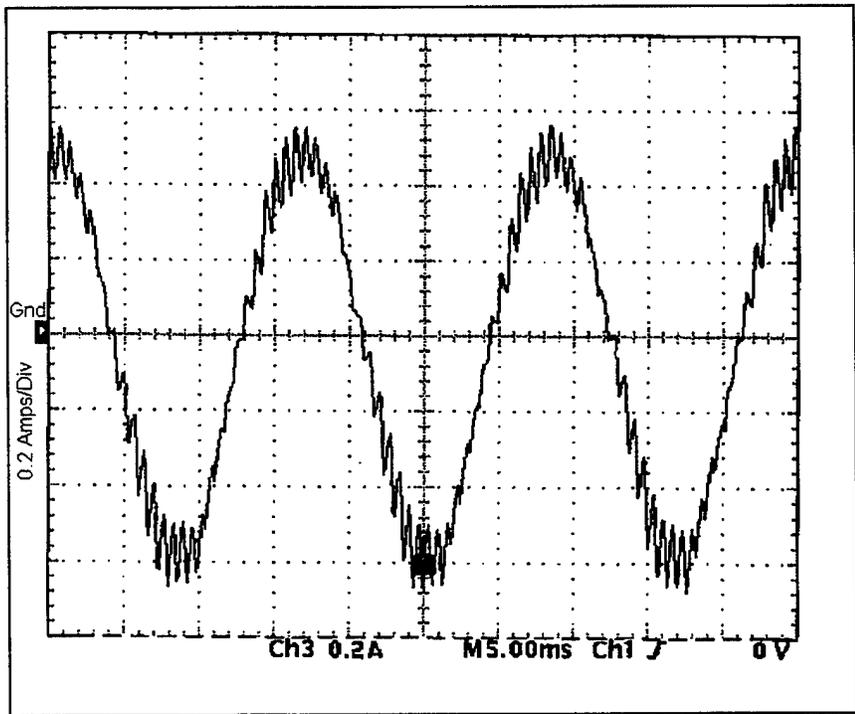


Figure 6-5 - Circuit Output for 1 Amp Commanded Current

difference in peak magnitudes can be attributed to the delays in the sensing circuitry and other non-idealities which were not modeled by the ACSL simulation. The 1.5 kHz harmonic superimposed on the 60 Hz fundamental is attributed to the switching and is observed on both waveforms.

A commanded current amplitude of 1 amp corresponds to synchronous reference frame commanded values of $i_{qs}^{e*} = 1.0$ and $i_{ds}^{e*} = 0.0$. Equations 4-30 through 4-32 (repeated here as Equations 6-1 through 6-3) can be used to predict the steady-state error.

$$\mathbf{i}_{qds}^e = \mathbf{A}\mathbf{i}_{qds}^{e*} \quad (\text{Eq. 6-1})$$

$$a_{11} = a_{22} = \frac{K'_p(R_{Load} + K'_p) + \frac{K'_i}{\omega_e} \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)}{\left(R_{Load} + K'_p \right)^2 + \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)^2} \quad (\text{Eq. 6-2})$$

$$a_{12} = -a_{21} = \frac{K'_p \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right) - \frac{K'_i}{\omega_e} (R_{Load} + K'_p)}{\left(R_{Load} + K'_p \right)^2 + \left(\frac{K'_i}{\omega_e} - \omega_e L_f \right)^2} \quad (\text{Eq. 6-3})$$

The values K'_p and K'_i in Equations 6-2 and 6-3 include the forward path gains of the system including the PWM gain. For the controller as implemented the forward path gain is 1/3.5, since this was the value used in the scale to ± 1 block, and the PWM gain is the DC voltage divided by two. This gives values of 28.6 and 428.6 for K'_p and K'_i , respectively. The steady-state values predicted by Equation 6-1 are found to be $i_{qs}^e = 0.4604$ and $i_{ds}^e = 0.1018$. These currents can be used directly to calculate the stator current phasor as $0.472 \angle 12.5^\circ$. Thus, the actual current, as predicted by Equations 6-1

through 6-3, will be 47% of the magnitude of the commanded current and will be out of phase with the commanded current by 12.5 degrees.

The dSPACE system has a built in program called TRACE31W which allows for monitoring of internal control signals. Using the TRACE31W program the values of commanded current and sensed current were captured and shown in Figure 6-6. The measured current is the signal at the output of the sensing block. The important information from the plot is that a phase difference of about 10 degrees exists between the desired and sensed current. The presence of this phase offset corresponds to the value of 12.5 degrees calculated previously, confirming our prediction. The amplitudes of the two signals cannot be compared as the sensed current is measured before any processing. The dc offset in the measured signal is due to the bias of the hall effect sensor.

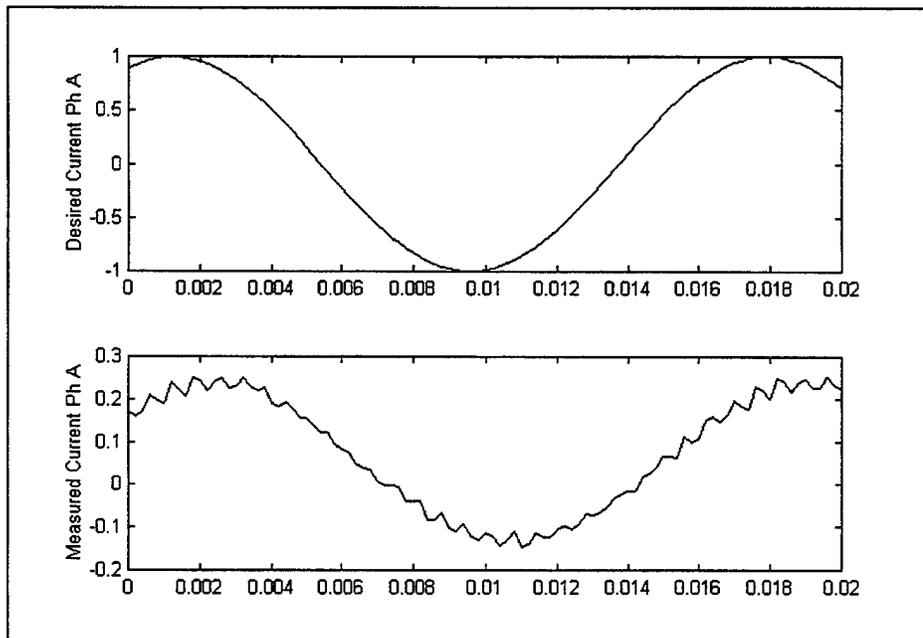


Figure 6-6 - Desired and Actual Phase Currents

The commanded current was raised to 2 amps and the output from the simulation and circuit were plotted in Figures 6-7 and 6-8 respectively. Again a steady-state error of

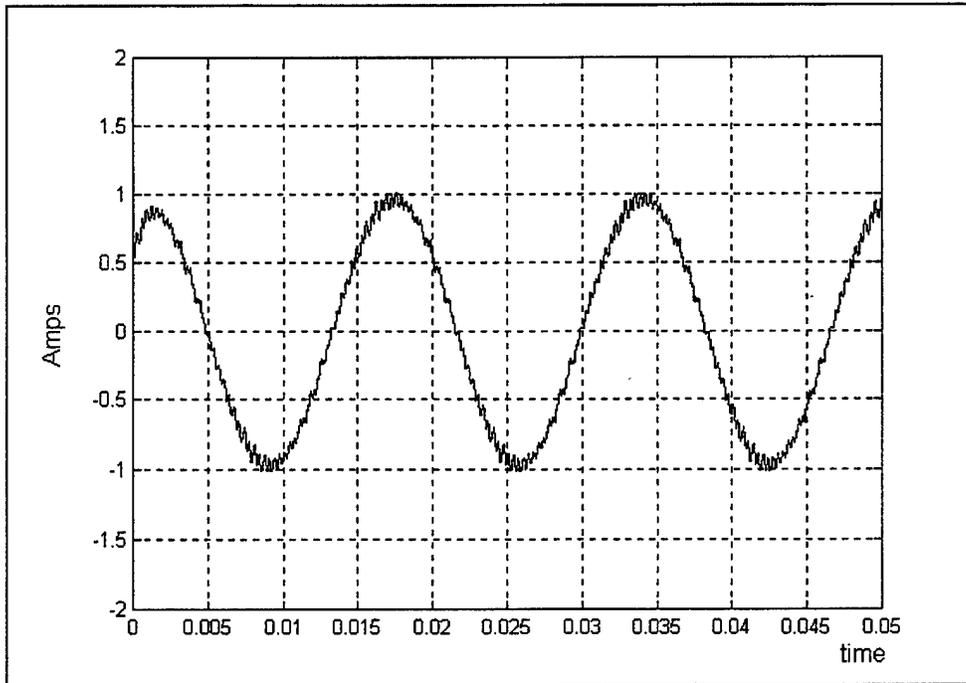


Figure 6-7 - ACSL Output for 2 Amp Commanded Current

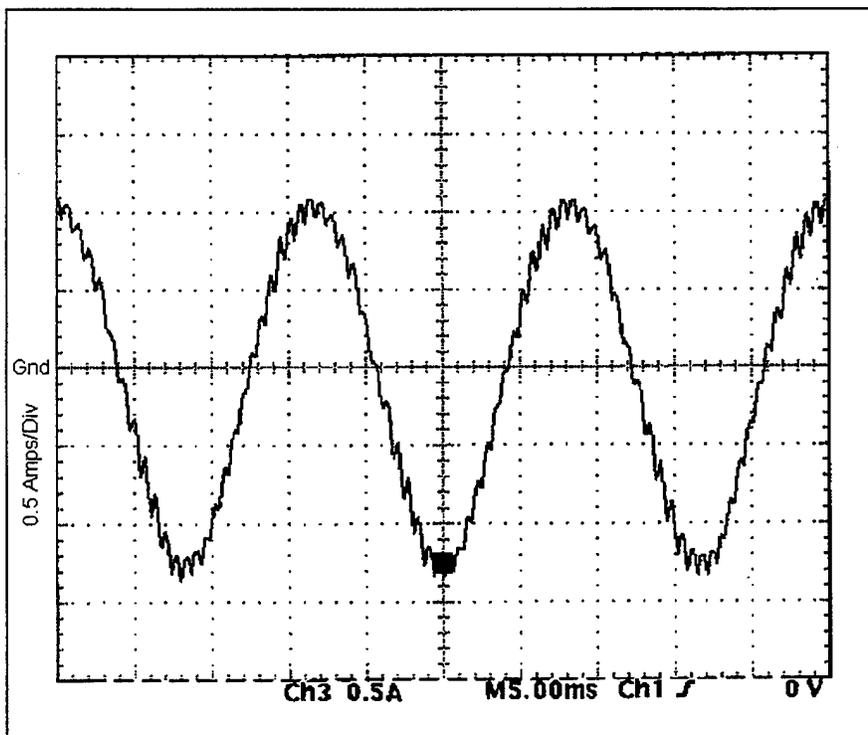


Figure 6-8 - Circuit Output for 2 Amp Commanded Current

approximately 50% exists. A 1.5 kHz switching harmonic signal can be seen on each of the plots.

E. TESTING OF SYNCHRONOUS REFERENCE FRAME CONTROLLER

The synchronous reference frame controller was then implemented in SIMULINK and merged into the dSPACE system. Values used for testing the synchronous controller are the same as for the stationary controller except that the DC source voltage was raised to 150V to maintain operation in the linear range. The SIMULINK block diagram for the controller is shown in Figure 6-9. The details of the blocks are included in Appendix F.

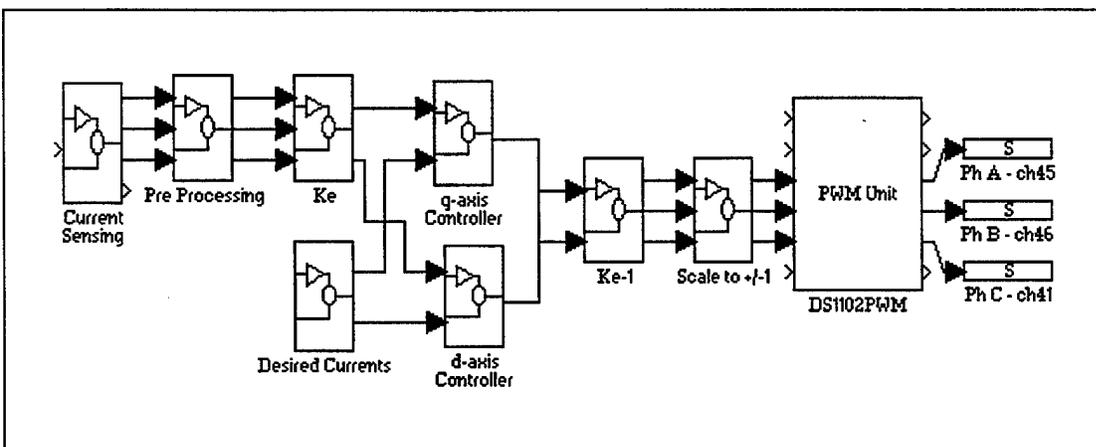


Figure 6-9 - SIMULINK Flowchart for Synchronous Current Controller

It was shown in Chapter 4 that a controller in the synchronous reference frame can achieve a zero steady-state error. An ACSL simulation was performed with the parameters used in testing. The output of the ACSL code (Figure 6-10) shows a current waveform of one amp peak value for a one amp commanded current and thus a zero steady-state error. Actual circuit output for one amp commanded current (Figure 6-11) is shown to be in perfect agreement with the ACSL simulation. Figures 6-12 and 6-13 illustrate the ACSL and circuit output for a commanded current of two amps.

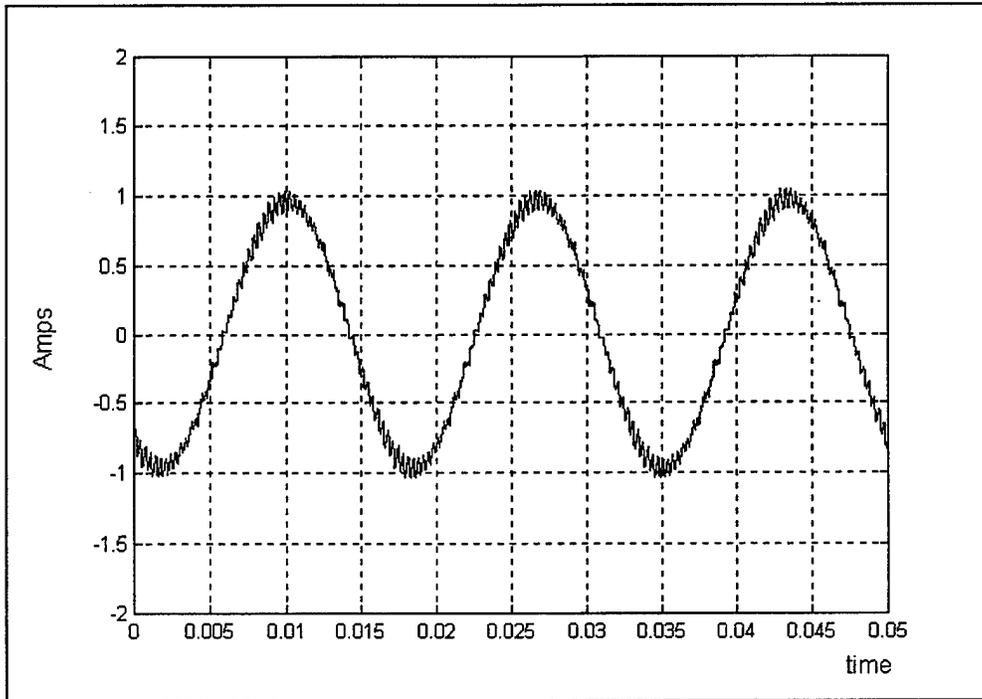


Figure 6-10 - ACSL Output for 1 Amp Commanded Current

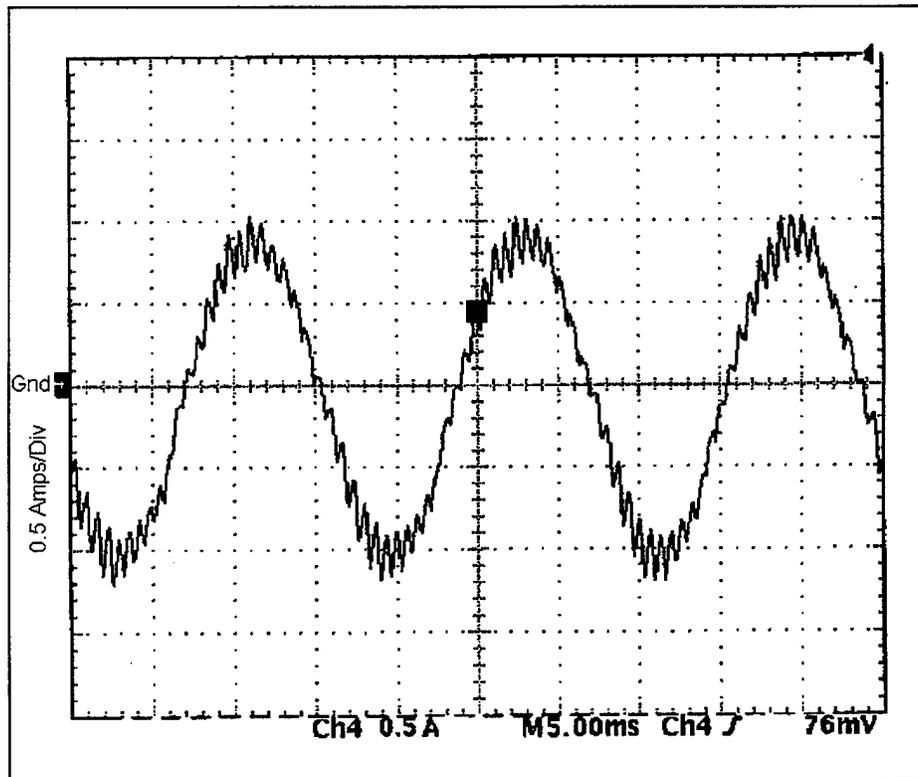


Figure 6-11 - Circuit Output for 1 Amp Commanded Current

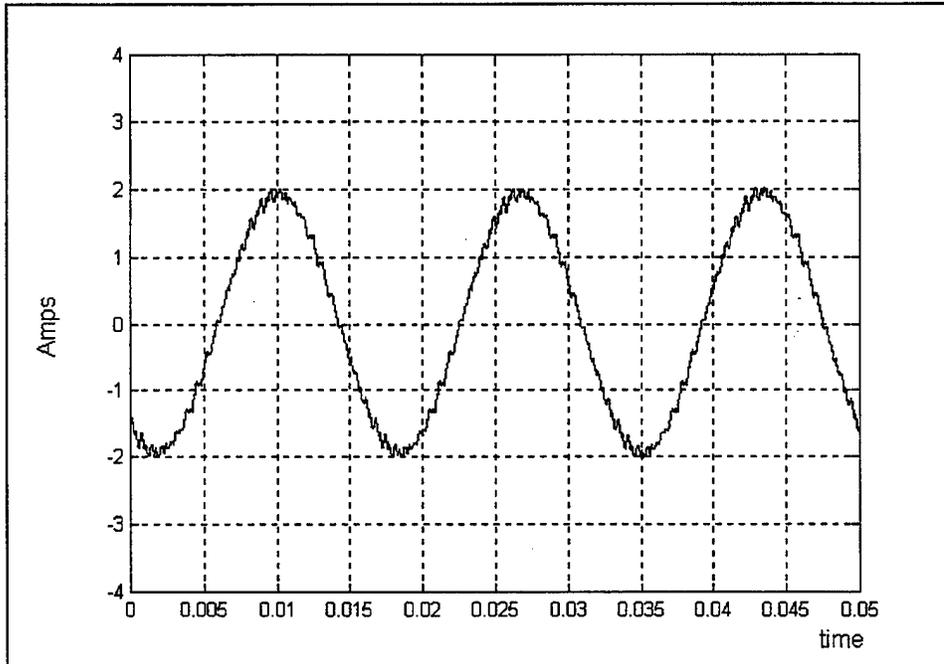


Figure 6-12 - ACSL Output for 2 Amps Commanded Current

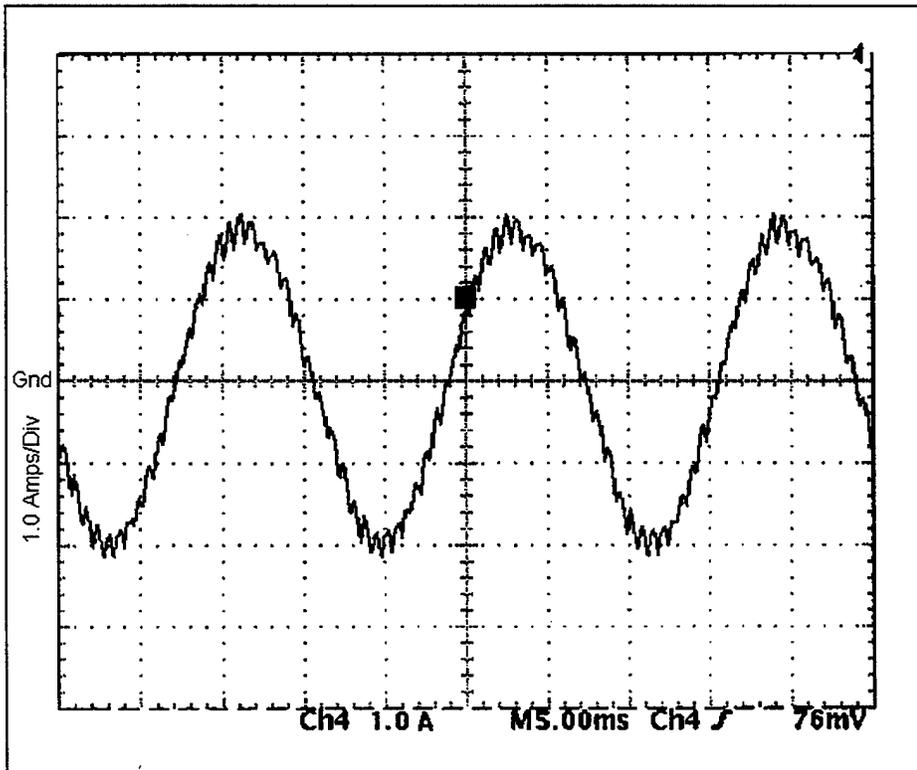


Figure 6-13 - Circuit Output for 2 Amps Commanded Current

In comparing the stationary and synchronous reference frame controllers it is obvious that the synchronous controller performs much better with regards to steady-state error. Although the steady-state error of the stationary controller can be calculated, and therefore corrected for, the error varies with the load. Unless the load is known precisely the correction may not be accurate. For this reason the synchronous controller is the preferred choice.

One drawback of the synchronous controller is that it is more computationally intensive than the stationary controller. When compiling the control algorithm and generating the C-code to be used by the DSP chip a time step and integration algorithm must be specified. These are specified as in the SIMULINK environment. The dSPACE system has a limit on how many calculations can be performed per second. As the time step specified becomes small this limits the number of computations which can occur during each step. Complicated algorithms require more computations than simple ones. So as the algorithms become more involved the time step at which they can be run becomes larger. When implementing these two control algorithms in the dSPACE using the Euler algorithm it was found that the minimum time step for the stationary algorithm was .0002 seconds corresponding to a frequency of 5 kHz, and for the synchronous algorithm was .0003 sec corresponding to 3.33 kHz. This difference was not significant for the test setup used. In addition, if other microprocessor resources are used to implement these algorithms they may be much faster and capable of minimizing the implementation issues between the two current regulator algorithms.

To compare the dynamic responses of the controllers a step change in the commanded current from one to two amps was performed. Using the TRACE31W program the commanded and actual q-axis synchronous current were captured. Figures 6-14 and 6-15 show the stationary and synchronous controller responses. The “noisy” signal in the plots represents the actual q-axis values and the other signal is the commanded values. The response times of both controllers are comparable; however the stationary controller has a large steady-state error as shown previously. Overall the synchronous controller outperformed the stationary controller.

The measured waveforms in Figures 6-14 and 6-15 appear jagged. This is a function of the noise present in the signals and the limitations of the TRACE31W program.

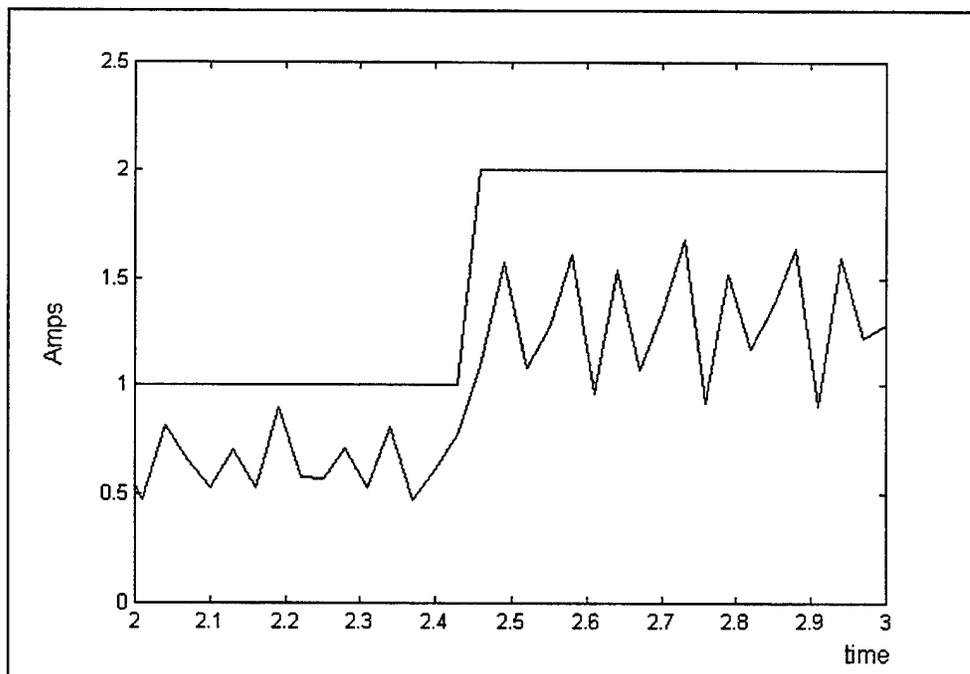


Figure 6-14 - Stationary Controller Step Response

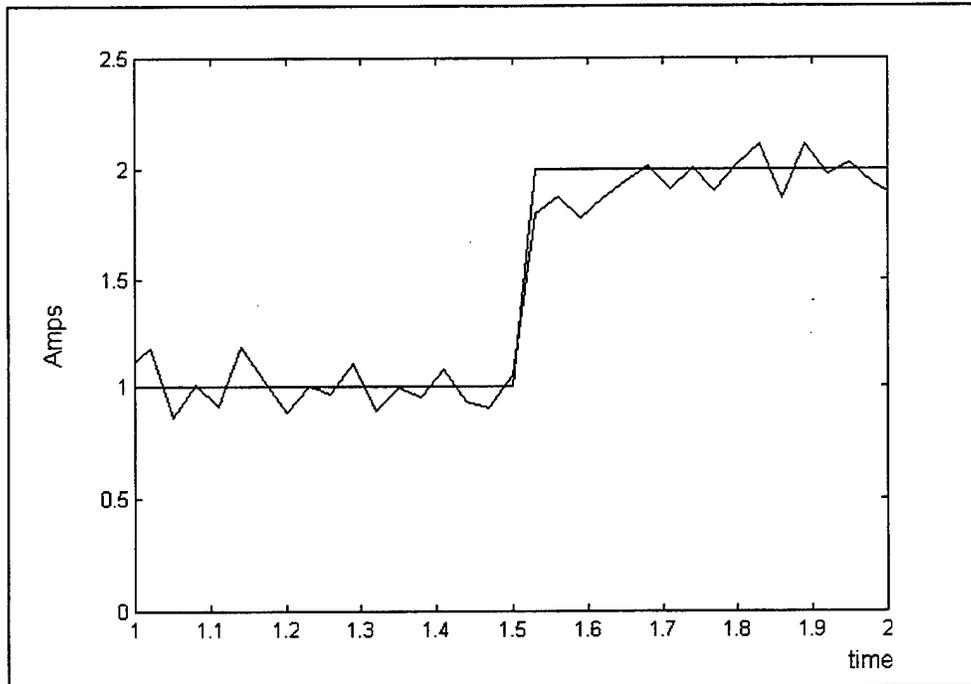


Figure 6-15 - Synchronous Controller Step Response

F. SPACE VECTOR CONTROL IMPLEMENTATION

The Space Vector Control modulation technique was not tested, however this section includes a brief discussion on how SVC could be implemented using the dSPACE system.

A SVC-based control algorithm with feedback could be implemented in SIMULINK. The same basic set-up of sensing and output channels which were used to test the current regulation algorithms could be utilized in a SVC program. The PWM unit would be replaced by a Digital to Analog converter, as SVC does not utilize sine-triangle PWM. The basic steps in the algorithm would include generating a desired voltage signal (assuming a voltage regulator is implemented), generating an actual voltage signal in the correct reference frame, comparing the two voltage signals to arrive at a commanded

voltage signal, and finally converting this commanded signal into the desired switching sequence.

The slowest part of the algorithm will be in converting the commanded signal into the desired output. Since none of the slave functions of the DS1102 board can be utilized for this purpose all of the computations must be performed on the master DSP. This will greatly limit the frequency at which a SVC algorithm could be run on dSPACE.

An algorithm based on a look-up table would be faster, but it is not readily implemented using the dSPACE system. If an alternate DSP were available for programming, a reasonably fast algorithm could be produced.

This chapter has undertaken the hardware implementation and testing of various algorithms on a hard-switched converter. The following chapter investigates the operation of an actual ARCP converter.

VII. ARCP PROTOTYPE UNIT

A prototype ARCP converter was constructed by the Applied Research Laboratory / Penn State University (ARL/PSU). This converter was delivered to the Naval Post Graduate School for incorporation into the Power Electronic Building Block Network Evaluation Simulator (PEBBNES) which is currently under construction. Funding for both the ARL/PSU converter and the PEBBNES is provided from the Naval Surface Warfare Center. This chapter discusses the prototype ARCP unit parameters, operational characteristics, the proposed controller to be used with the prototype ARCP unit, and recommendations for future ARCP evolution.

A. PHYSICAL DESCRIPTION OF UNIT

The converter consists of a User Interface (UI) board and three identical Pole boards (basically a leg of the inverter as described in Chapter II) mounted on a heat sink/base plate made of 3/8" aluminum. Overall dimensions of the unit are 14" wide, 24" deep and approximately 2 1/2" high[19]. Restrictions were placed on the size to allow incorporation into the PEBBNES. Complete specifications for the unit are listed in Reference 19. Figure 7-1 shows a photograph of the entire ARCP prototype unit.

The UI board contains a master control section and an output current detection and feedback section for each of the three phases. A 24 volt DC control voltage is required by the UI board, as well as by each of the Pole boards. Each Pole board requires a DC bus voltage, with a minimum output capacitance of 1100 μ F, for power conversion. Optical signals are required by the Pole boards to drive the main switches, one control

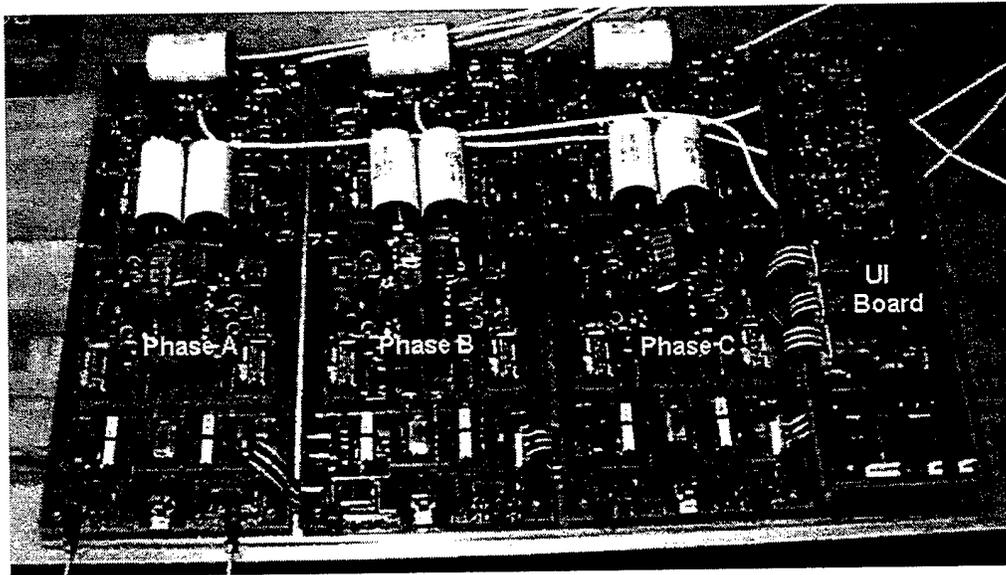


Figure 7-1 - ARCP Prototype Unit

signal for each switch. Figure 7-2 shows a photograph of a single phase of the ARCP including all of the major connections required. The main and auxiliary switches are located below the board, mounted directly onto the heat sink, with the electrical connections on the board.

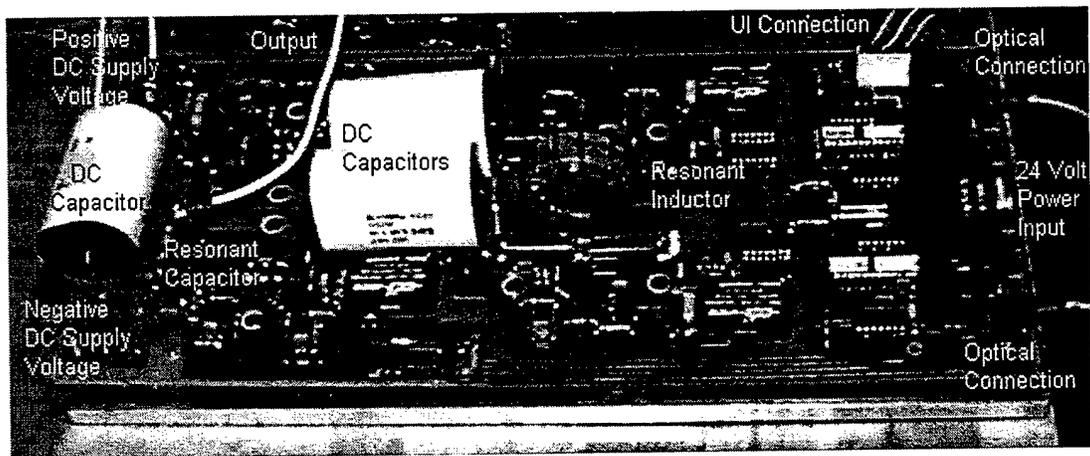


Figure 7-2 - Single Phase of ARCP Prototype

The controller interface is designed to be electrically isolated from the ARCP unit (by use of optical connections) except when the current feedback circuit is connected.

For this reason the current feedback circuit is not grounded to any part of the ARCP unit. Thus, the ground in the current feedback circuit will be in reference to the controller ground.

The main switches used in the prototype unit are IRCPC50U UltraFast IGBT's made by International Rectifier. They have rise and fall times rated at 28 and 45 nsec respectively.[20] With switching times so fast the IGBT's allow for very high frequency operation. The circuitry necessary to turn on and off the main and auxiliary switches is contained entirely on the Pole board. All that is required of the user is to provide 24 volt power and an optical signal to the main switches. The boost current level is set at approximately one amp for no load and automatically increases to approximately 16 amps at full load. The threshold current level is 12 amps.

B. OPERATION

Operation of the prototype ARCP closely mimics the ideal circuit operation presented in Chapter II. One of the main areas of concern is the circuit behavior during commutation between states. Figure 7-3 illustrates the transition from low to high voltage state with positive current, this corresponds to a Case 1 condition (diode conducting) from Chapter II. The top waveform is the current through the auxiliary circuit and the bottom waveform is output voltage of the ARCP measured across the lower main switch.

Figure 7-3 can be compared to the ideal commutation of Figure 2-10. Load current for the conditions shown in Figure 7-3 is approximately one amp, the DC supply voltage is 25 volts.

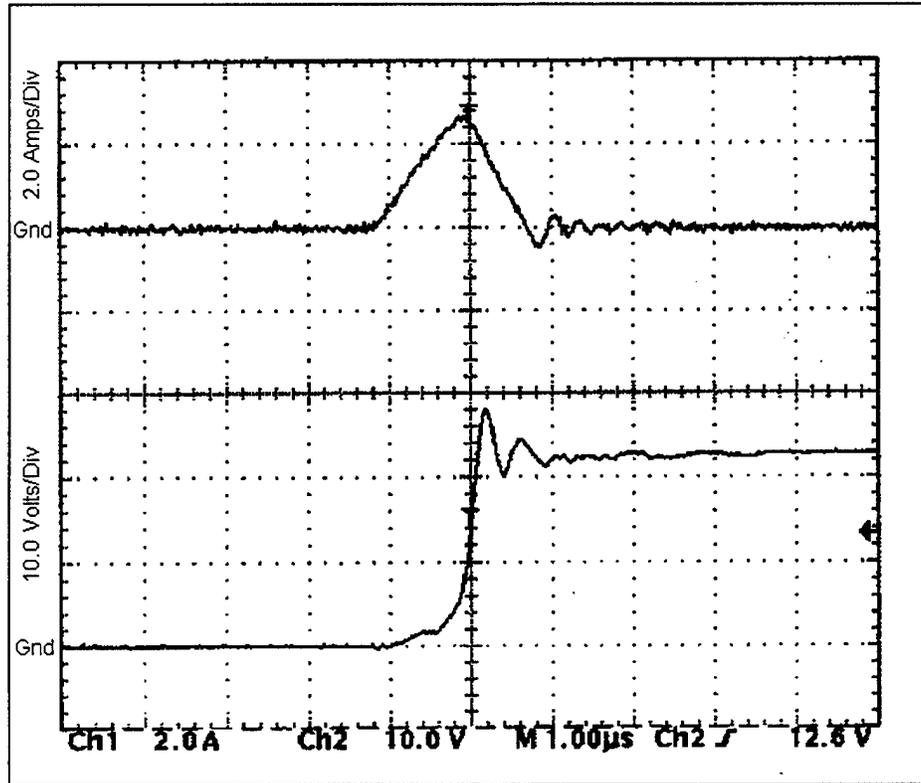


Figure 7-3 - ARCP Commutation from Conducting Diode

Following the trace of the current waveform, as the value reaches about one amp (the load current value) the lower main switch is opened and the circuit begins to resonate. As the current reaches its peak value (2.6 amps) the voltage is approximately at half of the final value. When the voltage reaches 25 volts the upper main IGBT is turned on, at this point the current in the auxiliary circuit is about one amp. This is the same value as the load current, since the load current is being supplied by the auxiliary circuit at this point. As time progresses the upper IGBT picks up the load and the auxiliary current falls to zero, at which point the auxiliary switch is turned off, completing the commutation. The major discrepancies between the real and ideal case is the small amount of ringing seen at the turn-on of the main IGBT and the turn-off of the auxiliary switches.

Commutation with the switch initially conducting is illustrated in Figure 7-4, this corresponds to a Case 2 commutation. A Case 2 commutation can be found by observing the circuit for a transition from upper to lower voltage states with positive load current, referenced out of the converter. In the previous condition the upper switch would be conducting. Load conditions are the same as before, DC voltage 25 volts and load current one amp. The ideal case for the conditions represented in Figure 7-4 is covered in Chapter II, Figure 2-16. Case 3 commutation could be examined by increasing the load current above the threshold level, and monitoring the commutation from a conducting switch.

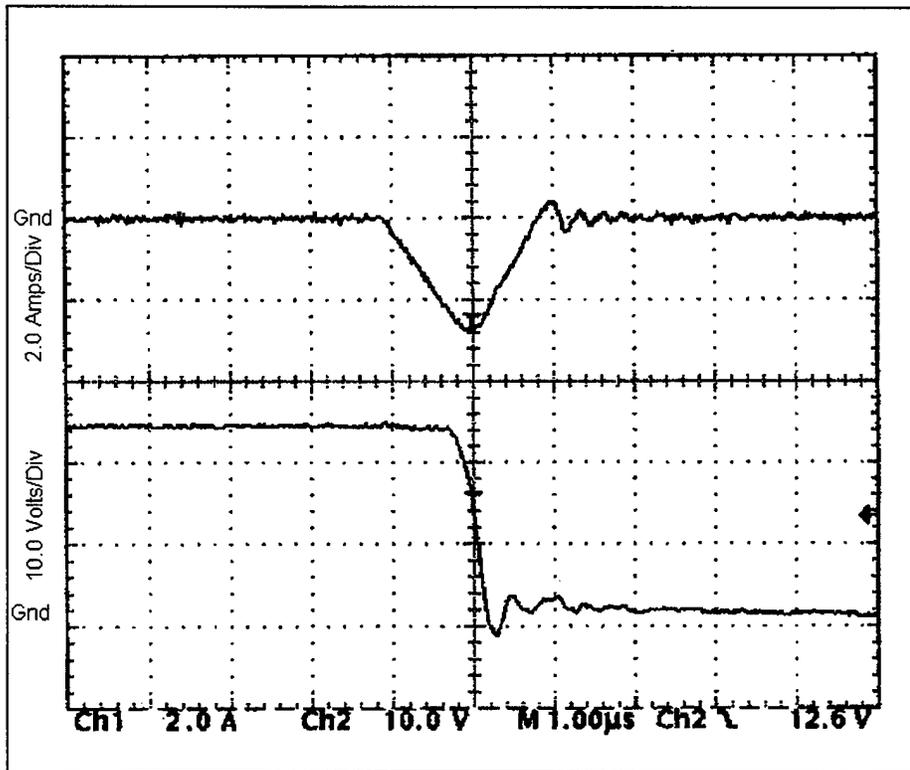


Figure 7-4 - ARCP Commutation from Conducting Switch

Single-phase testing of the unit was performed by utilizing the dSPACE system to generate modulating signals and using Hewlett Packard HFBR-1521 optical transmitters and HFBR-PNS005 fiber optic cable to interface with the ARCP prototype unit. A delay circuit feeding LM311 comparators was used to drive the optical transmitters. The delay circuit was required to achieve a 1 μ sec delay between switching of the main switches (a specification required by the prototype unit.)

Although three-phase testing was not completed, due primarily to delivery delays, extension of the testing to include all three phases is straightforward. In particular, it will consist of building two additional delay circuits identical to the one used for one-phase testing, connecting two additional outputs from the dSPACE system to drive the additional phases, and connecting supply and control power to the additional phases.

The effects on the current waveforms of changing the ARCP switching frequency and of changing the inductance in the RL load may be observed in the following studies. With a switching frequency of 1.5kHz, a DC supply voltage of 50 volts, a resistive load of 16 Ω , and a filter inductance of 11mH, the current, illustrated in Figure 7-5, follows a generally sinusoidal shape, but carries quite a bit of switching harmonics. Increasing the filter inductance to values of 43.5mH and 86mH while maintaining the switching frequency, supply voltage and load resistance constant is illustrated in Figures 7-6 and 7-7. The larger filter values reduce the harmonics of the output voltage, but the amplitude of the voltage is reduced due to the larger impedance seen by the ARCP output.

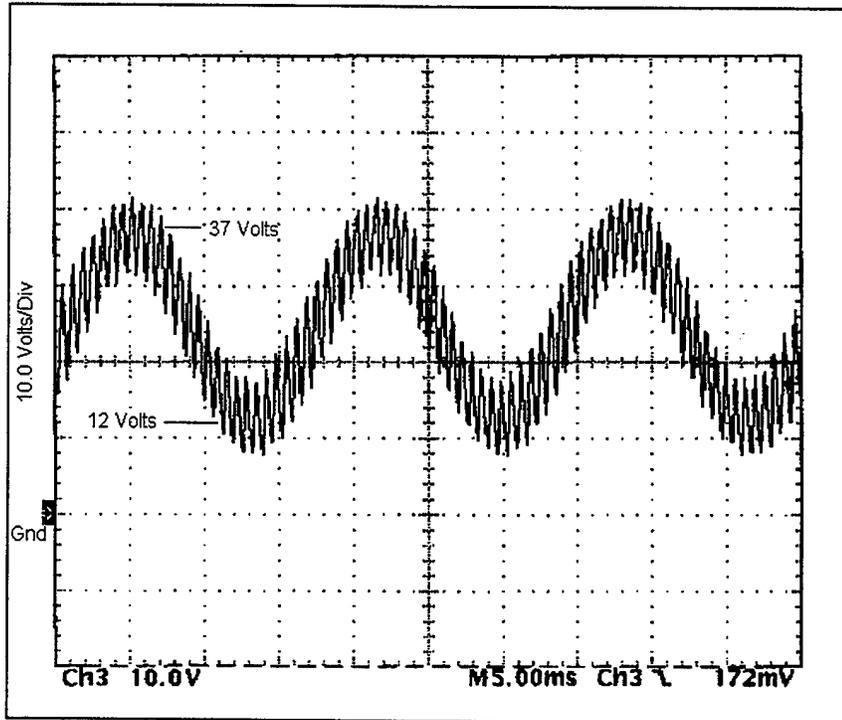


Figure 7-5 - ARCP Open-Loop Resistor Voltage, $f_{\text{switch}}=1.5\text{kHz}$, $L=11\text{mH}$

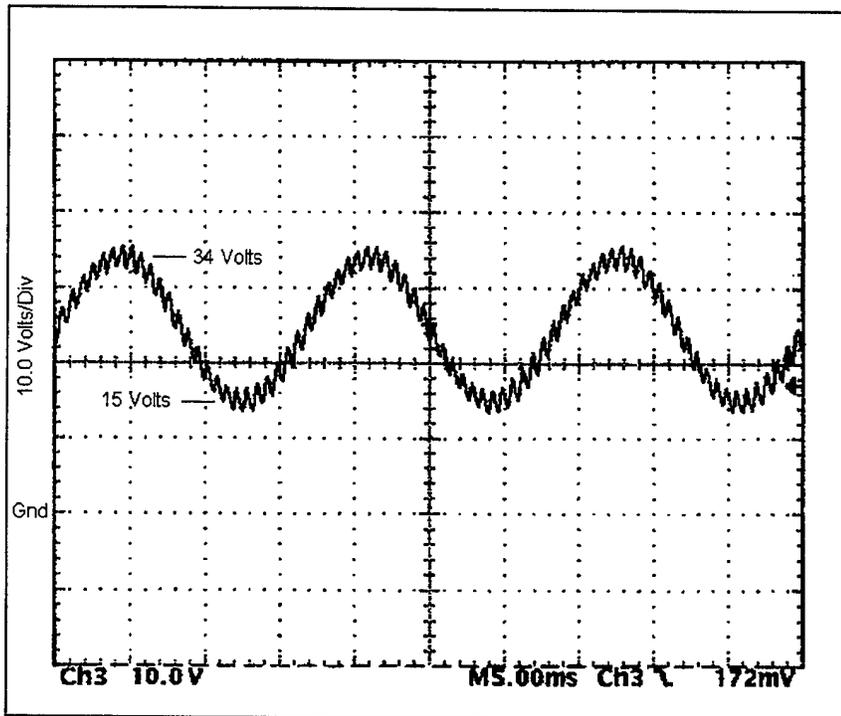


Figure 7-6 - ARCP Open-Loop Resistor Voltage, $f_{\text{switch}}=1.5\text{kHz}$, $L=43.5\text{mH}$

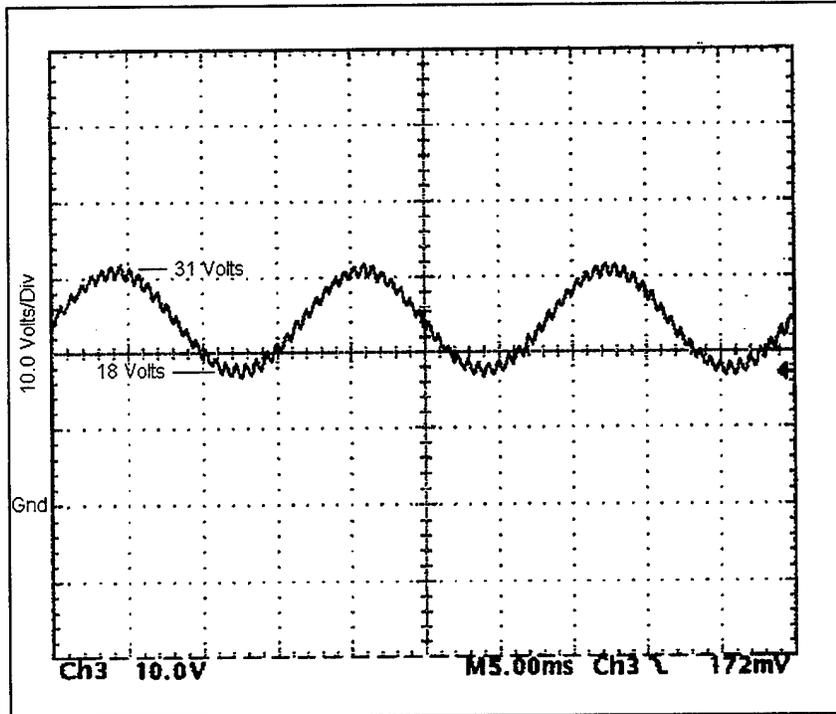


Figure 7-7 - ARCP Open-Loop Resistor Voltage, $f_{\text{switch}}=1.5\text{kHz}$, $L=86\text{mH}$

Figures 7-8 and 7-9 show the effect of increasing the switching frequency to 6kHz and 25kHz, respectively. The DC input voltage is 50 volts and the load resistance is 16Ω , as before. The value of filter inductance is 11mH. Comparing the voltage waveforms with Figure 7-5, it is apparent that the increased switching frequency reduces the harmonic content of the output voltage. However, unlike increasing the filter inductance value, higher switching frequencies do not cause a lower amplitude response.

Figures 7-5 through 7-9 are generated open-loop, closed-loop control algorithms (such as those presented in Chapter IV) can also be used to reduce the distortion seen in the output voltage waveform.

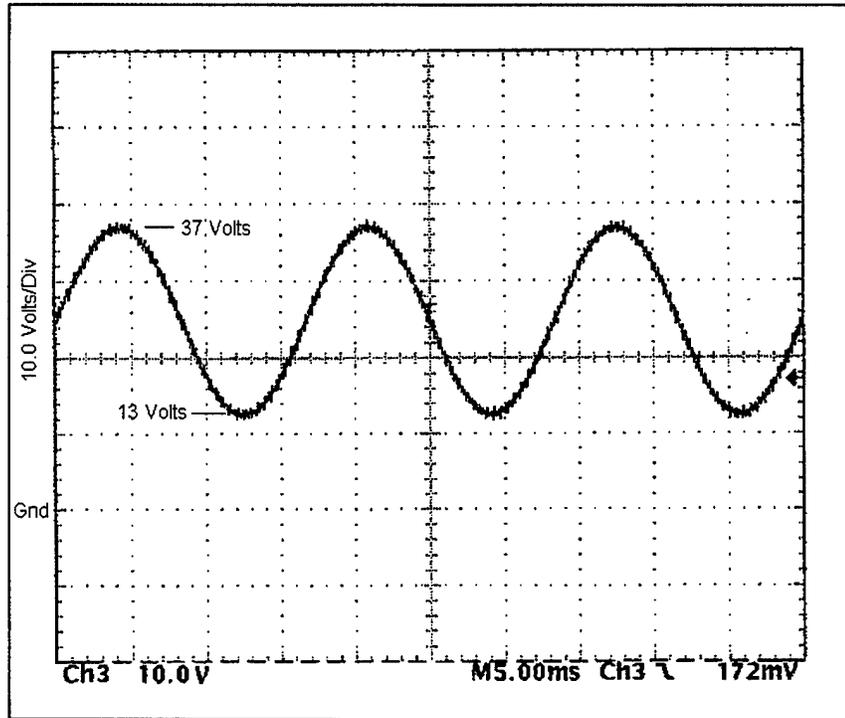


Figure 7-8 - ARCP Open-Loop Resistor Voltage, $f_{\text{switch}}=6\text{kHz}$, $L=11\text{mH}$

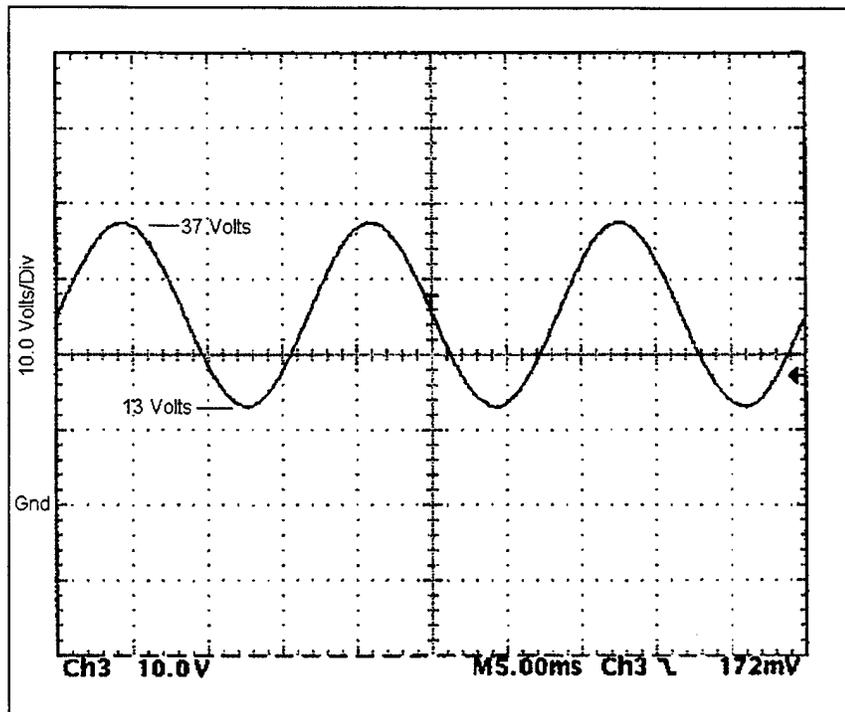


Figure 7-9 - ARCP Open-Loop Resistor Voltage, $f_{\text{switch}}=25\text{kHz}$, $L=11\text{mH}$

C. PROPOSED CONTROLLER FOR ARCP

The Naval Surface Warfare Center has constructed a controller specifically designed to interface with the prototype ARCP unit. These control units are limited in number and were not available for integration with the ARCP hardware unit.

The controllers are built around Texas Instrument's TMS320C30 DSP's. On and off chip RAM are made available for the DSP's to use in controlling the ARCP. The capability to download various control algorithms into the DSP is possible. Currently the process of changing control algorithms involves reprogramming EPROM's, but it is possible through further development to download a new algorithm directly from a computer into the DSP. The controller can become very useful in testing various control algorithms as the capability to change control schemes improves.

Optical output is provided to interface with the ARCP, four optical outputs per phase are provided. This allows the controller to command both the main and auxiliary switches if desired. Electrical connections for use in current feedback, voltage feedback or a combination of current and voltage feedback control schemes are provided. A total of 10 feedback connections are possible. Each controller is capable of receiving feedback from and providing control to an operating three-phase ARCP.

Capability to optically interconnect controllers is provided, this may lead to parallel ARCP operation or connection of the controller to a master control unit. The interconnection of controllers will allow communication between units. Thus, the controllers can be part of an intelligence network built into the power system.

D. RECOMMENDATIONS FOR FUTURE ARCP DEVELOPMENTS

Currently the controller used to drive the ARCP must generate signals for the upper and lower main switches and ensure that the proper delay between signals is achieved. This places an unnecessary burden on the controller. Since the only states which the ARCP can be in is with the upper main switch closed, or the lower main switch closed, or in a transition between the two previous states; only one signal is needed per-phase for the ARCP. With one signal, a logical one could represent the upper switch closed and a logical zero the lower switch closed. The necessary delays could be built into the ARCP unit. This would guarantee a more efficient commutation process for the ARCP since the switching points could be located very close to the optimum times. In addition the timing problem between the ARCP and the controller would be eliminated, and computation time used by the controller to generate two separate signals with delays could be used to perform other tasks. The effect of having one control signal per phase would have the effect of decentralizing the intelligence in the power network, allowing the system to operate more independently and efficiently.

The ability to change the boost and threshold current levels would allow the ARCP's to be 'tuned' to a specific load condition. This should be made an option so that the ARCP could operate in a default level to cover all operational conditions.

A physical improvement which would improve the operability of the ARCP would be to provide optical feedback to the controller vice electrical feedback. Electrical connections typically pick up noise, especially in an high EMI environment such as would be encountered by a power converter. Optical feedback lines would allow the

controller to be moved farther from the ARCP unit away from EMI, and thus improving performance. In addition having no common electrical connections between the controller and the ARCP would eliminate the possibility of a fault at the ARCP affecting the controller, or vice versa.

Providing some type of LC filter at the output of the ARCP would allow for 'clean' power to be provided to all loads. With a high switching frequency, the filter components would not have to be large, and may not be needed at all. However, providing them at the ARCP output may eliminate the need for each load connected to the ARCP to provide its own filtering.

If a filter were connected to the ARCP, additional feedback signals for inductor current and output capacitor voltage should be provided to the controller using optical hardware. This would allow the voltage feedback with inner current control loop algorithm discussed in Chapter IV to be easily implemented.

VIII. CONCLUSIONS

The Auxiliary Resonant Commutated Pole Converter provides a practical architecture for use as a power converter in shipboard applications. The savings provided by increased efficiency outweigh the cost of the added complexity of ARCP converters when compared to hard-switched converters. This savings becomes more pronounced when considering very high-frequency switching converters, since the switching losses of conventional hard-switched converters increase proportionally with switching frequency.

It was shown, through detailed simulation, that for evaluation of control algorithms the ARCP could be modeled as a hard-switched converter. Although losses in a hard switched inverter are higher, the behaviors of the ARCP and hard-switched converter are very similar on a macroscopic scale. This allowed the evaluation and design of control algorithms using simplified hard-switched converter models, reducing the development time.

Several control algorithms were investigated through simulation and reduced-scale circuit modeling. The major conclusion from the study of these algorithms is that when controlling time-varying quantities, such as sinusoidal voltages and currents, the steady-state response of the controllers have a zero error when the control is performed in a reference frame where the controlled quantities are DC values. For the cases studied, the synchronous reference frame provided DC quantities to be controlled. Although slightly more computationally intensive, control in the synchronous reference frame is the

preferred method when dealing with control algorithms implemented using Digital Signal Processors.

In Chapter V a new type of pulse-width-modulation technique, Space Vector Control (SVC), was investigated and simulated. Several advantages of SVC over sine-triangle modulation were pointed out; most significant is the capability of the SVC algorithm to realize a waveform 15% larger than the sine-triangle control without going into overmodulation. No hardware testing was performed using this modulation technique. It is recommended that a study be performed, using either an ARCP or hard-switched converter, which compares traditional sine-triangle modulation with SVC modulation. An efficient implementation of the SVC algorithm may prove to be the one drawback of Space Vector Control which makes it challenging for use in a DSP-based controller.

The ARCP prototype unit discussed in Chapter VII provides an excellent tool for evaluating the ARCP interaction in a shipboard DC power distribution network. With some modifications for power connection and control input this unit can be incorporated into the Power Electronics Building Block Network Evaluation Simulator (PEBBNES) currently under construction at the Naval Postgraduate School.

Recommendations for improvements to the ARCP prototype unit, given in Chapter VII, focus on simplifying the control interface (recommending all fiber optic connections for control and feedback) and freeing computation time on the controller (recommending only one control signal for each phase.)

APPENDIX A. LAPLACE TRANSFORM SOLUTION OF ARCP RESONANT STATE DYNAMICS

This appendix develops the equations for the resonant phase of commutation for the ARCP converter. LaPlace transforms are used to arrive at a solution. Figure A-1 shows the equivalent circuit for the analysis. The filter inductor is considered a constant current source during commutation and the DC capacitors are considered constant voltage sources.

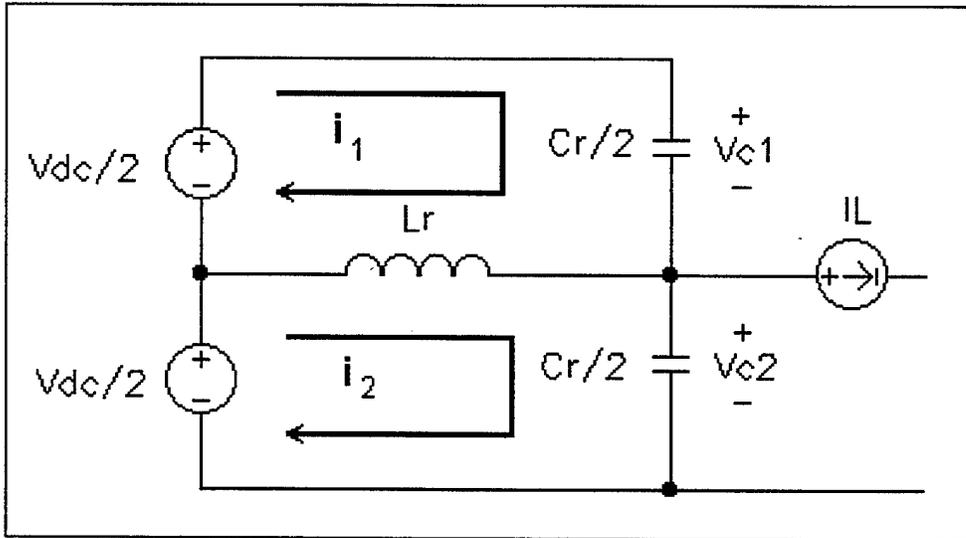


Figure A-1 - Equivalent Circuit during Resonant Phase

Loop Equations

$$\text{Loop 1: } \frac{V_{dc}}{2} - V_{c1} - L_r \left(\frac{di_2}{dt} - \frac{di_1}{dt} \right) = 0 \quad (\text{Eq A-1})$$

$$\text{Loop 2: } \frac{V_{dc}}{2} - L_r \left(\frac{di_1}{dt} - \frac{di_2}{dt} \right) - V_{c2} = 0 \quad (\text{Eq. A-2})$$

Defining

$$i_r = i_2 - i_1 \quad (\text{Eq. A-3})$$

Loop 1 becomes

$$\frac{V_{dc}}{2} - V_{C1} - L_r \frac{di_r}{dt} = 0 \quad (\text{Eq. A-4})$$

Loop 2 becomes

$$\frac{V_{dc}}{2} + L_r \frac{di_r}{dt} - V_{C2} = 0 \quad (\text{Eq. A-5})$$

Subtracting Equation A-5 from A-4

$$V_{C1} - V_{C2} - 2L_r \frac{di_r}{dt} = 0 \quad (\text{Eq. A-6})$$

Defining

$$V_{C2} = V_{out} \quad (\text{Eq. A-7})$$

Using the relationship

$$V_{C1} + V_{C2} = V_{dc} \quad (\text{Eq. A-8})$$

V_{C1} becomes

$$V_{C1} = V_{dc} - V_{C2} = V_{dc} - V_{out} \quad (\text{Eq. A-9})$$

And Equation A-10 results

$$V_{dc} - V_{out} - V_{out} - 2L_r \frac{di_r}{dt} = 0$$
$$V_{out} - \frac{V_{dc}}{2} + L_r \frac{di_r}{dt} = 0 \quad (\text{Eq. A-10})$$

Node Equation

Summing currents at the node between V_{C1} and V_{C2}

$$i_2 - i_1 - i_L + \frac{C_r}{2} \frac{dV_{C1}}{dt} - \frac{C_r}{2} \frac{dV_{C2}}{dt} = 0 \quad (\text{Eq. A-11})$$

Substituting the expression for i_r from Equation A-3

$$\frac{C_r}{2} \left(\frac{dV_{C1}}{dt} - \frac{dV_{C2}}{dt} \right) + i_r - i_L = 0 \quad (\text{Eq. A-12})$$

Simplifying gives Equation A-13

$$\frac{C_r}{2} \left(\frac{d(V_{dc} - V_{out})}{dt} - \frac{dV_{out}}{dt} \right) + i_r - i_L = 0$$

$$-C_r \frac{dV_{out}}{dt} + i_r - i_L = 0 \quad (\text{Eq. A-13})$$

LaPlace Transform Solution

The initial Conditions assuming commutation from low to high voltage with diode D2 conducting are given by

$$V_{out}(0) = 0 \quad (\text{Eq. A-14})$$

$$i_r(0) = i_L + i_{boost} \quad (\text{Eq. A-15})$$

Taking the LaPlace transform of Equation A-10 yields

$$V_{out}(s) - \frac{V_{dc}}{2s} + [2L_r(sI_r(s) - i_r(0))] = 0 \quad (\text{Eq. A-16})$$

Substituting in the initial conditions results in

$$V_{out}(s) - \frac{V_{dc}}{2s} + [2L_r(sI_r(s) - i_L - i_{boost})] = 0 \quad (\text{Eq. A-17})$$

Taking the LaPlace transform of Equation A-13 gives

$$-C_r[sV_{out}(s) - V_{out}(0)] + I_r(s) - \frac{i_L}{s} = 0 \quad (\text{Eq. A-18})$$

Substituting in the initial conditions results in

$$-C_r s V_{out}(s) + I_r(s) - \frac{i_L}{s} = 0 \quad (\text{Eq. A-19})$$

Solving for V_{out}

Solving Equation A-19 for $I_r(s)$

$$I_r(s) = \frac{i_L}{s} + C_r s V_{out}(s) \quad (\text{Eq. A-20})$$

Substituting into Equation A-17

$$V_{out}(s) - \frac{V_{dc}}{2s} + L_r \left[s \left(\frac{i_L}{s} + C_r s V_{out}(s) \right) - i_L - i_{boost} \right] = 0 \quad (\text{Eq. A-21})$$

Simplifying Equation A-21

$$V_{out}(s) - \frac{V_{dc}}{2s} + L_r C_r s^2 V_{out}(s) - L_r i_{boost} = 0$$

$$V_{out}(s) (1 + L_r C_r s^2) = \frac{V_{dc}}{2s} - L_r i_{boost}$$

$$V_{out}(s) = \frac{V_{dc}}{(1 + L_r C_r s^2) 2s} - \frac{L_r i_{boost}}{1 + L_r C_r s^2}$$

$$V_{out}(s) = \frac{\frac{1}{L_r C_r} \frac{V_{dc}}{2}}{\left(\frac{1}{L_r C_r} + s^2 \right) s} - \frac{\frac{1}{L_r C_r} (L_r i_{boost})}{\frac{1}{L_r C_r} + s^2} \quad (\text{Eq. A-22})$$

Taking the inverse LaPlace transform

$$V_{out}(t) = \frac{V_{dc}}{2} \left[1 - \cos\left(\frac{1}{\sqrt{L_r C_r}} t \right) \right] - \frac{1}{\sqrt{L_r C_r}} L_r i_{boost} \sin\left(\frac{1}{\sqrt{L_r C_r}} t \right) \quad (\text{Eq. A-23})$$

Defining the resonant frequency as $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$, Equation A-23 can be rewritten as

$$\boxed{V_{out}(t) = \frac{V_{dc}}{2} (1 - \cos \omega_0 t) - 2 \sqrt{\frac{L_r}{C_r}} i_{boost} \sin \omega_0 t} \quad (\text{Eq. A-24})$$

Solving for I_r

Solving Equation A-17 for V_{out}

$$V_{out}(s) = \frac{V_{dc}}{2s} - L_r(sI_r(s) - i_L - i_{boost}) \quad (\text{Eq. A-25})$$

Substituting Equation A-25 into Equation A-19

$$-C_r s \left[\frac{V_{dc}}{2s} - L_r(sI_r(s) - i_L - i_{boost}) \right] + I_r(s) - \frac{i_L}{s} = 0 \quad (\text{Eq. A-26})$$

Simplifying Equation A-26

$$\begin{aligned} -C_r s \left[\frac{V_{dc}}{2s} - L_r s I_r(s) + L_r i_L + L_r i_{boost} \right] + I_r(s) - \frac{i_L}{s} &= 0 \\ -\frac{V_{dc} C_r}{2} + L_r C_r s^2 I_r(s) - L_r C_r s(i_L + i_{boost}) + I_r(s) - \frac{i_L}{s} &= 0 \end{aligned}$$

$$I_r(s)(1 + L_r C_r s^2) = \frac{i_L}{s} + \frac{V_{dc} C_r}{2} + L_r C_r s(i_L + i_{boost})$$

$$I_r(s) = \frac{i_L}{s(1 + L_r C_r s^2)} + \frac{V_{dc} C_r}{2(1 + L_r C_r s^2)} + \frac{L_r C_r s(i_L + i_{boost})}{(1 + L_r C_r s^2)}$$

$$I_r(s) = \frac{\frac{i_L}{L_r C_r}}{s \left(\frac{1}{L_r C_r} + s^2 \right)} + \frac{\frac{1}{L_r C_r} V_{dc} C_r}{2 \left(\frac{1}{L_r C_r} + s^2 \right)} + \frac{s(i_L + i_{boost})}{\left(\frac{1}{L_r C_r} + s^2 \right)} \quad (\text{Eq. A-27})$$

Taking the inverse Laplace transform yields an expression for the resonant current

$$i_r(t) = i_L \left(1 - \cos \left(\frac{1}{\sqrt{L_r C_r}} t \right) \right) + \frac{\frac{1}{\sqrt{L_r C_r}} V_{dc} C_r \sin \left(\frac{1}{\sqrt{L_r C_r}} t \right)}{2} + (i_L + i_{boost}) \cos \left(\frac{1}{\sqrt{L_r C_r}} t \right) \quad (\text{Eq. A-28})$$

Substituting $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$, Equation A-28 may be rewritten as

$$i_r(t) = i_L(1 - \cos\omega_0 t) + \frac{V_{dc}}{2} \sqrt{\frac{C_r}{L_r}} \sin\omega_0 t + (i_L + i_{boost}) \cos\omega_0 t \quad (\text{Eq. A-29})$$

Combining terms results in Equation A-30

$$\boxed{i_r(t) = i_L + i_{boost} \cos\omega_0 t + \frac{V_{dc}}{2} \sqrt{\frac{C_r}{L_r}} \sin\omega_0 t} \quad (\text{Eq. A-30})$$

APPENDIX B. ACSL SIMULATION PROGRAMS

A. SINGLE-PHASE HARD SWITCHED INVERTER SIMULATION

PROGRAM

INITIAL

```
"----This Program simulates operation of a hard switched inverter with  "
" sine-triangle PWM. Ideal switching and components are assumed.      "
" Load consists of an LC filter with a resistive load.                 "
" DC Voltage = 500 Volts                                               "
" Switching Frequency = 6KHz                                           "
" Output Frequency = 60Hz                                              "

MAXTERVAL maxt = 1.0e-8          !"maximum integration step size    "
MINTERVAL mint = 1.0e-12        !"min time step: for var step algorithm"
CINTERVAL cint = 1.0e-7         !"data communication interval   "
ALGORITHM ialg = 5              !"integration algorithm--R.K. 4th "
NSTEPS  nstp = 1
CONSTANT tstop = 0.03           !"stop point for integration    "

CONSTANT Lf=10.1e-3             !"filter (output) inductance    "
CONSTANT Cf=2.0e-3              !"filter (output) capacitance   "
CONSTANT Vdc=500.0              !"DC source voltage            "
CONSTANT Rload=25.0             !"load resistance               "
CONSTANT ilic=15.0              !"initial load current          "
CONSTANT VLoadic=250.0          !"initial load voltage         "
CONSTANT friang = 6000.0        !"reference triangle frequency  "
CONSTANT Vtripk = 10.0         !"reference triangle peak value "
Ttri = 1.0/friang               !"reference triangle period     "
Tover2 = Ttri/2.0              !"reference triangle half period"
slope = 4.0*Vtripk*friang       !"reference triangle slope      "
we=60.0*2.0*3.14159265         !"radian frequency of control sinusiod"
Vout=0.0                        !"initial output voltage       "
"
```

END !"of initial"

DYNAMIC

```
TERMT (t .GE. (tstop-0.5*cint))
```

DERIVATIVE

```
"----sine-triangle modulation"
tt=mod(t,Ttri)                                !"form ref triangle  "
IF(tt.LT.Tover2) THEN
  Vtri=10.0 - tt*slope
ELSE
  Vtri=-10.0+slope*(tt-Tover2)
END IF

Vsin = 5.0*cos(we*t)                          !"control sinusiod  "
SCHEDULE hi.XN.(Vtri - Vsin)                  !"switch to HI state "
SCHEDULE lo.XP.(Vtri - Vsin)                  !"switch to LO state "

"----calculate derivatives of state variables"
iLoad=VLoad/Rload
pVLoad=(iL-iLoad)/Cf
piL=(Vout-VLoad)/Lf

"----calculate state variables"
VLoad=integ(pVLoad,VLoadic)
iL=integ(piL,iLic)

END ! "of derivative"

DISCRETE hi
  Vout=Vdc
END ! "of discrete"

DISCRETE lo
  Vout=0.0
END ! "of discrete"

END ! "of dynamic"

END ! "of program"
```

B. SINGLE-PHASE ARCP SIMULATION

PROGRAM

INITIAL

```

"-----This Program simulates operation of the Auxiliary Resonant      "
"  Commutated Pole (ARCP) converter. Ideal switching and components"
"  are assumed. Load consists of an LC filter with a resistive load.  "
"  Resonant Frequency = 250KHz                                       "
"  DC Voltage = 500 Volts                                             "
"  Switching Frequency = 6KHz                                        "
"  Output Frequency = 60 Hz                                          "

MAXTERVAL maxt = 1.0e-8      !"maximum integration step size      "
MINTERVAL mint = 1.0e-12    !"min time step:for var step algorithm"
CINTERVAL cint = 1.0e-7     !"data communication interval  "
ALGORITHM ialg = 5          !"integration algorithm--R.K. 4th  "
NSTEPS  nstp = 1
CONSTANT tstop = 0.03       !"stop point for integration    "

LOGICAL S1,S2,A1,A2,state1,state2,state3,state4,state5,state6
S1=.false.                  !"status of upper main switch, switch #1  "
S2=.true.                   !"status of lower main switch, switch #2  "
A1=.false.                  !"status of auxiliary switch #1         "
A2=.false.                  !"status of auxiliary switch #2         "
state1=.false.              !"transition Lo to Hi, IL pos           "
state2=.false.              !"transition Hi to Lo, IL pos and > Ithres  "
state3=.false.              !"transition Hi to Lo, IL pos and < Ithres  "
state4=.false.              !"transition Lo to Hi, IL neg and < Ithres  "
state5=.false.              !"transition Hi to Lo, IL neg           "
state6=.false.              !"transition Lo to Hi, IL neg and > Ithres  "

CONSTANT Lr=2.9e-6          !"resonant inductance                  "
CONSTANT Cr=.3e-6           !"resonant cap (total both switches)    "
CONSTANT Lf=10.1e-3         !"filter (output) inductance           "
CONSTANT Cf=2.0e-3          !"filter (output) capacitance          "
CONSTANT RLoad=25.0         !"load resistance                      "
CONSTANT Vdc=500.0          !"DC source voltage                   "
CONSTANT iLic=15.0          !"initial load current                 "
CONSTANT Voutic=0.0         !"initial output voltage              "
CONSTANT VLoadic=250.0      !"initial load voltage                 "
CONSTANT iric=0.0           !"initial auxillary circuit current    "
CONSTANT iboostswitch=4.0   !"boost current reqd before switching"

```

```

CONSTANT ithreshold=18           !"threshold current           "
wo=1.0/(sqrt(Lr*Cr))           !"resonant radian frequency  "
CONSTANT ftriang = 6000.0      !"reference triangle frequency"
CONSTANT Vtripk = 10.0         !"reference triangle peak value"
Ttri = 1.0/ftriang              !"reference triangle period   "
Tover2 = Ttri/2.0              !"reference triangle half period"
slope = 4.0*Vtripk*ftriang     !"reference triangle slope    "
we=60.0*2.0*3.14159265        !"radian frequency of control sinusiod"

```

END ! "of initial"

DYNAMIC

```

TERMT (t .GE. (tstop-0.5*cint))

```

DERIVATIVE

```

"----sine-triangle modulation"
tt=mod(t,Ttri)                  !"form ref triangle      "
IF(tt.LT.Tover2) THEN
  Vtri=10.0 - tt*slope
ELSE
  Vtri=-10.0+slope*(tt-Tover2)
END IF
Vsin = 5.0*cos(we*t)           !"control sinusiod      "
SCHEDULE hi.XN.(Vtri - Vsin)   !"switch to HI state    "
SCHEDULE lo.XP.(Vtri - Vsin)   !"switch to LO state    "

"----schedule switching points of specific components"
SCHEDULE S1on.XP.Vout-Vdc      !"S1 on                  "
SCHEDULE S1offS2.XN.ir+iboostswitch !"S1 off State2         "
SCHEDULE S1offS5.XN.(iboostswitch-iL+ir) !"S1 off State5        "
SCHEDULE S2on.XN.Vout          !"S2 on                  "
SCHEDULE S2offS1.XN.(iboostswitch+iL-ir) !"S2 off State1         "
SCHEDULE S2offS4.XP.ir-iboostswitch !"S2 off State4         "
SCHEDULE A1off.XP.ir           !"A1 off                 "
SCHEDULE A2off.XN.ir           !"A2 off                 "

"----determine characteristic equations for switch configuration"
IF(.not.(S1.or.S2).and.(A1.or.A2)) THEN
  pVout=(ir-iL)/Cr
ELSE IF (.not.(S1.or.S2)) THEN
  pVout=-iL/Cr
ELSE
  pVout=0.0
ENDIF

```

```

IF (A1.or.A2) THEN
  pir=(Vdc-2.0*Vout)/(2.0*Lr)
ELSE
  pir=0.0
ENDIF

```

```

"----calculate diode and switch currents"
IF(S1.and.((iL-ir).GT.0.0)) THEN
  iS1=iL-ir
ELSE
  iD1=-iL-ir
ENDIF

```

```

IF(S2.and.((iL-ir).LT.0.0)) THEN
  iS2=-iL-ir
ELSE
  iD2=iL-ir
ENDIF

```

```

"----calculate state variables"
Vout=integ(pVout,Voutic)
ir=integ(pir,iric)
iLoad=VLoad/RLoad

pVLoad=(iL-iLoad)/Cf
VLoad=integ(pVLoad,VLoadic)

piL=(Vout-VLoad)/Lf
iL=integ(piL,iLic)

```

END ! "of derivative"

```

"----determine state of converter during switching interval"
DISCRETE lo
  IF(iL.LT.0.0) THEN
    state5=.true.
    A1=.true.
  ELSE IF(iL.LT.ithreshold) THEN
    state2=.true.
    A1=.true.
  ELSE
    state3=.true.
    S1=.false.
  ENDIF
END ! "of discrete"

```

```

DISCRETE hi
  IF(iL.GT.0.0) THEN
    state1=.true.
    A2=.true.
  ELSE IF(ABS(iL).LT.ithreshold) THEN
    state4=.true.
    A2=.true.
  ELSE
    state6=.true.
    S2=.false.
  ENDIF
END ! "of discrete"

```

```

"----determine which switches are closed"
DISCRETE S1on
  S1=.true.
  pVout=0.0
  Vout=Vdc
  state1=.false.
  state4=.false.
  state6=.false.
END ! "of discrete"

```

```

DISCRETE S1offS2
  IF(state2) THEN
    S1=.false.
  END IF
END ! "of discrete"

```

```

DISCRETE S1offS5
  IF(state5) THEN
    S1=.false.
  END IF
END ! "of discrete"

```

```

DISCRETE S2on
  S2=.true.
  pVout=0.0
  Vout=0.0
  state2=.false.
  state3=.false.
  state5=.false.
END ! "of discrete"

```

```
DISCRETE S2offS1
  IF(state1) THEN
    S2=.false.
  END IF
END ! "of discrete"
```

```
DISCRETE S2offS4
  IF(state4) THEN
    S2=.false.
  END IF
END ! "of discrete"
```

```
DISCRETE A1off
  A1=.false.
  pir=0.0
  ir=0.0
END ! "of discrete"
```

```
DISCRETE A2off
  A2=.false.
  pir=0.0
  ir=0.0
END ! "of discrete"
```

```
END ! "of dynamic"
```

```
END ! "of program"
```

C. THREE-PHASE HARD-SWITCHED INVERTER SIMULATION

PROGRAM

INITIAL

```
"-----This Program simulates operation of a 3-Phase hard switched inverter"  
" with sine-triangle PWM. Ideal switching and components are assumed"  
" Load consists of an LC filter with a resistive load. "  
" DC Voltage 500 Volts "  
" Switching Frequency = 6kHz "  
" Output Frequency = 60Hz "
```

```
MAXTERVAL maxt = 1.0e-8 !"maximum integration step size "  
MININTERVAL mint = 1.0e-12 !"min time step:for var step algorithm"  
CINTERVAL cint = 1.0e-7 !"data communication interval "  
ALGORITHM ialg = 5 !"integration algorithm--R.K. 4th "  
NSTEPS nstp = 1  
CONSTANT tstop = 0.03 !"stop point for integration "  
CONSTANT Lf=10.1e-3 !"filter (output) inductance "  
CONSTANT CF=1.0e-4 !"filter (output) capacitance "  
CONSTANT Vdc=500.0 !"DC source voltage "  
CONSTANT Rload=25.0 !"load resistance "  
CONSTANT ftriang = 6000.0 !"reference triangle frequency "  
CONSTANT Vtripk = 10.0 !"reference triangle peak value "  
Ttri = 1.0/ftriang !"reference triangle period "  
Tover2 = Ttri/2.0 !"reference triangle half period "  
slope = 4.0*Vtripk*ftriang !"reference triangle slope "  
we=60.0*2.0*3.14159265 !"radian frequency of control sinusiod"  
pi2o3=2.0*3.14159265/3.0 !"120 degrees in radians "  
CONSTANT iqssic=8.0 !"initial q axis current "  
CONSTANT idssic=3.0 !"initial d axis current "  
CONSTANT A=9.0 !"control voltage magnitude "  
iLa=iqssic  
ilb=-0.5*iqssic-idssic*sqrt(3.0)/2.0  
ilc=-0.5*iqssic+idssic*sqrt(3.0)/2.0  
CONSTANT VqssLic=200.0  
CONSTANT VdssLic=0.0  
VLa=VqssL  
VLb=-0.5*VqssLic-(sqrt(3.0)/2.0)*VdssLic  
Vlc=-0.5*VqssLic+(sqrt(3.0)/2.0)*VdssLic  
Vag=0.0  
Vbg=0.0  
Vcg=0.0
```

END ! "of initial"

DYNAMIC

TERMT (t .GE. (tstop-0.5*cint))

DERIVATIVE

"----sine-triangle modulation"

tt=mod(t,Ttri)

!"form ref triangle "

IF(tt.LT.Tover2) THEN

Vtri=10.0 - tt*slope

ELSE

Vtri=-10.0+slope*(tt-Tover2)

END IF

Vsina = A*cos(we*t)

!"control sinusiod "

SCHEDULE hia.XN.(Vtri - Vsina)

!"switch A to HI state "

SCHEDULE loa.XP.(Vtri - Vsina)

!"switch A to LO state"

Vsinb = A*cos(we*t-pi2o3)

!"control sinusoid "

SCHEDULE hib.XN.(Vtri - Vsinb)

!"switch B to HI state "

SCHEDULE lob.XP.(Vtri - Vsinb)

!"switch B to LO state"

Vsinc = A*cos(we*t+pi2o3)

!"control sinusiod "

SCHEDULE hic.XN.(Vtri - Vsinc)

!"switch C to HI state "

SCHEDULE loc.XP.(Vtri - Vsinc)

!"switch C to LO state"

"----calculate line voltages"

Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)

Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)

Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"

Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)

Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"

piqss=(Vqss-VqssL)/Lf

pidss=(Vdss-VdssL)/Lf

"----find load voltage derivatives in stationary frame"

pVqssL=(iqss-(VqssL/Rload))/Cf

pVdssL=(idss-(VdssL/Rload))/Cf

"----calculate stationary currents"

iqss=integ(piqss,iqssic)

idss=integ(pidss,idssic)

```

"----calculate stationary voltages"
VqssL=integ(pVqssL,VqssLic)
VdssL=integ(pVdssL,VdssLic)

"----transform back to ABC quantities"
iLa=iqss
iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss
iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

VLa=VqssL
VLb=-0.5*VqssL-(sqrt(3.0)/2.0)*VdssL
VLc=-0.5*VqssL+(sqrt(3.0)/2.0)*VdssL

iLoada=VLa/RLoad
iLoadb=VLb/RLoad
iLoadc=VLc/Rload

END ! "of derivative"

DISCRETE hia
  Vag=Vdc
END ! "of discrete"

DISCRETE loa
  Vag=0.0
END ! "of discrete"

DISCRETE hib
  Vbg=Vdc
END ! "of discrete"

DISCRETE lob
  Vbg=0.0
END ! "of discrete"

DISCRETE hic
  Vcg=Vdc
END ! "of discrete"

DISCRETE loc
  Vcg=0.0
END ! "of discrete"

END ! "of dynamic"
END ! "of program "

```

D. TRHEE-PHASE ARCP SIMULATION

PROGRAM

INITIAL

```
"-----This Program simulates operation of the Three Phase Auxiliary      "
" Resonant Comutated Pole (ARCP) converter.                                "
" Ideal switching and components are assumed                              "
" Resonant Frequency = 250KHz                                           "
" DC Voltage = 500 Volts                                                "
" Switching Frequency = 6KHz                                           "
" Output Frequency = 60Hz                                              "

MAXTERVAL maxt = 1.0e-8          !"maximum integration step size      "
MININTERVAL mint = 1.0e-12       !"min time step: for var step algorithm"
CINTERVAL cint = 1.0e-7         !"data communication interval    "
ALGORITHM ialg = 5              !"integration algorithm--R.K. 4th  "
NSTEPS  nstp = 1
CONSTANT tstop = 0.00003        !"stop point for integration    "

LOGICAL S1a,S2a,A1a,A2a,state1a,state2a,state3a,state4a,state5a,state6a

S1a=.false.                    !"status of upper main switch, switch #1  "
S2a=.true.                     !"status of lower main switch, switch #2  "
A1a=.false.                    !"status of auxiliary switch #1          "
A2a=.false.                    !"status of auxiliary switch #2          "
state1a=.false.               !"transition Lo to Hi, IL pos           "
state2a=.false.               !"transition Hi to Lo, IL pos and > Ithres "
state3a=.false.               !"transition Hi to Lo, IL pos and < Ithres "
state4a=.false.               !"transition Lo to Hi, IL neg and < Ithres "
state5a=.false.               !"transition Hi to Lo, IL neg           "
state6a=.false.               !"transition Lo to Hi, IL neg and > Ithres "

LOGICAL S1b,S2b,A1b,A2b,state1b,state2b,state3b,state4b,state5b,state6b

S1b=.false.                   !"status of upper main switch, switch #1  "
S2b=.true.                    !"status of lower main switch, switch #2  "
A1b=.false.                   !"status of auxiliary switch #1          "
A2b=.false.                   !"status of auxiliary switch #2          "

state1b=.false.               !"transition Lo to Hi, IL pos           "
state2b=.false.               !"transition Hi to Lo, IL pos and > Ithres "
state3b=.false.               !"transition Hi to Lo, IL pos and < Ithres "
```

```

state4b=.false.      !"transition Lo to Hi, IL neg and < Ithres  "
state5b=.false.      !"transition Hi to Lo, IL neg                "
state6b=.false.      !"transition Lo to Hi, IL neg and > Ithres  "

```

LOGICAL S1c,S2c,A1c,A2c,state1c,state2c,state3c,state4c,state5c,state6c

```

S1c=.false.          !"status of upper main switch, switch #1  "
S2c=.true.           !"status of lower main switch, switch #2  "
A1c=.false.          !"status of auxiliary switch #1          "
A2c=.false.          !"status of auxiliary switch #2          "
state1c=.false.      !"transition Lo to Hi, IL pos              "
state2c=.false.      !"transition Hi to Lo, IL pos and > Ithres "
state3c=.false.      !"transition Hi to Lo, IL pos and < Ithres "
state4c=.false.      !"transition Lo to Hi, IL neg and < Ithres "
state5c=.false.      !"transition Hi to Lo, IL neg              "
state6c=.false.      !"transition Lo to Hi, IL neg and > Ithres "

```

```

CONSTANT Lr=2.9e-6    !"resonant inductance                    "
CONSTANT Cr=.3e-6     !"resonant cap (total both switches)    "
CONSTANT Lf=10.1e-3   !"filter (output) inductance            "
CONSTANT Cf=1.0e-4    !"filter (output) capacitance           "
CONSTANT RLoad=25.0   !"load resistance                        "
CONSTANT Vdc=500.0    !"DC source voltage                     "
CONSTANT iqssc=5.0    !"initial q axis current                 "
CONSTANT idssc=3.0    !"initial d axis current                 "
CONSTANT Vagic=0.0    !"initial output current                 "
CONSTANT Vbgic=0.0    !"initial output current                 "
CONSTANT Vcgic=0.0    !"initial output current                 "
CONSTANT iraic=0.0    !"initial auxillary circuit current      "
CONSTANT irbic=0.0    !"initial auxillary circuit current      "
CONSTANT ircic=0.0    !"initial auxillary circuit current      "
CONSTANT iboostswitch=5.0 !"boost current reqd before switching"
CONSTANT ithreshold=18 !"threshold current                       "
CONSTANT ftriang = 6000.0 !"reference triangle frequency           "
CONSTANT Vtripk = 10.0 !"reference triangle peak value          "
Ttri = 1.0/ftriang    !"reference triangle period              "
Tover2 = Ttri/2.0    !"reference triangle half period         "
slope = 4.0*Vtripk*ftriang !"reference triangle slope               "
we=60.0*2.0*3.14159265 !"radian frequency of control sinusiod"
pi2o3=2.0*3.14159265/3.0 !"120 degrees in radians                "
CONSTANT A=5.0       !"control voltage magnitude             "
iLa=iqssc
ilb=-0.5*iqssc-idssc*sqrt(3.0)/2.0
ilc=-0.5*iqssc+idssc*sqrt(3.0)/2.0
CONSTANT VqssLic=200.0

```

```

CONSTANT VdssLic=0.0
VLa=VqssL
VLb=-0.5*VqssLic-(sqrt(3.0)/2.0)*VdssLic
VLc=-0.5*VqssLic+(sqrt(3.0)/2.0)*VdssLic

```

```

END ! "of initial"

```

```

DYNAMIC

```

```

    TERMT (t .GE. (tstop-0.5*cint))

```

```

DERIVATIVE

```

```

"----sine-triangle modulation"
tt=mod(t,Ttri)                                !"form ref triangle  "
IF(tt.LT.Tover2) THEN
    Vtri=10.0 - tt*slope
ELSE
    Vtri=-10.0+slope*(tt-Tover2)
END IF

Vsina = A*cos(we*t)                            !"control sinusiod  "
SCHEDULE hia.XN.(Vtri - Vsina)                 !"switch A to HI state "
SCHEDULE loa.XP.(Vtri - Vsina)                 !"switch A to LO state"

Vsinb = A*cos(we*t-pi2o3)                     !"control sinusoid   "
SCHEDULE hib.XN.(Vtri - Vsinb)                 !"switch B to HI state "
SCHEDULE lob.XP.(Vtri - Vsinb)                 !"switch B to LO state"

Vsinc = A*cos(we*t+pi2o3)                     !"control sinusiod   "
SCHEDULE hic.XN.(Vtri - Vsinc)                 !"switch C to HI state "
SCHEDULE loc.XP.(Vtri - Vsinc)                 !"switch C to LO state"

"----schedule switching points of specific components for Phase A "
SCHEDULE S1aon.XP.Vag-Vdc                      !"S1 on              "
SCHEDULE S1aoff.XN.switcha                     !"S1 off             "
SCHEDULE S2aon.XN.Vag                          !"S2 on              "
SCHEDULE S2aoff.XN.switcha                     !"S2 off             "
SCHEDULE A1aoff.XP.ira                          !"A1 off             "
SCHEDULE A2aoff.XN.ira                          !"A2 off             "

```

```

"----schedule switching points of specific components for Phase B "
SCHEDULE S1bon.XP.Vbg-Vdc          !"S1 on          "
SCHEDULE S1boff.XN.switchb        !"S1 off         "
SCHEDULE S2bon.XN.Vbg              !"S2 on          "
SCHEDULE S2boff.XN.switchb        !"S2 off         "
SCHEDULE A1boff.XP.irb             !"A1 off         "
SCHEDULE A2boff.XN.irb             !"A2 off         "

"----schedule switching points of specific components for Phase C "
SCHEDULE S1con.XP.Vcg-Vdc          !"S1 on          "
SCHEDULE S1coff.XN.switchc        !"S1 off         "
SCHEDULE S2con.XN.Vcg              !"S2 on          "
SCHEDULE S2coff.XN.switchc        !"S2 off         "
SCHEDULE A1coff.XP.irc             !"A1 off         "
SCHEDULE A2coff.XN.irc             !"A2 off         "

"----generate control for main switches
switcha=(ira+iboostswitch)*state2a + (iboostswitch-iLa+ira)*state5a + &
        (iboostswitch+iLa-ira)*state1a - (ira-iboostswitch)*state4a
switchb=(irb+iboostswitch)*state2b + (iboostswitch-iLb+irb)*state5b + &
        (iboostswitch+iLb-irb)*state1b - (irb-iboostswitch)*state4b
switchc=(irc+iboostswitch)*state2c + (iboostswitch-iLc+irc)*state5c + &
        (iboostswitch+iLc-irc)*state1c - (irc-iboostswitch)*state4c

"----determine characteristic equations for switch configuration phase A"
IF(.not.(S1a.or.S2a).and.((A1a.or.A2a))) THEN
    pVag=(ira-iLa)/Cr
ELSE IF (.not.(S1a.or.S2a)) THEN
    pVag=-iLa/Cr
ELSE
    pVag=0.0
ENDIF

IF ((A1a.or.A2a)) THEN
    pira=(Vdc-2.0*Vag)/(2.0*Lr)
ELSE
    pira=0.0
ENDIF

"----calculate diode and switch currents"
IF(S1a.and.((iLa-ira).GT.0.0)) THEN
    iS1a=iLa-ira
ELSE
    iD1a=-(iLa-ira)
ENDIF

```

```

IF(S2a.and.((iLa-ira).LT.0.0)) THEN
  iS2a=-(iLa-ira)
ELSE
  iD2a=iLa-ira
ENDIF

```

```

"----determine characteristic equations for switch configuration phase B"
IF(.not.(S1b.or.S2b).and.((A1b.or.A2b))) THEN
  pVbg=(irb-iLb)/Cr
ELSE IF (.not.(S1b.or.S2b)) THEN
  pVbg=-iLb/Cr
ELSE
  pVbg=0.0
ENDIF

```

```

IF ((A1b.or.A2b)) THEN
  pirb=(Vdc-2.0*Vbg)/(2.0*Lr)
ELSE
  pirb=0.0
ENDIF

```

```

"----calculate diode and switch currents"
IF(S1b.and.((iLb-irb).GT.0.0)) THEN
  iS1b=iLb-irb
ELSE
  iD1b=-(iLb-irb)
ENDIF

```

```

IF(S2b.and.((iLb-irb).LT.0.0)) THEN
  iS2b=-(iLb-irb)
ELSE
  iD2b=iLb-irb
ENDIF

```

```

"----determine characteristic equations for switch configuration phase C"
IF(.not.(S1c.or.S2c).and.((A1c.or.A2c))) THEN
  pVcg=(irc-iLc)/Cr
ELSE IF (.not.(S1c.or.S2c)) THEN
  pVcg=-iLc/Cr
ELSE
  pVcg=0.0
ENDIF

```

```

IF ((A1c.or.A2c)) THEN
  pirc=(Vdc-2.0*Vcg)/(2.0*Lr)
ELSE
  pirc=0.0
ENDIF

"----calculate diode and switch currents"
IF(S1c.and.((iLc-irc).GT.0.0)) THEN
  iS1c=iLc-irc
ELSE
  iD1c=-(iLc-irc)
ENDIF

IF(S2c.and.((iLc-irc).LT.0.0)) THEN
  iS2c=-(iLc-irc)
ELSE
  iD2c=iLc-irc
ENDIF

"----calculate state variables phase A"
Vag=integ(pVag,Vagic)
ira=integ(pira,iraic)

"----calculate state variables phase B"
Vbg=integ(pVbg,Vbgic)
irb=integ(pirb,irbic)

"----calculate state variables phase C"
Vcg=integ(pVcg,Vcgic)
irc=integ(pirc,ircic)

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"
Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)
Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"
piqss=(Vqss-VqssL)/Lf
pidss=(Vdss-VdssL)/Lf

```

```

"----find load voltage derivatives in stationary frame"
pVqssL=(iqss-(VqssL/Rload))/Cf
pVdssL=(idss-(VdssL/Rload))/Cf

"----calculate stationary currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)
"----calculate stationary voltages"
VqssL=integ(pVqssL,VqssLic)
VdssL=integ(pVdssL,VdssLic)

"----transform back to ABC quantities"
iLa=iqss
iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss
iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

VLa=VqssL
VLb=-0.5*VqssL-(sqrt(3.0)/2.0)*VdssL
VLc=-0.5*VqssL+(sqrt(3.0)/2.0)*VdssL

"----calculate load currents"
iLoada=VLa/RLoad
iLoadb=VLb/RLoad
iLoadc=VLc/RLoad
END ! "of derivative"

"----determine state of phase A during switching interval"
DISCRETE loa
IF(iLa.LT.0.0) THEN
  state5a=.true.
  A1a=.true.
ELSE IF(iLa.LT.ithreshold) THEN
  state2a=.true.
  A1a=.true.
ELSE
  state3a=.true.
  S1a=.false.
ENDIF
END ! "of discrete"

```

```

DISCRETE hia
  IF(iLa.GT.0.0) THEN
    state1a=.true.
    A2a=.true.
  ELSE IF(ABS(iLa).LT.ithreshold) THEN
    state4a=.true.
    A2a=.true.
  ELSE
    state6a=.true.
    S2a=.false.
  ENDIF
END ! "of discrete"

```

"----determine state of phase B during switching interval"

```

DISCRETE lob
  IF(iLb.LT.0.0) THEN
    state5b=.true.
    A1b=.true.
  ELSE IF(iLb.LT.ithreshold) THEN
    state2b=.true.
    A1b=.true.
  ELSE
    state3b=.true.
    S1b=.false.
  ENDIF
END ! "of discrete"

```

```

DISCRETE hib
  IF(iLb.GT.0.0) THEN
    state1b=.true.
    A2b=.true.
  ELSE IF(ABS(iLb).LT.ithreshold) THEN
    state4b=.true.
    A2b=.true.
  ELSE
    state6b=.true.
    S2b=.false.
  ENDIF
END ! "of discrete"

```

"----determine state of phase C during switching interval"

```
DISCRETE loc
  IF(iLc.LT.0.0) THEN
    state5c=.true.
    A1c=.true.
  ELSE IF(iLc.LT.ithreshold) THEN
    state2c=.true.
    A1c=.true.
  ELSE
    state3c=.true.
    S1c=.false.
  ENDIF
END ! "of discrete"
```

```
DISCRETE hic
  IF(iLc.GT.0.0) THEN
    state1c=.true.
    A2c=.true.
  ELSE IF(ABS(iLc).LT.ithreshold) THEN
    state4c=.true.
    A2c=.true.
  ELSE
    state6c=.true.
    S2c=.false.
  ENDIF
END ! "of discrete"
```

"----determine which switches are closed Phase A"

```
DISCRETE S1aon
  S1a=.true.
  pVag=0.0
  Vag=Vdc
  state1a=.false.
  state4a=.false.
  state6a=.false.
END ! "of discrete"
```

```
DISCRETE S1aoff
  S1a=.false.
END ! "of discrete"
```

```
DISCRETE S2aon
  S2a=.true.
  pVag=0.0
  Vag=0.0
  state2a=.false.
  state3a=.false.
  state5a=.false.
END  !"of discrete"
DISCRETE S2aoff
S2a=.false.
END  !"of discrete"
```

```
DISCRETE A1aoff
  A1a=.false.
  pira=0.0
  ira=0.0
END  !"of discrete"
```

```
DISCRETE A2aoff
  A2a=.false.
  pira=0.0
  ira=0.0
END  !"of discrete"
```

```
"----determine which switches are closed Phase B"
DISCRETE S1bon
  S1b=.true.
  pVbg=0.0
  Vbg=Vdc
  state1b=.false.
  state4b=.false.
  state6b=.false.
END  !"of discrete"
```

```
DISCRETE S1boff
S1b=.false.
END  !"of discrete"
DISCRETE S2bon
  S2b=.true.
  pVbg=0.0
  Vbg=0.0
  state2b=.false.
  state3b=.false.
  state5b=.false.
END  !"of discrete"
```

```
DISCRETE S2boff
S2b=.false.
END ! "of discrete"
```

```
DISCRETE A1boff
A1b=.false.
pirb=0.0
irb=0.0
END ! "of discrete"
```

```
DISCRETE A2boff
A2b=.false.
pirb=0.0
irb=0.0
END ! "of discrete"
```

```
"----determine which switches are closed Phase C"
DISCRETE S1con
S1c=.true.
pVcg=0.0
Vcg=Vdc
state1c=.false.
state4c=.false.
state6c=.false.
END ! "of discrete"
```

```
DISCRETE S1coff
S1c=.false.
END ! "of discrete"
```

```
DISCRETE S2con
S2c=.true.
pVcg=0.0
Vcg=0.0
state2c=.false.
state3c=.false.
state5c=.false.
END ! "of discrete"
```

```
DISCRETE S2coff
S2c=.false.
END ! "of discrete"
```

```
DISCRETE A1coeff  
  A1c=.false.  
  pirc=0.0  
  irc=0.0  
END ! "of discrete"
```

```
DISCRETE A2coeff  
  A2c=.false.  
  pirc=0.0  
  irc=0.0  
END ! "of discrete"
```

```
END ! "of dynamic"
```

```
END ! "of program"
```

APPENDIX C. TOTAL HARMONIC DISTORTION CALCULATION

When evaluating total harmonic distortion it is assumed that the fundamental frequency is known. Although it is not absolutely necessary to know the fundamental frequency a priori, it must at least be estimated to perform the calculation. Since the estimation can become extremely complicated our assumption simplifies the task.

Total harmonic distortion is defined as

$$THD\% = 100 \times \sqrt{\frac{V_{s2}^2 + V_{s3}^2 + V_{s4}^2 + \dots}{V_{s1}^2}} = 100 \times \sqrt{\sum_{h \neq 1} \left(\frac{V_{sh}}{V_{s1}} \right)^2} \quad (\text{Eq. C-1})$$

where V indicates an RMS voltage, and h indicates the order of the harmonic.

To evaluate the harmonic components the principle of orthogonal functions will be used. The following discussion shows the development of the procedure.

Initially the quantity in question, in this case voltage, is defined in Equation C-2.

$$v_s = \sum_{n=1,3,5,\dots}^{\infty} V_n \sin(n\omega_0 t + \theta_n) \quad (\text{Eq. C-2})$$

Using a trigonometric expansion Equation C-2 becomes

$$v_s = \sum_{n=1,3,5,\dots}^{\infty} V_n [\sin(n\omega_0 t) \cos \theta_n + \cos(n\omega_0 t) \sin \theta_n] \quad (\text{Eq. C-3})$$

Multiplying v_s by $\sin(m\omega_0 t)$ and integrating over a fundamental period, the function C is obtained

$$C = \frac{2}{T} \int_0^T v_s \sin(m\omega_0 t) dt \quad (\text{Eq. C-4})$$

Substituting Equation C-3 into Equation C-4, Equation C-5 is obtained where C_1 and C_2 are given by Equations C-6 and C-7.

$$C = \frac{2}{T} \sum_{n=1,3,5,\dots}^{\infty} V_n (C_1 + C_2) \quad (\text{Eq. C-5})$$

$$C_1 = \int_0^T \sin(n\omega_0 t) \cos\theta_n \sin(m\omega_0 t) dt = 0 \quad \text{for } m \neq n \quad (\text{Eq. C-6})$$

$$C_2 = \int_0^T \cos(n\omega_0 t) \cos\theta_n \sin(m\omega_0 t) dt = 0 \quad \text{for all } m \text{ and } n \quad (\text{Eq. C-7})$$

Reducing Equation C-5, Equation C-8 is obtained

$$C = \frac{2}{T} V_n \int_0^T \cos\theta_n \sin^2(n\omega_0 t) dt \quad (\text{Eq. C-8})$$

Integrating and solving, Equation C-8 becomes

$$C = V_n \cos\theta_n \quad (\text{Eq. C-9})$$

The same procedure is repeated again, except v_s is initially multiplied by $\cos(m\omega_0 t)$, this will produce a sine function result. The results are summarized as

$$S = \frac{2}{T} \int_0^T v_s \cos(m\omega_0 t) dt \quad (\text{Eq. C-10})$$

$$S = \frac{2}{T} \sum_{n=1,3,5,\dots}^{\infty} V_n (S_1 + S_2) \quad (\text{Eq. C-11})$$

$$S_1 = \int_0^T \sin(n\omega_0 t) \cos\theta_n \cos(m\omega_0 t) dt = 0 \quad \text{for all } m \text{ and } n \quad (\text{Eq. C-12})$$

$$S_2 = \int_0^T \cos(n\omega_0 t) \sin\theta_n \cos(m\omega_0 t) dt = 0 \quad \text{for } m \neq n \quad (\text{Eq. C-13})$$

$$S = \frac{2}{T} V_n \int_0^T \sin \theta_n \cos^2(n\omega_0 t) dt \quad (\text{Eq. C-14})$$

$$S = V_n \sin \theta_n \quad (\text{Eq. C-15})$$

With both the sine and cosine functions available, the magnitude of the n th harmonic, V_n , and the respective phase angle, θ_n , can be evaluated using Equations C-16 and C-17.

$$V_n = \sqrt{S^2 + C^2} \quad (\text{Eq. C-16})$$

$$\theta_n = \tan^{-1}\left(\frac{S}{C}\right) \quad (\text{Eq. C-17})$$

The procedure is shown graphically in Figure C-1.

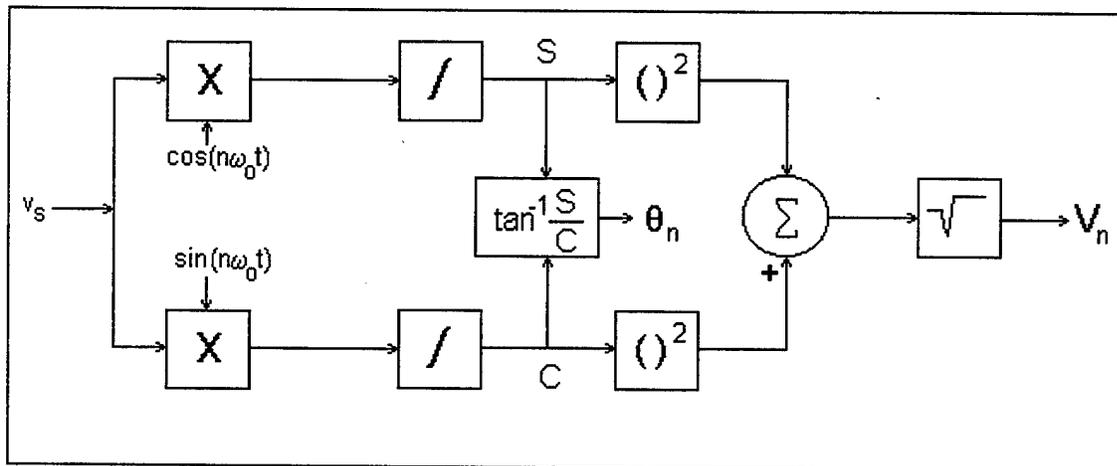


Figure C-1 - Harmonic Analyzer

APPENDIX D. CONTROLLER SIMULATION PROGRAMS

A. MATLAB SIMULATION FOR VOLTAGE FEEDBACK CONTROLLER

% This program simulates a stationary voltage feedback controller in the synchronous
% reference frame. A step response is generated and the poles and zeros of the transfer
% function along with the steady state matrix are output.

```
Kp=7          % Proportional Gain
Ki=50         % Integral Gain
U=50;        % Step Response Magnitude
t=linspace(0,.03,20000);

%% Simulation Parameters %%
Cf=.0001;
Lf=.01;
Rload=25;
we=2*pi*60;

%% System Matrices %%
A=[-1/(Cf*Rload) -we          1/Cf  0  0  0
    we          -1/(Cf*Rload)  0    1/Cf  0  0
    -(Kp+1)/Lf  0            0    -we  Ki/Lf  0
    0          -(Kp+1)/Lf    we    0  0    Ki/Lf
    -1         0            0    0  0    -we
    0         -1           0    0  we    0];
B=[1 0 Kp/Lf 0 0 0;0 1 0 Kp/Lf 0 0];
C=U*[1 0 0 0 0 0];
D=[0 0];

%% Poles and Zeros of Transfer Function %%
[num,den]=ss2tf(A,B,C,D,1);
R=roots(den)
P=roots(num)

%% Steady State Matrix %%
SS=-[1 0 0 0 0 0;0 1 0 0 0 0]*inv(A)*B

%% Step Response Output %%
step(A,B,C,D,1,t),title('MATLAB Step Response')
```

B. ACSL SIMULATION FOR VOLTAGE FEEDBACK CONTROLLER

PROGRAM

INITIAL

```

" This Program simulates operation of a 3-Phase hard switched inverter "
" with sine-triangle PWM. Ideal switching and components are assumed "
" Load consists of an LC filter with a resistive load. "
" DC Voltage 500 Volts "
" Switching Frequency = 6kHz Output Frequency = 60Hz "
MAXTERVAL maxt = 1.0e-8 !"maximum integration step size "
MININTERVAL mint = 1.0e-12 !"min time step:for var step algorithm "
CINTERVAL cint = 1.0e-7 !"data communication interval "
ALGORITHM ialg = 5 !"integration algorithm--R.K. 4th "
NSTEPS nstp = 1
CONSTANT tstop = 0.03 !"stop point for integration "
CONSTANT Lf=10.1e-3 !"filter (output) inductance "
CONSTANT CF=1.0e-4 !"filter (output) capacitance "
CONSTANT Vdc=500.0 !"DC source voltage "
CONSTANT Rload=25.0 !"load resistance "
CONSTANT ftriang = 6000.0 !"reference triangle frequency "
CONSTANT Vtripk = 10.0 !"reference triangle peak value "
Tri = 1.0/ftriang !"reference triangle period "
Tover2 = Tri/2.0 !"reference triangle half period "
slope = 4.0*Vtripk*ftriang !"reference triangle slope "
we=60.0*2.0*3.14159265 !"radian frequency of control sinusiod "
pi2o3=2.0*3.14159265/3.0 !"120 degrees in radians "
CONSTANT iqssic=8.0 !"initial q axis current "
CONSTANT idssic=3.0 !"initial d axis current "
iLa=iqssic
iLb=-0.5*iqssic-idssic*sqrt(3.0)/2.0
iLc=-0.5*iqssic+idssic*sqrt(3.0)/2.0
CONSTANT VqssLic=250.0
CONSTANT VdssLic=0.0
VLa=VqssL
VLb=-0.5*VqssLic-(sqrt(3.0)/2.0)*VdssLic
VLc=-0.5*VqssLic+(sqrt(3.0)/2.0)*VdssLic
Vag=0.0
Vbg=0.0
Vcg=0.0
CONSTANT K1=10.0 !"proportional gain "
CONSTANT K2=0.0 !"integral gain "
CONSTANT A=250.0 !"desired voltage magnitude "
Vmax=(Vdc/20.0) !"linear pulse width modulation gain "

```

END ! "of initial"

DYNAMIC

TERMT (t .GE. (tstop-0.5*cint))

DERIVATIVE

"----sine-triangle modulation"

tt=mod(t,Ttri)

!"form ref triangle "

IF(tt.LT.Tover2) THEN

Vtri=10.0 - tt*slope

ELSE

Vtri=-10.0+slope*(tt-Tover2)

END IF

"----calculate synchronous reference frame angle"

thetae=mod(integ(we,0.0),twopi)

"----calculate desired voltages"

Vdesa = A*cos(we*t)

!"desired phase A voltage "

Vdesb = A*cos(we*t-pi2o3)

!"desired phase B voltage "

Vdesc = A*cos(we*t+pi2o3)

!"desired phase C voltage "

"----transform desired voltages to qd0 quantities"

Vqsdes=(2.0/3.0)*(Vdesa-0.5*Vdesb-0.5*Vdesc)

!"desired q-axis voltage"

Vdsdes=(sqrt(3.0)/3.0)*(-Vdesb+Vdesc)

!"desired d-axis voltage"

"----determine error voltages"

Vqserr=Vqsdes-VqssL

Vdserr=Vdsdes-VdssL

"----generate commanded voltages (PI Controller)"

Vqscom=(K1*Vqserr + K2*integ(Vqserr,0.0))

Vdscom=(K1*Vdserr + K2*integ(Vdserr,0.0))

"----transform commanded quantities to ABC frame"

Vacom=Vqscom

Vbcom=-0.5*Vqscom-(sqrt(3.0)/2.0)*Vdscom

Vccom=-0.5*Vqscom+(sqrt(3.0)/2.0)*Vdscom

"----normalize voltages for use in switching control"

Vacont=Vacom/Vmax

Vbcont=Vbcom/Vmax

Vccont=Vccom/Vmax

"----transform desired Voltages to synchronous qd0 quantities"

Vqsedes=(2.0/3.0)*(Vdesa*cos(thetae)+Vdesb*cos(thetae-pi2o3)+&

Vdesc*cos(thetae+pi2o3))

```

Vdsedes=(2.0/3.0)*(Vdesa*sin(thetae)+Vdesb*sin(thetae-pi2o3)+&
  Vdesc*sin(thetae+pi2o3))

"----transform actual currents to synchronous qd0 quantities"
Vqse=(2.0/3.0)*(VLa*cos(thetae)+VLb*cos(thetaepi2o3)+&
  VLc*cos(thetae+pi2o3))
Vdse=(2.0/3.0)*(VLa*sin(thetae)+VLb*sin(thetae-i2o3)+VLc*sin(thetae+pi2o3))

"----schedule inverter switching"
SCHEDULE hia.XN.(Vtri - Vacont)          !"switch A to HI state"
SCHEDULE loa.XP.(Vtri - Vacont)          !"switch A to LO state"

SCHEDULE hib.XN.(Vtri - Vbcont)          !"switch B to HI state "
SCHEDULE lob.XP.(Vtri - Vbcont)          !"switch B to LO state"

SCHEDULE hic.XN.(Vtri - Vccont)          !"switch C to HI state "
SCHEDULE loc.XP.(Vtri - Vccont)          !"switch C to LO state"

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"
Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)
Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"
piqss=(Vqss-VqssL)/Lf
pidss=(Vdss-VdssL)/Lf

"----find load voltage derivatives in stationary frame"
pVqssL=(iqss-(VqssL/Rload))/Cf
pVdssL=(idss-(VdssL/Rload))/Cf

"----calculate stationary currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)

"----calculate stationary voltages"
VqssL=integ(pVqssL,VqssLic)
VdssL=integ(pVdssL,VdssLic)

```

"----transform back to ABC quantities"

iLa=iqss

iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss

iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

VLa=VqssL

VLb=-0.5*VqssL-(sqrt(3.0)/2.0)*VdssL

VLc=-0.5*VqssL+(sqrt(3.0)/2.0)*VdssL

iLoada=VLa/RLoad

iLoadb=VLb/RLoad

iLoadc=VLc/RLoad

END ! "of derivative"

DISCRETE hia

Vag=Vdc

END ! "of discrete"

DISCRETE loa

Vag=0.0

END ! "of discrete"

DISCRETE hib

Vbg=Vdc

END ! "of discrete"

DISCRETE lob

Vbg=0.0

END ! "of discrete"

DISCRETE hic

Vcg=Vdc

END ! "of discrete"

DISCRETE loc

Vcg=0.0

END ! "of discrete"

END ! "of dynamic"

END ! "of program"

C. ACSL SIMULATION FOR CURRENT FEEDBACK CONTROLLER IN THE STATIONARY REFERENCE FRAME

PROGRAM

INITIAL

```

" This Program simulates operation of a 3-Phase hard switched inverter "
" with sine-triangle PWM. Ideal switching and components are assumed. "
" Load consists of an LC filter with a resistive load. "
" A Controller operating in the stationary reference frame is included "
" DC Voltage = 500 Volts "
" Switching Frequency = 6KHz Output Frequency = 60Hz "

MAXTERVAL maxt = 1.0e-8 !"maximum integration step size "
MININTERVAL mint = 1.0e-12 !"min time step:for var step algorithm "
CINTERVAL cint = 1.0e-7 !"data communication interval "
ALGORITHM ialg = 5 !"integration algorithm--R.K. 4th "
NSTEPS nstp = 1
CONSTANT tstop = 0.032 !"stop point for integration "
CONSTANT Lf=10.1e-3 !"filter (output) inductance "
CONSTANT Vdc=500.0 !"DC source voltage "
CONSTANT Rload=25.0 !"load resistance "
CONSTANT ftriang = 6000.0 !"reference triangle frequency "
CONSTANT Vtripk = 10.0 !"reference triangle peak value "
Ttri = 1.0/ftriang !"reference triangle period "
Tover2 = Ttri/2.0 !"reference triangle half period "
slope = 4.0*Vtripk*ftriang !"reference triangle slope "
we=60.0*2.0*3.14159265 !"radian frequency of contrlo sinusiod"
pi2o3=2.0*3.14159265/3.0 !"120 degrees in radins "
CONSTANT twopi = 3.14259265 !"360 degrees in radians "
CONSTANT iqssic=5.0 !"initial q axis current "
CONSTANT idssic=3.0 !"initial d axis current "
iLa=iqssic
ilb=-0.5*iqssic-idssic*sqrt(3.0)/2.0
ilc=-0.5*iqssic+idssic*sqrt(3.0)/2.0
Vag=0.0
Vbg=0.0
Vcg=0.0
CONSTANT K1=0.10 !"proportional gain "
CONSTANT K2=0.001 !"integral gain "
CONSTANT A=9.0 !"desired current magnitude "
Vmax=(Vdc/20.0) !"pulse width modulation gain "

```

END ! "of initial"

DYNAMIC

TERMT (t .GE. (tstop-0.5*cint))

DERIVATIVE

"----sine-triangle modulation"

tt=mod(t,Ttri) !"form ref triangle "

IF(tt.LT.Tover2) THEN

Vtri=10.0 - tt*slope

ELSE

Vtri=-10.0+slope*(tt-Tover2)

END IF

"----calculate synchronous reference frame angle"

thetae=integ(we,0.0)

"----calculate desired currents"

Idesa = A*cos(thetae) !"desired phase A current "

Idesb = A*cos(thetae-pi2o3) !"desired phase B current "

Idesc = A*cos(thetae+pi2o3) !"desired phase C current "

"----transform desired currents to stationary qd0 quantities"

Iqsdes=(2.0/3.0)*(Idesa-0.5*Idesb-0.5*Idesc)

Idsdes=(sqrt(3.0)/3.0)*(-Idesb+Idesc)

"----transform desired currents to synchronous qd0 quantities"

Iqsedes=(2.0/3.0)*(Idesa*cos(thetae)+Idesb*cos(thetae-pi2o3)&
+Idesc*cos(thetae+pi2o3))

Idsedes=(2.0/3.0)*(Idesa*sin(thetae)+Idesb*sin(thetae-pi2o3)&
+Idesc*sin(thetae+pi2o3))

"----transform actual currents to synchronous qd0 quantities"

Iqse=(2.0/3.0)*(ILa*cos(thetae)+ILb*cos(thetae-pi2o3)+ILc*cos(thetae+pi2o3))

Idse=(2.0/3.0)*(ILa*sin(thetae)+ILb*sin(thetae-pi2o3)+ILc*sin(thetae+pi2o3))

"----determine error currents in stationary reference frame"

Iqserr=Iqsdes-iqss

Idserr=Idsdes-idss

"----generate commanded currents (PI Controller)"

Iqscom=(K1*Iqserr + K2*integ(Iqserr,0.0))

Idscom=(K1*Idserr + K2*integ(Idserr,0.0))

```

"----transform commanded quantities to ABC frame"
Iacom=Iqscm
Ibcom=-0.5*Iqscm - (sqrt(3.0)/2.0)*Idscom
Iccom=-0.5*Iqscm + (sqrt(3.0)/2.0)*Idscom

"----normalize voltages for use in switching control"
Vacont=Iacom*Rload/Vmax
Vbcont=Ibcom*Rload/Vmax
Vccont=Iccom*Rload/Vmax

"----schedule inverter switching"
SCHEDULE hia.XN.(Vtri - Vacont)           !"switch A to HI state"
SCHEDULE loa.XP.(Vtri - Vacont)           !"switch A to LO state"

SCHEDULE hib.XN.(Vtri - Vbcont)           !"switch B to HI state "
SCHEDULE lob.XP.(Vtri - Vbcont)           !"switch B to LO state"

SCHEDULE hic.XN.(Vtri - Vccont)           !"switch C to HI state "
SCHEDULE loc.XP.(Vtri - Vccont)           !"switch C to LO state"

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"
Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)
Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"
piqss=(Vqss-RLoad*iqss)/Lf
pidss=(Vdss-Rload*idss)/Lf

"----calculate stationary currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)

"----transform back to ABC quantities"
iLa=iqss
iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss
iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

END ! "of derivative"

```

```
DISCRETE hia
  Vag=Vdc
END ! "of discrete"
```

```
DISCRETE loa
  Vag=0.0
END ! "of discrete"
```

```
DISCRETE hib
  Vbg=Vdc
END ! "of discrete"
```

```
DISCRETE lob
  Vbg=0.0
END ! "of discrete"
```

```
DISCRETE hic
  Vcg=Vdc
END ! "of discrete"
```

```
DISCRETE loc
  Vcg=0.0
END ! "of discrete"
```

```
END ! "of dynamic"
```

```
END ! "of program"
```

D. ACSL SIMULATION FOR CURRENT FEEDBACK CONTROLLER IN THE SYNCHRONOUS REFERENCE FRAME

PROGRAM

INITIAL

```

"-----This Program simulates operation of a 3-Phase hard switched inverter "
" with sine-triangle PWM. Ideal switching and components are assumed."
" Load consists of an LC filter with a resistive load. "
" A Controller operating in the stationary reference frame is included "
" DC Voltage = 500 Volts "
" Switching Frequency = 6KHz Output Frequency = 60Hz "

MAXTERVAL maxt = 1.0e-8 !"maximum integration step size "
MININTERVAL mint = 1.0e-12 !"min time step:for var step algorithm "
CINTERVAL cint = 1.0e-7 !"data communication interval "
ALGORITHM ialg = 5 !"integration algorithm--R.K. 4th "
NSTEPS nstp = 1
CONSTANT tstop = 0.032 !"stop point for integration "
CONSTANT Lf=10.1e-3 !"filter (output) inductance "
CONSTANT Vdc=500.0 !"DC source voltage "
CONSTANT Rload=25.0 !"load resistance "
CONSTANT ftriang = 6000.0 !"reference triangle frequency "
CONSTANT Vtripk = 10.0 !"reference triangle peak value "
Ttri = 1.0/ftriang !"reference triangle period "
Tover2 = Ttri/2.0 !"reference triangle half period "
slope = 4.0*Vtripk*ftriang !"reference triangle slope "
we=60.0*2.0*3.14159265 !"radian frequency of contrlo sinusiod"
pi2o3=2.0*3.14159265/3.0 !"120 degrees in radians "
CONSTANT twopi = 3.14259265 !"360 degrees in radians "
CONSTANT iqssic=5.0 !"initial q axis current "
CONSTANT idssic=3.0 !"initial d axis current "
iLa=iqssic
ilb=-0.5*iqssic-idssic*sqrt(3.0)/2.0
ilc=-0.5*iqssic+idssic*sqrt(3.0)/2.0
Vag=0.0
Vbg=0.0
Vcg=0.0
CONSTANT K1=0.10 !"proportional gain "
CONSTANT K2=0.001 !"integral gain "
CONSTANT A=9.0 !"desired current magnitude "
Vmax=(Vdc/20.0) !"pulse width modulation gain "

```

END ! "of initial"

DYNAMIC

TERMT (t .GE. (tstop-0.5*cint))

DERIVATIVE

"----sine-triangle modulation"

tt=mod(t,Ttri)

!"form ref triangle "

IF(tt.LT.Tover2) THEN

Vtri=10.0 - tt*slope

ELSE

Vtri=-10.0+slope*(tt-Tover2)

END IF

"----calculate synchronous reference frame angle"

thetae=integ(we,0.0)

"----calculate desired currents"

Idesa = A*cos(thetae)

!"desired phase A current "

Idesb = A*cos(thetae-pi2o3)

!"desired phase B current "

Idesc = A*cos(thetae+pi2o3)

!"desired phase C current "

"----transform desired currents to synchronous qd0 quantities"

Iqsdes=(2.0/3.0)*(Idesa*cos(thetae)+Idesb*cos(thetae-pi2o3)+&
Idesc*cos(thetae+pi2o3))

Idsdes=(2.0/3.0)*(Idesa*sin(thetae)+Idesb*sin(thetae-pi2o3)+&
Idesc*sin(thetae+pi2o3))

"----transform actual currents to synchronous qd0 quantities"

Iqse=(2.0/3.0)*(ILa*cos(thetae)+ILb*cos(thetae-pi2o3)+ILc*cos(thetae+pi2o3))

Idse=(2.0/3.0)*(ILa*sin(thetae)+ILb*sin(thetae-pi2o3)+ILc*sin(thetae+pi2o3))

"----determine error currents"

Iqserr=Iqsdes-iqse

Idserr=Idsdes-idse

"----generate commanded currents (PI Controller)"

Iqscom=(K1*Iqserr + K2*integ(Iqserr,0.0))

Idscom=(K1*Idserr + K2*integ(Idserr,0.0))

"----transform commanded quantities to ABC frame"

Iacom=Iqscom*cos(thetae)+ Idscom*sin(thetae)

Ibcom=Iqscom*cos(thetae-pi2o3) + Idscom*sin(thetae-pi2o3)

Iccom=Iqscom*cos(thetae+pi2o3) + Idscom*sin(thetae+pi2o3)

```

"----normalize voltages for use in switching control"
Vacont=Iacom*Rload/Vmax
Vbcont=Ibcom*Rload/Vmax
Vccont=Iccom*Rload/Vmax

"----schedule inverter switching"
SCHEDULE hia.XN.(Vtri - Vacont)           !"switch A to HI state "
SCHEDULE loa.XP.(Vtri - Vacont)           !"switch A to LO state"

SCHEDULE hib.XN.(Vtri - Vbcont)           !"switch B to HI state "
SCHEDULE lob.XP.(Vtri - Vbcont)           !"switch B to LO state"

SCHEDULE hic.XN.(Vtri - Vccont)           !"switch C to HI state "
SCHEDULE loc.XP.(Vtri - Vccont)           !"switch C to LO state"

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"
Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)
Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"
piqss=(Vqss-RLoad*iqss)/Lf
pidss=(Vdss-Rload*idss)/Lf

"----calculate stationary currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)

"----transform back to ABC quantities"
iLa=iqss
iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss
iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

END ! "of derivative"

DISCRETE hia
  Vag=Vdc
END ! "of discrete"

```

DISCRETE loa
Vag=0.0
END !"of discrete"

DISCRETE hib
Vbg=Vdc
END !"of discrete"

DISCRETE lob
Vbg=0.0
END !"of discrete"

DISCRETE hic
Vcg=Vdc
END !"of discrete"

DISCRETE loc
Vcg=0.0
END !"of discrete"

END !"of dynamic"

END !"of program"

E. MATLAB SIMULATION FOR VOLTAGE CONTROLLER WITH INNER CURRENT CONTROL LOOP

```

% Voltage Controller with Inner Current Control Loop
% State Space Model

% States
%
% [xvqe xvde xiqe xide Vloadqe Vloadde iloadqe iloadde ilqe ilde]'
%

%% Gains %%

Kpv = 0.25    % Voltage Proportional Gain
Kiv = 1.0     % Voltage Integral Gain
Kpc = 10.0   % Current Proportional Gain
Kic = 1.0    % Current Integral Gain
Kpwm=1.0     % PWM Gain
U=50.0       % Magnitude of Step Change

%% Simulation Parameters %%

we= 2*pi*60; % Electrical Frequency
Lf = .0101;  % Filter Inductance
Cf = .0001;  % Filter Capacitance
Rload = 25;  % Load Resistance
Lload = .0001;% Load Inductance

%% System Matrices %%

A=[0, 0, 0, 0, -1, 0, 0, 0, 0, 0;
   0, 0, 0, 0, 0, -1, 0, 0, 0, 0;
   Kiv, 0, 0, 0, -Kpv, 0, 1, 0, -1, 0;
   0, Kiv, 0, 0, 0, -Kpv, 0, 1, 0, -1;
   0, 0, 0, 0, 0, -we, -1/Cf, 0, 1/Cf, 0;
   0, 0, 0, 0, we, 0, 0, -1/Cf, 0, 1/Cf;
   0, 0, 0, 0, 1/Lload, 0, -Rload/Lload, -we, 0, 0;
   0, 0, 0, 0, 0, 1/Lload, we, -Rload/Lload, 0, 0;
   Kpc*Kiv*Kpwm/Lf, we*Kic*Kpwm, Kic*Kpwm/Lf, 0, ((1-Kpc*Kpv)*Kpwm-1)/Lf,
   -Kpv*we*Kpwm, Kpc*Kpwm/Lf, we*Kpwm, -Kpc*Kpwm/Lf, -we;
   -we*Kiv*Kpwm; Kpc*Kiv*Kpwm/Lf, 0, Kic*Kpwm/Lf; Kpv*we*Kpwm,
   ((1-Kpc*Kpv)*Kpwm-1)/Lf, -we*Kpwm, Kpc*Kpwm/Lf, we, -Kpc*Kpwm/Lf;];

```

```

B=[1, 0, Kpv -we*Cf, 0, 0, 0, 0, Kpwm*(Kpc*Kpv/Lf-(we*we*Cf)),
  -Kpwm*(Kpc*we*Cf/Lf+Kpv*we)];

C=U*[0 0 0 0 1 0 0 0 0];

D=[0];

%% Determine Poles and Zeros %%
[num,den]=ss2tf(A,B,C,D);
R=roots(den)
P=roots(num)

%% Display Step Response %%
figure(1)
step(A,B,C,D,1)
title(['Kpv=',num2str(Kpv),' Kpc=',num2str(Kpc),' Kiv=',num2str(Kiv),
  ' Kic=',num2str(Kic)])

```

F. ACSL SIMULATION FOR VOLTAGE CONTROLLER WITH INNER CURRENT CONTROL LOOP

PROGRAM

INITIAL

```

"-----This Program simulates operation of a 3-Phase hard switched inverter "
" with sine-triangle PWM. Ideal switching and components are assumed."
" Load consists of an LC filter with an LR load. A current controlled "
" voltage regulated pulse width modulation (VRPWM) control scheme "
" is implimented in the synchronous reference frame. "
" DC Voltage 500 Volts          VRPWM Control "
" Switching Frequency = 6kHz    Output Frequency = 60Hz "

MAXTERVAL maxt = 1.0e-8          !"maximum integration step size "
MINTERVAL mint = 1.0e-12        !"min time step:for var step algorithm "
CINTERVAL cint = 1.0e-7         !"data communication interval "
ALGORITHM ialg = 5              !"integration algorithm--R.K. 4th "
NSTEPS nstp = 1
CONSTANT tstop = 0.03           !"stop point for integration "

CONSTANT Lf=10.1e-3             !"filter (output) inductance "
CONSTANT CF=1.0e-4              !"filter (output) capacitance "
CONSTANT Vdc=500.0              !"DC source voltage "
CONSTANT Rload=25.0             !"load resistance "
CONSTANT Lload=0.1e-3           !"load inductance "
CONSTANT ftriang = 6000.0       !"reference triangle frequency "
CONSTANT Vtripk = 10.0          !"reference triangle peak value "
Ttri = 1.0/ftriang              !"reference triangle period "
Tover2 = Ttri/2.0               !"reference triangle half period "
slope = 4.0*Vtripk*ftriang      !"reference triangle slope "
we=60.0*2.0*3.14159265          !"radian frequency of control sinusiod"
pi2o3=2.0*3.14159265/3.0        !"120 degrees in radians "
twopi=2.0*3.14159265            !"360 degrees in radians "
CONSTANT iqssic=0.0!5.5         !"initial q axis converter current "
CONSTANT idssic=0.0!6.0         !"initial d axis converter current "
CONSTANT iqssLic=0.0!6.0        !"initial q axis load current "
CONSTANT idssLic=0.0            !"initial d axis load current "
CONSTANT Kpv = 1.0              !"voltage loop proportional gain "
CONSTANT Kiv = 1.0              !"voltage loop integral gain "
CONSTANT Kpc = 1.0              !"current loop proportional gain "
CONSTANT Kic = 1.0              !"current loop integral gain "
iLa=iqssic
ilb=-0.5*iqssic-idssic*sqrt(3.0)/2.0

```

```

ilc=-0.5*iqssic+idssic*sqrt(3.0)/2.0
CONSTANT VqssLic=150.0
CONSTANT VdssLic=0.0
Vag=0.0
Vbg=0.0
Vcg=0.0
CONSTANT Vcom=150.0
Vmax=(Vdc/(2.0*Vtriplk))
END ! "of initial"

DYNAMIC
  TERMT (t .GE. (tstop-0.5*cint))

DERIVATIVE
  "----sine-triangle modulation"
  tt=mod(t,Ttri)                                !"form ref triangle  "
  IF(tt.LT.Tover2) THEN
    Vtri=10.0 - tt*slope
  ELSE
    Vtri=-10.0+slope*(tt-Tover2)
  END IF

  "----calculate synchronous reference frame angle"
  thetai=mod(integ(we,0.0),twopi)

  "----calculate feedforward capacitor current"
  icqcom=(Vcom-VqssL)*Kpv + integ(Vcom-VqssL,0.0)*Kiv
  icdcom=-VdssL*Kpv - integ(VdssL,0.0)*Kiv - Vcom*we*Cf

  "----calculate feedforward current"
  ifqcom=icqcom + iqssL
  ifdcom=icdcom + idssL

  "----calculate feedback current error"
  iqerr=ifqcom - iqss
  iderr=ifdcom - idss

  "----calculate voltage control signals"
  Vgq=iqerr*Kpc + integ(iqerr,0.0)*Kic + we*Lf*ifdcom + VqssL
  Vgd=iderr*Kpc + integ(iderr,0.0)*Kic - we*Lf*ifqcom + VdssL

  "----transform control quantities to ABC frame"
  Vacom=Vgq*cos(thetae) + Vgd*sin(thetae)
  Vbcom=Vgq*cos(thetae-pi2o3) + Vgd*sin(thetae-pi2o3)
  Vccom=Vgq*cos(thetae+pi2o3) + Vgd*sin(thetae+pi2o3)

```

```

"----normalize voltages for use in switching control"
Vacont=Vacom/Vmax
Vbcont=Vbcom/Vmax
Vccont=Vccom/Vmax

"----schedule inverter switching"
SCHEDULE hia.XN.(Vtri - Vacont)           !"switch A to HI state "
SCHEDULE loa.XP.(Vtri - Vacont)           !"switch A to LO state"

SCHEDULE hib.XN.(Vtri - Vbcont)           !"switch B to HI state "
SCHEDULE lob.XP.(Vtri - Vbcont)           !"switch B to LO state"

SCHEDULE hic.XN.(Vtri - Vccont)           !"switch C to HI state "
SCHEDULE loc.XP.(Vtri - Vccont)           !"switch C to LO state"

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to synchronous reference frame"
Vqss=(2.0/3.0)*(Vas*cos(thetae)+Vbs*cos(thetae-i2o3)+Vcs*cos(thetae+pi2o3))
Vdss=(2.0/3.0)*(Vas*sin(thetae)+Vbs*sin(thetae-pi2o3)+Vcs*sin(thetae+pi2o3))

"----find converter current derivatives in synchronous frame"
piqss=-we*idss + (Vqss-VqssL)/Lf
pidss= we*iqss + (Vdss-VdssL)/Lf

"----find load current derivatives in synchronous frame"
piqssL=-we*idssL + (VqssL-Rload*iqssL)/Lload
pidssL= we*iqssL + (VdssL-Rload*idssL)/Lload

"----find load voltage derivatives in synchronous frame"
pVqssL=-we*VdssL + (iqss-iqssL)/Cf
pVdssL= we*VqssL + (idss-idssL)/Cf

"----calculate synchronous converter currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)

"----calculate synchronous load currents"
iqssL=integ(piqssL,iqssLic)
idssL=integ(pidssL,idssLic)

```

```

"----calculate synchronous load voltages"
VqssL=integ(pVqssL,VqssLic)
VdssL=integ(pVdssL,VdssLic)

"----transform back to ABC quantities"
iLa=iqss*cos(thetae)+ idss*sin(thetae)
iLb=iqss*cos(thetae-pi2o3) + idss*sin(thetae-pi2o3)
iLc=iqss*cos(thetae+pi2o3) + idss*sin(thetae+pi2o3)

VLa=VqssL*cos(thetae)+ VdssL*sin(thetae)
VLb=VqssL*cos(thetae-pi2o3) + VdssL*sin(thetae-pi2o3)
VLc=VqssL*cos(thetae+pi2o3) + VdssL*sin(thetae+pi2o3)

iLoada=iqssL*cos(thetae)+ idssL*sin(thetae)
iLoadb=iqssL*cos(thetae-pi2o3) + idssL*sin(thetae-pi2o3)
iLoadc=iqssL*cos(thetae+pi2o3) + idssL*sin(thetae+pi2o3)

END ! "of derivative"

DISCRETE hia
  Vag=Vdc
END ! "of discrete"

DISCRETE loa
  Vag=0.0
END ! "of discrete"

DISCRETE hib
  Vbg=Vdc
END ! "of discrete"

DISCRETE lob
  Vbg=0.0
END ! "of discrete"

DISCRETE hic
  Vcg=Vdc
END ! "of discrete"

DISCRETE loc
  Vcg=0.0
END ! "of discrete"

END ! "of dynamic"
END ! "of program"

```


APPENDIX E. SPACE VECTOR CONTROL SIMULATION PROGRAM

PROGRAM

INITIAL

```

"   This Program simulates operation of a 3-Phase hard switched inverter   "
"   w/ Space Vector PWM. Ideal switching and components are assumed."

MAXTERVAL maxt = 1.0e-8           !"maximum integration step size      "
MININTERVAL mint = 1.0e-12        !"min time step for var step algorithm"
CINTERVAL cint = 1.0e-7           !"data communication interval       "
ALGORITHM ialg = 5                 !"integration algorithm--R.K. 4th   "
CONSTANT tstop = 0.03              !"stop point for integration        "

CONSTANT Lf=10.1e-3                !"filter (output) inductance       "
CONSTANT CF=1.0e-4                 !"filter (output) capacitance      "
CONSTANT Vdc=500.0                 !"DC source voltage                 "
CONSTANT Rload=25.0                !"load resistance                   "
CONSTANT fswitch = 6000.0          !"reference switch frequency        "
LOGICAL sequence                   !"true = 7 to 8                     "
sequence=.true.                    !"initialization                    "
state=7                             !"starting switch configuration     "
Tsw = 1.0/fswitch                  !"reference switching period        "
wosin=60.0*2.0*3.14159265          !"radian frequency of desired sinusiod"
r150=5.0*3.14159265/6.0             !"150 degrees in radians           "
r120=2.0*3.14159265/3.0            !"120 degrees in radians           "
r90=3.14159265/2.0                 !"90 degrees in radians            "
r60=3.14159265/3.0                !"60 degrees in radians            "
r30=3.14159265/6.0                !"30 degrees in radians            "
rm30=-3.14159265/6.0              !" -30 degrees in radians          "
rm90=-3.14159265/2.0              !" -90 degrees in radians          "
rm150=-5.0*3.14159265/6.0         !" -150 degrees in radians         "
CONSTANT iqssic=8.0                !"initial q axis current           "
CONSTANT idssic=3.0                !"initial d axis current           "
CONSTANT AA=100.0                  !"commanded voltage magnitude      "
iLa=iqssic
iLb=-0.5*iqssic-idssic*sqrt(3.0)/2.0
iLc=-0.5*iqssic+idssic*sqrt(3.0)/2.0
CONSTANT VqssLic=200.0
CONSTANT VdssLic=0.0

```

```

VLa=VqssL
VLb=-0.5*VqssLic-(sqrt(3.0)/2.0)*VdssLic
VLC=-0.5*VqssLic+(sqrt(3.0)/2.0)*VdssLic
Vag=0.0
Vbg=0.0
Vcg=0.0

```

END ! "of initial"

DYNAMIC

```

TERMT (t .GE. (tstop-0.5*cint))

```

DERIVATIVE

```

"----space vector modulation"

```

```

Vcosa = AA*cos(wosin*t)           !"des phase A Voltage"

```

```

Vcosb = AA*cos(wosin*t-r120)      !"des phase B Voltage"

```

```

Vcosc = AA*cos(wosin*t+r120)      !"des phase C Voltage"

```

```

Vq=(2.0/3.0)*(Vcosa-0.5*Vcosb-0.5*Vcosc) !"des q-axis voltage  "

```

```

Vd=(sqrt(3.0)/3.0)*(-Vcosb+Vcosc)      !"des d-axis voltage  "

```

```

"----determine sextant of operation"

```

```

beta=atan2(Vd,Vq)

```

```

IF((beta.GT.r90).AND.(beta.LT.r150)) THEN

```

```

    sextant=1

```

```

ELSE IF ((beta.GT.r150).OR.(beta.LT.rm150)) THEN

```

```

    sextant=2

```

```

ELSE IF ((beta.GT.rm150).AND.(beta.LT.rm90)) THEN

```

```

    sextant=3

```

```

ELSE IF ((beta.GT.rm90).AND.(beta.LT.rm30)) THEN

```

```

    sextant=4

```

```

ELSE IF ((beta.GT.rm30).AND.(beta.LT.r30)) THEN

```

```

    sextant=5

```

```

ELSE

```

```

    sextant=6

```

```

END IF

```

```

"----calculate switching times"

```

```

Vbar=sqrt(Vq**2+Vd**2)           !"desired magnitude  "

```

```

IF (Vbar.gt.Vdc) THEN           !"limit magnitude  "

```

```

    Vbar=Vdc

```

```

END IF

```

```

IF (beta.GT.0.0) THEN
  gamma=mod(atan2(Vd,Vq),r60)           !"desired angle      "
ELSE
  gamma=mod(atan2(Vd,Vq),r60)+r60
END IF

a=Vbar/Vdc
K=Tsw*a/sin(r60)

IF (sequence) THEN
  t1=bound(5e-6,Tsw,K*sin(r60-gamma))
  t2=bound(5e-6,Tsw,K*sin(gamma))
ELSE
  t1=bound(5e-6,Tsw,K*sin(gamma))
  t2=bound(5e-6,Tsw,K*sin(r60-gamma))
END IF

tzero=(Tsw-(t1+t2))/2.0

"----generate switching of inverter"
tt=mod(t,Tsw)
SCHEDULE switcht1.xp.tt-tzero
SCHEDULE switcht2.xp.tt-(t1+tzero)
SCHEDULE switcht3.xp.tt-(t1+t2+tzero)

"----calculate line voltages"
Vas=(2.0/3.0)*Vag - (1.0/3.0)*(Vbg + Vcg)
Vbs=(2.0/3.0)*Vbg - (1.0/3.0)*(Vag + Vcg)
Vcs=(2.0/3.0)*Vcg - (1.0/3.0)*(Vag + Vbg)

"----transform to stationary reference frame"
Vqss=(2.0/3.0)*(Vas-0.5*Vbs-0.5*Vcs)
Vdss=(sqrt(3.0)/3.0)*(-Vbs+Vcs)

"----find current derivatives in stationary frame"
piqss=(Vqss-VqssL)/Lf
pidss=(Vdss-VdssL)/Lf

"----find load voltage derivatives in stationary frame"
pVqssL=(iqss-(VqssL/Rload))/Cf
pVdssL=(idss-(VdssL/Rload))/Cf

```

```

"----calculate stationary currents"
iqss=integ(piqss,iqssic)
idss=integ(pidss,idssic)

"----calculate stationary voltages"
VqssL=integ(pVqssL,VqssLic)
VdssL=integ(pVdssL,VdssLic)

"----transform back to ABC quantities"
iLa=iqss
iLb=-0.5*iqss-(sqrt(3.0)/2.0)*idss
iLc=-0.5*iqss+(sqrt(3.0)/2.0)*idss

VLa=VqssL
VLb=-0.5*VqssL-(sqrt(3.0)/2.0)*VdssL
VLc=-0.5*VqssL+(sqrt(3.0)/2.0)*VdssL

iLoada=VLa/RLoad
iLoadb=VLb/RLoad
iLoadc=VLc/RLoad

```

END ! "of derivative"

```

DISCRETE switcht1
IF (sequence) THEN
  IF ((sextant.EQ.1).OR.(sextant.EQ.2)) THEN
    Vcg=0.0
    state=2
  ELSE IF ((sextant.EQ.3).OR.(sextant.EQ.4)) THEN
    Vag=0.0
    state=4
  ELSE
    Vbg=0.0
    state=6
  END IF
ELSE
  IF ((sextant.EQ.1).OR.(sextant.EQ.6)) THEN
    Vag=Vdc
    state=1
  ELSE IF ((sextant.EQ.2).OR.(sextant.EQ.3)) THEN
    Vbg=Vdc
    state=3
  ELSE
    Vcg=Vdc
    state=5

```

```
END IF
END IF
END ! "of discrete"
```

```
DISCRETE switcht2
```

```
IF (.not.sequence) THEN
  IF ((sextant.EQ.1).OR.(sextant.EQ.2)) THEN
    if (state.EQ.1) then
      Vbg=Vdc
    else
      Vag=Vdc
    end if
    state=2
  ELSE IF ((sextant.EQ.3).OR.(sextant.EQ.4)) THEN
    if (state.EQ.3) then
      Vcg=Vdc
    else
      Vbg=Vdc
    end if
    state=4
  ELSE
    if (state.EQ.5) then
      Vag=Vdc
    else
      Vcg=Vdc
    end if
    state=6
  END IF
ELSE
  IF ((sextant.EQ.1).OR.(sextant.EQ.6)) THEN
    if (state.EQ.2) then
      Vbg=0.0
    else
      Vcg=0.0
    end if
    state=1
  ELSE IF ((sextant.EQ.2).OR.(sextant.EQ.3)) THEN
    if (state.EQ.2) then
      Vag=0.0
    else
      Vcg=0.0
    end if
    state=3
  ELSE
    if (state.EQ.4) then
```

```
        Vbg=0.0
    else
        Vag=0.0
    end if
    state=5
END IF
END IF
END ! "of discrete"
```

```
DISCRETE switcht3
IF (state.EQ.1) THEN
    Vag=0.0
    state=8
    sequence=.false.
ELSE IF (state.EQ.2) THEN
    Vcg=Vdc
    state=7
    sequence=.true.
ELSE IF (state.EQ.3) THEN
    Vbg=0.0
    state=8
    sequence=.false.
ELSE IF (state.EQ.4) THEN
    Vag=Vdc
    state=7
    sequence=.true.
ELSE IF (state.EQ.5) THEN
    Vcg=0.0
    state=8
    sequence=.false.
ELSE
    Vbg=Vdc
    state=7
    sequence=.true.
END IF
END ! "of discrete"
```

```
END ! "of dynamic"
```

```
END ! "of program"
```

APPENDIX F. SIMULINK PROGRAMS

A. STATIONARY REFERENCE FRAME CONTROLLER

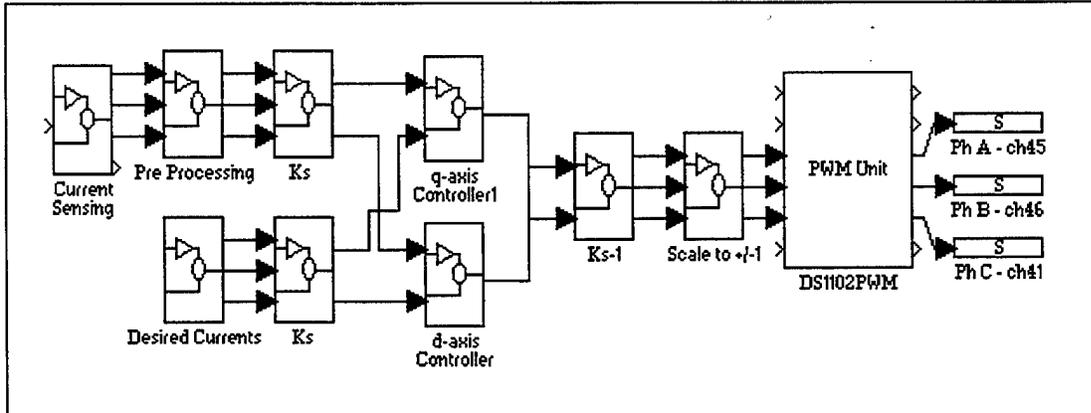


Figure F-1 - Stationary Controller

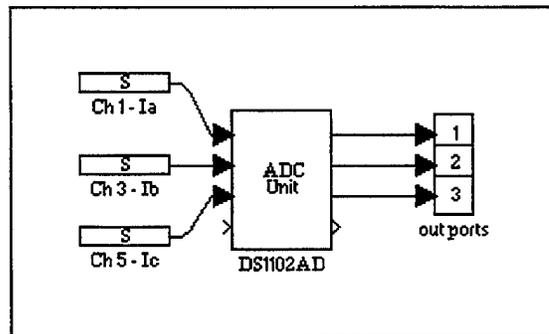


Figure F-2 - Current Sensing Block

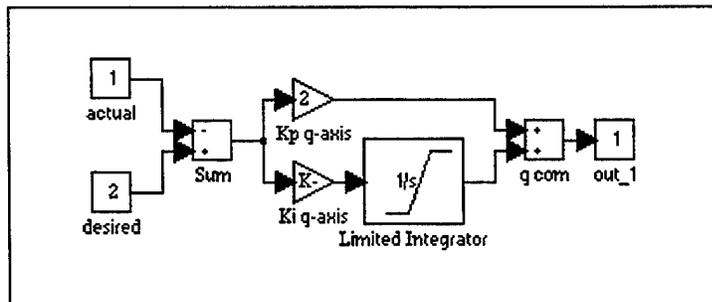


Figure F-3 - Controller Block

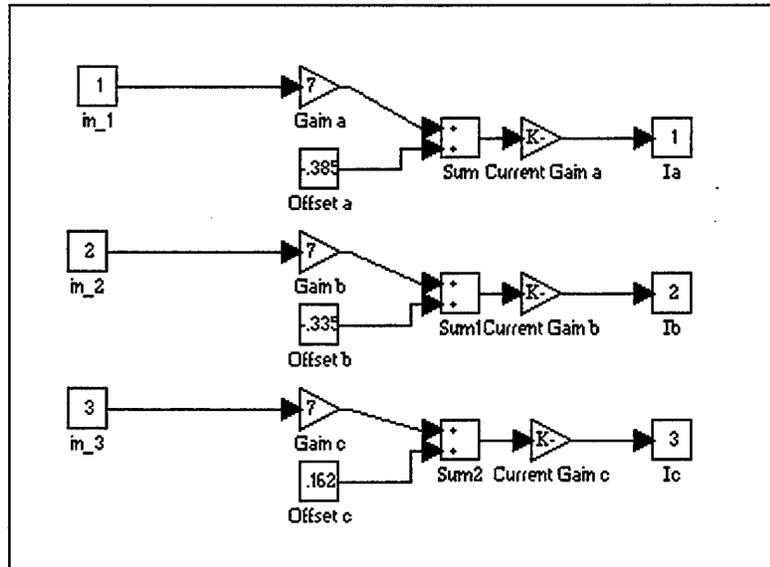


Figure F-4 - Pre-Processing Block

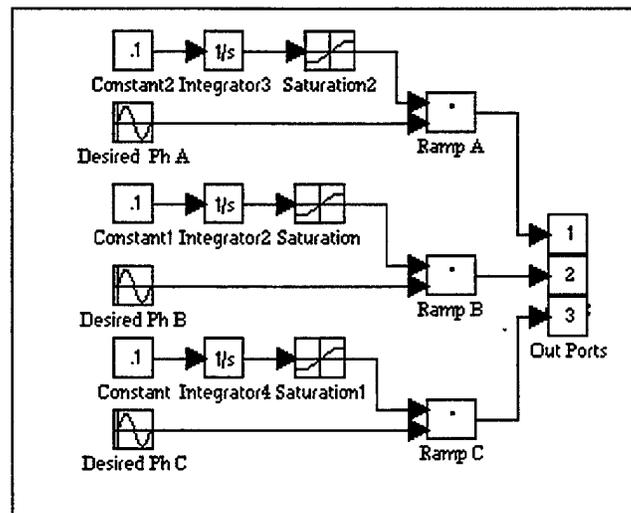


Figure F-5 - Desired Currents Block

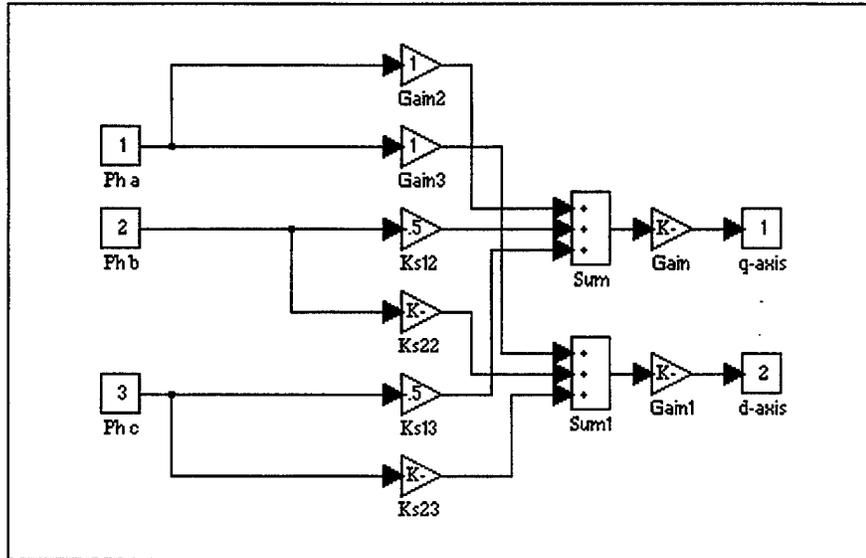


Figure F-6 - Ks Block

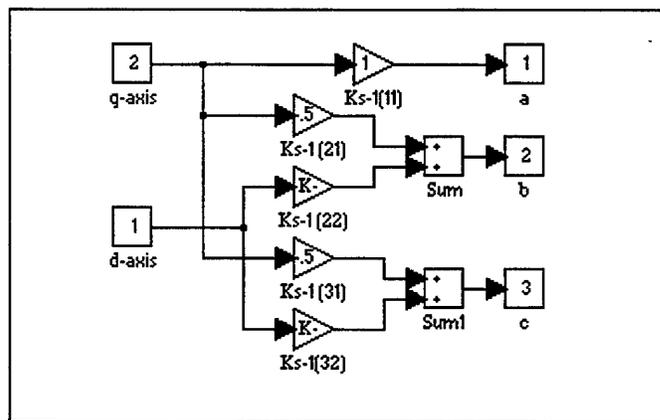


Figure F-7 - Ks Inverse Block

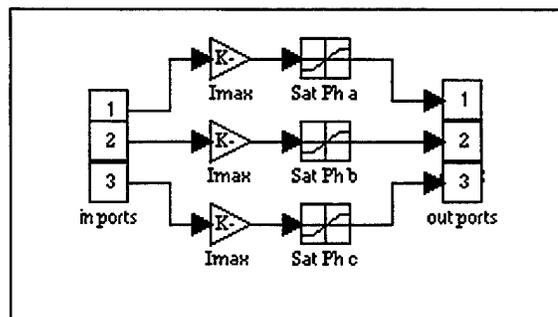


Figure F-8 - Scale to ± 1 Block

B. SYNCHRONOUS REFERENCE FRAME CONTROLLER

The Current Sensing, Pre-Processing, Controller and Scale to ± 1 blocks for the synchronous controller are the same as in the stationary controller above. Blocks Ke, Desired Currents and Ke Inverse are shown here.

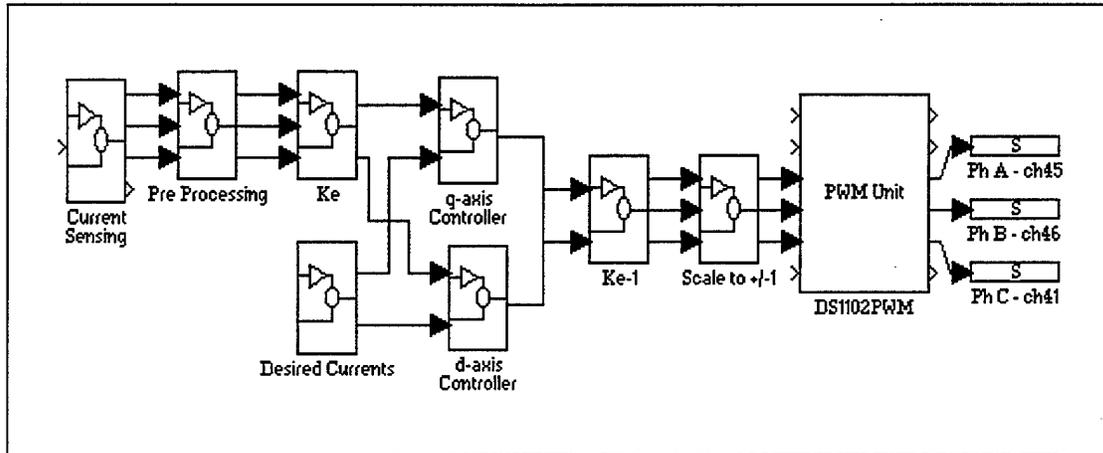


Figure F-9 - Synchronous Controller

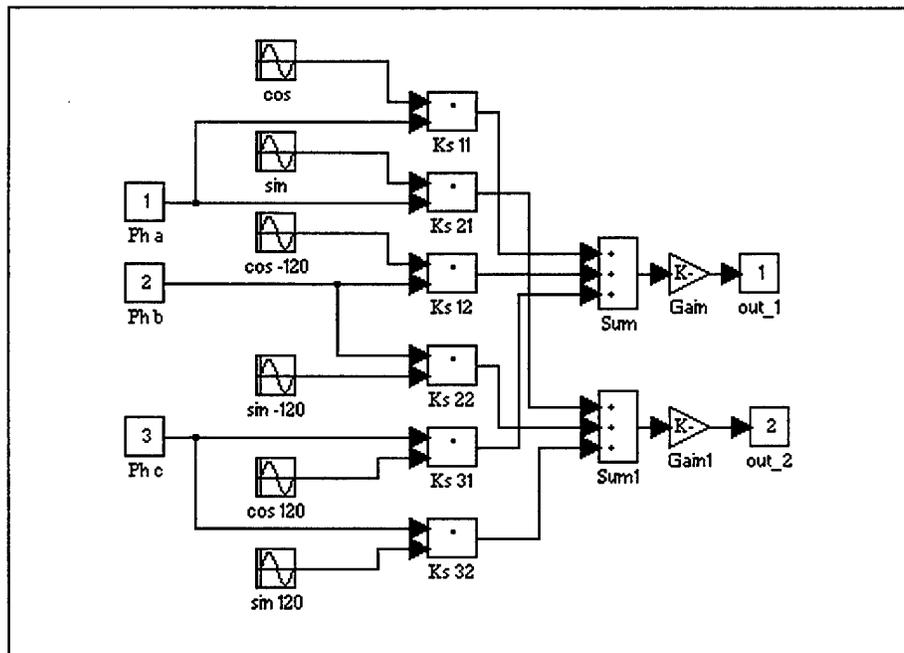


Figure F-10 - Ke Block

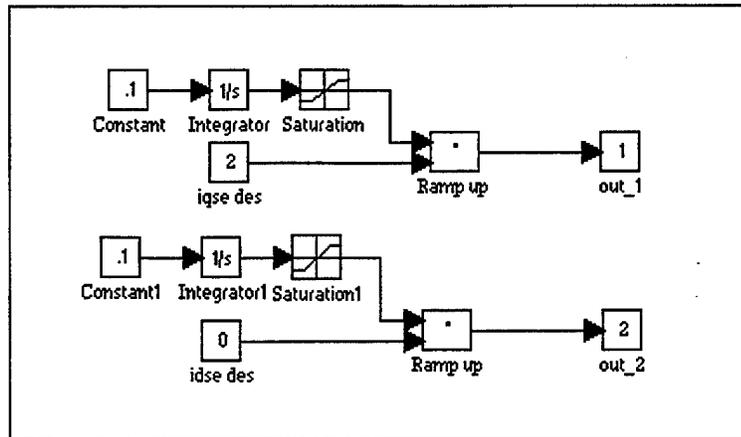


Figure F-11 - Desired Currents Block

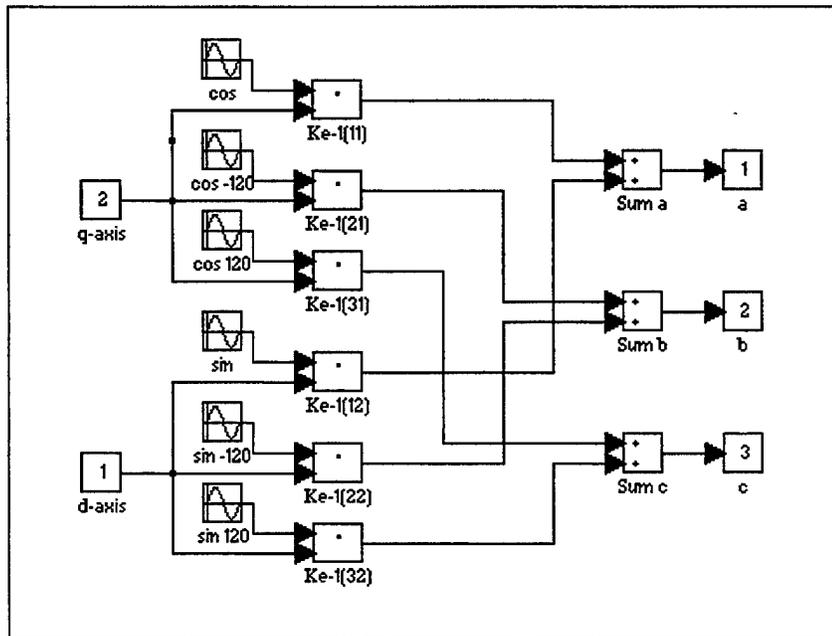


Figure F-12 - Ke Inverse Block

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