**REPORT DOCUMENTATION PAGE**

**1. AGENCY USE ONLY (LEAVE BLANK) 2. REPORT DATE 3. REPORT TYPE AND DATES COVERED**
Final 1-1-92 to 2-29-96

**4. TITLE AND SUBTITLE**
Reliability Management through Testing

**5. FUNDING NUMBERS**
N00014-92-J-1662
(R&T $400012srf)

**6. AUTHOR(S)**
Yashwant K. Malaiya

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
Colorado State University
Fort Collins, CO 80525

**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
Office of Naval Research, Code 314
800 North Quincy Street
Arlington, VA 22217-5660

**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**

**11. SUPPLEMENTARY NOTES**

**12. DISTRIBUTION/AVAILABILITY STATEMENT**
Unlimited

**13. ABSTRACT (Maximum 200 words)**
This final report mentions the research results of this project. They are grouped into technology-specific testing, IPPQ Testing, fault modeling and testing of storage elements and arrays and reliability growth for design faults.

**14. SUBJECT TERMS**
Reliability, Testing, VLSI, Design faults

**15. NUMBER OF PAGES**
cover + 8

**16. PRICE CODE**

**17. SECURITY CLASSIFICATION OF REPORT**
Unclassified

**18. SECURITY CLASSIFICATION OF THIS PAGE**
Unclassified

**19. SECURITY CLASSIFICATION OF ABSTRACT**
Unclassified

**20. LIMITATION OF ABSTRACT**
UL

DTIC QUALITY INSPECTED 

**Standard Form 298 (Rev. 2-89)***

**Prepared for: DROU§**

**Date 02/23/97 15:27 3505 277 3769 UNR ALBUQUERQUE**
RELIABILITY MANAGEMENT THROUGH TESTING

FINAL REPORT

BMDO/IST
ONR


PI: Yashwant K. Malaiya
Colorado State University
Fort Collins CO 80523
1 Abstract

This objective of this project was to develop methods for achieving high reliability through testing. We looked at both technology dependent faults and design faults. Testing is used as the major approach to identify faults.

The project looked at testing at multiple levels. Some of the investigations were carried out at the transistor level. We also examined the problem of testing at the chip level where we used some of the results obtained at the lower level. The technologies examined were primarily CMOS and BiCMOS. We have taken a critical look at faults in the storage elements, which have not been examined by the researchers before. Some of the results were extended for memory systems which are arrays of storage elements. We also looked at IDDQ based testing, which is a new approach that is now receiving considerable attention.

Design faults are the primary source of software failures. They are now also becoming important for complex hardware designs. We have looked at testing based techniques for eliminating design faults as well as methods to evaluate the effectiveness of such testing.

We have obtained a number of ground-breaking results which have been reported in the literature. We expect that our work will influence not only the research being conducted at industrial or research organizations but also commercial implementations.

The research results are broadly classified in the next section.

2 Research Results

The related publications are indicated by the numbers as used in the list of publications below.

2.1 Technology Specific Testing

The major focus here has been on BiCMOS technology. In this technology, some of the limitations of CMOS are overcome by use of bipolar technology. We have identified some specific testing problems with BiCMOS. The problem of transistor level fault modeling is addressed in [2,6,22,39,41]. A new testable design for stuck-open faults is presented in [5,21]. Test generation for BiCMOS is considered in [1,3,19,24]. A new high-speed BiCMOS domino technology is presented in [7]. In addition fault modeling in ECL devices was addressed in [2,23,29].

2.2 IDDQ Testing

The quiescent power supply current IDDQ is very sensitive to some of the important kinds of failure modes in VLSI. IDDQ testing has now been accepted in industry and has started to play a significant role in achieving low reject rates with a limited testing time. We have examined the issues of resolution available with IDDQ testing in [12, 32]. The impact of Built-in Current sensors is evaluated in [18]. We have developed a new static memory architecture that allows high speed IDDQ testing [8,Pat.1]. It uses differential monitoring of elevated IDDQ and allows blocks to be accessed in parallel for high speed testing.
2.3 Storage elements/arrays

In the past only limited attention had been paid to faults within the storage elements. We have examined the affect of transistor level defects in storage elements and have shown that some of the resulting faulty behavior patterns can not be modeled by existing models [2,25,29,34,40]. We have also examined fault modeling in static RAMs which are arrays of storage elements [8,9,14,30]. The papers [13,31] address testing of unclocked circuits.

2.4 Reliability Growth for Design faults

Some experimental software failure data has now began to become available that allows us to develop accurate models and techniques for evaluating reliability growth. The hardware verification community has started to look at software testing based techniques. Our results on reliability growth models and computational techniques have been reported in [17,26,28,36]. The papers [35,37,38,book-chapter2] report that in some cases, neural net technique can be effectively used to project software reliability. Different testing strategies can very significantly vary in effectiveness, [4,5,16,20,42,43] look at related issues. Our work on static estimation [4,20,33,42] include a new model for fault exposure ratio. A new test generation approach termed Antirandom Testing is reported in [10]. Preliminary ideas on a new integrated software tool were presented in [11]. A new model for calculating reliability using test coverage has been proposed and evaluated in [16].

3 Publications

3.1 Books/Book Chapters


4 Patents


4.1 Papers


4.2 Invention Disclosures reported to CSU:


(b) "BiCMOS Domino: A Novel High-Speed Dynamic BiCMOS Logic Family," A.P. Jayasumana, Y.K. Malaiya and S.M. Menon, 1993

5 Technical & Professional Recognitions/Contributions by PI

5.1 Conferences

(a) General Chair, The Fourth International Symposium on Software Reliability Engineering (ISSRE), Denver, Nov. 1993.

(b) General Chair, Sixth International Conference on VLSI Design (VLSI Design '93), Bombay, India, 1993.

(c) Program Chair, Fifth International Conference on VLSI Design (VLSI Design '92), Bangalore, India, 1992.

(d) General Chair, IEEE International Workshop on IDDQ Testing (IDDQ-95), Washington D.C., October 1995.


5.2 Editing (Periodicals)


- Editor, MicroArch (-93)

5.3 Organizations

- Vice chair, IEEE CS Award Committee (1995-) (Service Awards).

- Vice Chair, TCSE Software Reliability Engineering Committee (-Current).

- Chair, Test Technology TC Subcommittee on Software Testing, (1993-96).

- Member, Executive Committee, IEEE CS Technical Activities Board (-current); IEEE CS Conference and Tutorials Board (1994);

5.4 IEEE Awards

- IEEE CS Golden Core Award, June 1996.

- IEEE CS Certificate of Appreciation Award, Oct. 20, 1996

6 Research Team

6.1 Student participants

- S. Menon, PhD (now at South Dakota School of Mines Technology)
- W. Alassadi, PhD (now at American Micro Devices, Austin TX)
- N. Li, PhD (now at Microsoft, Redmond WA)
- N. Karunanidhi, PhD (now at Bellcore, Morristown, NJ)
- K. Wu, MS (now at HP, Fort Collins CO)

6.2 Faculty participant

- Prof. A. P. Jayasumana, Colorado State Uni.

6.3 Collaborators

- R. Karcich, StorageTech
- B. Skibbe, StorageTech
- Prof. P. Srimani, Colorado State Uni.
- Prof. A. von Mayrhauser, Colorado State Uni.
- Prof. D. Whittley, Colorado State Uni.