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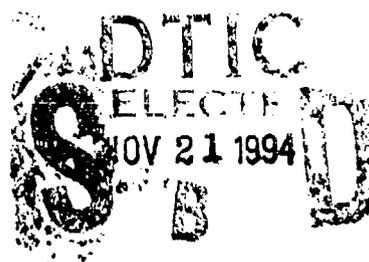
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FABRICATION OF PLZT/ITO GRATING FOR OPTICAL SWITCHING AND RECONFIGURABLE OPTICAL INTERCONNECT APPLICATIONS

Joanne H. Maurice and Pierre J. Talbot



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13. ABSTRACT (Maximum 200 words) A two-dimensional opto-electronic diffraction grating based on PLZT ceramic material for optical switching and reconfigurable optical interconnect applications is demonstrated. Integratable chips are fabricated consisting of numerous fine interleaved transparent indium-tin oxide (ITO) electrodes on a polycrystalline PLZT ceramic substrate. The chips measure one centimeter square. The electrode features are scaled and measure from 12.5 um to 100 um. Reported here are chip material and fabrication details.					
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Acknowledgment

This work was performed in part at the National Nanofabrication Facility at Knight Laboratory, Cornell University, Ithaca, NY.

1. Introduction^{1,2,3,4,8}

Electro-optics is the most recent area of applications to emerge for PLZT ceramics. Primarily this is because PLZT offers a low-cost, versatile alternative to crystal technology. General advantages over electro-optic crystals include a much lower cost, the fact that ceramics can be hot-pressed into any size or shape, the availability of larger samples of any size or shape, the availability of larger samples that are *uniform*, higher ON-OFF efficiencies or contrast ratio (due to a deep OFF state), more easily controlled optic axis variable grain size allowing for optimized electro-optic and scattering properties, and a mature manufacture and processing technology. Compared to liquid crystal or mechanical shutters, advantages include a faster response time (in the μs range), lighter weight, less vibration, and a wider operating temperature range (-40°C to $+80^{\circ}\text{C}$). Thin films of PLZT are epitaxially grown on sapphire substrates by sputter deposition and exhibit both excellent optical transparency and strong electro-optic effects. PLZT ceramic technology for electro-optic applications is very promising for future integrated optics applications, yet so far the only major research activities on PLZT and its applications have been in Japan.

In Figure 1 is a schematic of a typical PLZT/ITO ceramic electro-optic phase grating fabricated by Photonics Center staff at Cornell University's National Nanofabrication Facility (NNF). Several such devices were fabricated, averaging in size 1 cm x 1 cm overall. Two grating structures can be present on the device. One grating structure is formed when a voltage is applied to the ITO interleaved electrode fingers by the quadratic electro-optic effect, as described above. Another, an "intrinsic" grating is present when no voltage is applied, and results from the difference in the index of refraction between the ITO and PLZT materials. The electrode widths and spacings between electrodes are equal and scaled on various grating devices from 100 μm to 12.5 μm . Details concerning

fabrication of the devices follow. First, properties of both materials are discussed.

2. **PLZT Material Properties**^{1,2,3,4,5,6}

PLZT, developed at Sandia National Laboratory, is lead-lanthanum zirconate titanate ($\text{PbZrO}_3\text{-PbTiO}_3\text{-LaO}_3$). It is polycrystalline with a grain size less than 5 μm , has high transparency in the visible and near-IR wavelengths of the optical spectrum, a large electro-optic coefficient, and a fast response time. It is an excellent insulator. PLZT is intrinsically non-birefringent, allowing for flexible orientation of incident-beam polarization. Its composition is denoted by a (y/z/1-z) notation, where y is the percentage of lead sites occupied by lanthanum, and z/1-z is the zirconate-to-titanate ratio in the material. The substitution of lanthanum atoms in lead sites produces transparency in the otherwise opaque PZT material. For the composition of the PLZT samples reported here, transmission is about 65% in the visible and near-infrared, with the rest of the light reflected. Our samples have an unpoled index of approximately 2.5. The zirconium-titanium ratio determines the principle electro-optic behavior. Depending on composition, PLZT displays one of three crystal structures: rhombohedral, tetrahedral, or cubic. Our wafers are cubic (9.5/35/65), exhibiting a quadratic electro-optic effect. The utilization of quadratic PLZT compositions reduces the required driving voltages compared to linear electro-optic materials. Our samples are of two thicknesses, 12.5 mils and 25 mils thick, cut from dense, hot-pressed cylindrical blocks.

3. **ITO Material Properties**^{7,9}

ITO is the accepted abbreviation for indium-tin oxide mixtures. Our ITO is a thin film mixture of 90% InO_3 and 10% SnO_3 . Thin films of SnO_3 and InO_3 are optically transparent in the visible and near-infrared wavelengths of the

spectrum, with an index of approximately 1.8 or 1.9, yet have high electrical conductivity, with a sheet resistance between 10 and 100 ohms per square. One deposition process for these transparent conducting films is to first evaporate the indium, which allows the tin oxide to adhere better, and to then sputter the tin oxide, for example, by magnetron sputter deposition. Usually, ITO thin films are prepared by a chemical deposition process that includes a physical deposition process (such as spray coating), a sputtering process, and a reactive vacuum evaporation. Often, to increase their transparency, the sputtered films are annealed in air at 400-500°C. We contract-coated our PLZT wafers, as the ITO target is more costly and, due to the low vapor pressure of tin, the deposition procedure too contaminating to the vacuum system of the evaporating device. A typical ITO thin film measuring 0.5 μm thick has a sheet resistance of 25 Ω/sq .

4. Fabrication

4.1 Introductory Comments

Fabrication of ITO structures on PLZT substrates took place at the National Nanofabrication Facility at Cornell University's Knight Laboratory under a User Program contract with the facility. The gratings have electrode and spacing widths of 100 μm , 50 μm , 25 μm , and 12.5 μm . The grating structures are interfaced to the external world by aluminum bonding/contact pads.

Two independent sets of PLZT/ITO gratings were fabricated by two separate processing techniques common to microelectronic device fabrication: first, dry etching, a subtractive process, and then lift off, an additive one. These techniques are methods of pattern transfer. Lift-off generally yields better defined edges than etching. In each case the PLZT wafers were contract-coated with ITO by Thin Film Devices, Inc., CA.

4.2 Mask Generation

In both etched and lift-off cases, chrome-on-glass lithographic mask plates are first generated. Two masks are required, one for the electrode grating pattern and the other for the aluminum bonding-pad pattern. For this, CAD was used to generate the physical layout of both the electrode grating pattern and the aluminum bonding-pad pattern. The design data was then "fractured" into a file representation consisting of rectangles. The fractured data files are recorded on magnetic tape, which is then sent to an optical pattern generator. The pattern generator sequentially reads the tape and writes the fractured rectangle pattern to the photosensitive film on the mask plate in a series of flash exposures. Once developed, the pattern is transferred to the photoresist layer, which is then "descummed" in an oxygen-plasma reactive-ion etcher to remove any excess exposed resist remnants. Next, a chrome etchant is used to wet-etch away the chrome areas of the mask *not* protected (covered) by photoresist. An image of the pattern is left in the chrome. Finally the remaining resist, which has served as a protective coating through the processing thus far, is stripped away with a photoresist remover.

The two masks are now used to pattern the wafers. As mentioned above, two sets of devices were fabricated, the first set by etching, the other by lift-off. Both masks are used in each processing case.

4.3 Dry-Etch Process

Lithography and pattern transfer by etching follow.

The ITO-coated PLZT wafers are first cleansed with alternating and overlapping baths of acetone and alcohol, spin-coated with a positive resist, and

"soft baked" for 1 minute at 90°C. The electrode-grating mask is then proximity aligned with the resist-coated wafer and 1:1 contact lithography performed on an HTG Mask Aligner (405 nm) to pattern the resist. The resist pattern is developed. Exposed areas become more soluble in the developer and are removed by the development process.

As in generating the mask above, the remaining photoresist serves to protect ITO-coated areas during etching. The set of wafers is etched in an argon-ion barrel etcher which provides isotropic, undirectional etching of the ITO film layer. The wafer is etched through a depth equal to the ITO layer, which is approximately 1400 angstroms. In this way the electrode-grating pattern is transferred to the wafer.

Finally, the remaining resist is stripped away with a solvent, leaving the ITO grating-electrode pattern.

4.4 Lift-Off Process

In the lift-off case, the wafers are ITO coated *after* the lithography for the grating-electrode pattern has been performed. The lithography steps involved in lift-off are as follows. The PLZT wafers are cleansed, and positive resist is spun and soft cured, as above. Here, however, the photoresist is spun directly on the PLZT substrate. The wafers are then contact exposed (HTG Mask Aligner), patterning the resist, "hard baked" in ammonia to cure or solidify the resist, "flood exposed," and then developed.

This lithographic process is known as "image reversal." Image reversal not only reverses the tone, producing a negative image, but more importantly, in so doing, generates highly desirable undercut profiles in the resist which are

required for lift-off (Figure 2). As indicated, this is a two-part process. First there is the "hard bake," usually in an ammonia-diffusion oven (for example, a YES Oven) for 80 minutes at 90°C. In this step exposed areas (previously rendered soluble by the first exposure) now become insoluble, while the unexposed areas remain unaffected. Following the ammonia-diffusion hard bake, the resist is "flood exposed" with UV light to reverse the pattern (405 nm, 90 seconds), a step that now exposes previously unexposed areas. Once developed, the original tone resulting from the first exposure alone is reversed.

Lift-off is next. The resist is developed and oxygen-plasma descummed in a reactive ion-etcher (RIE) system (to cleanse developed areas of residual resist) and ITO coated. Following deposition, the remaining protective resist is stripped away in a dissolving solvent, carrying the unwanted ITO portions with it. To finish, the wafers are again RIE descummed, and an annealing bake is performed to evaporate out any remaining solvent. The stripping step is lift-off. To make lift-off easier, we used a resist layer that was approximately three times the depth of the desired ITO deposition.

The lift-off technique greatly improves edge definition in subsequent deposition and lift-off steps because a *slanted sidewall slope* is formed, the undercut profile of which is favorable, as the remaining (protective) resist then removes cleanly -- "lifts off" -- leaving well-defined edges to the deposition pattern behind (Figure 3), as commented upon in the next section.

4.5 Process Comparison

Both sets of finished gratings were examined with a high-quality optical microscope and profile-depth characterized with an Alpha-Stepper Stylus Profiler instrument. By these measures, better results were attained by the lift-off process

than were by the etching process alone. The difference between the two alternatives has to do with the sidewall slope of the photoresist. In the etching case, the slant of the sidewall slope generally works against us, creating more ill-defined edges in our lithography. In lift-off processing however, the slant of the sidewall slope created during pattern reversal now works to our favor by generating the undercut profile favorable to lift-off, as shown in Figure 2, lifting off easily with a solvent and leaving well-defined metallization patterns (ITO electrodes and aluminum pads) behind.

Also, in subsequent testing, gratings processed by the lift-off technique exhibited cleaner far-field diffraction patterns, both transmitted and reflected, when light from a HeNe laser was incident upon them.

4.6 Aluminum Contact-Pad Evaporation

Contact lithography is performed using the contact-pad mask and the HTG Mask Aligner. Positive photoresist is spun on the ITO-patterned wafers. Image reversal is performed as above to pattern the resist for deposition of aluminum contact/bonding pads. The pads are deposited along two edges of the chip using a thermal evaporator. Lastly, lift-off is performed leaving ITO electrode gratings on a PLZT substrate with aluminum contact pads to serve as interface to an external power supply or voltage source.

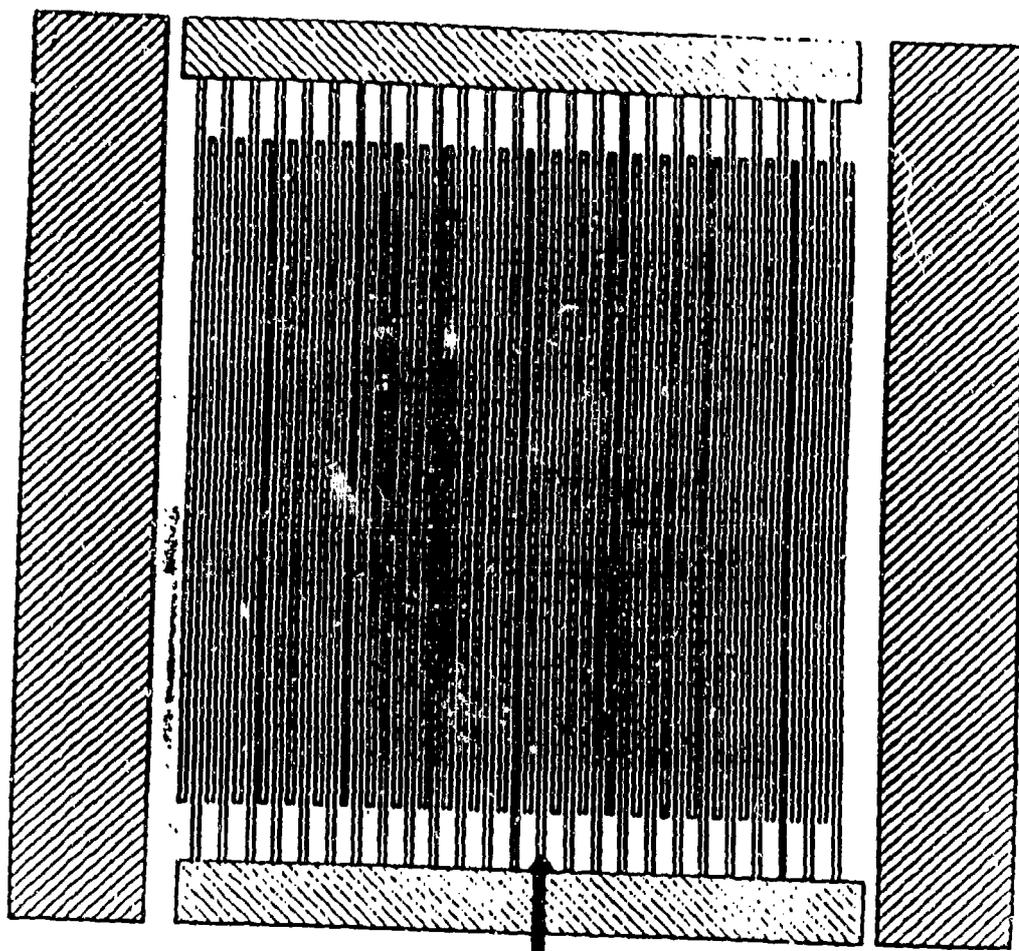
5. Applications

The device applies in general to reconfigurable waveguide structures and free-space or plane-to-plane optical interconnect devices. Applications include electro-optic diffraction gratings, electro-optic dynamic variable focal length lenses, electro-optic variable Fresnel lens arrays, electro-optic variable grating

prisms, and reconfigurable electro-optic crossbar switches. Examples of these are shown in Figures 4, 5, 6, and 7. PLZT technology has already found applications in flash goggles, color filters, displays, and image storage.

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Polycrystalline PLZT
Ceramic Wafer

Transparent ITO Electrode
Grating

Figure 1: Polycrystalline PLZT/ITO ceramic electro-optic phase grating



Figure 2: Photoresist undercut sidewall slope favorable to lift-off

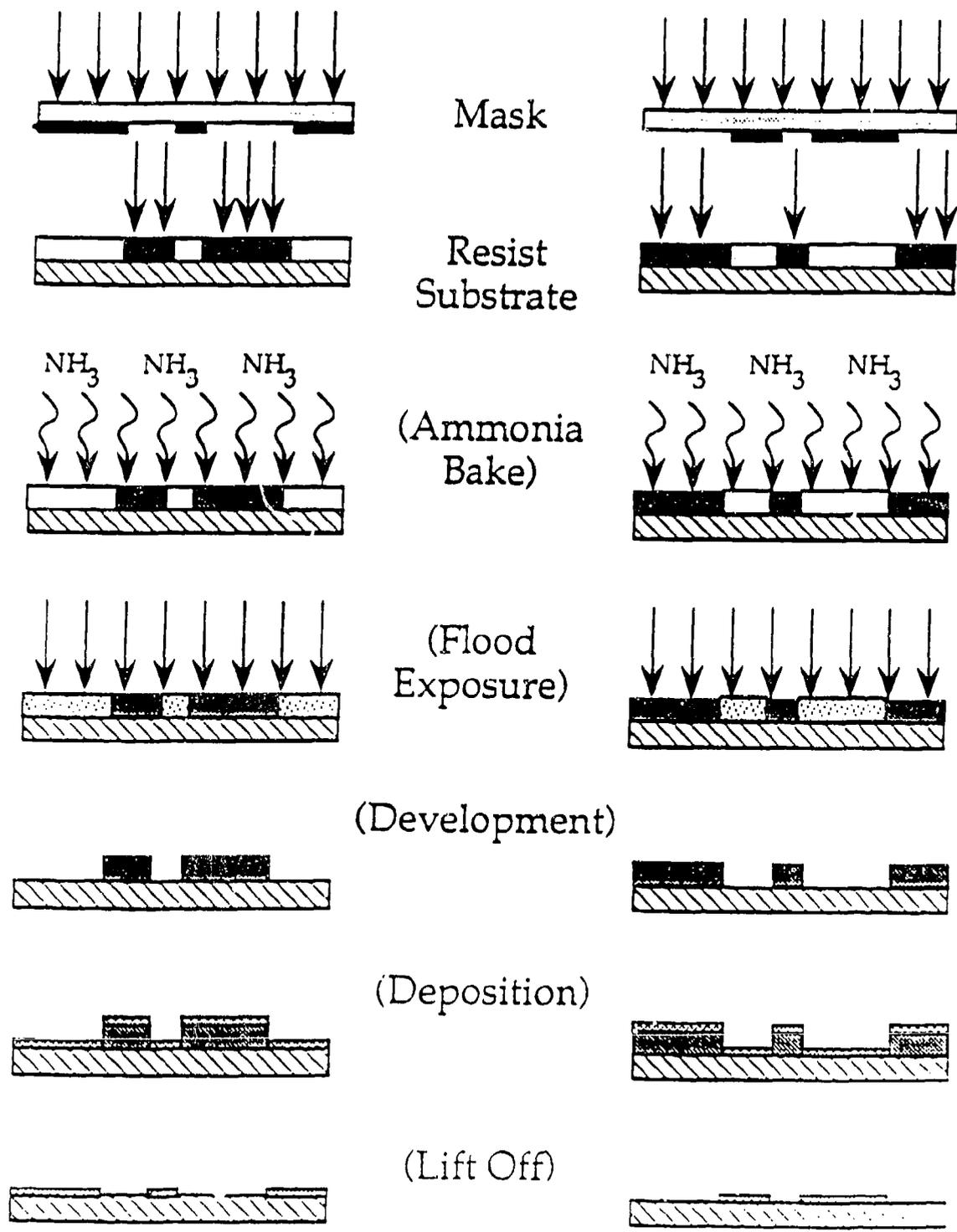


Figure 3: Image reversal and lift-off using ammonia bake and flood exposure (slanted sidewall slopes omitted for simplicity)

PLZT Double ITO Grating

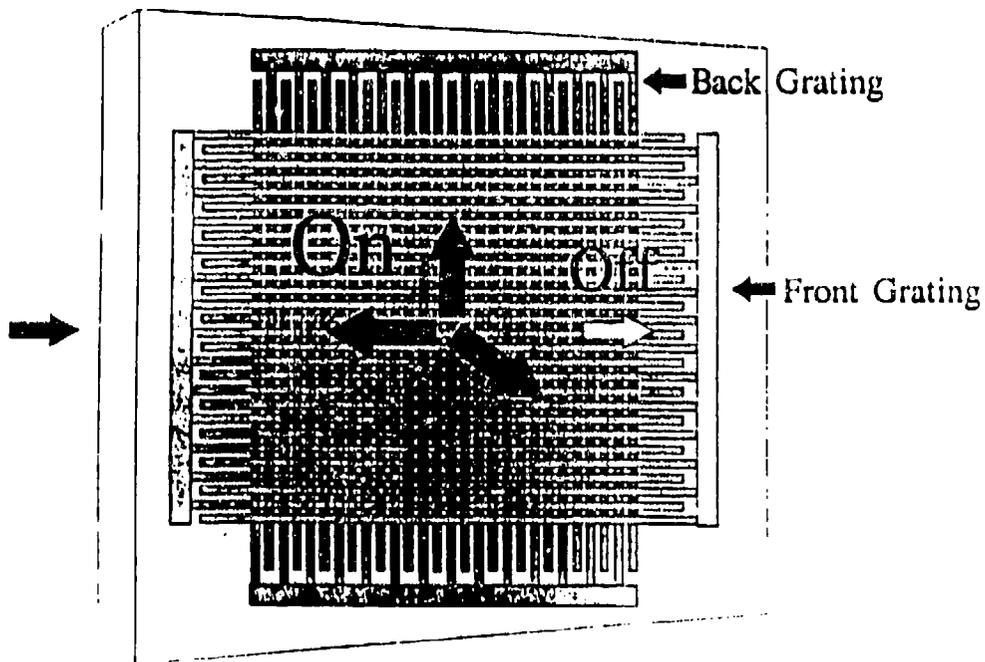


Figure 4: PLZT double ITO grating

Transparent ITO Fresnel Conducting Contact Structures

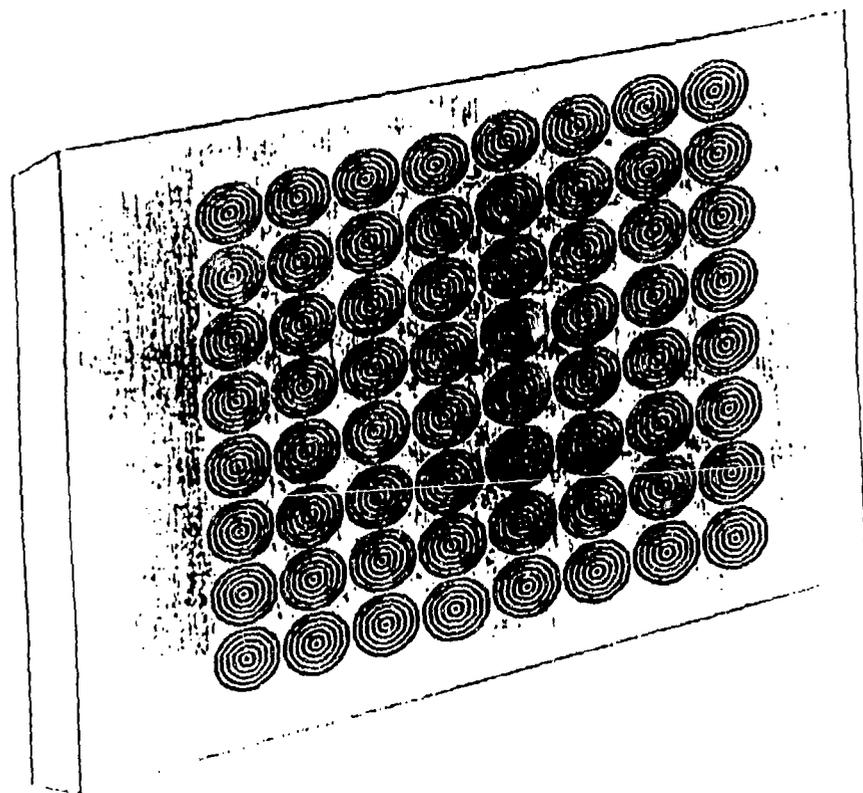
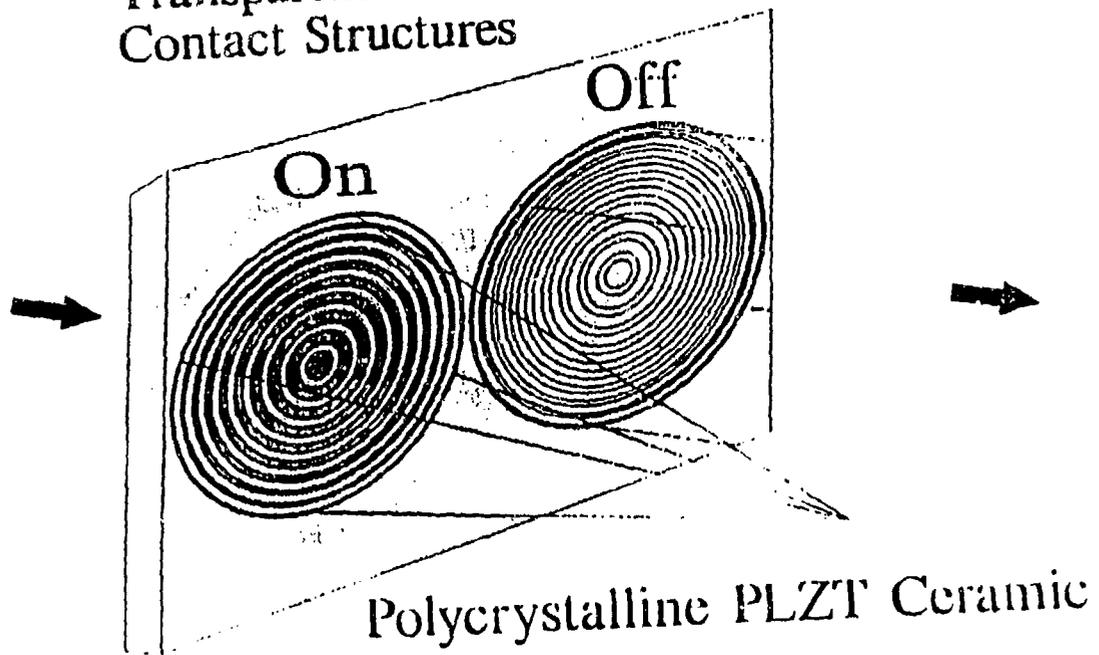
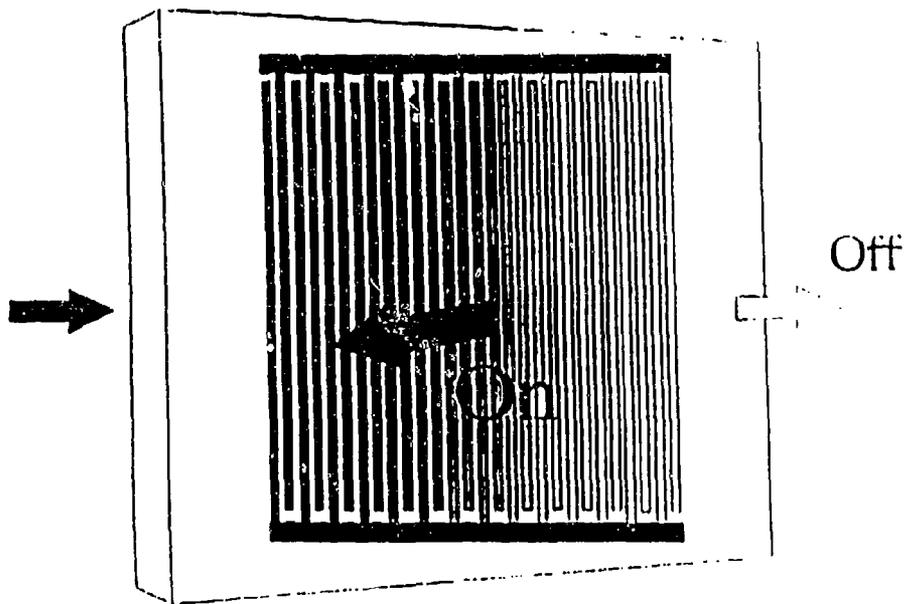


Figure 5: Variable focal length Fresnel diffraction lens and lens array



Progressive Linear Decrease in ITO Conducting Contact Spacing

Figure 6: Variable grating prism

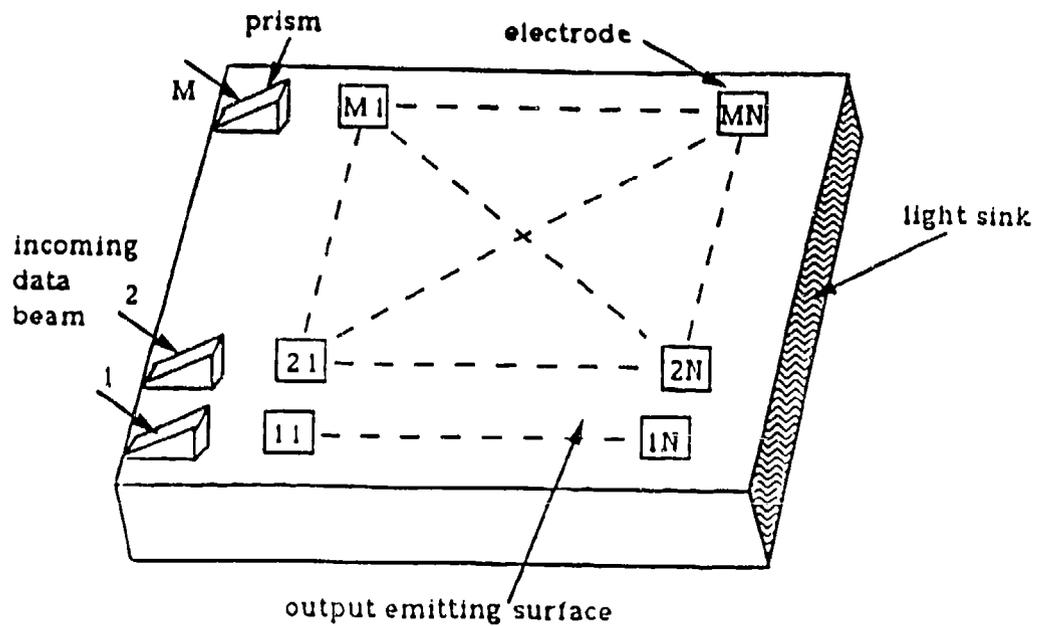
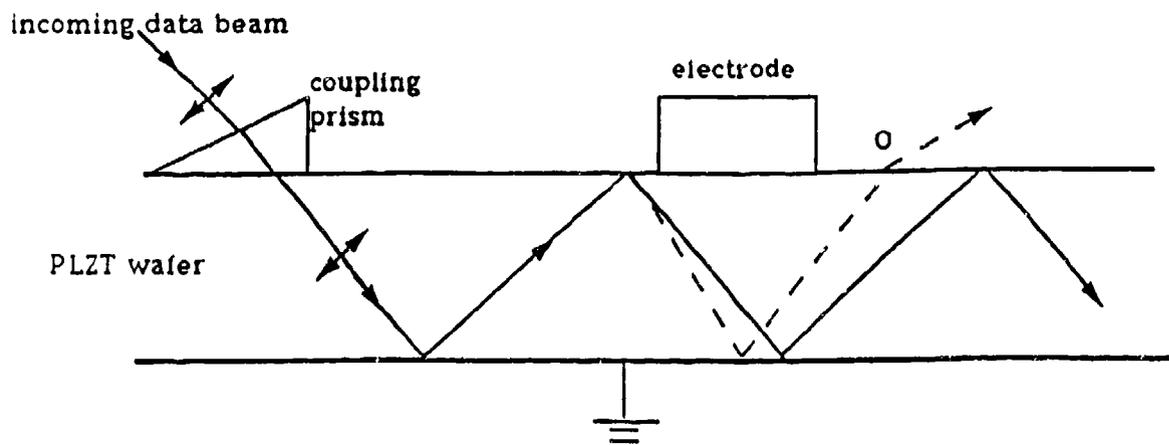


Figure 7: Principle of voltage-controlled total-internal-reflection switch and its application in an $m \times n$ reconfigurable crossbar switch

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