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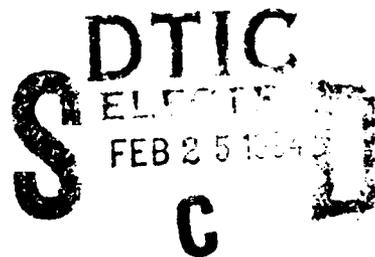


**GaAs/GaN Strained Layer Superlattice Materials for High Temperature Transistors**

**Phase - I Final Technical Report**

**Author : Jonathan Kuznia**

**January 10, 1994**



**Managed by:**

**U .S. Army Research Office**

**Research Triangle Park, NC 27709-2211**

**Sponsored by:**

**Strategic Defense Initiative Organization (SDIO)**

**Contract No: DAALO3-9 -C-0036**

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<b>1. AGENCY USE ONLY (Leave blank)</b>		<b>2. REPORT DATE</b> Jan 10, 1994	<b>3. REPORT TYPE AND DATES COVERED</b> Final - July 1 - December, 1992	
<b>4. TITLE AND SUBTITLE</b> GaAs/GaN Strained Layer Superlattice Materials for High Temperature Transistors			<b>5. FUNDING NUMBERS</b> DAAL03-92-C-0036	
<b>6. AUTHOR(S)</b> Jonathan N. Kuznia				
<b>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</b> APA Optics, Inc. 2950 NE 84th Lane Blaine MN 55449 USA			<b>8. PERFORMING ORGANIZATION REPORT NUMBER</b>	
<b>9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)</b> U. S. Army Research Office P. O. Box 12211 Research Triangle Park, NC 27709-2211			<b>10. SPONSORING / MONITORING AGENCY REPORT NUMBER</b>  ARO 30481.1-EL-S&I	
<b>11. SUPPLEMENTARY NOTES</b> The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.				
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<b>13. ABSTRACT (Maximum 200 words)</b> During this program, we were successful in depositing single crystal layers of GaAs on GaAs on GaN epilayers and single crystal GaN on GaAs substrates. These two developments represent an important advance in the technology base required to grow GaN/GaAs short period superlattices. Due to the large difference in bandgap energy between GaAs and GaN (1.4-3.6 eV), superlattices based on these two materials can potentially provide electronic devices which operate at elevated temperatures over a wide range of wavelengths (365-860 nm). For the first time, tertiary butyl arsine (TBA) was used to grow GaAs on GaN substrates. From an industry safety perspective, this is extremely important since TBA is less toxic and deadly as compared to pure arsine. During this program, the growth of ternary GaAsN was also attempted. Unfortunately, poor results were obtained and further growths were curtailed. During the growth of the ternary GaAsN, an important growth aspect was determined. When attempting to grow GaAsN at low temperatures, arsenic incorporation far exceeded nitrogen leaving the film GaAs. At elevated temperatures, nitrogen was preferentially incorporated leaving a GaN film. Such growth knowledge will prove important for future GaAs/GaN superlattice work.				
<b>14. SUBJECT TERMS</b>  Single Crystal GaN-GaAs, GaN/GaAs Superlattices			<b>15. NUMBER OF PAGES</b>  7	
			<b>16. PRICE CODE</b>	
<b>17. SECURITY CLASSIFICATION OF REPORT</b>  UNCLASSIFIED	<b>18. SECURITY CLASSIFICATION OF THIS PAGE</b>  UNCLASSIFIED	<b>19. SECURITY CLASSIFICATION OF ABSTRACT</b>  UNCLASSIFIED	<b>20. LIMITATION OF ABSTRACT</b>  UL	

## 1.0 Summary of Results of Phase I Study

This document summarizes the work done under a Phase I program (Contract # DAALO3-92-C-0036). During the course of the program we have demonstrated for the first time the deposition of GaAs on GaN, GaN on GaAs, GaN/GaAs superlattices and the ternary GaAsN by techniques such as Low Pressure Metalorganic Chemical Vapor Deposition (LPMOCVD) and Atomic Layer Epitaxy (ALE). We believe we are in a position with the experience gained from this effort to optimize these growth techniques and fabricate devices based on GaN/GaAs superlattices. The following are the specific results achieved:

1. Demonstrated the deposition of thin GaAs layers on GaN by LPMOCVD.
2. Demonstrated the deposition of GaAs on GaN by ALE.
3. Demonstrated the deposition of GaN on GaAs by ALE.
4. Demonstrated the growth of thick GaN/GaAs superlattices by ALE.
5. Characterized all epilayers by X-ray diffraction and Reflection High Energy Electron Diffraction (RHEED).
6. Developed a Phase II program.

## 2.0 Phase I Objectives and Progress Summary

### 2.1 Growth of GaAs on GaN

Thin layers of GaAs were first deposited using LPMOCVD on thick GaN baselines with and without a AlN buffer layer. Xray diffraction and RHEED measurements indicated clearly the single crystal nature of the GaAs epilayer. Low temperature ALE was also used to deposit the GaN epilayers. Once again Xray and RHEED measurements indicated that the GaAs epilayer was single crystal.

### 2.2 Growth of GaN on GaAs

Initial depositions of GaN on GaAs by low temperature ALE resulted in polycrystalline material characterized by an "arcing" pattern seen in RHEED measurements. However when the GaAs surface was "nitrided" before the GaN epi-deposition good quality single crystal GaN was obtained. These results will be discussed in detail in Technical Description section.

### 2.3 Growth of GaAs/GaN superlattices

Thick superlattices of GaN/GaAs were deposited. X-ray diffraction showed peaks characteristic of GaAs (111) and GaN (002) and (004) planes. Attempts to deposit the ternary GaAsN which is more lattice matched to GaN than GaAs were also made. Interesting results about the preferential incorporation of either N or As at different temperatures were observed from this experiment with the ternary. These results provide valuable information about the growth conditions required to grow GaN/GaAs superlattices by ALE. This will be discussed in the next section.

## 3.0 Technical Description: Research, Data and Future Work

### 3.1 System Design

The initial part of the program focussed on system modifications that needed to be incorporated to allow growth of arsenide based semiconductors in our APA LPMOCVD reactor. Tertiarybutylarsine (TBA) was chosen as the arsenic source. TBA offers the advantage that it safer and easier to handle than arsine which is often the source of choice for MOCVD growth of the arsenides. Although a reduced risk is associated with the use of TBA, extreme care must be taken. A schematic of the modified system is shown in Fig. 1. The vapor pressure of the TBA is extremely temperature

sensitive, so the TBA bubbler is immersed in a temperature controlled bath. Hydrogen is used as the carrier gas. An APA proprietary high speed switching manifold is used to control gas flow into the reactor. This manifold allows for gases to be admitted in pulses for atomic layer epitaxy. The treatment of the unused TBA is an important safety issue. This is done by flowing the TBA through a cracking furnace where it breaks down into  $AsH_3$ . A special scrubber is then used to remove the As species.

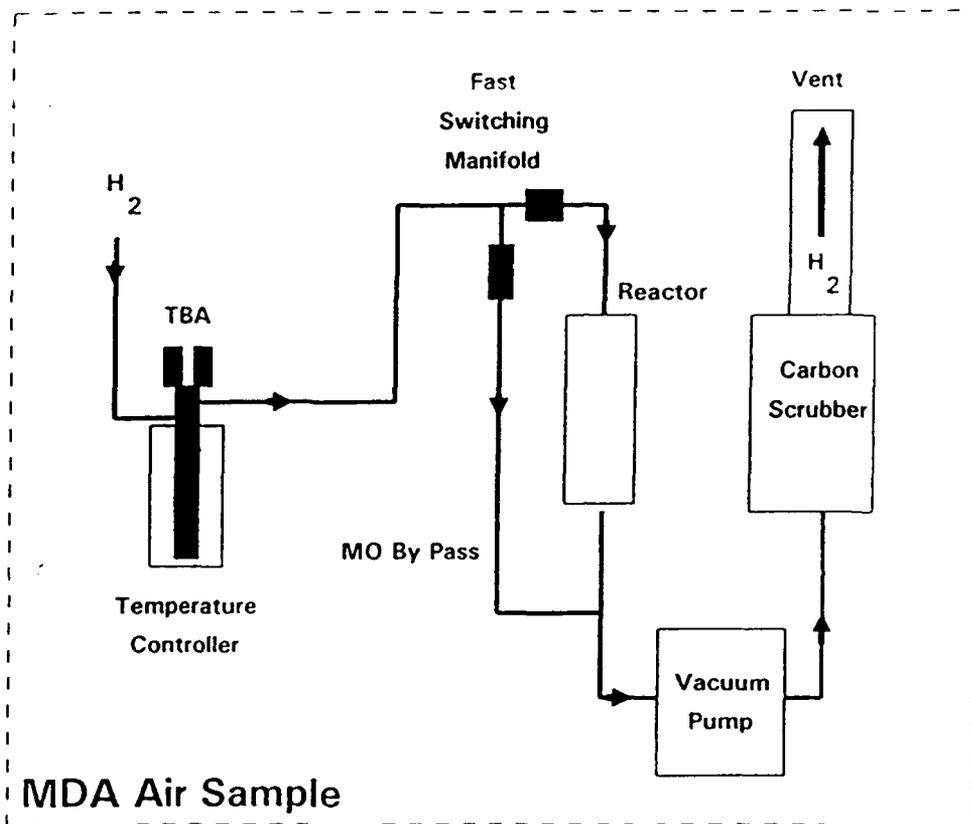


Figure 1. TBA system incorporation and gas flow arrangement in modified LPMOCVD reactor.

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### 3.2 Growth and Characterization

#### 3.2.1 Growth of GaAs on GaN

Several structures were deposited and characterized to determine optimum growth conditions. One of the first structures investigated consisted of a 1 micron layer grown on a 3.0 micron GaN layer. Growth conditions of the GaN layer have been previously presented (c.f. Khan et. al. Appl. Phys. Lett. 58, 526 (1991)). Following the growth of GaN at  $1000^{\circ}C$  the substrate temperature was lowered to  $600^{\circ}C$  and the TBA was allowed to flow for 30 seconds. This initial step was to help convert the GaN surface to GaAs. The GaAs growth then proceeded as was reported earlier. The x-ray spectrum for this sample is shown in Fig. 2. The presence of a single GaAs peak indicates the material to be single crystal.

The next step was to use low temperature Atomic Layer Epitaxy (ALE) for the deposition of GaAs. This technique because of the lower temperature, has the advantages of realizing sharp and distinct interfaces as well as a tendency to suppress defect formation due to the large lattice mismatch between GaAs and GaN. A series of samples consisting

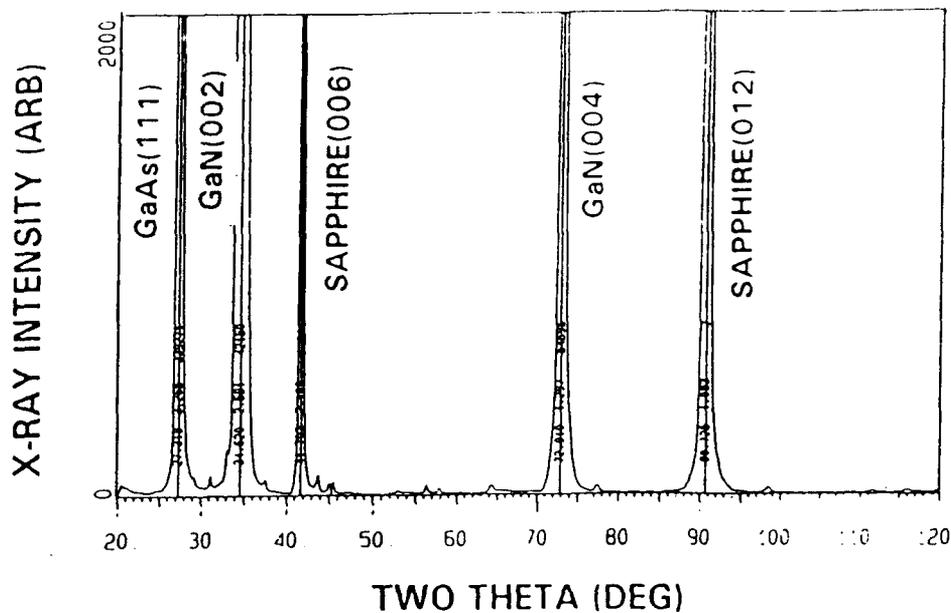
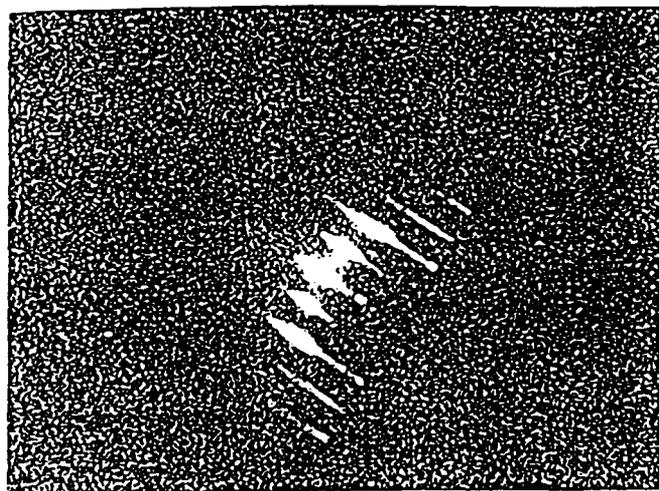
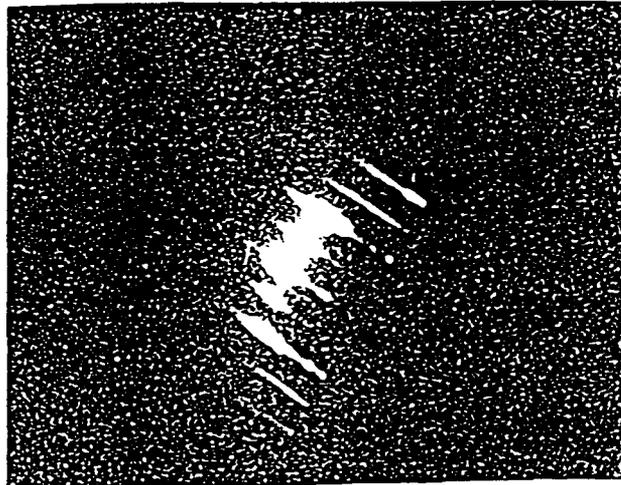


Figure 2. X-ray spectrum of a GaAs/GaN/Al<sub>2</sub>O<sub>3</sub> structure displaying single crystal peaks from GaN and GaAs.

of a few monolayers (10-50) of GaAs on 1 micron GaN (growth previously described) were deposited. A 1H<sub>2</sub>-1TEG-1H<sub>2</sub>-1TBA pulse sequence was typically used for the growth. Growth temperature was typically 450°C while growth pressures were typically 76 Torr. RHEED from such a sample is shown in Fig. 3. Note the streaky nature of the RHEED patterns indicating that single crystal GaAs is deposited. Xray diffraction data of the same sample is shown in Fig. 4. The single peak from GaAs (111) plane is clearly visible indicating the single crystal nature of the GaAs epilayer.



GaAs OVER GaN  
0°



GaAs OVER GaN  
60°

Figure 3. RHEED images of a GaAs epilayer grown on GaN.

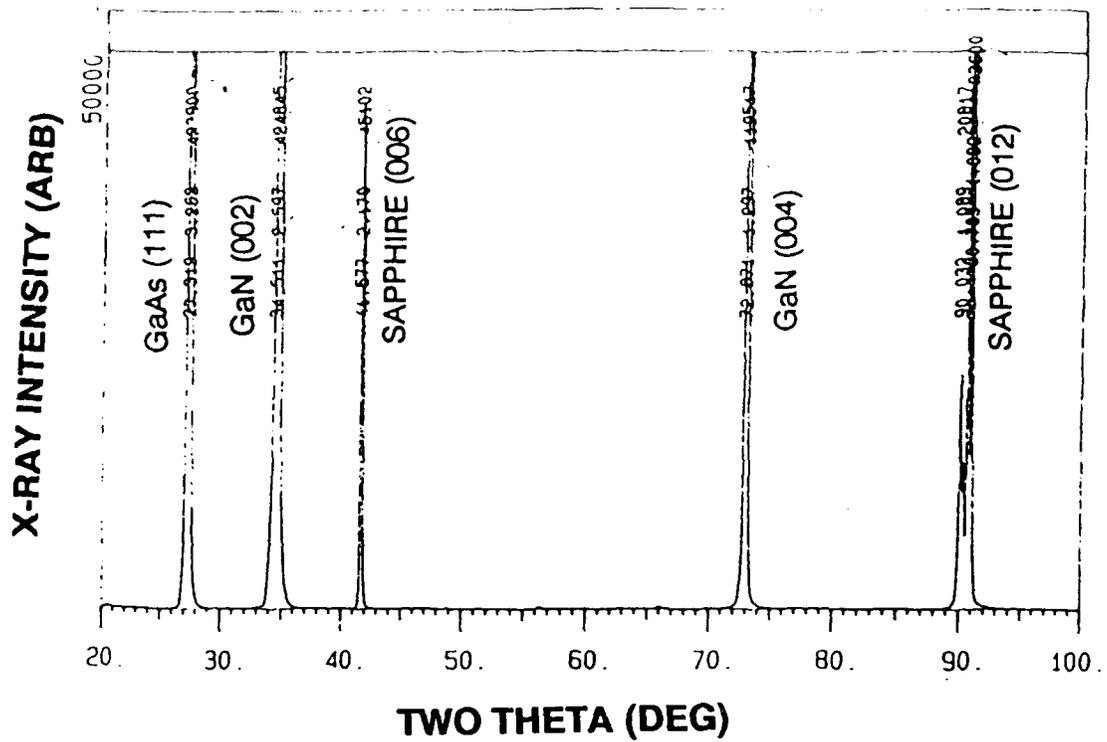


Figure 4. X-ray spectrum of GaAs/GaN/Al<sub>2</sub>O<sub>3</sub> structure grown by ALE.

### 3.2.2 Growth of GaN on GaAs

Initial attempts to grow GaN on GaAs (deposited as indicated above) at 450°C by ALE using a 1H<sub>2</sub>-1TEG-1H<sub>2</sub>-1NH<sub>3</sub> pulse sequence resulted in polycrystalline material indicated by an "arcing" pattern in RHEED measurements. Migration enhanced epitaxy using a 1H<sub>2</sub>-1TEG-1H<sub>2</sub>-5NH<sub>3</sub> pulse sequence resulted in a slight improvement in the GaN crystallinity. The best results were obtained using a surface nitriding approach. This was tested by first converting the thin GaAs layer deposited on GaN to GaN by flowing ammonia for 10 minutes with the substrate temperature raised from 450°C to 700°C. Auger data indicated complete conversion with no visible trace of As as seen in Fig. 5. Also RHEED showed a streaky pattern characteristic of wurtzitic GaN as seen in Fig. 6. The experiment was repeated for GaAs substrates with similar results. Once again Auger data indicated the absence of As on the surface while the RHEED image was characteristic of single crystal wurtzitic GaN.

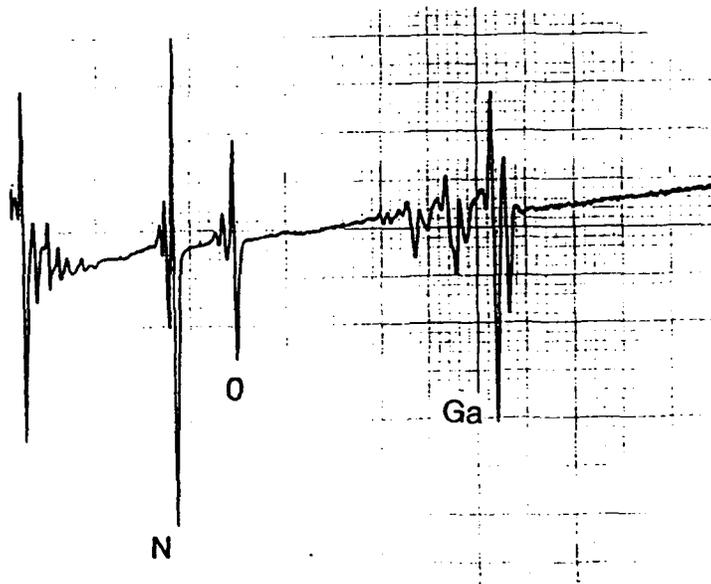


Figure 5. Auger Spectrum after nitriding, showing absence of As on surface.

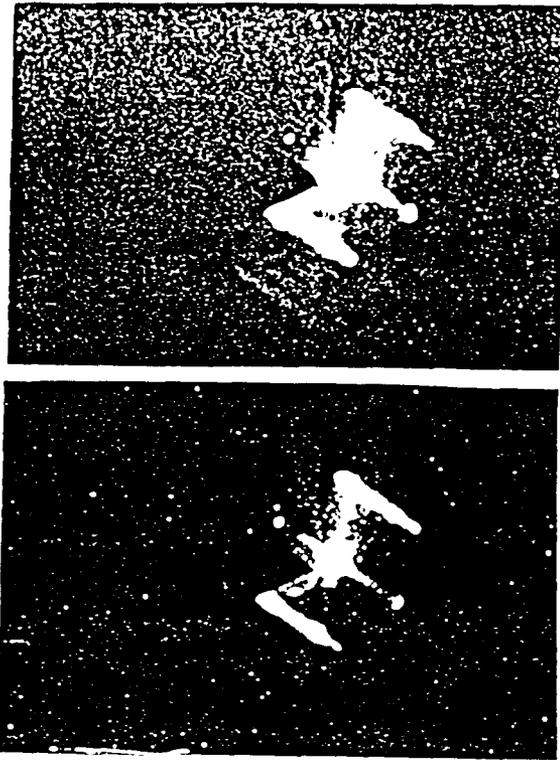


Figure 6. RHEED images of GaN epilayers on GaAs (111) grown by ALE.

### 3.2.3 Growth of GaN/GaAs Superlattices

A series of GaN/GaAs superlattices were grown using ALE and the nitriding technique. X-ray diffraction from a typical GaN/GaAs superlattice is shown in Fig. 7. Peaks from GaAs (111) and GaN (002) and (004) planes are clearly visible

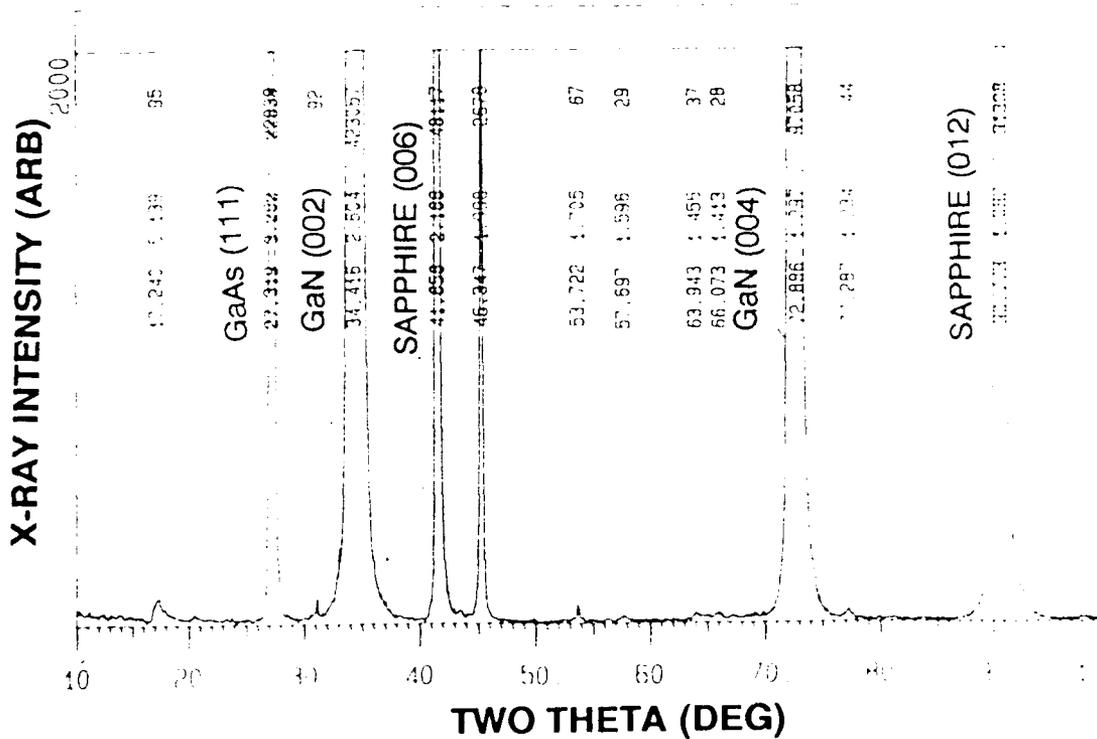


Figure 7. X-ray spectrum of a GaN/GaAs superlattice grown by ALE.

### 3.2.4 Growth of GaAsN and Future Work

The deposition of the ternary alloy GaAsN was also attempted. The ternary provides the flexibility of the formation of GaAsN/GaN quantum well structures which are not as highly strained as GaN/GaAs superlattices. However it was found that the simultaneous incorporation of As and N was not achievable. N showed a tendency to preferentially incorporate at higher temperatures (750 - 1000°C) while As tended to dominate the incorporation at lower temperatures (600-700°C). These findings were very similar to the those discovered by H. Okumura et. al. (c.f. J. Cryst. Growth 120, 114 (1992)) in their successful attempt of depositing GaN/GaAs multilayers by Gas Source Molecular Beam Epitaxy (GSMBE). Though our attempts to grow GaAsN proved to be unsuccessful, the findings will prove useful in optimizing our growth conditions of GaN/GaAs multilayers by ALE. The GaN/GaAs superlattices can be deposited at low temperatures (450-600°C) with an intermittent supply of TBA (the As source) and a constant supply of NH<sub>3</sub> (the N source). At these low temperatures As will dominate the incorporation whenever the TBA supply is on for GaAs growth while GaN will be deposited during the off period of the TBA pulse. These ideas will be emphasized in a Phase II program

## 4.0 Conclusion

We have successfully deposited:

1. Single crystal GaAs on GaN
2. Single crystal GaN on GaAs
3. Single crystal layers of GaN and GaAs to form a GaN/GaAs superlattice.

We recommend continuing the work under a Phase II program. We will optimize the growth parameters for the deposition of high quality GaN/GaAs superlattices. We will then be in a position to fabricate devices for high temperature applications based on these superlattices.

# REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on Reverse Side.)

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b. ADDRESS (include ZIP Code) <b>2950 NE 84th Lane Blaine MN 55449</b>	d. AWARD DATE (YYMMDD) <b>920701</b>	d. AWARD DATE (YYMMDD) <b>920701</b>	4. REPORTING PERIOD (YYMMDD) a. FROM <b>920701</b> b. TO <b>931231</b>

## SECTION I - SUBJECT INVENTIONS 27709-2211

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (if "None," so state)		6. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED							
a. NAME(S) OF INVENTOR(S) (Last, First, MI)	b. TITLE OF INVENTION(S)	d. ELECTION TO FILE PATENT APPLICATIONS	e. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER						
NONE	NONE	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">(1) United States</td> <td style="width: 50%;">(2) Foreign</td> </tr> <tr> <td>(a) Yes (b) No</td> <td>(a) Yes (b) No</td> </tr> <tr> <td style="text-align: center;">(1) Yes (2) No</td> <td style="text-align: center;">(1) Yes (2) No</td> </tr> </table>	(1) United States	(2) Foreign	(a) Yes (b) No	(a) Yes (b) No	(1) Yes (2) No	(1) Yes (2) No	
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(1) Yes (2) No	(1) Yes (2) No								

## SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

7. EMPLOYER OF INVENTORS NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		8. EMPLOYER OF INVENTORS EMPLOYED BY CONTRACTOR/SUBCONTRACTOR	
(1) (a) Name of Inventor (Last, First, MI)	(2) (a) Name of Inventor (Last, First, MI)	(b) Name of Employer	(c) Address of Employer (include ZIP Code)

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, MI) <b>Jain, Anil K.</b>	c. I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.	
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