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GAAS SIGMA-DELTA MODULATOR MODELING
FOR ANALOG TO DIGITAL CONVERTERS (ADCS)



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DEC 1992

INTERIM REPORT FOR 06/01/92-12/29/92

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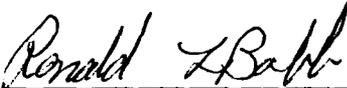
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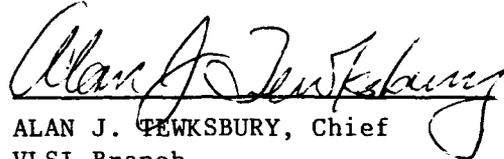
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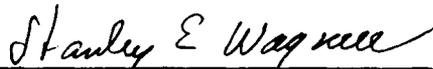
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In this project, a sigma-delta modulator has been designed. The circuit was designed and simulated using model parameters corresponding to the Vitesse 1.2 micron GaAs MESFET technology. The clock rate of the circuit is 512-Mhz and preliminary results show that it can be used for a 9-10 bit A/D converter accepting a 4-Mhz input signal. This bandwidth could be used for video signals such as television.

SIGMA-DELTA MODULATOR ANALOG-TO-DIGITAL
GAAS MESFET CONVERTERS

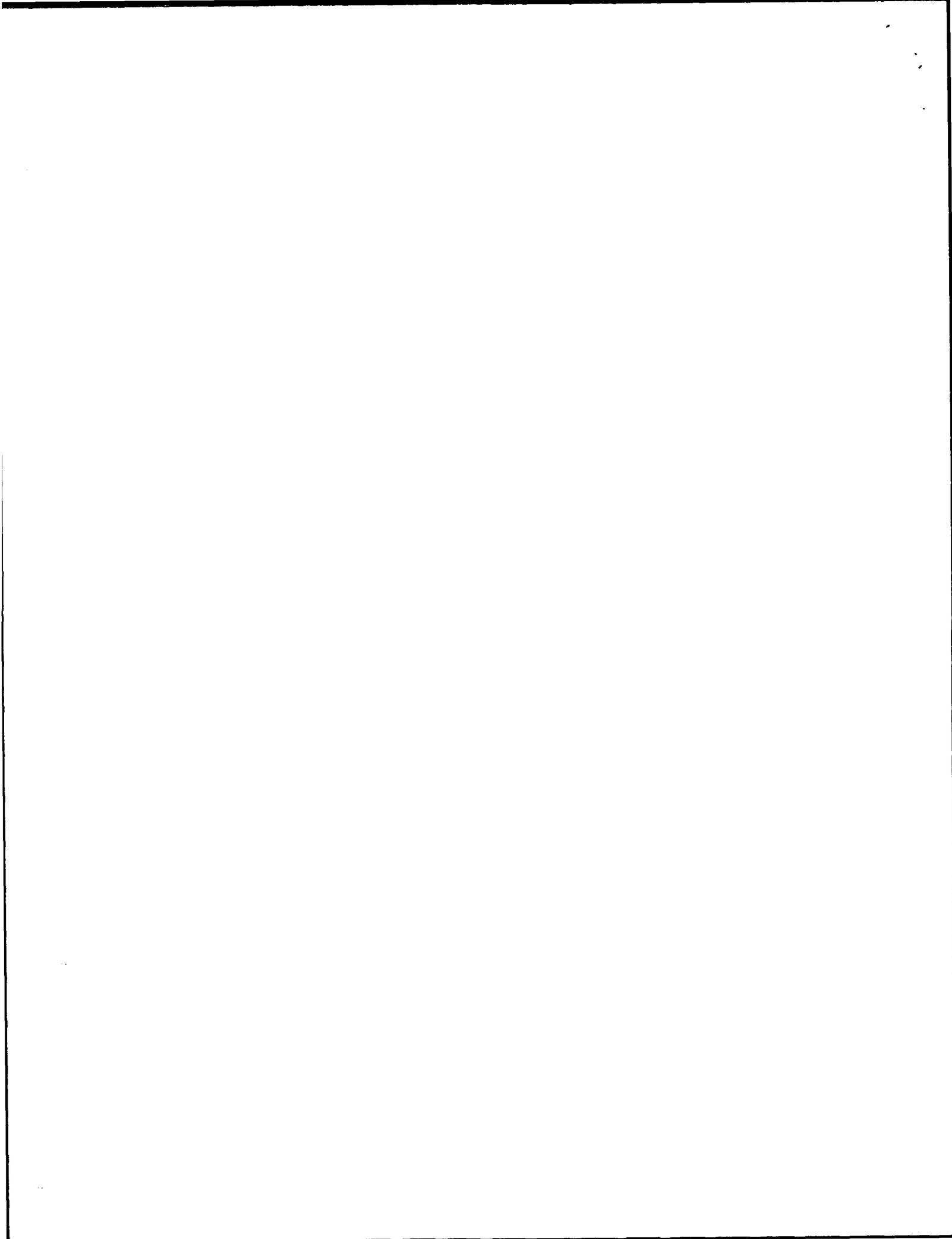
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1 Introduction

The idea behind sigma-delta A/D conversion is oversampling. The oversampling rate is much greater than the Nyquist frequency. Oversampling allows time resolution to be traded for amplitude resolution. Unlike ordinary delta A/D conversion, sigma-delta A/D allows amplitude resolution to increase more than the time resolution decreases. The basic components of a sigma-delta A/D converter are a modulator and a filter.

The purpose of the modulator is to encode the analog input into a stream of bits and to push most of the noise generated from this quantization into frequencies higher than the input bandwidth. The modulator encodes the bits such that the recent average of the bits is approximately the input. The output is an oscillation around the input. These oscillations correspond to the quantization noise and their frequency should be as high as possible.

The purpose of the filter is to remove most of the quantization noise which is located in the higher frequencies. Two approaches can be used for the filter. One approach is to take the modulator output through a low-pass filter directly [4]. Another approach is to first decimate the modulator output and then put it through a low-pass filter [2],[3]. In either approach, the order of the first stage of the filter should be greater than the order of the modulator so that more noise will not be generated [2],[4].

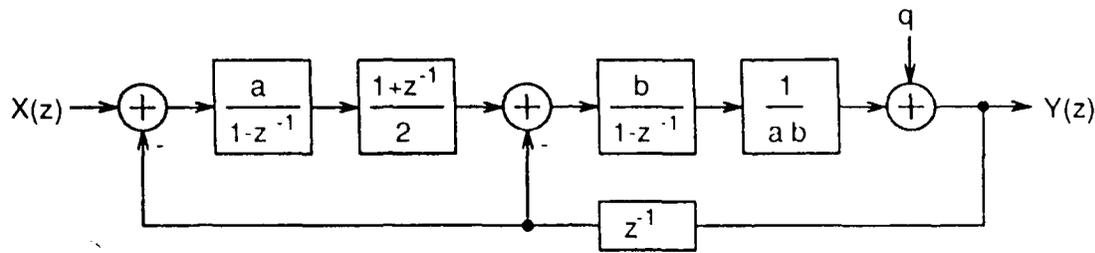


Figure 1 Sigma-delta model

2 Sigma-Delta Model

The sigma-delta modulator designed is a second-order modulator. Figure 1 shows a z-domain view of the second-order modulator. It consists primarily of two integrators and a comparator.

The integrators are modeled as discrete time accumulators amplified by integrating coefficients. The sigma-delta modulator designed uses continuous time adders and integrators. To model the sigma-delta modulator in the z-domain, special treatment is given to inputs of the adders which are not constant over each clock period. For these signals, an extra transfer function is inserted which calculates the average value over each period.

The clocked comparator output is constant over each period, so it goes to the adders with just a delay. For the first integrator, $X(z)$ is approximately constant over each clock period, so its output is linear during each clock period. Because this function is linear, the average value needed for the second integrator is simply the average of the current value and the previous value.

The comparator is modeled as an amplifier and a white-noise source caused by quantization. The assumption that the quantization can be modeled as a white noise source has been used by many other authors [1]-[3]. The amplifier stage of the comparator is used in the model to compensate for the integrating coefficients and make the average of $Y(z)$ be $X(z)$. The average of $Y(z)$ must be $X(z)$ because the feedback causes the average input to the first integrator to be zero.

From Figure 1, the relationship between $X(z)$ and $Y(z)$ is

$$ab(Y(z) - q) = \frac{b}{1-z^{-1}} \left[\left(\frac{1+z^{-1}}{2} \right) \left(\frac{a}{1-z^{-1}} \right) (X(z) - z^{-1}Y(z)) - z^{-1}Y(z) \right] \quad (1)$$

$$(1 - z^{-1})^2 (Y(z) - q) = \frac{1+z^{-1}}{2} X(z) - \left(\frac{1+z^{-1}}{2} + \frac{1-z^{-1}}{a} \right) z^{-1} Y(z) \quad (2)$$

$$\left[1 + \left(\frac{1}{2} + \frac{1}{a} - 2 \right) z^{-1} + \left(\frac{1}{2} - \frac{1}{a} + 1 \right) z^{-2} \right] Y(z) = \frac{1+z^{-1}}{2} X(z) + (1 - z^{-1})^2 q \quad (3)$$

To reduce excess frequency components, the z^{-1} and z^{-2} terms on the left hand side of (3) should be made zero. The solution to this restriction is

$$a = \frac{2}{3} \quad (4)$$

The frequency response of the noise term in equation (3) is

$$N'(\omega) = N(e^{j\omega T}) = q(1 - 2e^{-j\omega T} + e^{-2j\omega T}) \quad (5)$$

$$N'(\omega) = qe^{-j\omega T}(e^{j\omega T} + e^{-j\omega T} - 2) \quad (6)$$

$$N'(\omega) = -2qe^{-j\omega T}(1 - \cos\omega T) \quad (7)$$

$$|N'(\omega)| = 2q(1 - \cos\omega T) \quad (8)$$

This noise function peaks at half of the sampling frequency and is very small for frequencies much smaller than the sampling frequency.

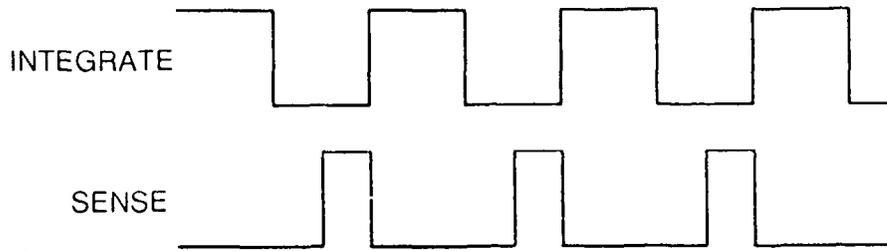


Figure 3 Sigma-delta timing

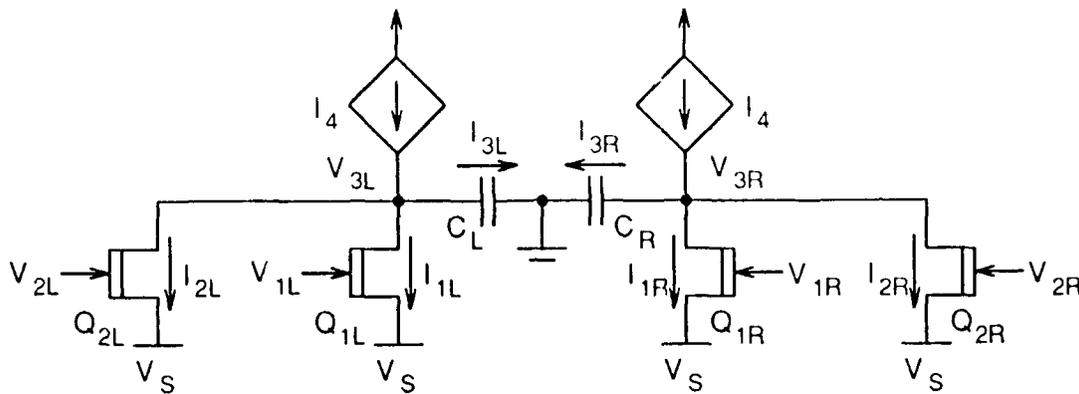


Figure 4 Model of the adder/integrator

A timing diagram is shown in Figure 3. The two clocks should be non-overlapping. The clock frequency is 512-Mhz.

Because the sense amplifiers do not sense instantaneously, the integrators need to be clocked. By having the clocking the integrators, the feedback from the comparator can be constant while the integrators are integrating. The comparator switches when the integrators are off.

Another advantage of having the integrator clocked is that the first sense amplifier can be sampling constant inputs. This improves the accuracy of the comparator.

Two main power supplies are used in this circuit. The sourcing supply is +8.0V and the sinking power supply is -4.0V. Lower supplies can be used for the sense amplifiers (+4.0V and -2.0V).

3.1 Adder/Integrator

A model of the adder/integrator is shown in Figure 4. Instead of using a standard op-amp configuration, the square law of the transistors is exploited to perform the integration.

From the characteristics of capacitors, the output is

$$\Delta V_3 = \frac{1}{C} \int \Delta I_3 dt \quad (9)$$

and the current through the capacitors is

$$\Delta I_3 = -(\Delta I_1 + \Delta I_2) \quad (10)$$

For the integration to be linear with respect to the input, it is necessary that each of these current differences be linear with respect to the inputs. Neglecting output resistance and velocity saturation effects, the current through the left branch due to the first input is

$$I_{1L} = \frac{\beta_1}{2} \left(\bar{V}_1 + \frac{\Delta V_1}{2} - V_S - V_T \right)^2 \quad (11)$$

$$I_{1L} = \frac{\beta_1}{2} \left[\left(\frac{\Delta V_1}{2} \right)^2 - (V_S + V_T - \bar{V}_1) \Delta V_1 + (V_S + V_T - \bar{V}_1)^2 \right] \quad (12)$$

Similarly the current through the right branch is

$$I_{1R} = \frac{\beta_1}{2} \left[\left(\frac{\Delta V_1}{2} \right)^2 + (V_S + V_T - \bar{V}_1) \Delta V_1 + (V_S + V_T - \bar{V}_1)^2 \right] \quad (13)$$

The current difference due to the first input is then

$$\Delta I_1 = -\beta_1 (V_S + V_T - \bar{V}_1) \Delta V_1 \quad (14)$$

Similarly, the current difference due to the second input is

$$\Delta I_2 = -\beta_2 (V_S + V_T - \bar{V}_2) \Delta V_2 \quad (15)$$

Assuming the common mode voltages of V_1 and V_2 are constant and using equations (5), (6), (10), and (11), the output of the integrator is

$$\Delta V_3 = \frac{1}{C} \left[\beta_1 (V_S + V_T - \bar{V}_1) \int \Delta V_1 dt + \beta_2 (V_S + V_T - \bar{V}_2) \int \Delta V_2 dt \right] \quad (16)$$

The input range is limited by the threshold voltage and the maximum voltage across the Schottky junction (V_D). The input range is

$$V_T + V_S - \bar{V} \leq \Delta V \leq V_D + V_S - \bar{V} \quad (17)$$

To allow the maximum positive swing to equal the maximum negative swing V_S should be

$$V_S = \frac{-V_T - V_D}{2} + \bar{V} \quad (18)$$

For the transistors of this circuit, V_D was close to the magnitude of the threshold voltage, so V_S chosen was ground.

Dependent current sources are necessary because the average current going through the input transistors is not constant due to the square law of the transistors. The dependent current sources should keep all transistors in saturation for all possible inputs.

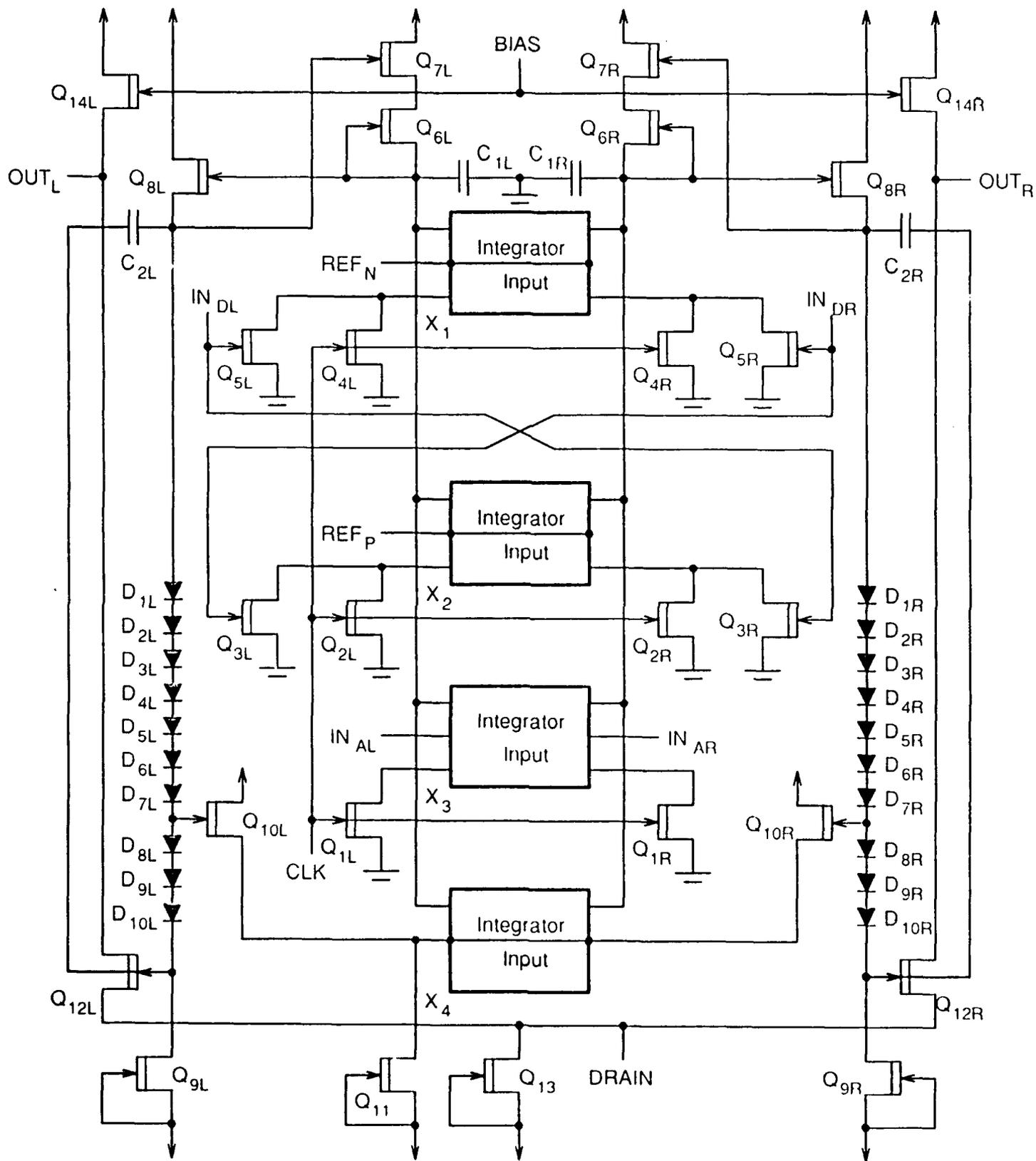


Figure 5 Digital/analog adder/integrator

The implementation of the adder/integrator is shown in Figure 5. It consists of an integrating stage, a level shifting stage, and an output stage. This circuit adds an analog signal to a digital signal and integrates it.

To implement the dependent current sources, independent current sources coupled with dependent current sinks were used. The independent current sources are Q_{6L} and Q_{6R} . The dependent current sinks are in X_4 . Q_{6L} and Q_{6R} are sized to be able to source the maximum amount of total current that X_1 , X_2 , and X_3 sink. The transistors in X_4 are sized to be able to sink all of the current from Q_{6L} and Q_{6R} when X_1 , X_2 , and X_3 are off.

For the integrating stage, transistors are in cascode configurations. This increases the output resistance, but the backgating effects of Q_{6L} and Q_{6R} become dominant in determining the output resistance.

To increase the output resistance of Q_{6L} and Q_{6R} , a threshold of voltage is kept across each of them, which is just enough to keep them in saturation. To obtain this, a half a threshold rise obtained from Q_{8L} and Q_{8R} and the other half comes from Q_{7L} and Q_{7R} . To achieve the half a threshold rise due to Q_{7L} and Q_{7R} , the sizing between them and Q_{6L} and Q_{6R} is 4. This should be true of the other transistors with respect to Q_{9L} and Q_{9R} , but the backgating and lambda effects forced them to be much larger.

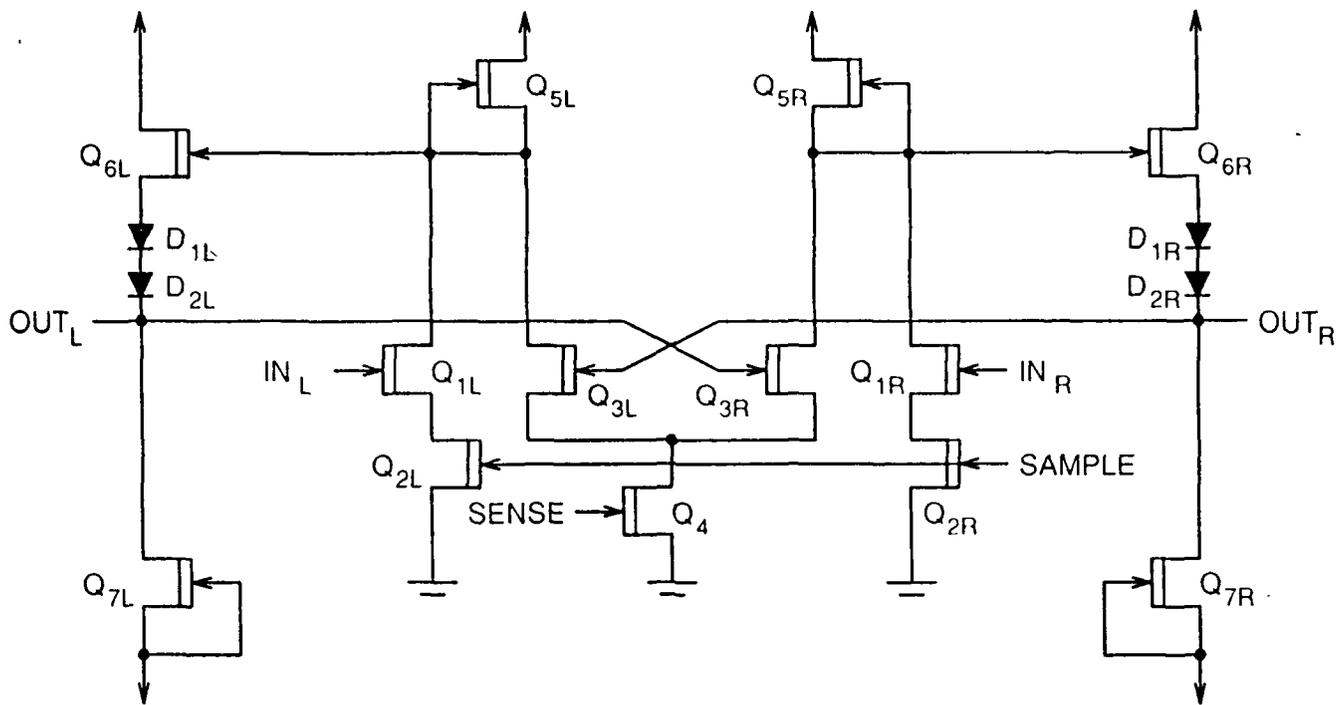


Figure 7 Sense amplifier

of the second integrator. When Q_{2L} or Q_{2R} of Figure 6 is turned off, the drain of Q_{2L} or Q_{2R} must go to ground. This change in voltage causes capacitive feed through to the input. The changes in voltages also cause spikes in the output currents of Figure 6. One way this problem may be alleviated is to provide a dummy current path when a branch is turned off [4].

The level shifting diodes D_{1L} - D_{7L} and D_{1R} - D_{7R} create a sufficient voltage drop to be able to turn off X_4 and keep transistors in X_1 , X_2 , and X_3 in saturation. The level shifting diodes D_{8L} - D_{10L} and D_{8R} - D_{10R} create a sufficient voltage drop to be able to keep Q_{12L} and Q_{12R} in saturation when the output voltages are minimum and X_4 is sinking all current from Q_{6L} and Q_{6R} . Because of the amount of diodes in the level shifting, the feed-forward capacitors C_{2L} and C_{2R} are used to improve the dynamic response.

The last stage of the circuit in Figure 5 biases the outputs. The outputs are approximately biased around BIAS because Q_{13} is double the size of Q_{14L} and Q_{14R} . Because the output stage is differential, the common mode element is removed. This is important for the first integrator because equation (16) for the second integrator would not be valid if the common mode element was not removed. The gain of the output stage is

$$A = \sqrt{\frac{\beta_{12}}{\beta_{14}}} \quad (19)$$

3.2 Sense Amplifier

The sense amplifier is shown in Figure 7. Buffered FET logic is used in the sense amplifier. The SAMPLE and SENSE clocks are non-overlapping.

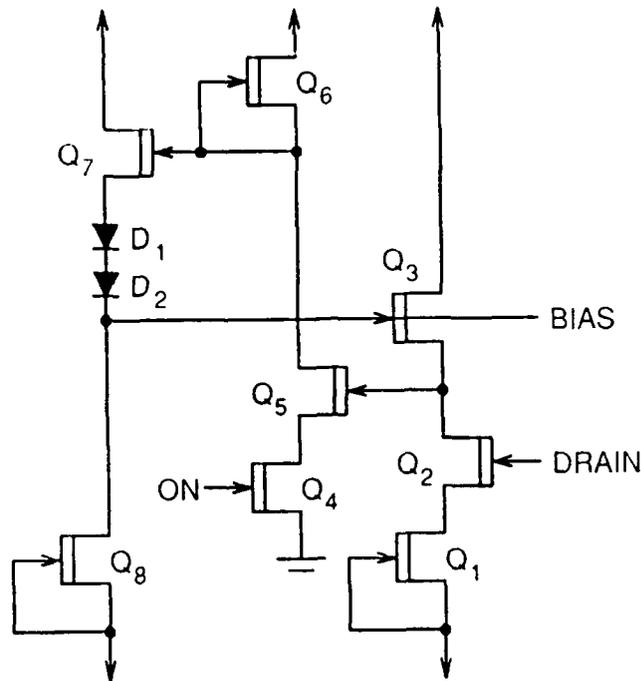


Figure 8 Biasing circuit

During the SAMPLE phase, Q_{1L} and Q_{1R} partially pull down their drains. Assuming enough time is given for sampling, the drains will reflect the inputs at the end of the phase. During the SENSE phase, Q_{3L} and Q_{3R} are cross-coupled to form a flip-flop. This flip-flop switches to one of its steady states depending on what its initial conditions were. These initial conditions are determined by the SAMPLE phase. If the drain of Q_{3L} is initially higher, then the gate of Q_{3L} will be lower, so it sinks less current than Q_{3R} . This causes the voltage difference to be greater. This will continue until a steady state is reached. If the drain of Q_{3L} is initially lower, then the opposite will happen.

3.3 Biasing Circuit

The biasing circuit is shown in Figure 8. One reason for this circuit is to bias the output of the second adder/integrator so that the input transistors to the first sense amplifier can be guaranteed to be on. The sense amplifier would not work if this were not the case. Another reason for this circuit is to cause the sensing to start close to the unstable operating so that it can occur quickly.

The right half of the biasing circuit is equivalent to the output stage of the adder/integrator. Q_1 and Q_3 correspond to Q_{13} and Q_{14} of Figure 5. To make the current through Q_1 correspond closely to the current through Q_{14} of Figure 5, Q_2 is used. Q_2 is sized the same as Q_1 so that its gate to source voltage is approximately zero making the drain of Q_{13} approximately equal to the drain of Q_1 .

The left half of the biasing circuit corresponds to half the the sense amplifier during the sampling phase. Q_4 is used because of the small voltage drop across Q_2 in Figure 7. Since Q_3 is

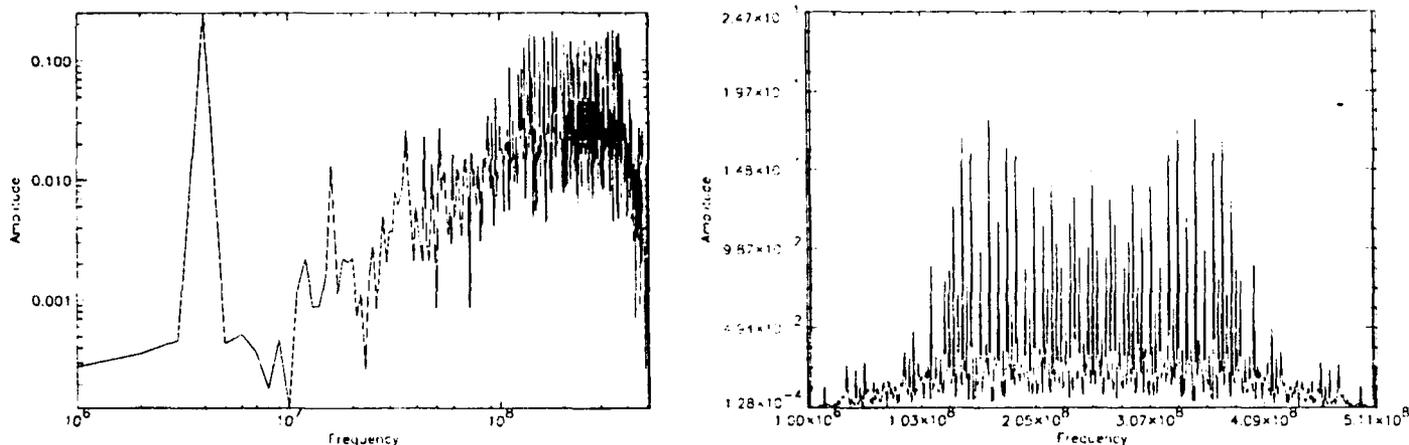


Figure 9 Output Spectrum

the same size as Q_1 , the input to the left half of the biasing circuit should be approximately equal to its output. This bias point corresponds to a high gain biasing for the sampling. When the inputs to the sense amplifier are equal, they should approximately equal to BIAS and the outputs should be equal to BIAS.

4 Simulation and Performance Evaluation

The circuit was modeled using the HSPICE software and parameters for the Vitesse 1.2 micron MESFET process. The models for the transistors include many of the non-linearities including backgating. A 4-Mhz input with an amplitude of half the reference voltage was used with a 512-Mhz sampling frequency. Only 4 input cycles or 512 sample cycles were simulated because of the time needed. It took 1 day on the fastest machine available. Because only 4 input cycles were used, the accuracy of the FFT analysis is limited. One author [3] suggests that at least 32,768 samples or 256 input cycles are needed for an accurate FFT. This would take about 2 months to simulate.

After the transistor level simulation was done, an FFT of the modulator output was performed to characterize the performance in the frequency domain. The PV-WAVE software was used for the frequency analysis and the results of the signal to noise plus distortion ($S / N+D$) are shown in Figure 9 for both linear and logarithmic scales. These results include the effects of noise due to quantization as well as other distortions introduced by actual transistor level circuit effects. If the quantization noise corresponded to white noise (as assumed in the earlier theoretical discussion), then the frequency response at the output would correspond to equation (8). This would predict a peak noise at half the sampling frequency (256-Mhz). As seen in Figure 9, the noise plus distortion peaks in the neighborhood of 256-Mhz, but as one would expect, does not correspond exactly to the white noise assumption.

Assuming the baseband is less than 10-Mhz, the simulated signal to peak noise plus distortion density shown in Figure 9 is 473. The number of effective bits resulting from the decimated

filtered output of the modulator can be predicted for the signal to noise plus distortion ratio [5]. This result suggests at least an 8-bit resolution (i.e. $2^8 < 473$) for an input with magnitude of one half the reference voltage. A 9-bit or 10-bit resolution may be obtained if the maximum magnitude of the input approaches the reference voltage. As stated above, the accuracy of these results is limited due to the restricted length of the time domain output. The actual accuracy may be considerably better if sufficient input cycles could be simulated to eliminate initial transients from early cycles. If a faster and more abstract model (compared to HSPICE) were used, the accuracy of the circuit non-linearities would be lost and a longer time simulation would not necessarily result in a better prediction of the results. Additional work is needed on this problem.

5 Conclusion

The design and simulation results for a second-order sigma-delta modulator using GaAs MES-FET's has been presented. Several unique circuits have been introduced including a novel integrator which is based on drain and source currents of the FET's satisfying the square law. The frequency analysis of the simulated modulator output indicates a resolution of 9-10 bits for input frequencies up to 4-Mhz. This performance was based on a limited time domain output sequence because of the excessive computer time required for the simulation. Further work is required to increase the accuracy of the frequency analysis presented. Longer simulations are needed without sacrificing the effects of distortion introduced at the circuit level. Of course, actual performance could be obtained by fabricating a circuit and measuring the performance.

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